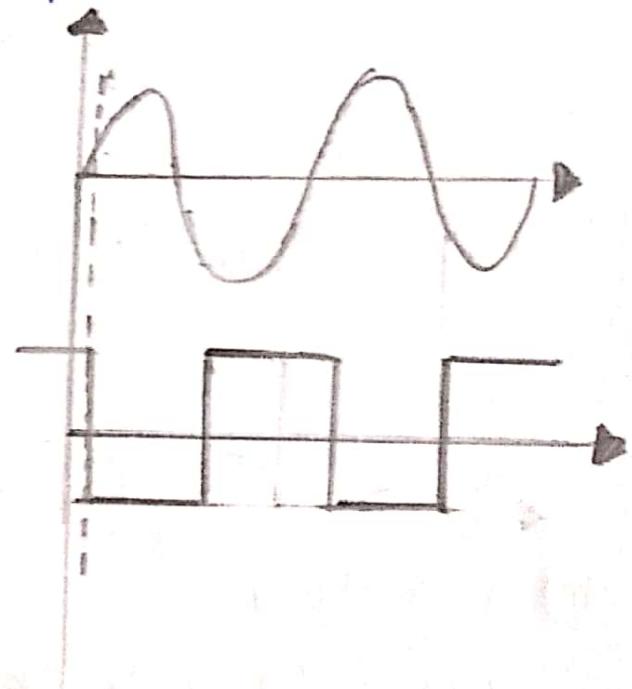
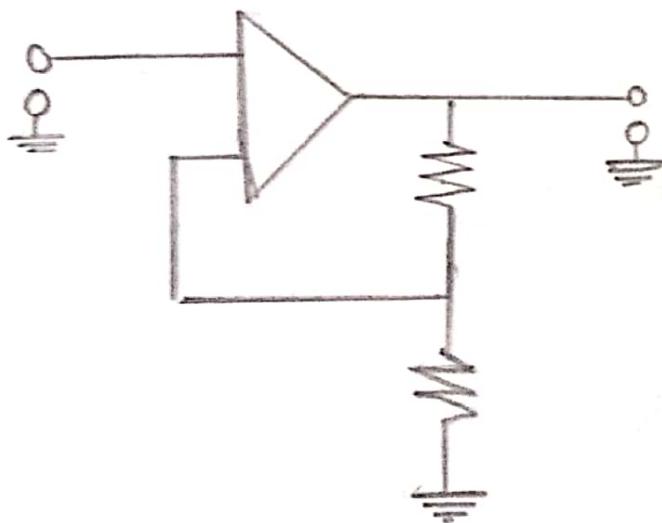


ANALOG DIGITAL ELECTRONICS

ASSIGNMENT-II

Q1 With hysteresis characteristic explain the working of schmitt trigger circuit [inverting]

Ans The input Voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means, the circuit uses positive voltage feedback, that is here feedback voltage aids the input voltage rather than opposing it. For instance let us assume that the input voltage at inverting is slightly positive than feedback voltage at the non-inverting, this produces a $-V_o$ output voltage.



Due to -ve output the feedback voltage from voltage divider circuit is also -ve and available at the non-inverting input. This is fed to input and circuit is driven into -ve saturation. The output is driven into +ve saturation at $+V_{sat}$. This is the reason circuit is also called regenerative comparator.

Step

$$UTP = \frac{R_2}{R_1 + R_2} V_{sat}$$

Step

$$LTP = \frac{R_2}{R_1 + R_2} (-V_{sat})$$

Step

$$V_{hys} = UTP - LTP$$

$$= \frac{R_2}{R_1 + R_2} V_{sat} - \frac{R_2}{R_1 + R_2} (-V_{sat})$$

Q2

$$= 2 \left(\frac{R_2}{R_1 + R_2} \right) V_{sat}$$

$$= 2 \beta V_{sat}$$

hysteresis loop can be shifted to either side of zero point by connecting a voltage source as shown

(i) $V_0 = +V_{sat}$

$$UTP = \frac{(V_{sat} - V_R)R_2}{R_1 + R_2} + V_R$$

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$$= \beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2}$$

(ii) $V_0 = -V_{sat}$

$$LTP = \frac{(-V_{sat} - V_R)R_2}{R_1 + R_2} + V_R$$

$$= -\beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2}$$

If V_R is positive loop is shifted to right if $-V_R$ then loop is shifted to left V_{hys} is same

Design procedure

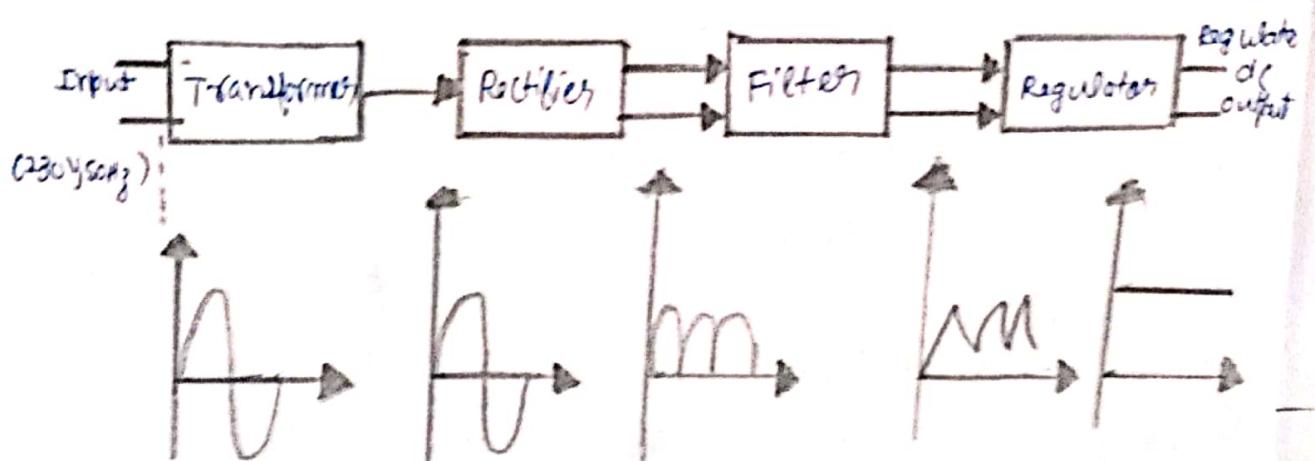
Step 1: $I_2 \geq I_B(\text{max})$

$$I_2 = 50 \mu\text{A}$$

Step 2: $R_2 = \frac{\text{Trigger Voltage}}{I_2}$

Step 3: $R_1 = \frac{V_0 - (\text{Trigger voltage})}{C_2}$

Q2. Discuss the block diagram of regulated power supply



The ac voltage is applied to the primary of a step-down transformer. The transformer steps down the ac voltage to desired dc output with help of turns ratio.
• rectifier converts ac to pulsating dc voltage i.e. voltage containing ripples

- The filter circuit is used to make the ripples smoother by reducing it until output has some ripples

• regulator block is used removes all ripples from filter and makes output voltage smooth. It also keeps the output voltage constant under variable load condition.

$$V_{out} = R_p (I_1 + I_2 + \dots + I_n)$$

..... 7

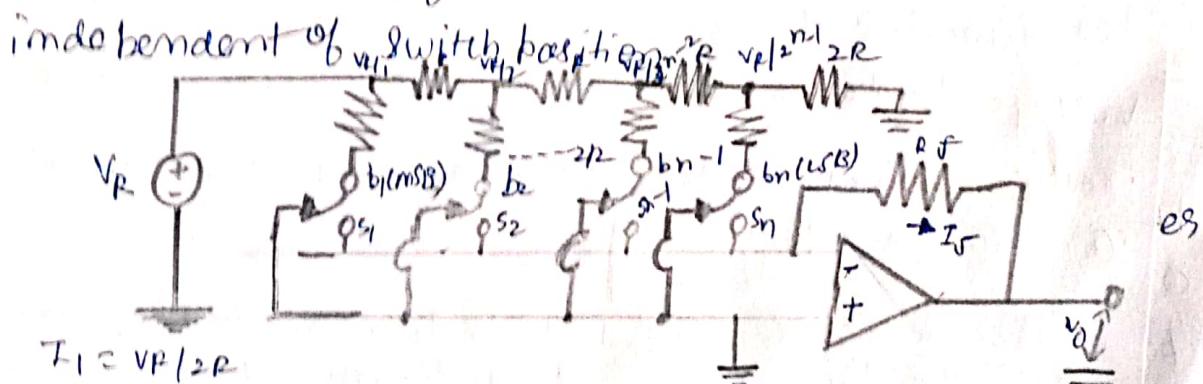
- This voltage regulator is the one which is redesigned to keep the output voltage of a power supply nearly constant / when varying input voltage conditions and varying load conditions.

Q3 Explain Working of R-2R ladder D to A conversion

Ans In R-2R ladder network only two values R and $2R$ are used. Hence can be used in IC-based applications. The R-2R ladder DAC is as shown.

- Here DAC uses shunt resistors for generating n binary weighted currents, it uses voltage scaling. Identical resistors

- Each binary bit connects switch either to ground or inverting terminal of op amp. Due to virtual ground concept both positions are at ground potential and currents through resistances are constant and independent of switch position irrespective of $V_R/2^{n-1} 2R$



$$I_1 = V_R / 2R$$

$$I_2 = \frac{V_R}{2} = \frac{V_R}{4R}$$

$$I_3 = \frac{V_R}{2^2} = \frac{V_R}{8R}$$

$$I_n = \frac{V_R / 2^{n-1}}{2R}$$

$$V_O = -I_F P_f$$

$$\begin{aligned}
 V_O &= -R_f (I_1 + I_2 + \dots + I_n) \\
 &= -R_f \left[\frac{V_R}{2^R} b_1 + \frac{V_R}{4^R} b_2 + \dots + \frac{V_R}{2^n R} b_n \right] \\
 &= -\frac{V_R}{R} R_f (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n})
 \end{aligned}$$

when $R_f = R$, V_O can be

$$V_O = -V_R (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n})$$

This V_O expression indicates that DAC works on principle of summing output of DAC is

analog and to digital inputs

ADVANTAGES:-

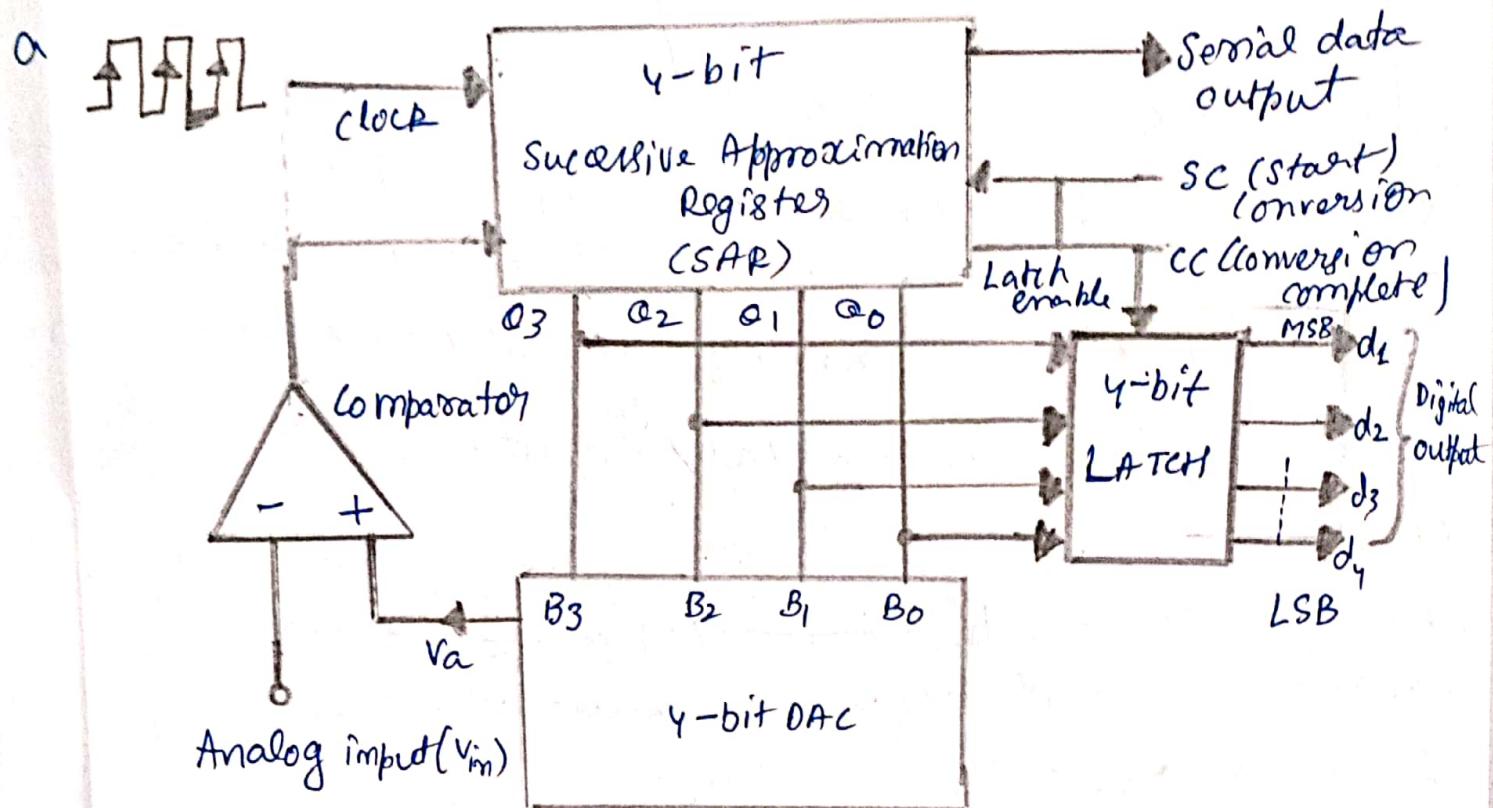
- As it uses only two types of resistors in fabrication and accuracy value of e^{-2R} can be designed.
- Binary input length can be increased by adding more $R-2R$ sections.
- No dc voltages remain constant with changing binary input is inverted $R-2R$, DAC. This helps in avoiding slow down effect by stray capacitance.

Q4 Explain Successive Approximation A to D Converter

Ans. It consists of a successive approximation register

Ex. the output of which is connected to DAC as well as output latch circuit. The input analog signal is compared with the analog output signal of DAC. The output of comparator is feedback to SAR-control unit. In output

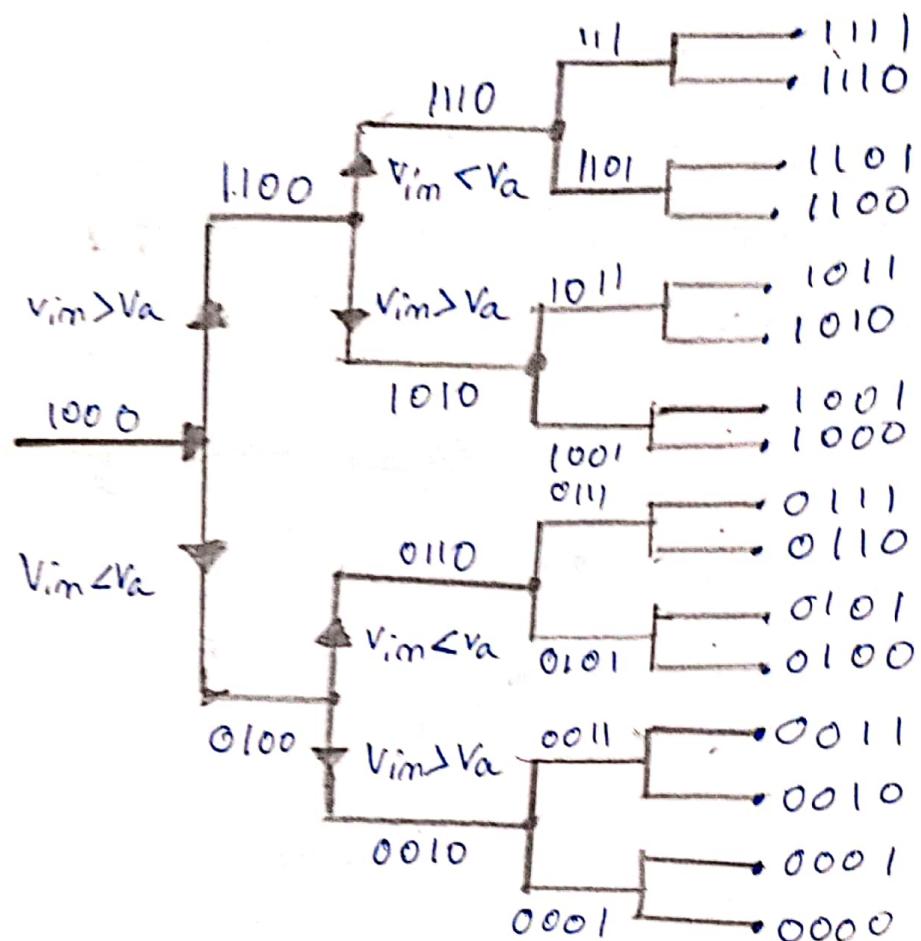
- logic inside SAR adjusts its digital output until it is equal to analog input signal V_a . The operation is clearly understood with the help of code tree



OPERATION:

- At the start of conversion cycle, the start conversion terminal is made high - on the first clock pulse, the output of SAR is made 1000. The DAC produces an analog signal V_a proportional to 1000. This analog signal is compared with input analog signal (V_{in}). If $V_{in} > V_a$, then comparator output will be high and SAR keeps Q₃ high. On the other hand if $V_{in} < V_a$, then the comparator output becomes low and SAR resets Q₃ to low. If $V_{in} > V_a$, SAR follows the upward path in code tree and if $V_{in} < V_a$, downward path.
- on 2nd clock pulse, SAR will set the next MSB Q₂ to high. Depending on the output of DAC, SAR will either

Set or reset Q_2 . This process is continued till the SAR examines all the bits. As soon as LSB Q_0 is examined, the SAR makes the c terminal high which enables the latch and digital data appears at the output of the latch.



The conversion time for n -bit ADC of this type is $(n+2)$ clock periods. n -clock for n -bit digital conversion one clock digital readout, other clock is to clear the approximation input at DAC before the next conversion.

ADVANTAGES

- High speed
- High resolution

Q5 Explain the following op-amp applications
 (a) Non Linear Amplifier (b) Relaxation oscillator
 (c) current to Voltage converter

Ans(a)

NON LINEAR AMPLIFIER

Non linearity is behaviour of circuit particularly in an amplifier in which output signal strength don't

Vary in direct proportion to input signal strength

- It gives non linear relationship between input and output signals. The non linear amplification can be achieved in simple way by just connecting a non linear function. Large change in input voltage causes small change in output voltage.

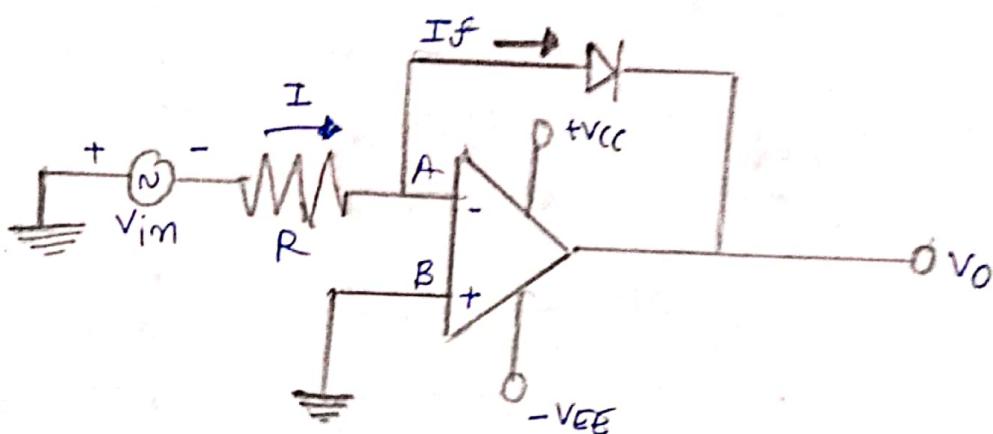


Fig shows Non Linear Amplifier where diode D is used in +ve feedback path. By virtual ground concept as node B is grounded node A will be virtually grounded
 $\therefore V_A = 0$

$$I = \frac{V_{im} - V_A}{R}$$

$$V_A = 0$$

$$I = \frac{V_{im}}{R}$$

can show large variation

(b) RELAXATION OSCILLATOR

Let I_F be current through h - diode, the voltage across diode is $V_A = V_0 \sin \theta$ since $V_A = 0 \therefore$ Voltage $= -V_0$

substituting we get

$$-V_0 = \eta V_T \ln \left[\frac{I_F}{I_S} \right]$$

where .

$V_T \rightarrow$ voltage equivalent of temperature

$I_S \rightarrow$ diode forward current

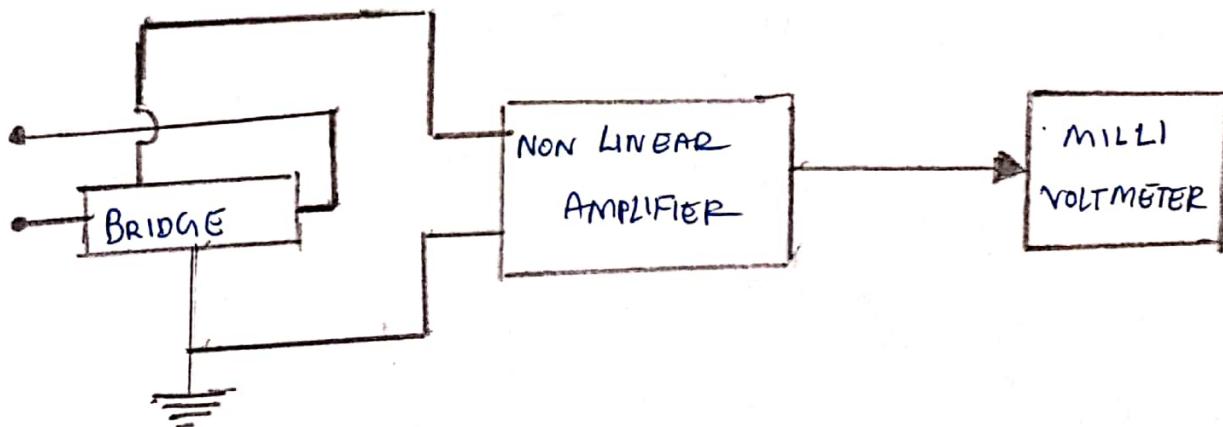
$I_r \rightarrow$ Diode reverse saturation current

$$I = I_F$$

$$I_F = I = \frac{V_{im}}{R}$$

$$V_0 = \eta \cdot V_T \ln \left[\frac{V_{im}}{V_{rref}} \right]$$

and $I_S R$ is constant hence denoted as V_{ref}



non linear Amplifier in AC bridge balanced detectors. In this large changes in bridge output voltage get converted to small changes and milli Voltmeter can show large variation in voltage at input

(b) RELAXATION OSCILLATOR

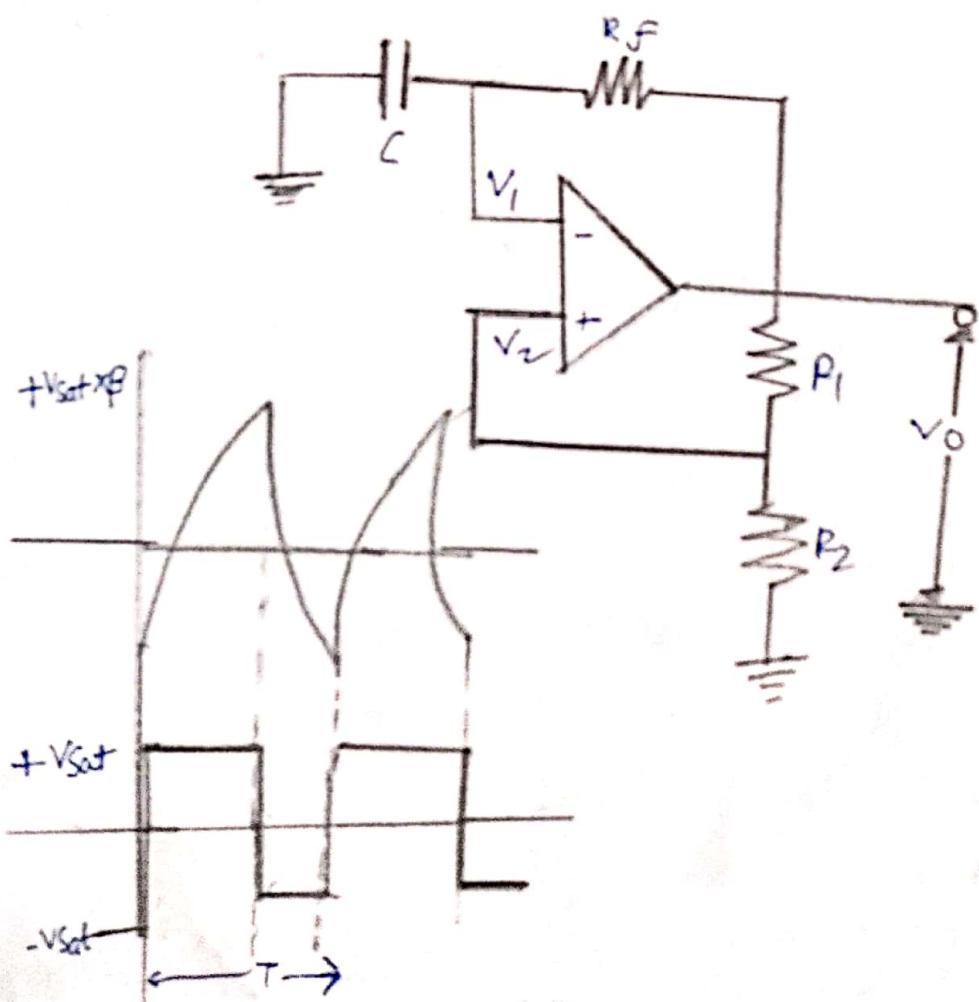
waves may appear in output

It is an - non-linear electronic oscillator
 that generates non sinusoidal - output depends on
 charging time of capacitor - connected in oscillator
 circuit

- It contains feedback loop that has switching device in form of transistor, relay, operational amplifiers, comparators, tunnel diode etc.

Feedback resistor R_1 & R_2 form an inverting Schmitt trigger. When $v_o = V_{sat}$ the feedback voltage is known as threshold voltage given by

$$V_{th} = \frac{R_1 \cdot (+V_{sat})}{R_1 + R_2}$$



Assume output is at $+V_{sat}$ i.e. $V_o = +V_{sat}$ then
 $V_2 = V_{UT}$ and capacitor towards $+V_{sat}$ through the
feedback provided by resistor R_f to inverting terminal
where capacitor voltage $V_c < V_{UT}$ output is $+V_{sat}$ when
 $> V_{UT}$ Voltage at inverting terminals $>$ no inverting
 $V_o = -V_{sat} \therefore V_2 = V_{LT}$

Capacitor starts discharging via R_f to 0V and
capacitor voltage $V_c = V_{LT}$ when $V_c < V_{LT}$ the V_o
 $= +V_{sat}$ capacitor discharges from V_{LT} to 0V
and charges to V_{UT} this repeats.

Frequency is found by

$$V_c(t) = V_{max} + (V_{initial} - V_{max}) e^{-t/\tau}$$

$V_c(t) \rightarrow$ Instantaneous voltage across capacitor
 $V_{max} \rightarrow$ Voltage towards which capacitor charges

$V_{initial} \rightarrow$ Initial voltage

Consider charging from V_{LT} to V_{UT}

$$V_{UT} = V_{sat} + (V_{LT} - V_{sat}) e^{(-T_1/k_{FC})}$$

where

$V_{UT} \rightarrow$ Instantaneous voltage

$V_{LT} \rightarrow$ Initial voltage at $t = T_1$

$$-(V_{LT} - V_{sat}) e^{(-T_1/k_{FC})} = V_{sat} - V_{UT}$$

unwanted switching transients may appear, ...

$$e^{-\frac{T_1}{R_F C}} = \frac{(+V_{sat} - V_{OT})}{(+V_{sat} - V_{LT})}$$

$$\Rightarrow -\frac{T_1}{R_F C} = \ln \left(\frac{+V_{sat} - V_{OT}}{+V_{sat} - V_{LT}} \right)$$

$$T_1 = -R_F C \ln \left(\frac{+V_{sat} - V_{OT}}{+V_{sat} - V_{LT}} \right) = R_F C \ln \left(\frac{V_{sat} - V_{OT}}{V_{sat} - V_{LT}} \right)$$

Time taken for one oscillation can be given as

$$T = 2T_1 = 2R_F C \ln \left[\frac{V_{sat} - V_{LT}}{V_{sat} - V_{OT}} \right]$$

$$f_0 = \frac{1}{T}$$

where $f_0 \rightarrow$ frequency of oscillation

$$f_0 = \frac{1}{2R_F C \ln \left[\frac{V_{sat} - \{(R_1 \times V_{sat}) / (R_1 + R_2)\}}{V_{sat} - \{(R_1 \times V_{sat}) / (R_1 + R_2)\}} \right]}$$

$$T = 2R_F C \ln \left[\frac{V_{sat} - \{(R_1 \times V_{sat}) / (R_1 + R_2)\}}{V_{sat} - \{(R_1 \times V_{sat}) / (R_1 + R_2)\}} \right]$$

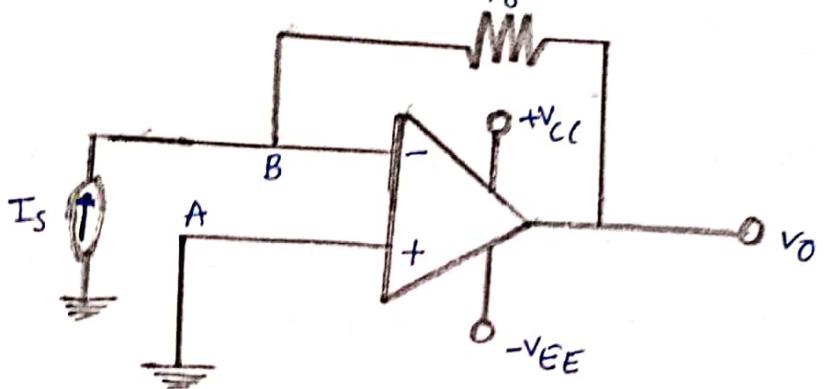
$$T = 2R_F C \ln \left[\frac{V_{sat} \cdot \left[1 + \frac{R_1}{R_1 + R_2} \right]}{V_{sat} \left[1 - \frac{R_1}{R_1 + R_2} \right]} \right]$$

$$T = 2R_F C \ln \left[\frac{2R_1 + R_2}{R_2} \right]$$

(a) Current to Voltage converter

few devices such as photo diodes and PV cells that produce an output current \propto to an incident light or radiation may appear in output

.. energy-energy. The current can be converted to voltage by using I to V converter and the amount of light or radiant energy can be measured.



Circuit produces output voltage \propto to the input current. Input current I_S is applied at inverting terminal of op-amp and op-amp output produced is $V_0 = A \cdot I_S$ where A is gain of circuit. A can be denoted by R as it is measured in ohms. This is also called as transresistor amplifier, node B is virtual ground $\therefore V_B = 0$

$$I_S = \frac{V_B - V_0}{R} = -\frac{V_0}{R}$$

$$V_0 = I_S \cdot R$$

$$\therefore V_0 \propto I_S$$

Q6 What are the hazards in digital circuits?

Explain different types of hazards?

Q7 Hazards

When the input to a combinational circuit changes unwanted switching transients may appear in output

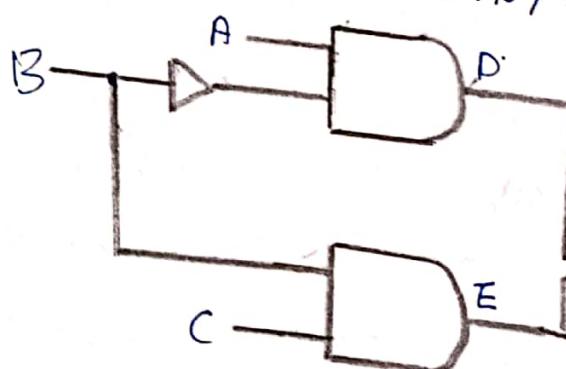
These transients occur when different paths from input to output have different propagation delays.

There are 3 types

(a) Static-1-Hazard

For some combination of propagation delays, a circuit output may momentarily go to 0 when it should remain a constant 1.

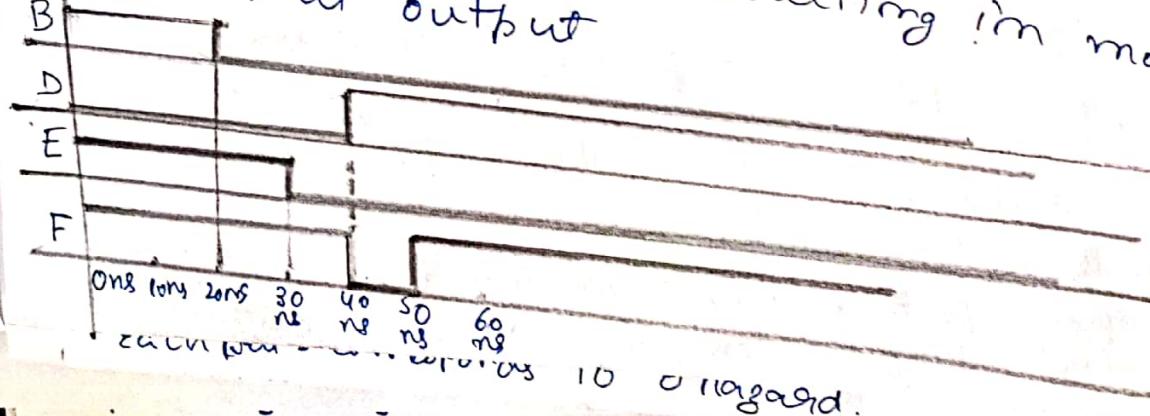
Consider $F = \sum m(3, 4, 5, 7)$



A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

If $A = C = 1$, then $F = B + B' = 1$. So F output should remain a constant 1 when B changes from 1 to 0.

If each gate has delay of 10 ns. F will go to 0 (glitch) at output



- If the circuit is free of hazards then for any combination of delays that might exist in the circuit and for any single input change, output will not contain a transient.
- If circuit has hazard then there is some delay and some input change for which the circuit output contains a transient.
- Quite often the inertial delay value is assumed to be same as delay of gate; if so then circuit will generate a glitch only for inverter delays $>$ long.
- If gate always responds to input changes no matter how closely spaced the changes may be, gate is said to have an ideal or transport delay.
- Hazards can be eliminated via K-map by putting extra loops to terms which don't have a common loop.

Ex

A	BC	
	0	1
00	0	(1)
01	0	(2)
11	(1)	(3)
10	0	0

$$F = AB' + BC + AC$$

b) Static Hazard

If output momentarily go to 1 when it should be 0

Ex:- $F = (A+C)(A'+D)(B'+C'+D)$

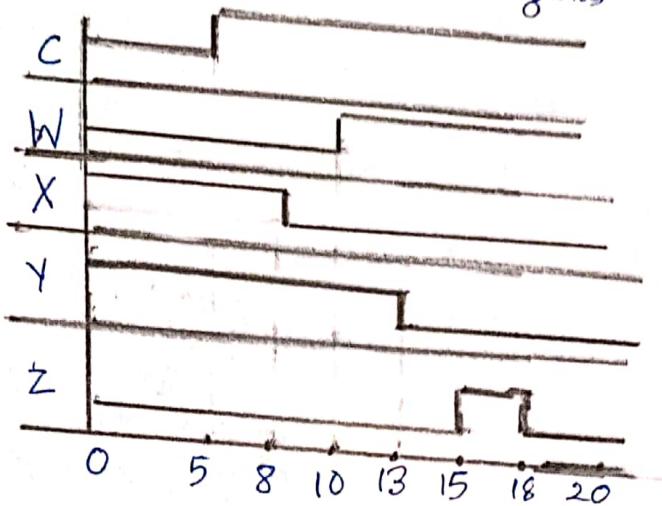
- The K-map shows that there are 4 function pairs of adjacent cells which are not covered by a common loop.
- Each pair corresponds to a hazard.

AB

CP	00	01	11	10
00	0 1 0	1	1	
01	0 0	0 0		
11	1 1	0 0		
10	1 0 1			

K MAP \$

- before with hazards
- used to eliminate hazards



The timing diagram assumes gated delay of

- (a) 3 ns for each inverter
- 5 ns for each AND gate

We can eliminate

0 hazards by looping additional prime Implicants that cover the adjacent 0's

The resulting equation is

$$f = (A+C)(A'+B')(B'+C'+D)(C+D')(A+B'+D) \\ (A'+B'+C)$$

(c) Dynamic Hazards

When output is supposed to change from 0 to 1 (or 1 to 0) the output may change three or more times, we say that circuit has dynamic hazard.

- A dynamic hazard is of term is of form $x+x'$ and
- (a) adjacent input combinations of k map differ by 1 and opposite function values
- (b) For those input patterns, the charge may propagate over at least 3 paths.

Q7 Explain Simulation and testing of digital circuits

Ans Logic circuits can be tested by either simulating or building

- Simulation is generally easier, faster and more economical. As logic circuits becomes more complex simulation is important to design before building it.

WHY SIMULATION?

- (a) Verification \rightarrow design is logically correct or not
- (b) Verification \rightarrow timing of logic is correct or not
- (c) Simulation \rightarrow faulty components in circuit is detected.

- For using a computer program for circuit component and connections is specified, inputs is specified and output is observed.

WORKING OF SIMULATOR

STEP 1:- Circuit inputs are applied to first set of gates in circuit and output is calculated

STEP 2:- Outputs of gates which changed are fed to next level input. If any change output is calculated

STEP 3:- Step 2 is repeated until no more changes circuit is in steady-state condition and outputs may be read

These steps are repeated every time circuit input changes

- The two logic values 0 and 1 aren't sufficient two more come into play

- i) When a gate input or output is unknown we represent this by X

- ii) There might be no connection at input which represents output circuits or high impedance represented by Z

∴ Four logic values are 0, 1, X, Z

RULES FOR SIMULATION

• AND GATE

- for an AND gate if one of inputs is 0 the output is always 0 regardless of other input
- If one input is 1 and the other input is X then output is X

- If one input is 1 and others is Z then output is X

• OR GATE

- If one of the inputs is 1, output is 1 regardless other input

- If one input is 0 and the other input is X or Z

	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

AND GATE

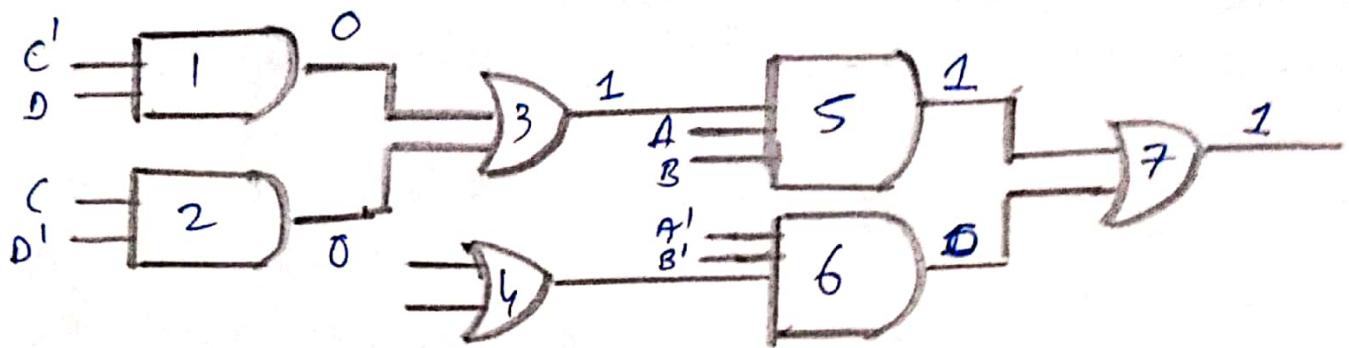
	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

OR GATE

TESTING

- We take an example for testing $F = AB(CD + CD')$ is realized by circuit

$$+ A'B'(C + D)$$



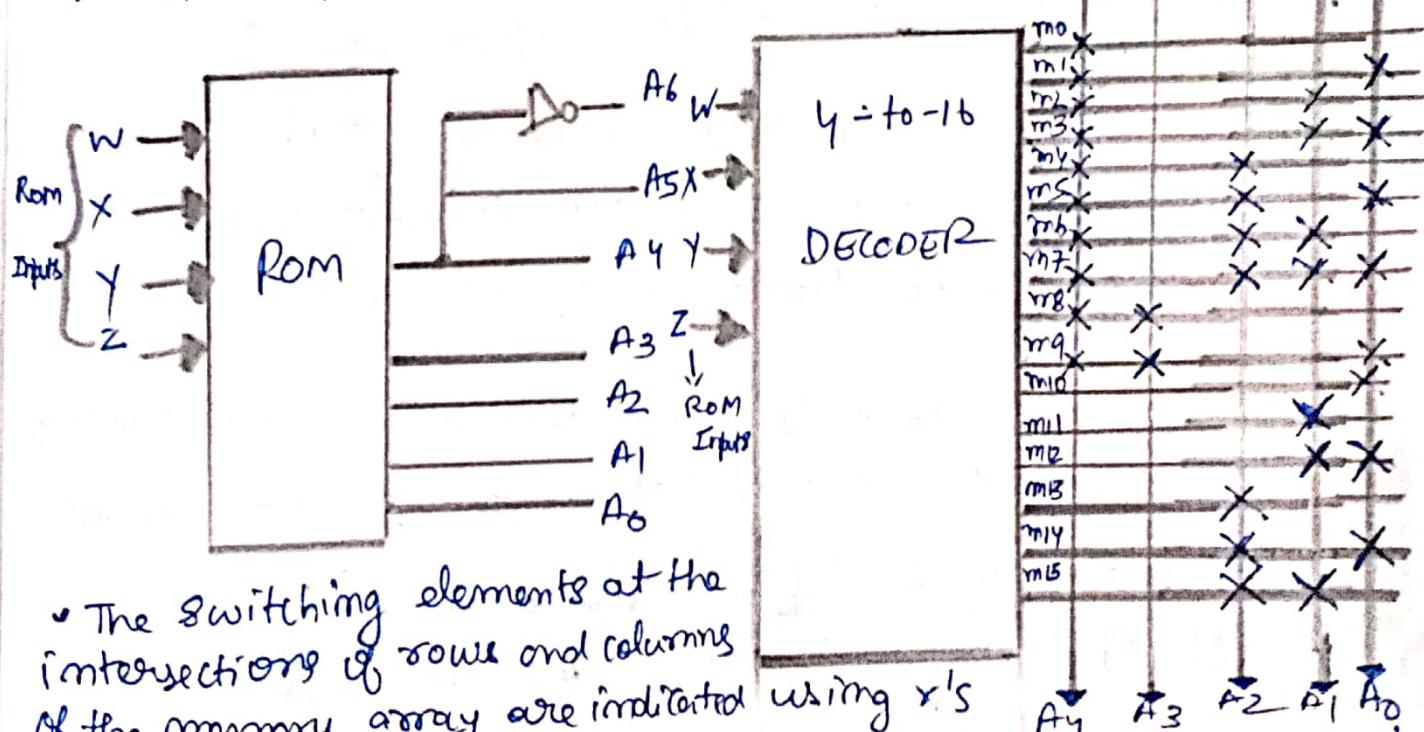
Now output 8 should be 0 but it's 1 the defect can be found by backtracking the connections or output

- The output of gate 7 is wrong but consistent with the inputs as $1 + 0 = 1 \therefore$ one of inputs to gate 2 is wrong
- For correct output in gate 7 inputs should be 0's this shows that output of gate 5 is wrong but again it's consistent with its ~~other~~ inputs as $1 + 1 = 1 \therefore$ one of the inputs is wrong
- We see that either output of gate 3 is wrong or A or B input is wrong but A and B values are fixed to 1 \therefore output of gate 3 is wrong
- Output of gate 3 is not consistent with inputs as $0 + 0 \neq 1$ i.e. output of gate 2 and 3 but ~~input~~ \therefore input is connected wrongly or the gate 3 is defective, or inputs to gate 3 is defective

Q8 Design a Hexadecimal (Binary) to ASCII Code converter
using suitable ROM. Give the connection diagram
of ROM

Ans Truth table and logic circuit for the converter

INPUT		HEX DIGIT	ASCII CODE FOR HEX DIGIT							
W	X	Y	Z	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
0	0	0	0	0	1	1	0	0	0	0
0	0	0	1	0	1	1	0	0	0	1
0	0	1	0	0	1	1	0	0	1	0
0	0	1	0	0	1	1	0	0	1	1
0	0	1	1	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0	1	0	0
0	1	0	1	0	1	1	0	1	0	1
0	1	1	0	0	1	1	0	1	1	0
0	1	1	1	0	1	1	0	1	1	1
1	0	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	1	0	0	0
1	0	1	0	1	1	1	1	0	0	1
1	0	1	1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0	0	1	0
1	1	0	1	1	0	0	0	1	0	1
1	1	1	0	1	0	0	0	0	1	0
1	1	1	1	1	0	0	0	1	1	0



The switching elements at the intersections of rows and columns of the memory array are indicated using 'x's. An 'x' indicates that the switching element is present and connected and no 'x' indicates that the corresponding element is absent or not connected. It is logically equivalent to the ROM OUTPUTS.

Q9 Explain three-state buffer with example?

Ans Three State Buffers

- A gate output can only be connected to a limited number of other device inputs without degrading the performance of digital system
- The buffer input and output are same
- Three states of Buffer is 0, 1 and Z

There are 4 types

- Input \rightarrow Inverted
Output \rightarrow Non Inverted
- Input \rightarrow Inverted
Output \rightarrow Inverted
- Input \rightarrow non Inverted
Output \rightarrow Inverted
- Input \rightarrow Non Inverted
Output \rightarrow Non Inverted

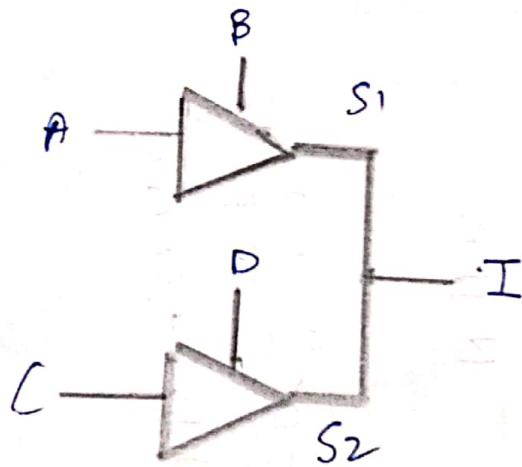
T.T

(a) B A C	(b) B A C	(c) B A C	(d) B A C
0 0 Z	0 0 Z	0 0 0	0 0 1
0 1 Z	0 1 Z	0 1 1	0 1 0
1 0 0	1 0 1	1 0 Z	1 0 Z
1 1 1	1 1 0	1 1 Z	1 1 Z

(a) Ex: 2 to 1 multiplexes using 3 State Buffer

When outputs of 2-3 state buffer are tied together it is logically equivalent

- To select 'A' input when $B=0$ and 'C' input when $B=1$
- When $B=0$ top buffer is enabled so that $D=A$; when $B=1$, the lower buffer is enabled so that $D=C \therefore D=B'A + BC$
- If one of buffers is disabled combination output is same as other buffer
- If both are disabled output is Z . If both are enabled conflict can occur. If $A=0$ and $C=1$ we don't know what hardware will do hence unknown (X)
- If one of buffer is unknown output is unknown
- S_1 and S_2 are output w/ 2 buffers would have without connecting together.
- Four values $0, 1, Z, X$



		S ₂			
		X	0	1	Z
		X	X	X	X
		0	X	0	0
S_1		1	X	X	1
		Z	X	0	1

- Also used for selecting one of two sources as input. They have common enable signal.

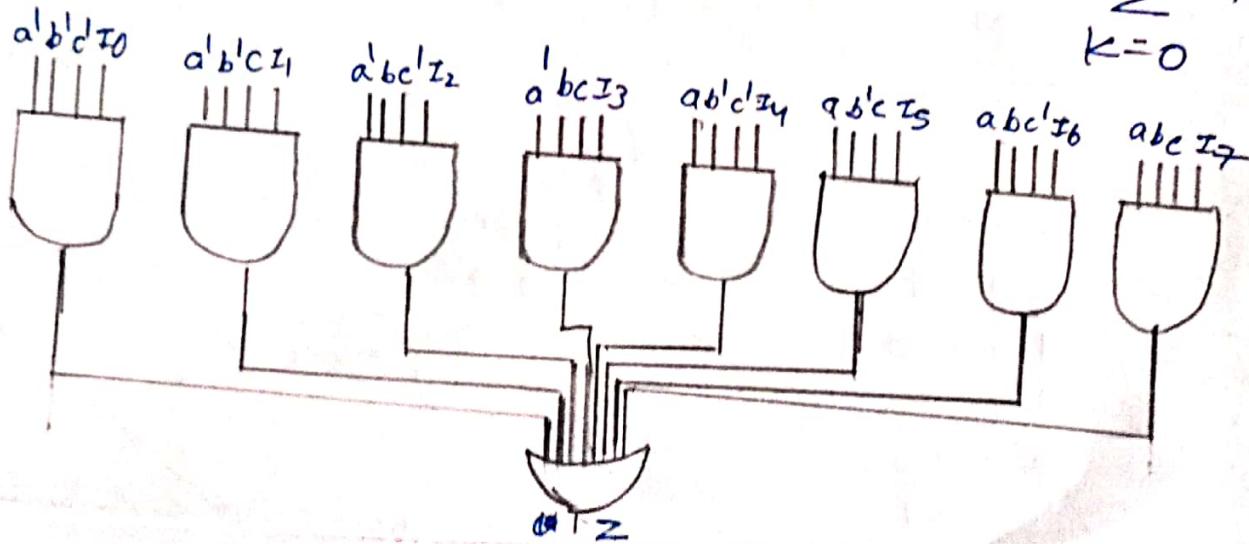
Q10 What is multiplexers? write the 8:1 MUX

Ans MULTIPLEXERS

- A multiplexer has a group of data inputs and a group of control inputs and connect it to output terminal.
- When Control input A is 0, the switch is in the upper position and the MUX output is Z_{I_0} .
- When A is 1, the switch is in the lower position and the MUX output is Z_I .
- MUX acts like a switch that selects one of data inputs and transmits it to the output.
- 8 to 1 mux selects one of 8 data inputs using 3 control inputs

$$Z = A'B'C'I_0 + A'B'C'I_1 + A'BC'I_2 + A'BC'I_3 \\ + AB'C'I_4 + AB'C'I_5 + ABC'I_6 + ABC'I_7$$

- When control inputs are $A+B+C=011$, output is Z_3 .
- A multiplexer with n control inputs can be used to select any one of 2^n data inputs. general equation for output is 2ⁿ:1 MUX: $Z = \sum_{k=0}^{2^n-1} m_k I_k$

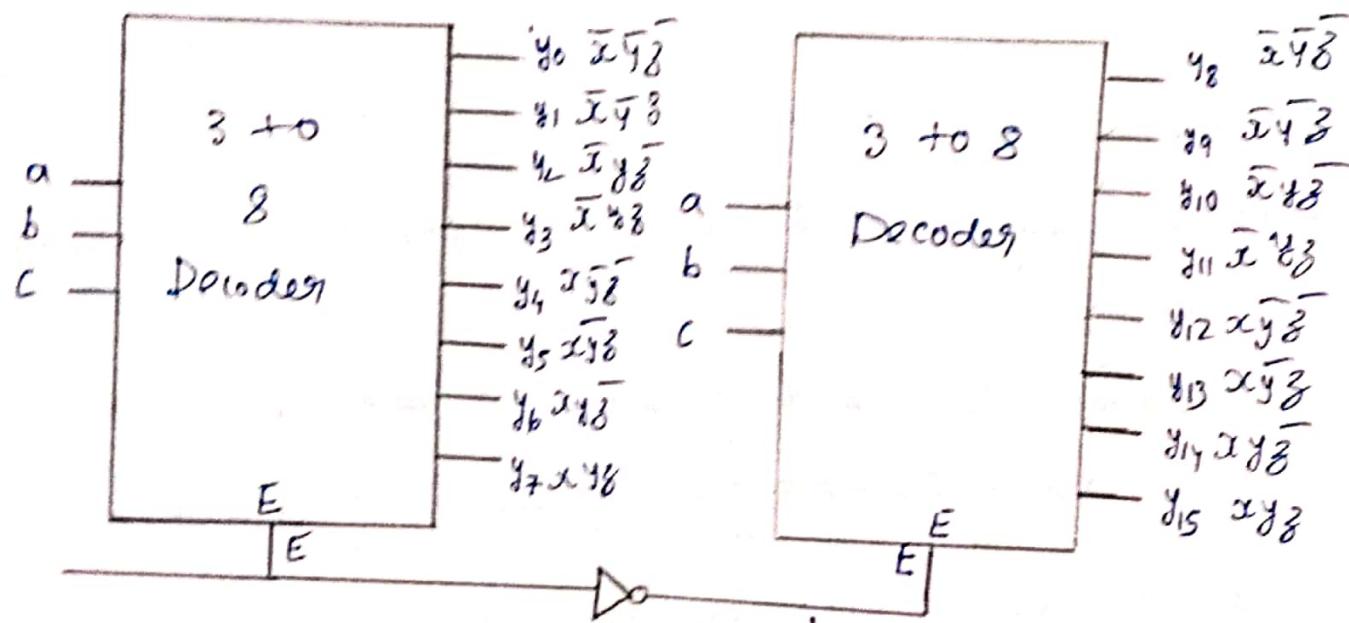


Q11 Define Decoder? Construct 4:16 decoder using 3:8 Decoder

A. Decoder is another commonly used type of integrated circuit.

• Figures shown

- Decoder generates all of the min terms of the three input variables. Exactly one output lines will be 1 for each combination of values



Q12 Using PLA, Implement $F_1 = \sum(0, 1, 4, 6)$
 $F_2 = \sum(2, 3, 4, 6)$

$$\text{Ans } F_1 = (0, 1, 4, 6)$$

$$F_2 = \sum(2, 3, 4, 6)$$

a bc	00	01	11	10
00	1	1	0	0
01	1	0	0	0
11	0	0	0	0
10	0	1	0	1

a bc	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	1	0	0	0
10	1	1	0	1

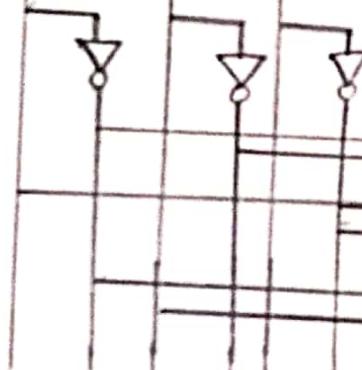
$$Y = \bar{a}\bar{b} + a\bar{c}$$

$$Y = \bar{a}b + a\bar{c}$$

PLA Diagram

Input's

A B C



AND array

OR Array

} word
line

PLA TABLE

Product
Term

$A'B'$

$A'C'$

$A'B$

Inputs Outputs Outputs

$A'B' C$

0 0 -

1 - 0

0 1 -

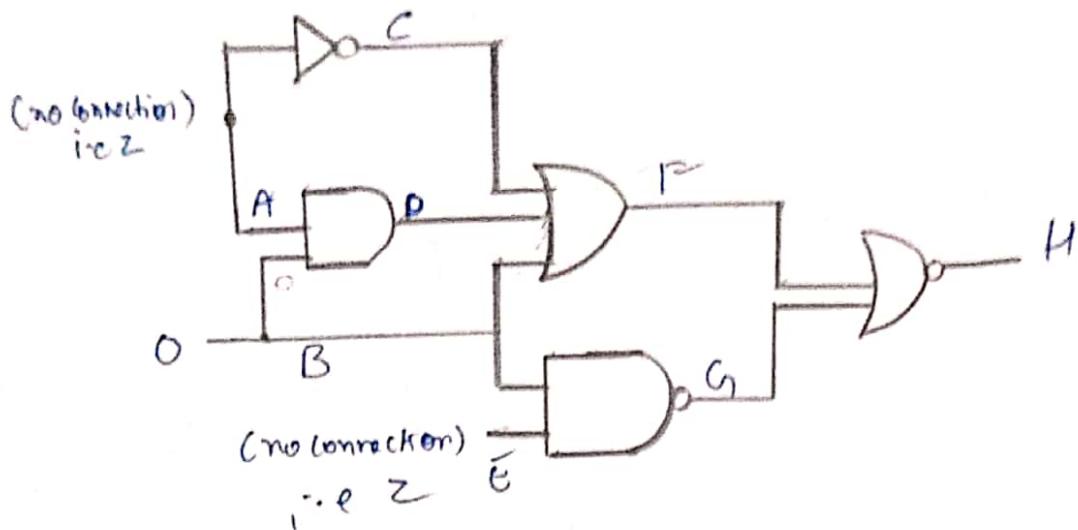
F_1 F_2

1 0

1 1

0 1

Q13 Using Four Valued Logic Final ABCEPHH



By From circuit

$$A=Z, C=X$$

$$B=0, E=Z$$

Z is given to not gate we don't know what it does if $C=X$

$A=Z \therefore \text{output} = 0 = P$ as in AND gate if input is 0 then output is 0 regardless $I_2=0$

$E=Z$ to NAND gate output = 1
 $I_3=0$

$$\therefore H=1$$

Input to first OR gate F

$D=0$
 $I_4=X$
 $I_5=0$

$\left. \begin{array}{l} \\ \end{array} \right\}$ output = $F=X$ as any one input is X then output is X

Finally input of second NOR gate

$F=X$
 $H=1$

$\left. \begin{array}{l} \\ \end{array} \right\}$ output = 1 = H

$A=Z \quad C=X \quad E=Z \quad H=1$ as in OR gate if one of input
 $B=0 \quad D=0 \quad F=X \quad H=1$ is 1 then output is 1 regardless