Realize a J-K Master / slave Flip-flop using NAND gate and verify its Truth-table and implement the same in HDL.

A flip-flop is an electronic circuit with two stable states that can be used to store binary data.

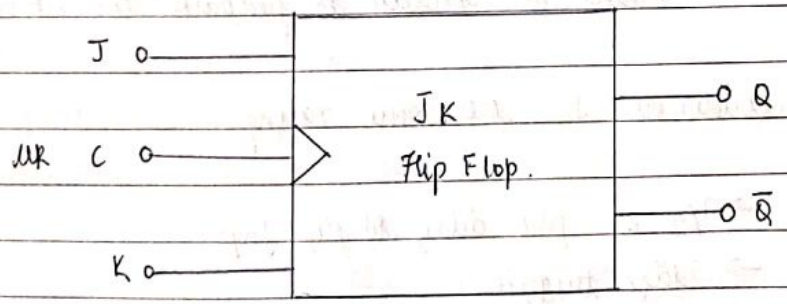
Flipflops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements

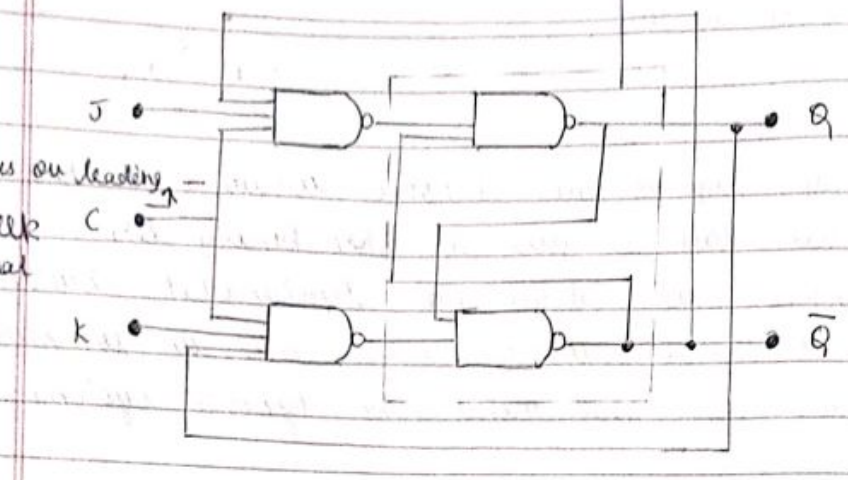
J-K-Flip flop.

→ Is the most widely used flip-flop. It is considered to be universal flip-flop circuit. The sequential operation of the J-K Flip Flop is the same as for RS flip-flop with the same SET and RESET input.

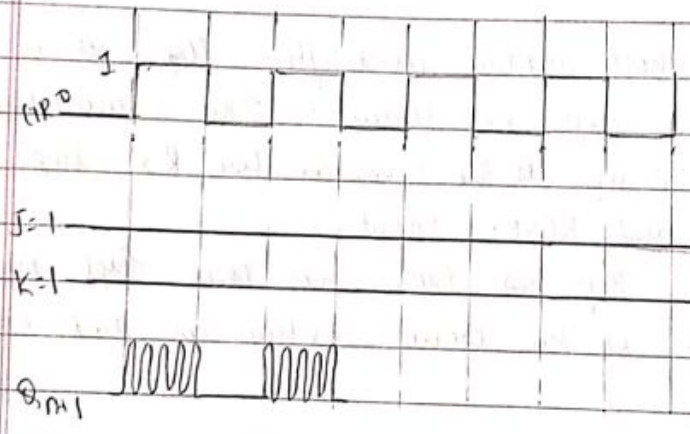
→ The JK Flip flop name has been kept on the inventor name of the circuit known as Jack Kilby.



RS Flip Flop



J-K Flip-Flop



Racing is because of feedback connection.

Condition to overcome racing

→ T/2 < prop-delay of flip-flop
→ edge triggered
→ Master slave

J-K-Flip flop

Race-Around condition - In J-K Flip-flop - For JK flip-flop, if J = K = 1, and if clk = 1

for a long period of time, then Q output will racing as long as 'clk' is high, which makes the output of the flip flop unstable or uncertain. This problem is called race around condition in J-K flip flop.

This problem (Race Around condition) can be avoided by ensuring that the clock input is at logic "1" only for a very short time. This introduced the concept of Master slave J-K flip flop.

Racing is uncontrolled phenomenal whereas toggling is controlled phenomenal.

It does the function as J-K Flip-Flop with difference that Master Master slave units are pulse triggered ones rather than edge triggered ones. The Master Slave JK FlipFlop consists of flip-flops's one a master and other slave.

The clock input is given to the master and the clock' is given to the slave such that when the clock is high master is enabled and the slave is disabled and the output of the master is at steady state.

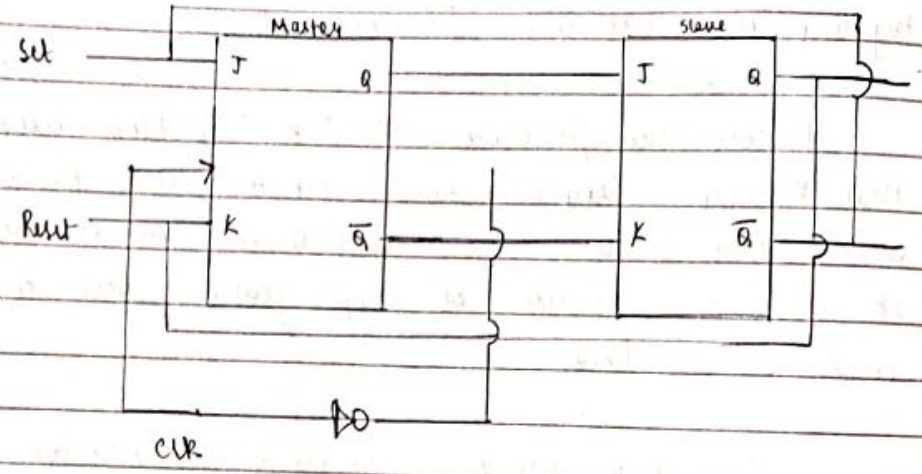
When the clock goes low the clock' is high and the master is disabled while slave is enabled now the output of master reaches the slave output thereby overcoming the race around problem.

A JK Flip-flop is positive edge triggered, where as slave is negative edge trigged. Therefore master first responds to J and K inputs and then slave.

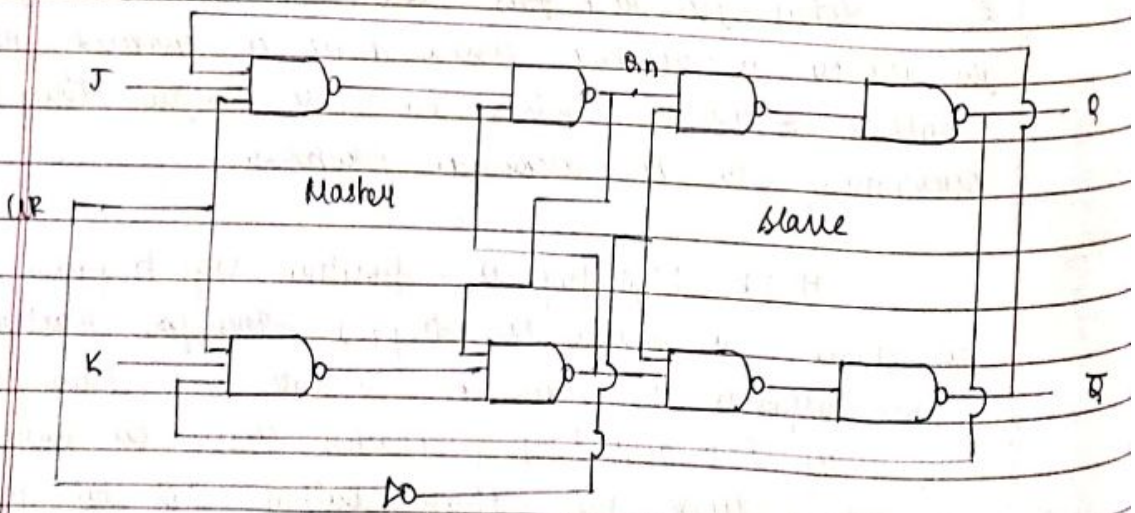
If J=0 and K=1, master resets on arrival of positive clock edge. High output of the master drives the K input of the slave. for the trailing edge

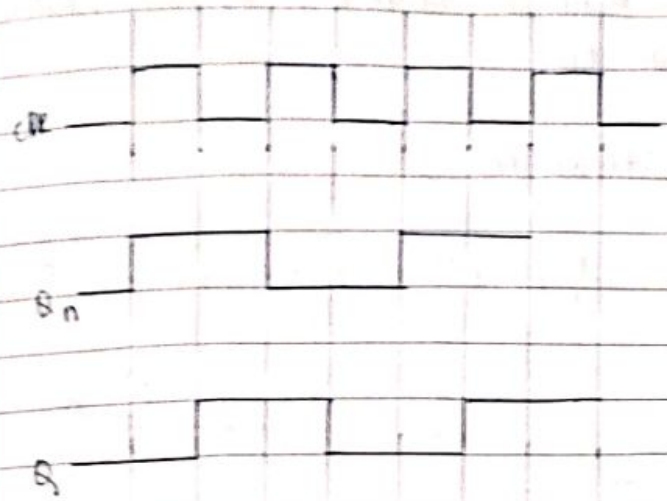
of the clock pulse the slave is forced to reset.
If both the inputs are high, it changes the state or toggles on the arrival of the positive clock edge and the slave toggles on the negative clock edge. The slave does exactly what master does.

Master - slave J-K Flip flop

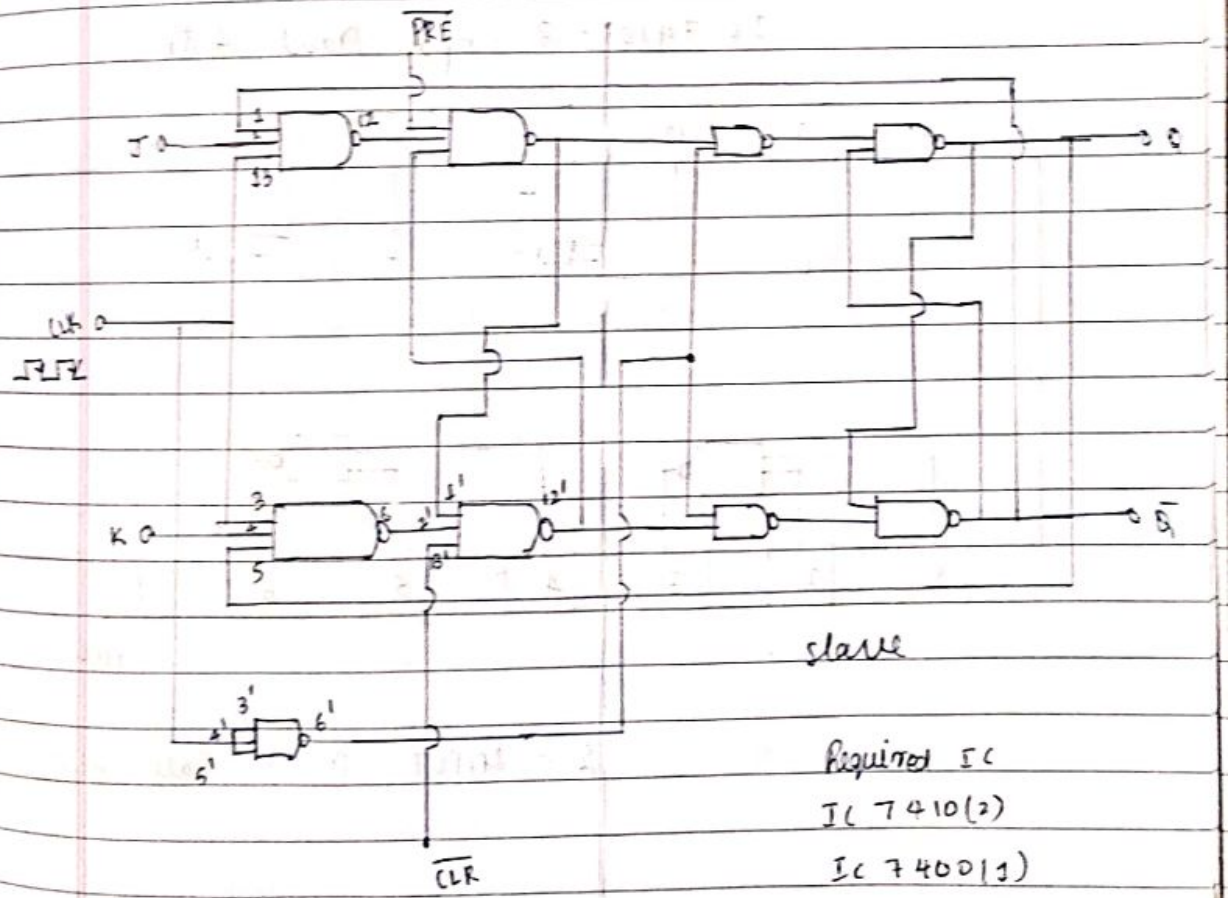


Master - slave JK Flip - Flop





Master - slave J K Flip flop.



slave

Required IC

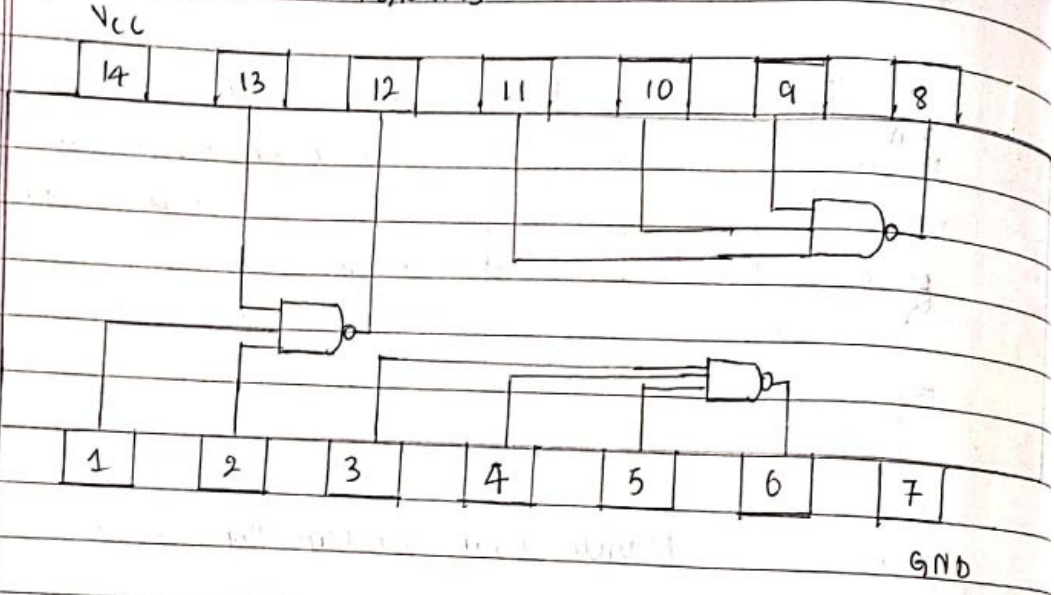
IC 7410(3)

IC 7400(1)

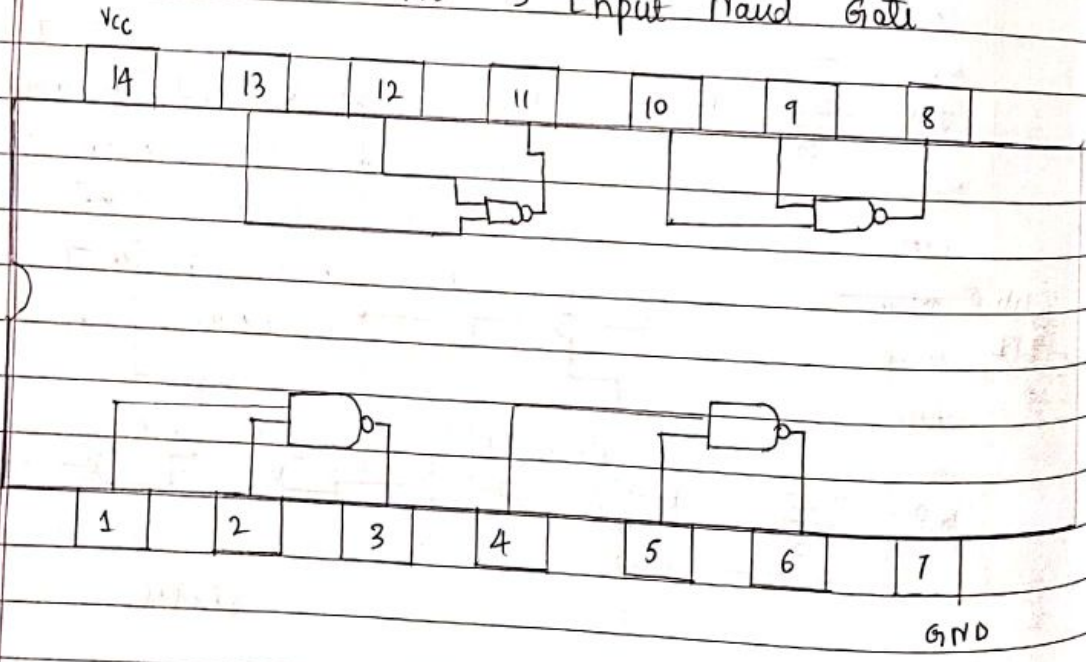
Master

Components required: IC 7410, IC 7400, patch wires, trainer kit

PIN DIAGRAMS



IC 7410 - 3 Input Nand Gate



2 - INPUT NAND Gate 74L500

J - K - Flip - flop Truth - Table

clk	J	K	Q	$\bar{Q}$	State
1	0	0	Q	Q'	No change
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles.

VHDL Code for Master Slave Flip-flop.

```
entity tt is
    Port ( clr , rst , clk , j , k : in std_logic;
           qn : inout std_logic := '0';
           q : out std_logic);

end tt;

architecture Behavioral of tt is
begin
 process( clk, rst , clr)
 begin

 if rising_edge(clk) then

        if j='1' and k='1' then qn <= not qn;
        else if j='0' and k='0' then qn <= qn
        else qn <= j;

 end if;
 end if;
 end if;
 if falling_edge(clk) then
```

q 1 = qn
and if;
and process;
and Behavioral;

Design and Implement an asynchronous counter using decade counter IC to count up from 0 to n ($n <= 9$) and demonstrate on 7-segment display (using IC-7447).

A decade counter is a binary counter that is designed to count to 1010 (decimal 10).

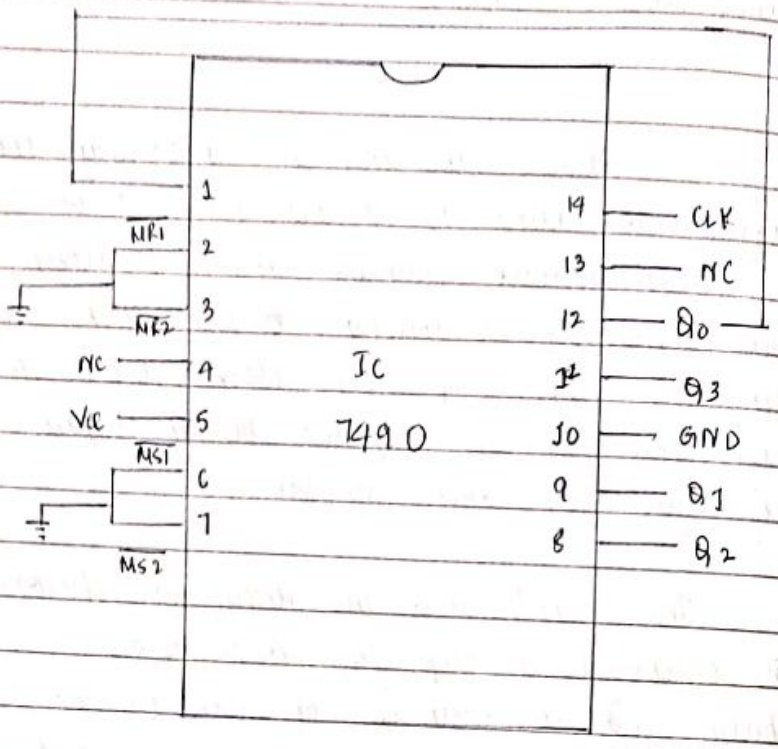
Asynchronous counter is a counter in which the clock signal is connected to the clock input of only first stage flip-flop. The clock input of the second stage flip flop is triggered by the output of the first stage flip-flop and so-on.

This introduces an inherent propagation delay time through a flip-flop. A transition of input clock pulse and a transition of the output of a flip-flop can never occur exactly at the same-time. Therefore, the two flip-flops are never simultaneously triggered, which results in asynchronous counter operation

The 74LS90, is 4-bit ripple type Decade counter. It consists of 4 master/slave flip-flops.

A gated AND asynchronous Master Reset (MR_1, MR_2) is provided on all counter which overrides and clocks and resets (mass) all the flip-flops. A gated AND asynchronous Master Set (MS_1 MS_2) is provided on LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Logic Diagram of Decade counter



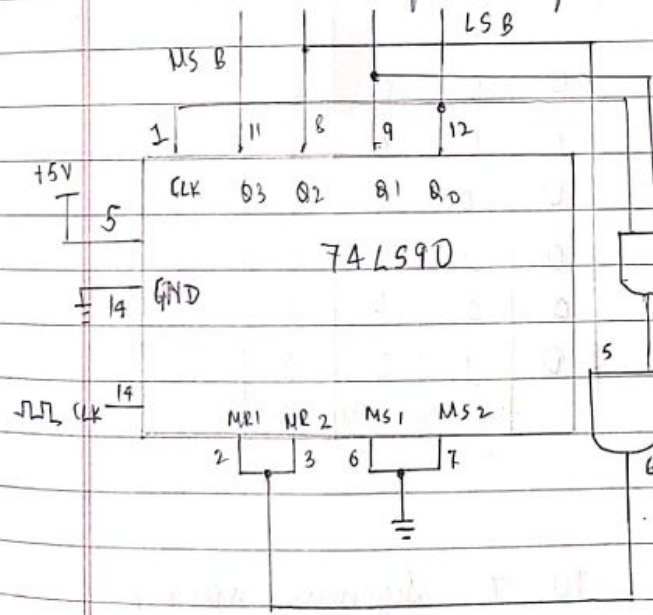
Procedure

When clock pulses are applied, the desired count sequence is observed on output pins Q_3, Q_2, Q_1, Q_0 as illustrated in the truth Table.

For counting Mod - 7 disconnect the ground terminal of MR1 and MR2 and then connect it to output terminal of AND gate.

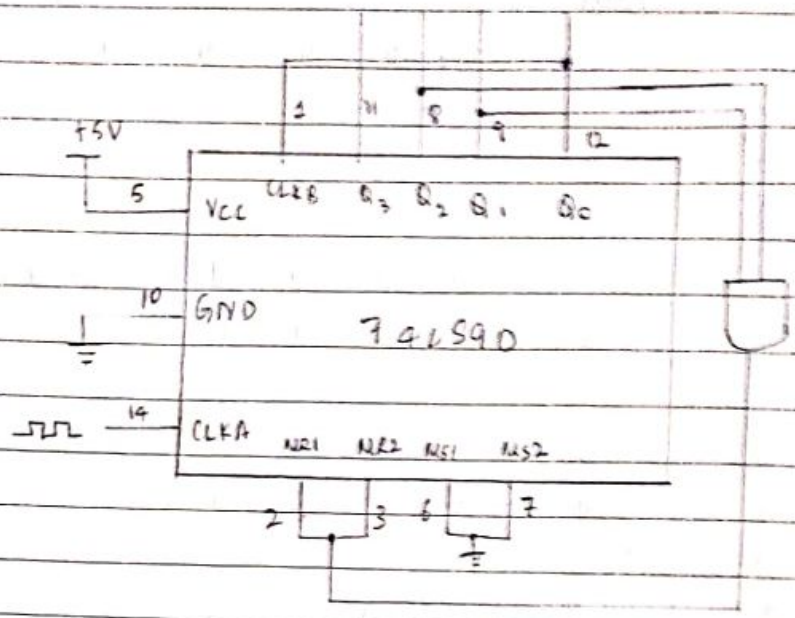
Clock pulse	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0

Logic diagram of MOD - 7 counter



Clock pulse	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	Sequence repeats			

Logic Diagram of IC 7490 - 6 counter

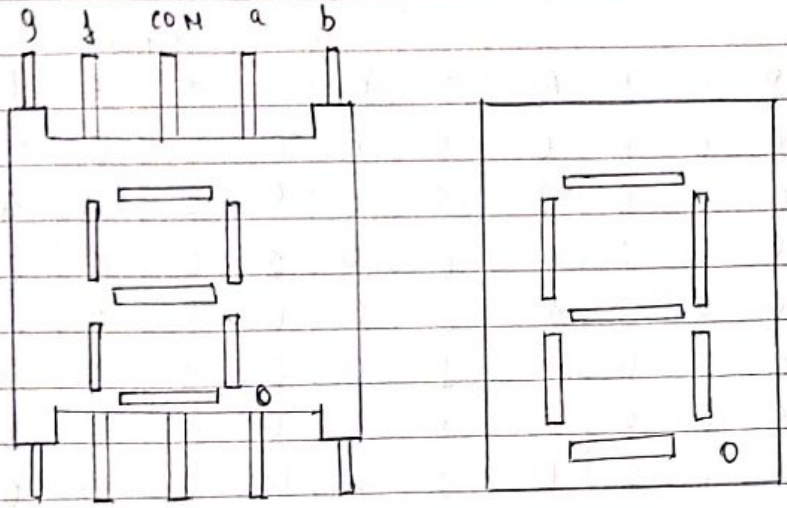


Clock pulse	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	sequence repeats			

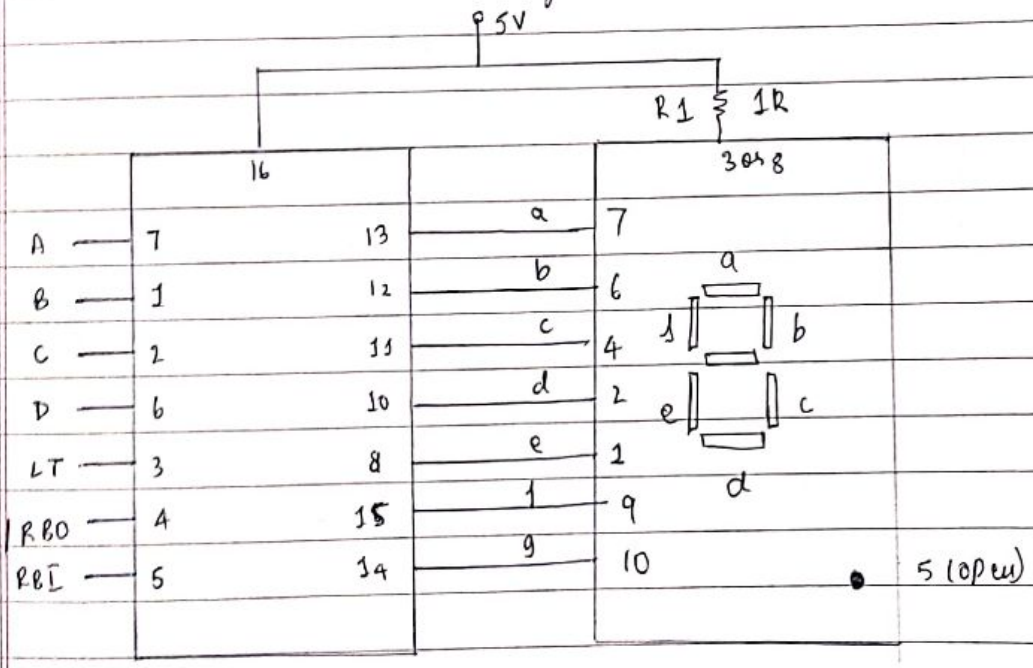
BCD TO 7 - Segment Decoder

A decoder is combinational circuit that converts the binary information from 'n' input lines to a maximum of 2^n unique output lines. The IC-7447 is a BCD to 7 - segment pattern converter. The IC7447 takes the Binary

coded Decimal (BCD) as the input and outputs the relevant 7 Segment code.



Circuit Diagram:



Truth - Table.

BCD Inputs				Outputs Logic levels from IC 7447 to 7 - segments							Display number
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9