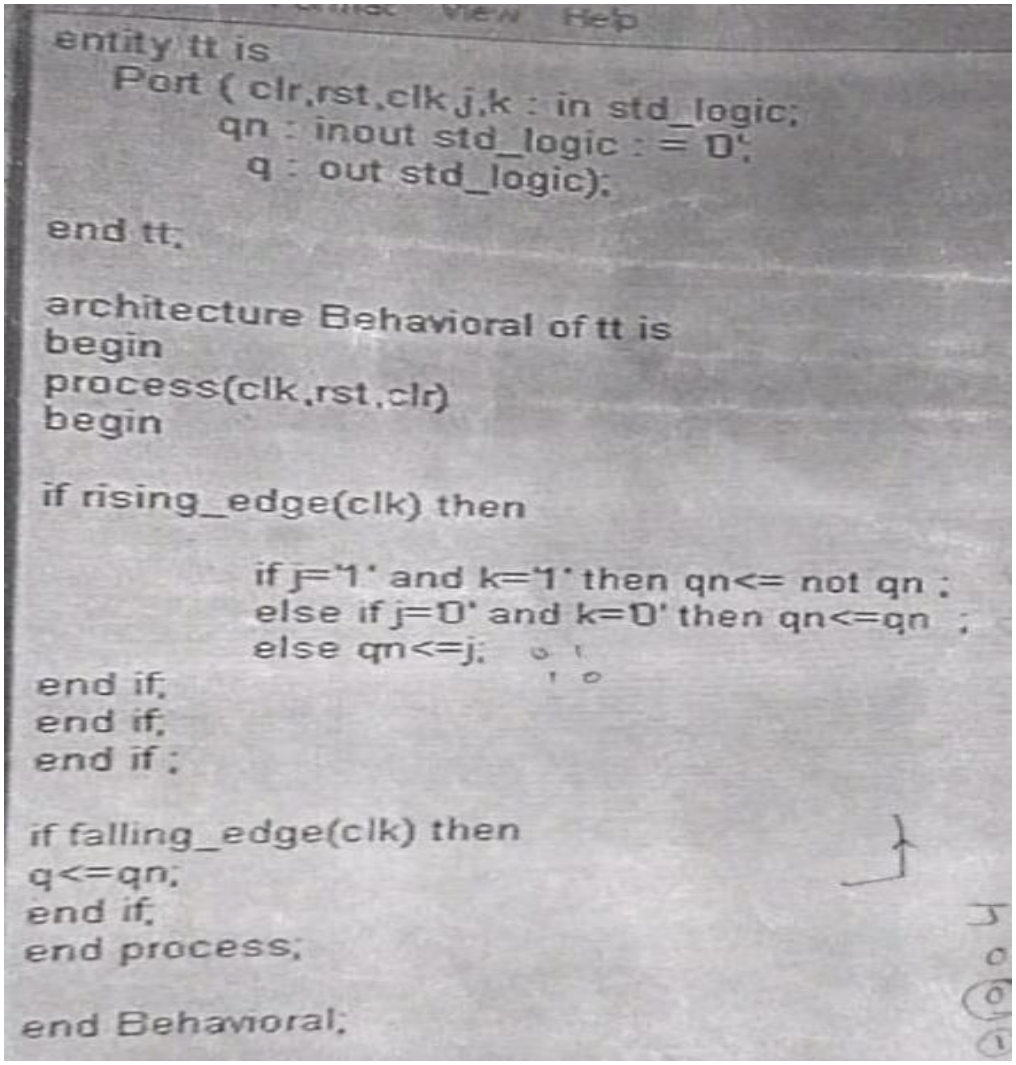
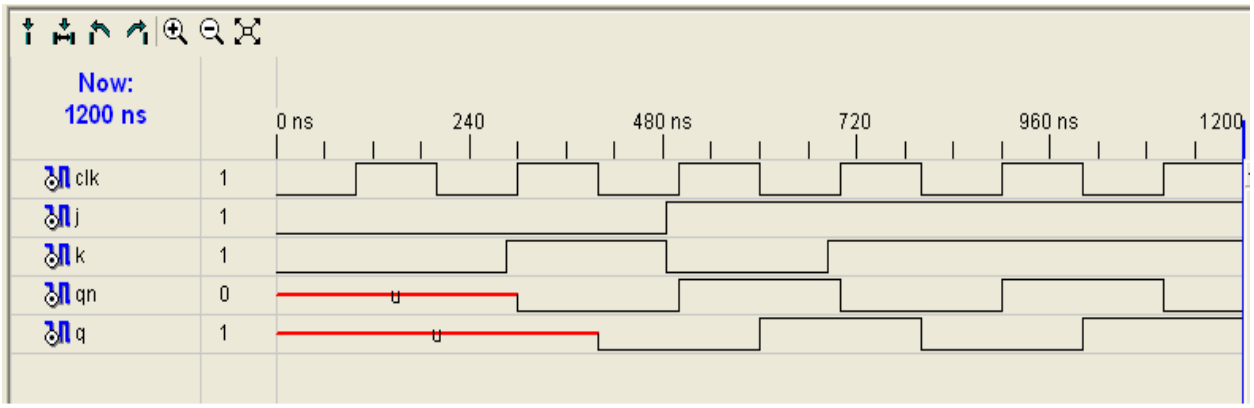
EXPERIMENT 6: VHDL Code for Master-Slave Flip-Flop



```
entity tt is
    Port ( clr,rst,clk,j,k : in std_logic;
           qn : inout std_logic := '0';
            q : out std_logic);

end tt;

architecture Behavioral of tt is
begin
process(clk,rst,clr)
begin

if rising_edge(clk) then

            if j='1' and k='1' then qn<= not qn ;
            else if j='0' and k='0' then qn<=qn ;
            else qn<=j;
end if;
end if;
end if ;

if falling_edge(clk) then
q<=qn;
end if;
end process;

end Behavioral;
```


Now:
1200 ns
0 ns
240
480 ns
720
960 ns
1200
clk
1
j
1
k
1
qn
0
u
q
1
u