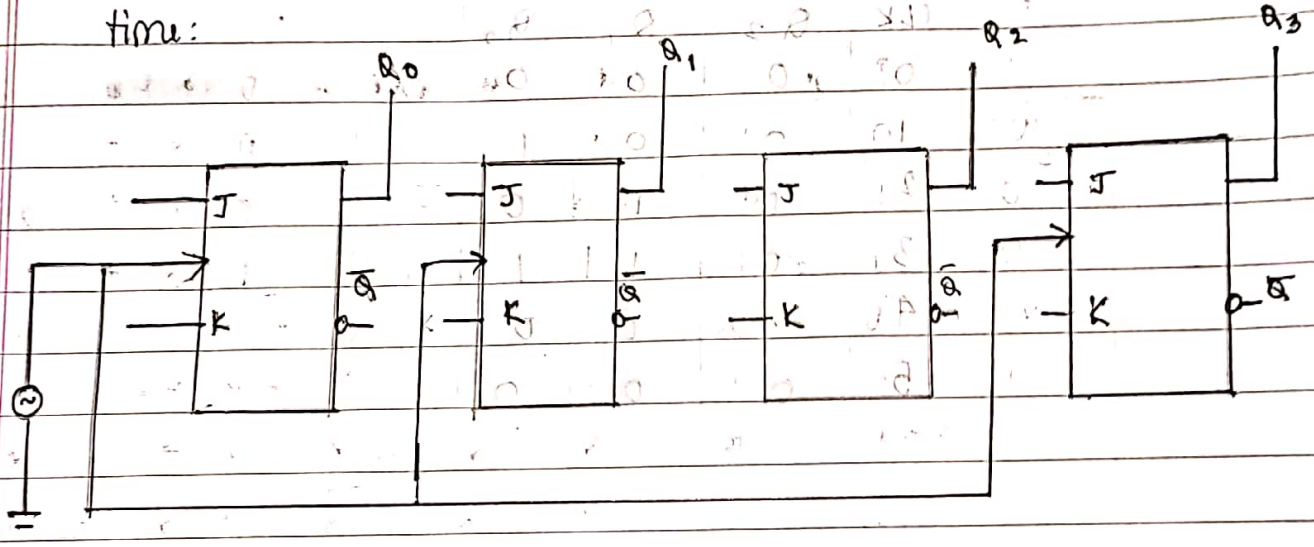
Design and implement a mod-n ($n < 8$) synchronous up counter using J-K flip-flop ICs and demonstrate its working.

Synchronous counter: In contrast to an asynchronous counter, is one whose output bits change state simultaneously, with no ripple. The only way we can build such a such a counter circuit from J-K flip flops is to connect all the clock inputs together, so that each and every flip-flop receives the exact same clock pulse at the exact same time:



How to design synchronous counter

For synchronous counters, all the flip-flops are using the same CLOCK signal. Thus, the output would change synchronously.

Procedure to design synchronous counter are as follows:-

STEP 1: Obtain the State Diagram.

STEP 2: Obtain the Excitation Table using state transition table for any particular FF (JK or SR). Determine number of FF used.

STEP 3: Obtain and simplify the function of each FF input using K-Map.

STEP 4: Draw the circuit.

COUNT TABLE - mod-5

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0

TRUTH - TABLE of JK FF

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (toggles)

FF Excitation Table

⇒ The table, which lists the required input for a given change of state, is called as

Truth - Table:

CLK	J	K	Q_{n+1}	
0	X	X	Q_n	} memory
1	0	0	Q_n	
1	0	1	0	
1	1	0	1	
1	1	1	$\bar{Q}_n$	(toggle)

Characteristic Table:

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation Table:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

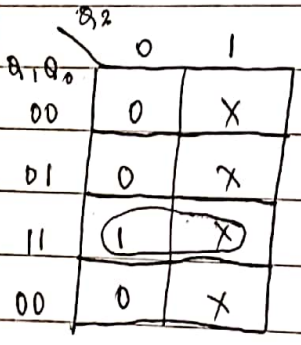
State Table for MOD - 5 counter

→ The table, which represents the relationship between present state and the next state, is called a state table.

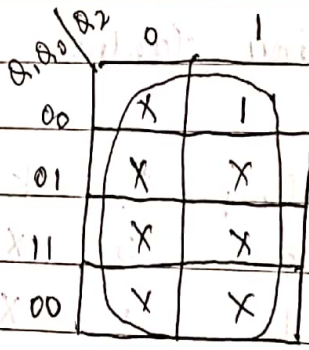
Excitation table is defined for a flip-flop where as State Table is defined for a counter.

Present State			Next State			Excitation Table		
						J_2K_2	J_1K_1	J_0K_0
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0			
0	0	0	0	0	1	0 X	0 X	1 X
0	0	1	0	1	0	0 X	1 X	X 1
0	1	0	0	1	1	0 X	X 0	1 X
0	1	1	1	0	0	1 X	X 1	X 1
1	0	0	0	0	0	X 1	0 X	0 X
1	0	1	X	X	X	X X	X X	X X
1	1	0	X	X	X	X X	X X	X X
1	1	1	X	X	X	X X	X X	X X

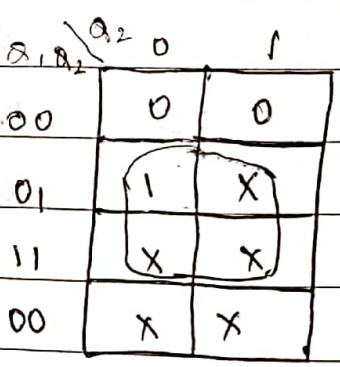
K-map mod 5



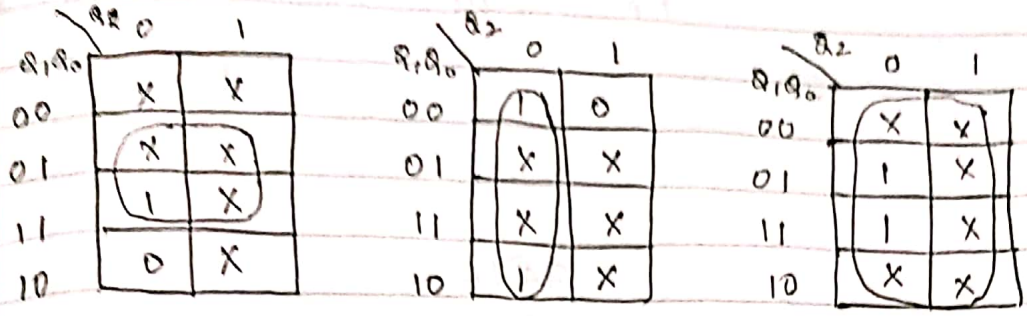
$\bar{J}_2 = Q_1Q_0$



$K_2 = 1$



$\bar{J}_1 = Q_0$



$K_1 = Q_0$ $\quad J_0 = \bar{Q}_2$ $\quad K_0 = 1$

$K_1 = \bar{Q}_0$ $\quad \bar{K}_0 = 0$

Mod - 6 up counter

Components required : IC_{7476}, IC_{7408}, patch chords, trainer kit.

Notes and observation :

Each 7476 IC has 2 J-K - flops flips (FFs) since we are dealing with 3 - bit counters, 3 FFs are needed. So 2 7476 IC's are used.

J and K inputs of FFs can be connected to logic '1' to operate the FF's in toggle mode.

When $P_R = '1'$, $C_R = '0'$, counter is cleared

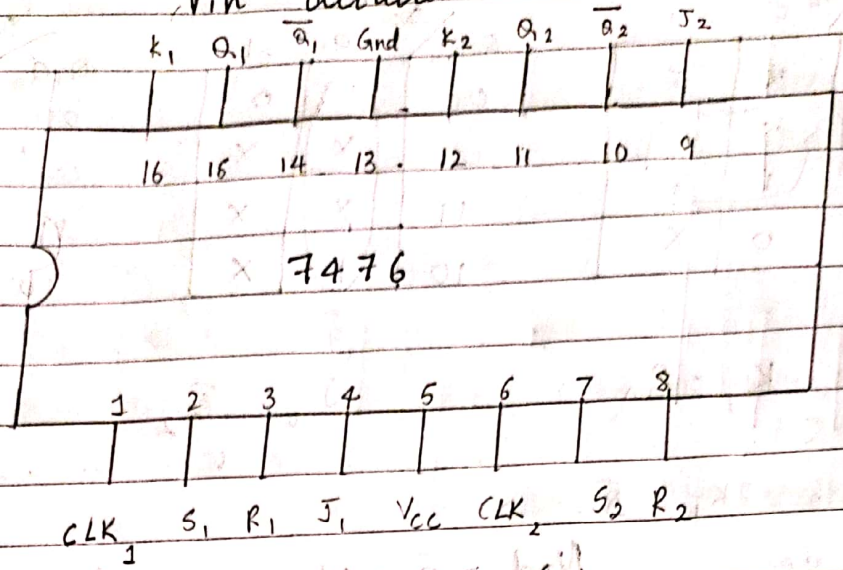
$Q_0 = Q_1 = Q_2 = 0$.

When $P_R = '0'$, $M_R = '1'$, counter is preset

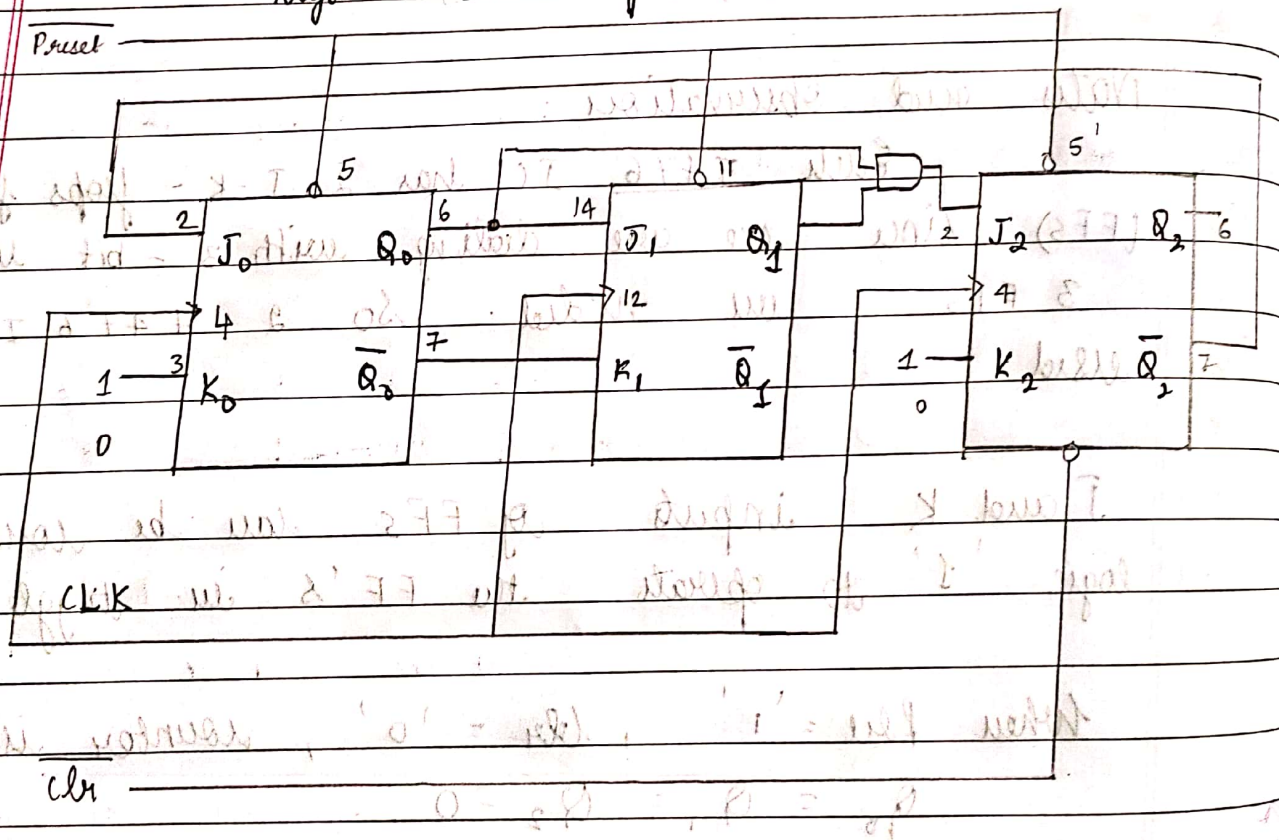
$Q_0 = Q_1 = Q_2 = 1$.

Keep $P_R = '1'$, $M_R = '1'$, for normal count mode.

Pin details : IC 74109 (IC 7476)

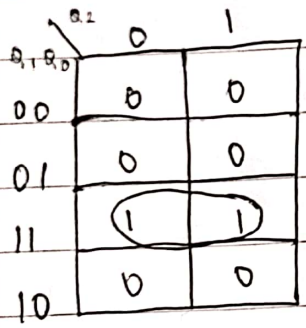


Logic circuit for mod-6 counter

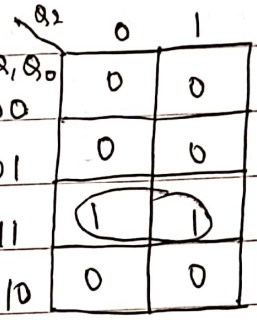


Mod 8

Present State			Next State			Excitation Table					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	0	1	1	1	1
0	1	0	0	1	1	0	0	0	0	1	1
0	1	1	1	0	0	1	1	1	1	1	1
1	0	0	1	0	1	0	0	0	0	1	1
1	0	1	1	1	0	0	0	1	1	1	1
1	1	0	1	1	1	0	0	0	0	1	1
1	1	1	0	0	0	1	1	1	1	1	1

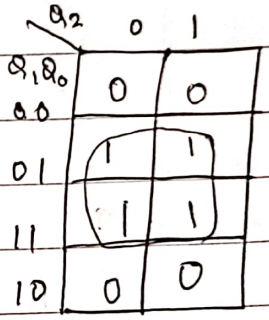


$J_2 = Q_1 Q_0$

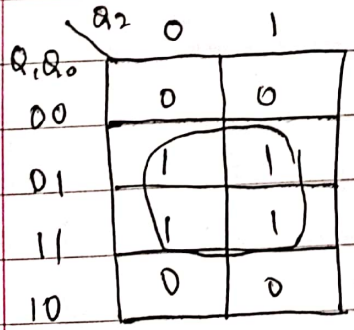


$K_2 = Q_1 Q_0$

$\overline{K_2} = \overline{Q_1 Q_0}$

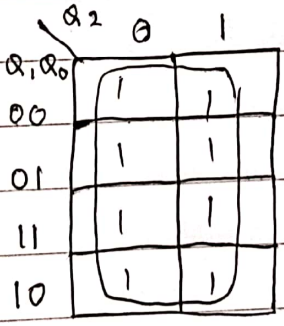


$J_1 = Q_0$

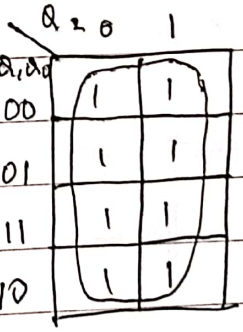


$K_1 = Q_0$

$\overline{K_1} = \overline{Q_0}$



$J_0 = 1$



$K_0 = 1$

$\overline{K_0} = 0$

Logic circuit for mod - 8 counter