1. Half Adder
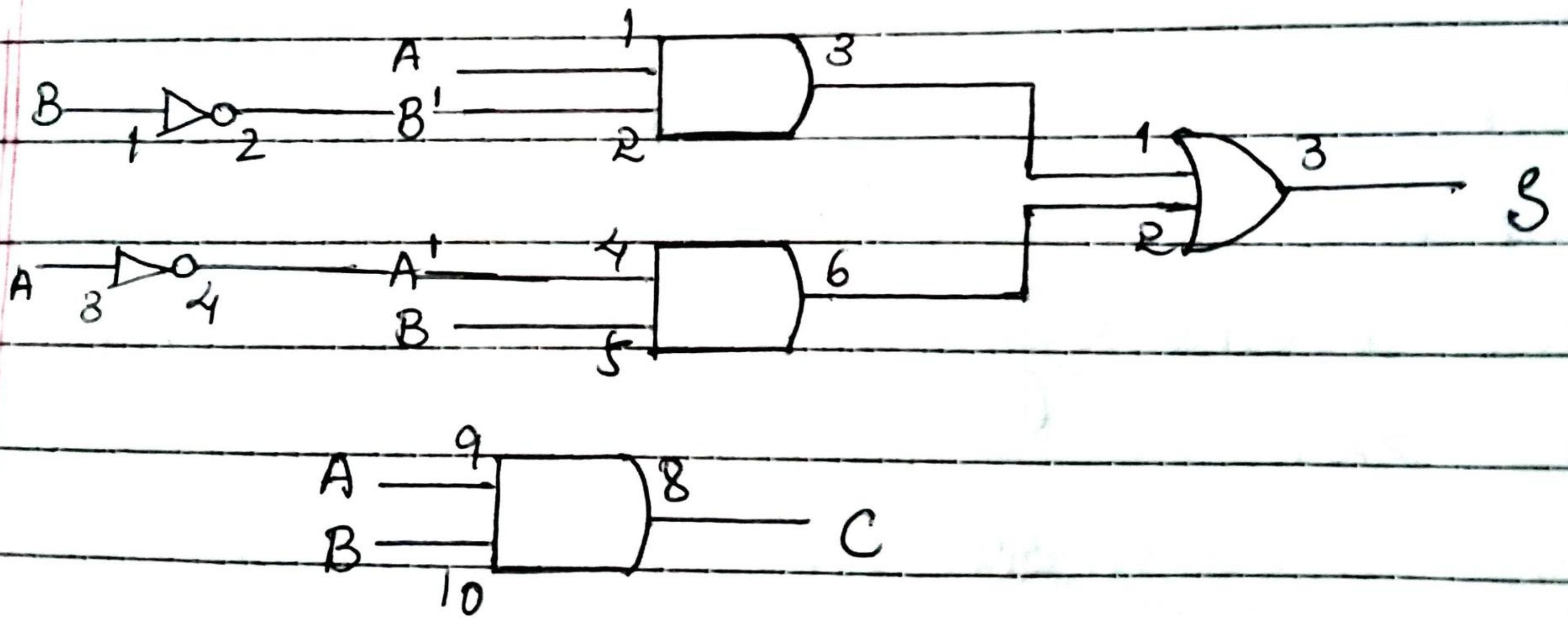
- The half adder add digits A and B.
- It has two outputs S
- The carry signal rep into the next digit of addition.

Truth Table :

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Using basic gate

A

B $\xrightarrow{}$ B' 1 ─┐
  1   2   2 ─┘ AND gate (1,2 → 3)

A $\xrightarrow{}$ A' 4 ─┐
  3   4   5 ─┘ AND gate (4,5 → 6)

OR gate (1,2 → 3) → S

A ─── 9 ─┐
B ───   └── 8 ── C
     10

Full Adder [Using K-map].

Input			Output	
A	B	C_{IN}	C_{OUT}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

2. Full Adder

A ----> Full
B ----> Adder ----> Sum
C ----> ----> Carry

Sum:

$$\overline{A}\,\overline{B}\,C_{in}$$

$$\overline{A}\,\overline{B}\,C_{in} + \overline{A}B\overline{C}_{in}$$

$$\overline{A}B\overline{C}_{in}$$

$$A\overline{B}\,\overline{C}_{in}$$

$$A\overline{B}\,C_{in} + ABC_{in}$$

$$Y = \overline{A}\,\overline{B}\,C_{in} + \overline{A}BC_{in} + A\overline{B}\,\overline{C}_{in} + ABC_{in}$$

$$Y = A \oplus B \oplus C_{in}$$

Carry:

$$A\overline{B}$$

$$A\overline{B}\,C_{in}$$

$$\overline{A}B$$

$$\overline{A}BC_{in}$$

$$AB$$

$$Y = A\overline{B}\,C_{in} + \overline{A}BC_{in} + AB$$
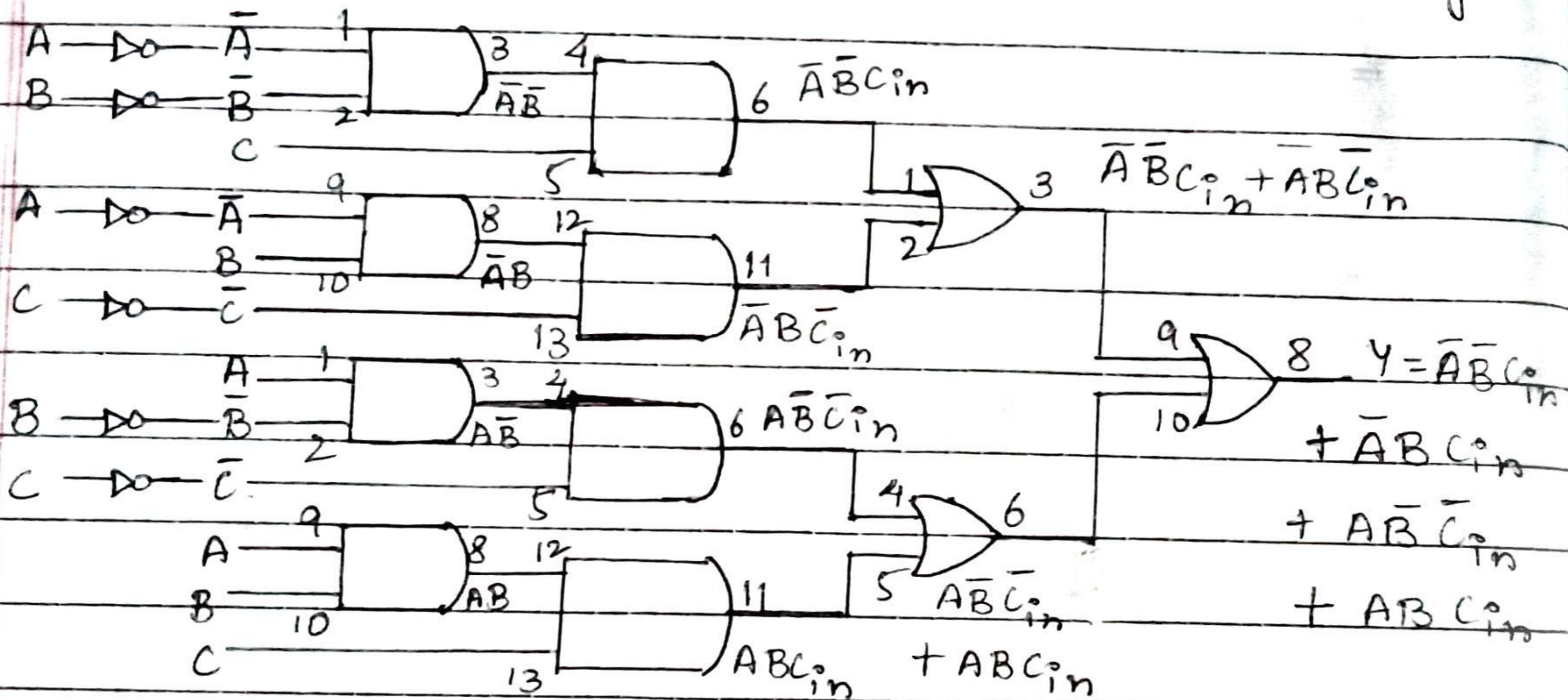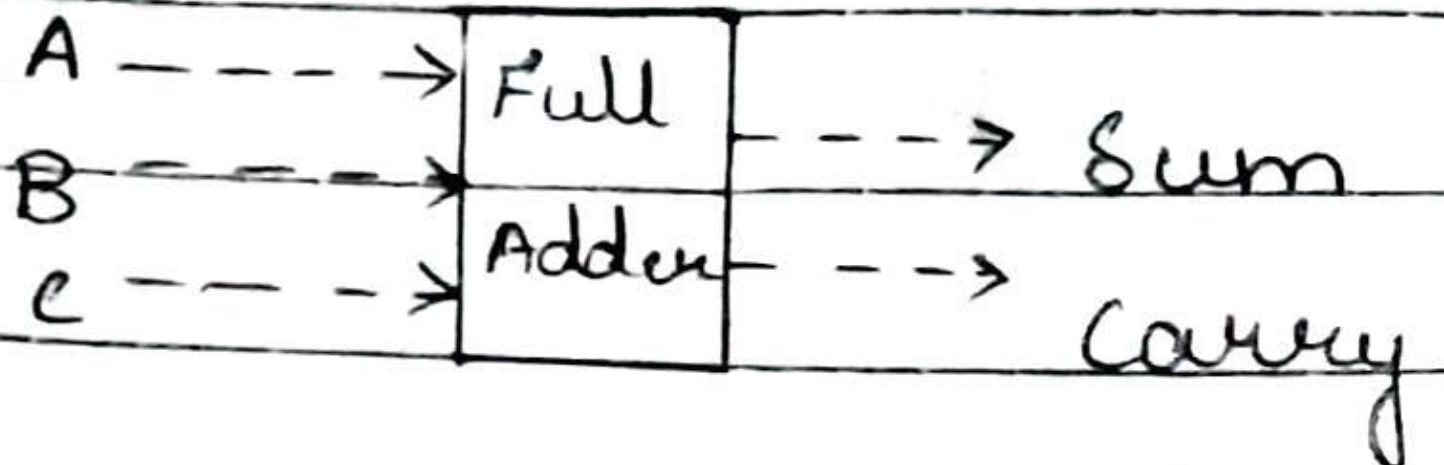
$$Y = AB + C_{in}(A \oplus B)$$
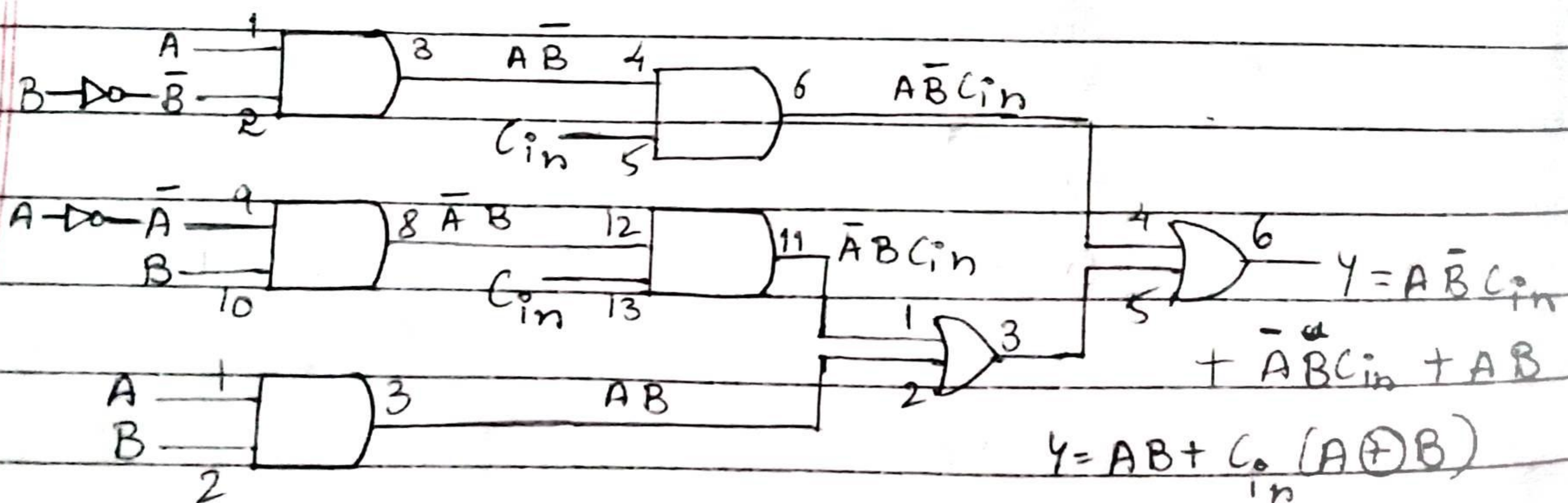
3. Half Subtractor

- Half subtractor subtrac[...] digits A & B.
- It has two outputs di[...] borrow (B).
- Borrow signal represe[...] digit of multi digit [...]

Truth Table:

Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

X

Y

Using AND-OR:

B $\xrightarrow{1}$ ▷o $\xrightarrow{2}$ $\bar{B}$

A $\overline{A}$

1
2 — $A\bar{B}$

3

A $\xrightarrow{3}$ ▷o $\xrightarrow{4}$ $\bar{A}$

4
5
6 — $\bar{A}B$

$D = A \oplus B$

A $\xrightarrow{5}$ ▷o $\xrightarrow{6}$ $\bar{A}$

B

9
10
8 — $B = \bar{A}B$
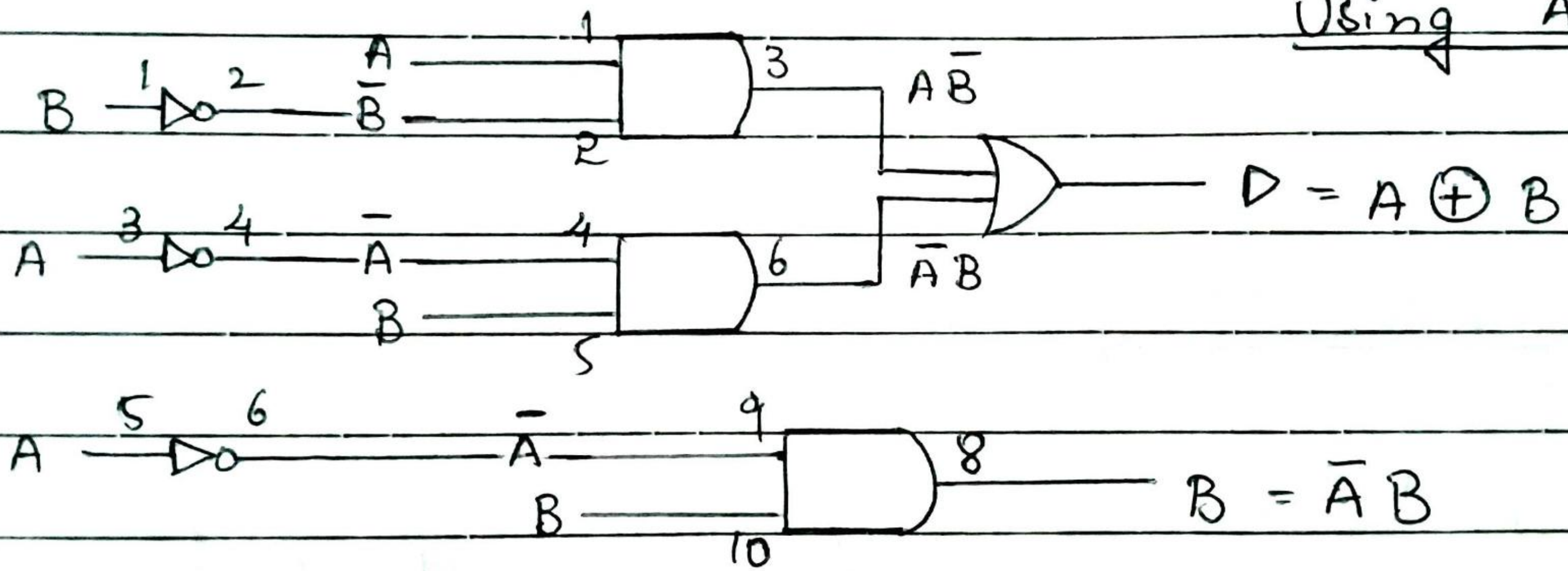
4. Full Subtractor

Truth Table :

Input			Output	
A	B	C_{in}	Br	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Top circuit (SUM):

A ─1
B ──2─ B̄ ──2 →³ A B̄ 4 → 6 A B̄ Cim̄
Cim ──4 Cim
5

A ─5─6─ Ā ─9 → 8 R
B ──8─9─ B̄ ─10   Ā B̄ 13 12 11 Ā B̄ Cim
Cim 13

A ─1
B ──2 →³ 4 AB 5 → 6 ABCim 4 5 6
Cim

A ─10─11─ Ā ─9 → 8 Ā B̄ 12 11 13 Ā B Cim̄
B ─13─ B̄ ─10
Cim ─12─13 Cim̄

A B̄ Cim̄
A B̄ eim + Ā B̄ Cim   1 3 2

A B̄ Cim

9 8 → Y
10

= Ā B Cim
+ Ā B̄ Cim̄
+ Ā B̄ C

A B Cim + Ā B̄ Cim + AB

or

Y = A ⊕ B ⊕ C
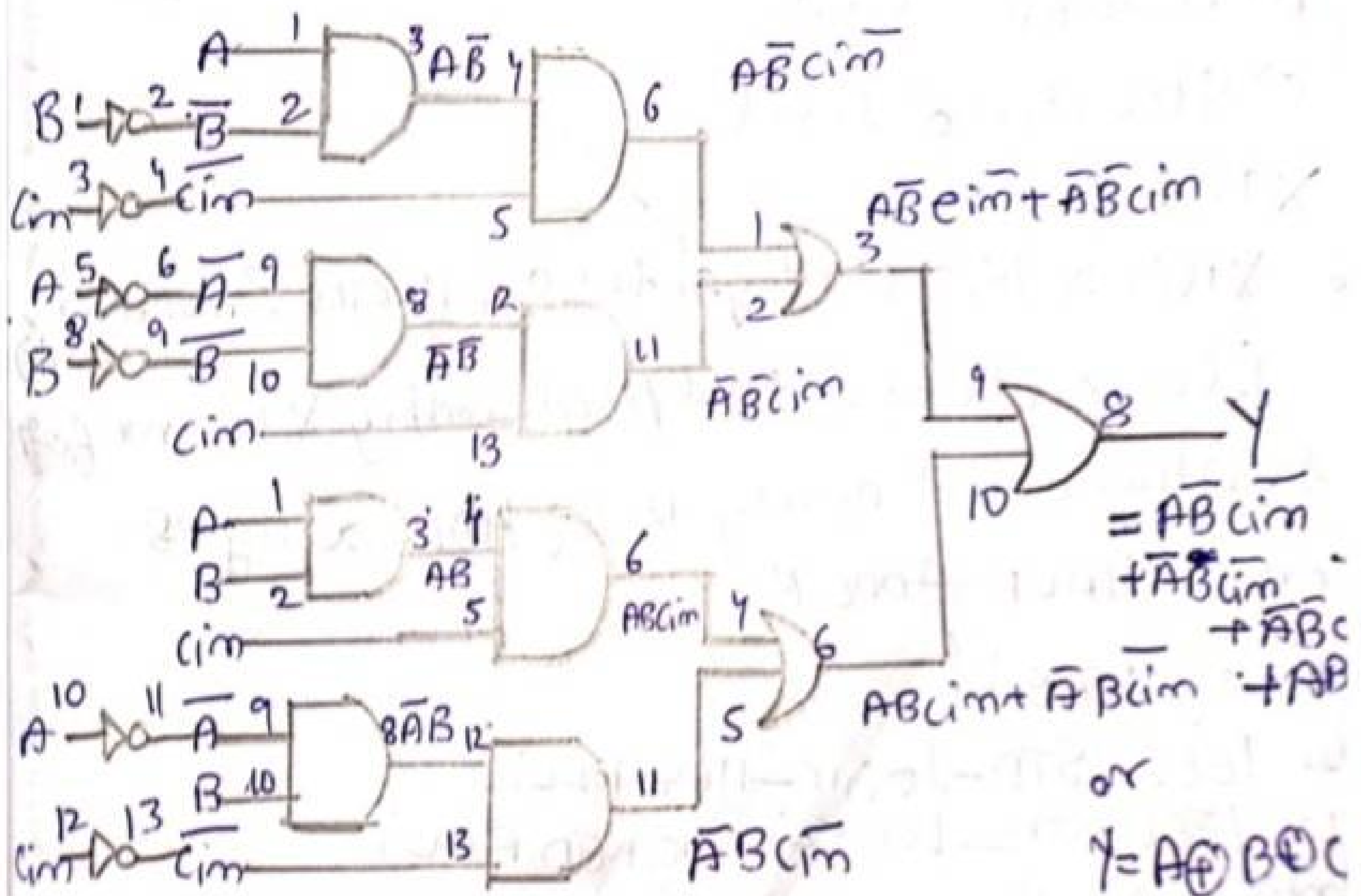
Scanned with CamScanner

Bottom circuit (CARRY):

Ā ─1
B ─2 →³ Ā B 1 →³ Ā B + Ā B̄ Cim
Ā B̄ 6 9 8 Ā B̄ Cim 2

B̄ ─5
Cim ─10

A ─1
B ─2 AB 5 → 6 ABcim 4 5 → 6 Y
Cim

Ā B + Ā B̄ Cim

Y = Ā B + Ā B̄ Cim
+ ABcim
or
Y = Ā B + Cim(A⊕B)

VHDL
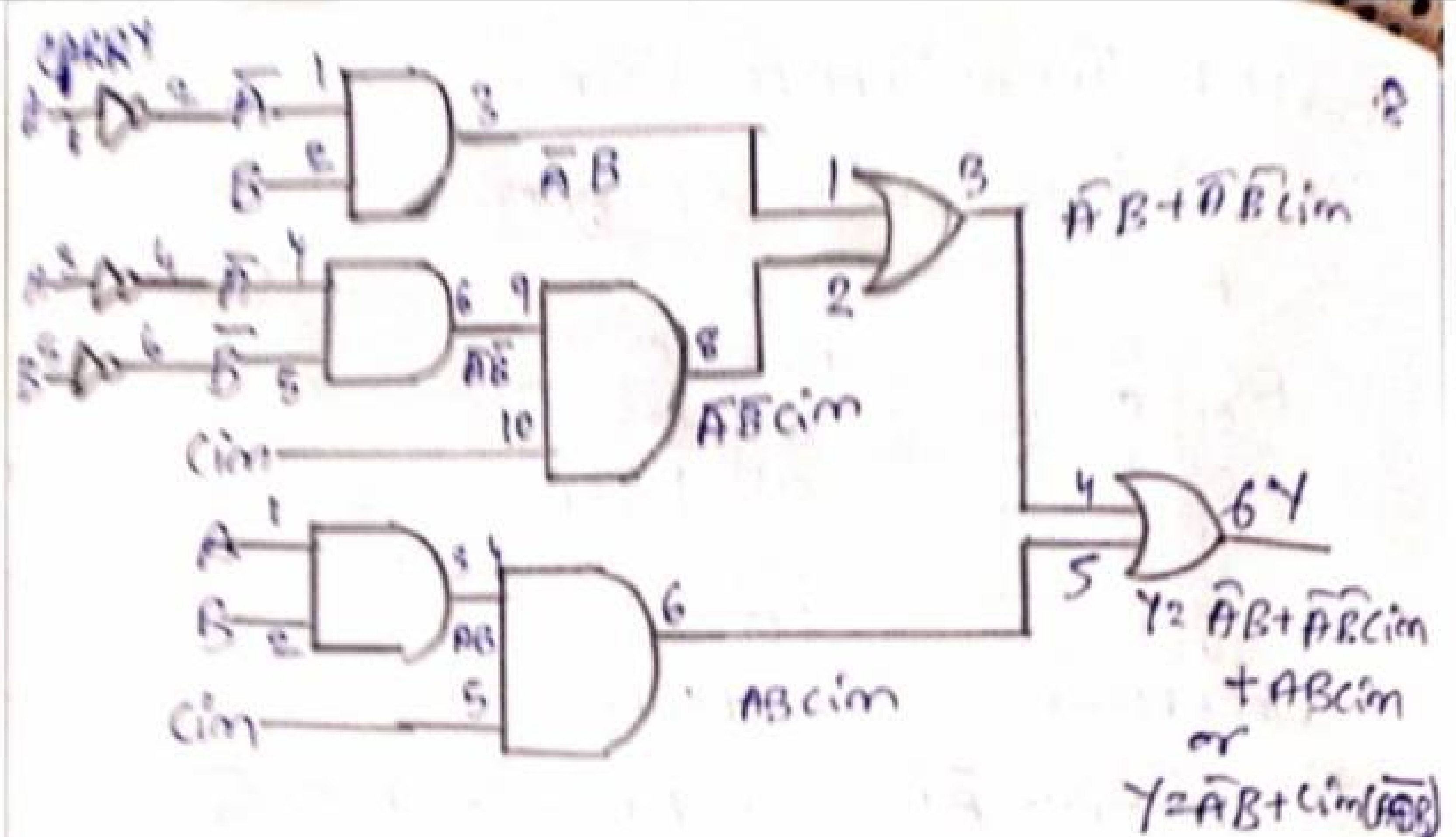
Scanned by TapScanner

Binary Input				Gray Code Output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0

1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	0	1	0	0	0

K-map

B3   B2   B1   B0

G3

Ga

G1

G0
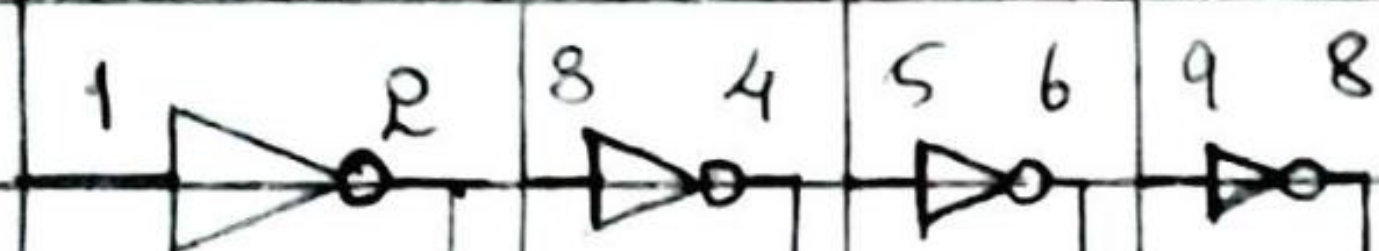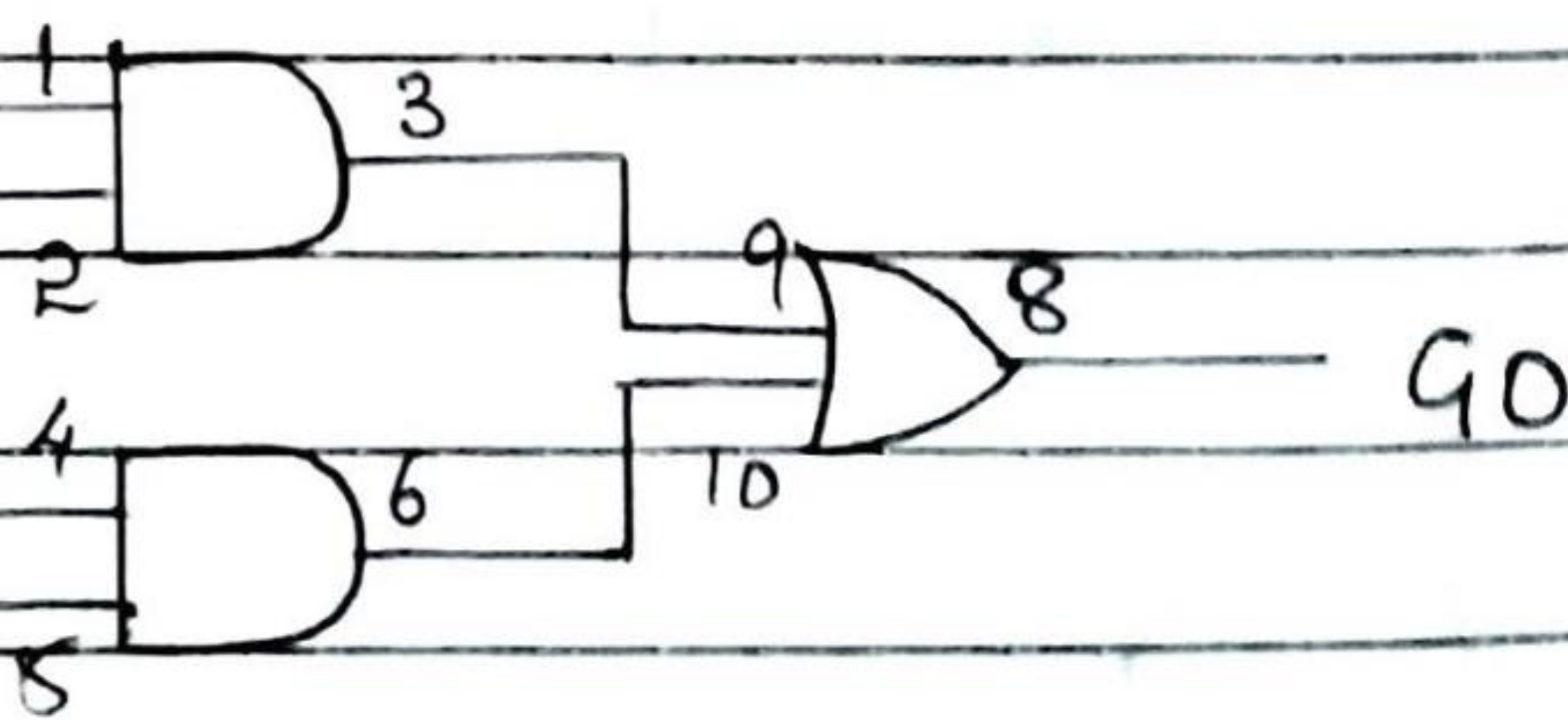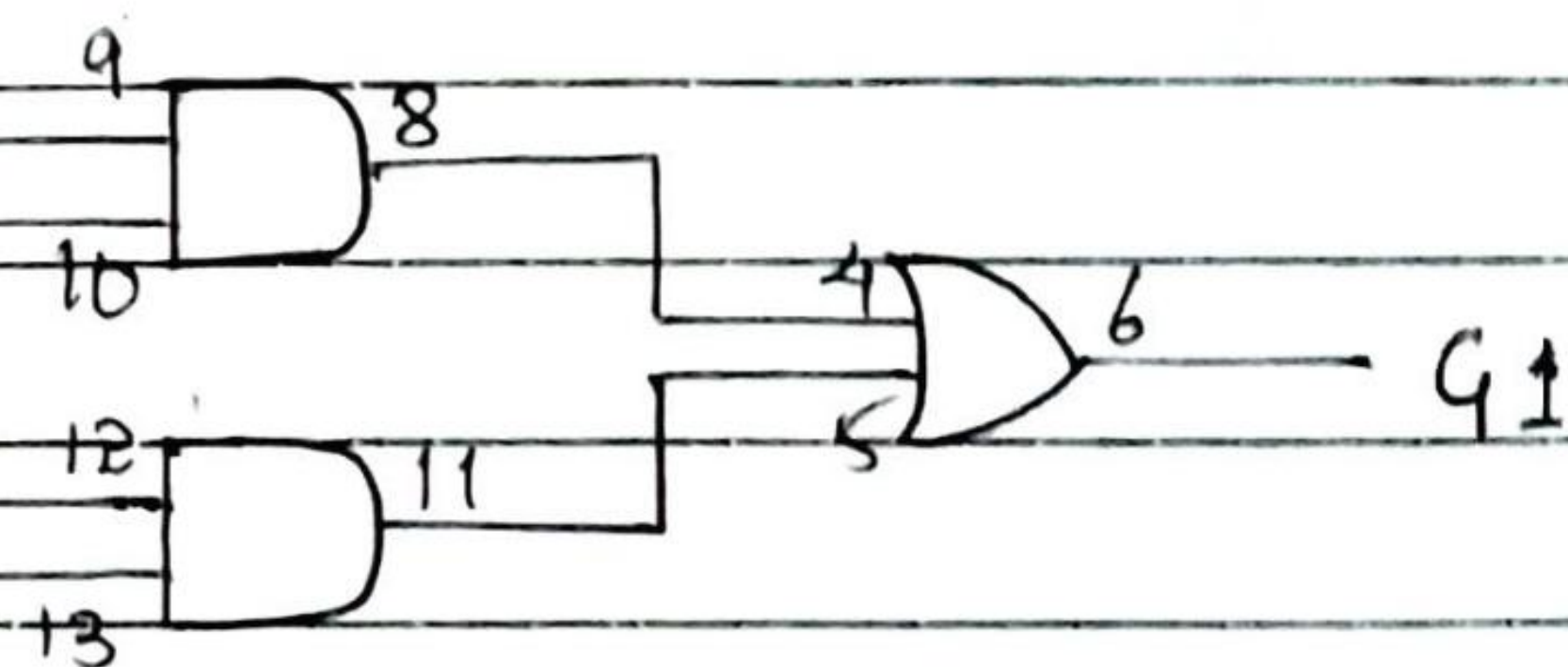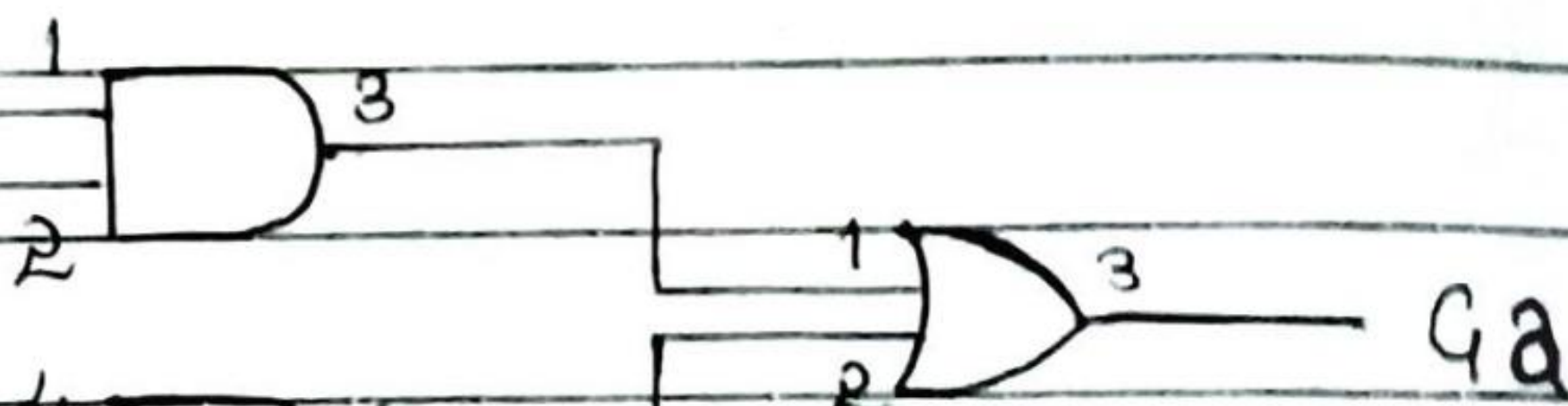
Gray to Binary :

Gray Code Input				Binary Code Output			
$G3$	$G2$	$G1$	$G0$	$B3$	$B2$	$B1$	$B0$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0

0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	01	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	01	1	1	1	0	1
1	0	0	01	1	1	1	0
1	0	0	0	1	1	1	1

G3 G2 G1 G0

1 2 3 4 5 6 7 8

B3

1 2

1 3
2

4 6 1 3
5 2

B2

3 4

9 8
10

12 11 4 6
13 5

B1

5 6

1 3
2

4 6 9 8
5 10

B0

V1
10V

U1
555_TIMER_RATED

X SC1

Exl Trig

A   B

VCC

R1
7.2KΩ

RST   OUT

DIS

R2
2.6KΩ

THR

D1

TRI

DIODE
_VIRT-
-UAL

CON

GND

C1
100µF

C2
10nF

V1
15V

R1
10KΩ

R2
110KΩ

C1
100μF

R3
5KΩ/2.5KΩ/3.3KΩ

U1
741

7 1 5

3 +

2 −

6

4

V2
15V

XBC1

Ext Trig

A   B
+   −   +   −