

## TWO STAGE CE AMPLIFIER

Objective: To design a two stage R-C coupled common Emitter amplifier with given specifications.

specifications: Gain of stage I = 20

Gain of stage II = 40

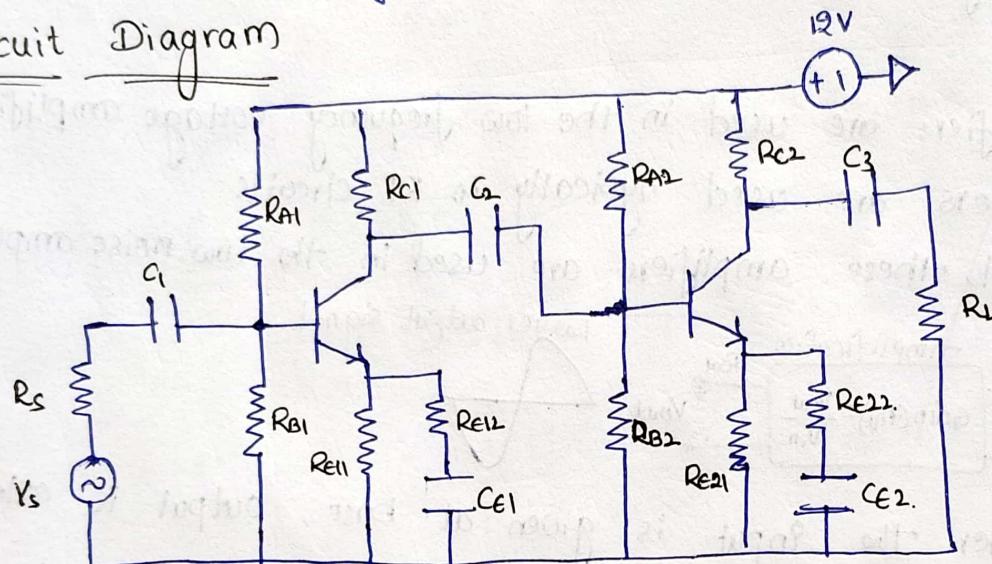
function generator source resistance =  $50\Omega$

Load Resistance =  $4.7\text{ k}\Omega$

Bandwidth 20Hz - 20 KHZ.

$\beta$  range (100-200).

### Circuit Diagram



Theory: The process of increasing the strength of weak input signal in terms of voltage, current or power is known as amplification. When we cascade 2 CE amplifiers the gain gets multiplied so the overall gain is very high.

\* Why CE is used for high voltage / current gain?

• High transconductance ( $g_m$ )

• The current gain ( $\beta$ ) of a transistor amplifies the input signal.

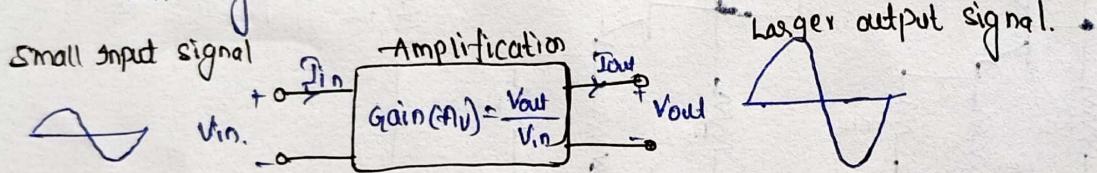
• The voltage gain is  $A_V \approx -g_m R_C$  (approximately), where  $R_C$  is the collector resistance.

- ⇒ Collector Load Effect:
  - A large collector resistance ( $R_C$ ) increases the output voltage gain, enhancing gain.
- ⇒ Phase Reversal:
  - CE amplifiers provide  $180^\circ$  phase shift, making them useful for signal processing.
- ⇒ Efficient power gain:
  - CE amplifiers offer both current gain and voltage gain, leading to high power gain compared to CB or CC configurations.

This makes CE amplifiers widely used in audio amplification, signal processing, and communication circuits.

### Applications:

- The CE amplifiers are used in the low-frequency voltage amplifiers
- These amplifiers are used typically in RF circuits
- In general, these amplifiers are used in the low noise amplifiers.



In CE amplifier the input is given at base, output is collected at collector and emitter is common for both base & collector terminal.

- \* Now, we design CE amplifier by considering the following conditions:
  1. Designed to achieve maximum voltage swing.
  2. Gain is independent of variation in  $V_{be}$  and  $\beta$ .
  3.  $I_C$  is independent of  $\beta$
  4. Power consumption is less than 200 mW.

## Stage two calculations:

$$V_{CC} = 12V \text{ (given)}$$

$\rightarrow V_C = \frac{V_{CC}}{2} = 6V$  ( $\because$  To avoid clipping of output signal i.e. to get maximum voltage swing).

$$\rightarrow V_E = 0.1V_{CE} = 1.2V.$$

$$V_{BE} = 0.7 \text{ V (for active region)}$$

$$V_B - V_E \geq 0.7$$

$$\rightarrow V_B \geq 1.9V$$

$$\rightarrow \text{gain} = \frac{-g_m(R_C || R_L)}{1 + g_m R_E'}$$

$$I_{C2} = \frac{V_{CE}}{2R_{C2}} \quad \text{as} \quad R_{C2} \ll R_L.$$

$$\text{Let us consider } R_{C2} = 560\Omega; P = \frac{(6)^2}{560} = 64.8mW \ll 200mW$$

$$\therefore I_{C2} = \frac{6}{560} = 10.71 \text{ mA}$$

$$g_{m2} = \frac{I_{C2}}{V_{th}} = \frac{10.71 \text{ mA}}{25 \text{ mV.}} = 0.4284 \quad (\because V_{th} \approx 25 \text{ mV.})$$

$$\text{for stage 2: } 40 = \frac{-0.4284(560 || 4700)}{1 + 0.4284(R_E')}$$

$$\Rightarrow R_E' = 10.17 \Omega (R_{E22})$$

$$\ast I_{C2} = I_{E2} = 10.71 \text{ mA.}$$

$$\therefore V_E = (I_{E2})(R_{E2})$$

$$1.2 = 10.71 \times 10^3 \times R_E$$

$$R_{E2} = \frac{1.2 \times 10^3}{10.71}$$

$$R_{E2} = 112.$$

$$R_E = R_{E21} + R_{E22}.$$

$$112 = R_{E21} + 10.17$$

$$R_{E21} = 112 - 10.17 = 101.83 \Omega.$$

Here the swamping resistor  $R_{E22}$  provide negative feedback.

capac

- Used to get desired gain

- parameters of transistors like  $\beta$ ,  $I_C$ ,  $V_{th}$  are temperature dependent which effects gain, by emitter resistance we can stabilize the gain.

→ voltage divider to get voltage at base (to get active region)  
& also to make  $I_C$  independent of  $B$ .

$$R_{A2} \parallel R_{B2} \ll \beta R_{E22}$$

The measured  $\beta$  value is 200

$$R_{A2} \parallel R_{B2} \ll (200) \times 10.2$$

$$R_{A2} \parallel R_{B2} \ll 2040$$

$$V_B = \frac{V_{cc} R_2}{R_1 + R_2} \Rightarrow \frac{12 R_2}{R_1 + R_2} \geq 1.9$$

$$\frac{V_{cc} R}{R_1 + R_2} \geq \frac{1}{6}$$

$$\frac{R_1}{R_2} \leq 5$$

Let  $R_2$  i.e

$R_{B2} = 1.5 \text{ k}\Omega$   
 $R_{A2} = 6 \text{ k}\Omega$

calculation of capacitors: (stage 2)

1. capacitor at collector of stage 2: ( $C_3$ )

$$R_{A2} \parallel R_L \gg \frac{1}{2 \times \pi \times f \times C_3}$$

$$C_3 \gg \frac{1}{2 \times \pi \times f \times (R_{A2} \parallel R_L)}$$

$$C_3 \gg \frac{1}{2 \times \pi \times 20 \times 500.38}$$

$$C_3 \gg 15.9 \mu\text{F}$$

for  $f = 20 \text{ Hz}$ :

$$R_{A2} \parallel R_L = 560 \parallel 14 \text{ k}\Omega \\ = 500.38$$



capacitor at emitter ( $C_{E2}$ )

$$(R_{E22} + \frac{1}{g_{m2}}) \parallel R_{E21} \gg \frac{1}{2\pi f (C_{E2})}$$

$$C_{E2} \gg \frac{1}{2\pi f \left[ (R_{E22} + \frac{1}{g_{m2}}) \parallel R_{E21} \right]}$$

$$C_{E2} \gg \frac{1}{2\pi f \times 10 \times 11.13}$$

$$C_{E2} \gg 14.98 \text{ nF}$$

### Stage one calculations:

$$V_{CC} = 12 \text{ V.}$$

$$V_C = 6 \text{ V.}$$

$$V_E = 1.2 \text{ V.}$$

The load for first stage is same as input impedance of second stage.

$$R_{in \text{ stage 2}} = R_{E21} \parallel R_{B21} \parallel \beta R_{E22} + \frac{\beta}{g_{m2}}$$

$$= (6 \text{ k}\Omega) \parallel (1.5 \text{ k}\Omega) \parallel 900(10.17) + \frac{200}{0.4284}$$

$$= 6 \text{ k}\Omega \parallel 1.5 \text{ k}\Omega \parallel 2.5 \text{ k}\Omega.$$

$$= 1.2 \text{ k}\Omega \parallel 2.5 \text{ k}\Omega$$

$$= 810.8 \text{ }\Omega. \text{ (R}_L \text{ of stage one)}$$

Let  $R_{C1} = 590 \Omega$

$$I_{C1} = \frac{V_{CE}}{2R_{C1}} = \frac{12}{2 \times 590} = 10.17 \text{ mA}$$

$$g_{m1} = \frac{I_{C1}}{V_{TH}} = \frac{10.17 \text{ mA}}{25 \text{ mV}} = 0.4068$$

$$\text{gain of stage 1} = A_{v1} = \frac{g_{m1} (R_{C1} \parallel R_{in})}{1 + g_{m1} R_{E12}}$$

$$R_{C1} \parallel R_{in} = 341.5 \Omega$$

$$20 = \frac{0.4068 (590 \parallel 810.8)}{1 + 0.4068 (R_{E12})}$$

$$R_{E12} = 14.6 \Omega$$

$$I_{C1} = I_{E1} = 10.17 \text{ mA}$$

$$V_E = (I_{E1})(R_{E1})$$

$$R_{E1} = \frac{1.2 \times 10^3}{10.17}$$

$$= 118 \Omega$$

$$\therefore R_{E1} = R_{E11} + R_{E12}$$

$$R_{E11} = R_{E1} - R_{E12}$$

$$= 118 - 14.6$$

$$= 103.4 \Omega$$

$$* V_B \geq 1.9V$$

$$\frac{12 R_{B1}}{R_{A1} + R_{B1}} \geq 1.9V \quad \text{and} \quad R_{A1} \parallel R_{B1} < \beta(R_{E12})$$

$$R_{A1} \parallel R_{B1} < (18.6)(14.6)$$

Let

$$R_{A1} \parallel R_{B1} < 2715.6$$

Measured value of  $\beta$  is 186

$$\text{Let } R_{A1} = 4.5 \text{ k}\Omega$$

$$R_{B1} = 1 \text{ k}\Omega$$

$$\text{then } \frac{12(4.5 \text{ k}\Omega)}{5.5 \text{ k}\Omega} > 12 \left( \frac{1 \text{ k}\Omega}{5.5 \text{ k}\Omega} \right) = 2.18 > 1.9V \quad (\text{Active region})$$

$$1 \text{ k}\Omega \parallel 4.5 \text{ k}\Omega = 818.2 \Omega < 2715.6 \Omega$$

$$\boxed{\begin{array}{l} R_{A1} = 4.5 \text{ k}\Omega \\ R_{B1} = 1 \text{ k}\Omega \end{array}}$$

Calculation of capacitors: (Stage 1)

b. capacitor at base of stage 1. ( $C_1$ )

$$(R_{A1} \parallel R_{B1} + R_s) \gg \frac{1}{2\pi f C_1}$$

$$C_1 \gg \frac{1}{2\pi f (R_{A1} \parallel R_{B1} + R_s)}$$

$$C_1 \gg \frac{1}{2\pi f \times 20 \times 868.2}$$

$$C_1 \gg 9.16 \mu\text{F}$$

capacitor at emitter (CE1)

$$(R_{E12} + \frac{1}{g_m1}) \parallel R_{E11} \gg \frac{1}{2\pi f C_{E1}}$$

$$C_{E1} \gg \frac{1}{2\pi f (R_{E12} + \frac{1}{g_m1}) \parallel R_{E11}}$$

$$C_{E1} \gg \frac{1}{2\pi \times 20 \times 14.67}$$

$$C_{E1} \gg 5.45 \mu F$$

3) capacitor b/w collector of stage 1 and base of stage 2

$$(R_{C1} \parallel R_{in}) \gg \frac{1}{2\pi f C_2}$$

$$C_2 \gg \frac{1}{2\pi \times 20 \times (R_{C1} \parallel R_{in})}$$

$$C_2 \gg \frac{1}{2\pi \times 20 \times 341.5}$$

$$C_2 \gg 23.3 \mu F.$$

\* final values of Resistors & capacitors considered to design the

circuit are:

1)  $R_{A1} = 4.5 k\Omega$  (Measured value  $4.41 k\Omega$ )

2)  $R_{B1} = 1 k\Omega$  (Measured value  $934 \Omega$ )  $\beta_1 = 186$

3)  $R_{C1} = 590 \Omega$  (Measured value  $582 \Omega$ )  $\beta_2 = 200$ .

4) \*  $R_{E11} = 103.4 \Omega$  (Measured value  $133 \Omega$ )

5) \*  $R_{E12} = 14.6 \Omega$  (Measured value  $11.5 \Omega$ )

6)  $R_{A2} = 6 k\Omega$  (Measured value  $5.86 k\Omega$ )

7)  $R_{B2} = 1.5 k\Omega$  (Measured value  $1.32 k\Omega$ )

$R_{C2} = 560 \Omega$  (Measured value  $560 \Omega$ )

8)  $R_{E21} = 101.83 \Omega$  (Measured value  $100.3 \Omega$ )

9)  $R_{E22} = 10.17 \Omega$  (Measured value  $10.1 \Omega$ )

10)  $C_1 \gg 9.16 \mu F$  (considered value  $33 \mu F$ )

11)  $C_2 \gg 23.3 \mu F$  (considered value  $100 \mu F$ )

12)  $C_3 \gg 15.9 \mu F$  (considered value  $22 \mu F$ )

13)  $C_{E1} \gg 54.245 \mu F$  (considered value  $1000 \mu F$ )

14)  $C_{E2} \gg 714.98 \mu F$  (considered value  $1000 \mu F$ )

## Result:

- 1) For 2 stage amplifier measured gain  $A = \frac{V_{out}}{V_{in}} = \frac{5V}{5mV} = 1000$ .
- 2) Measured lower cutoff frequency for 80% of max value i.e at  $4V$ . ( $AV=800$ ) is  $25\text{Hz}$
- 3) Measured higher cutoff frequency for  $AV=800$  is  $200\text{kHz}$
- 4) Bandwidth  $= f_H - f_L = 200\text{kHz} - 25\text{Hz}$  ( $\because f_H \gg f_L$ )  
 $= 200\text{kHz}$
- 5). We got gain 1000 instead of 800 it is because of the gain of first stage which is 25 rather 20. By measuring the resistor values with multimeter the Resistors,  $R_{e1}$  &  $R_{e2}$  are not equal to the theoretical calculated values. Hence the gain we got experimentally is higher than expected gain.

→ for  $R_{e2} = 11.5\Omega$

$$\begin{aligned}\text{gain} &= \frac{g_m(R_{e1} || R_e)}{1 + g_m R_{e2}} \\ &= \frac{0.4068(590 || 1810.8)}{1 + 0.4068(11.5)} \\ &= 24.5\%.\end{aligned}$$

## Theory of capacitance

→ we have used the capacitance

1)  $C_1$

connects input signal & base of stage of 1 transistor. blocks DC.

2)  $C_2$  (coupling capacitors)

connects output of stage 1 & input of stage 2. Blocks DC & passes AC signal.

3)  $C_3$  - connects stage 2 output & load. blocks DC.

4)  $C_E$  (Emitter bypass capacitor) - connected in parallel with one of emitter resistance.

5) (other than swamping resistance)

these capacitances are used to increase the ac gain by passing emitter resistance at high frequencies.

5)  $C_E$  → same as  $C_E$

## Frequency Response

the voltage gain of a CE amplifier varies with signal frequency. It is because the reactance of the capacitor in circuit changes with signal frequency and hence effects the output voltage.

The curve drawn between Voltage gain & the signal frequency of an amplifier is known as frequency response.

→ The range of frequencies is divided into three parts

1) at low frequencies: Reactance of capacitance is high. passes only small part of the signal & also capacitors cannot shunt the emitter resistance effectively. causes drop in voltage gain

2) at high frequencies: Reactance of capacitors is relatively small increases loading effect causes gain drop.

3) at mid frequencies: This is a range of frequencies where gain remains constant because, the reactance of capacitors is neither too high nor too low. They allow AC signals pass through them & also bypass emitter resistors effectively.

### Bandwidth

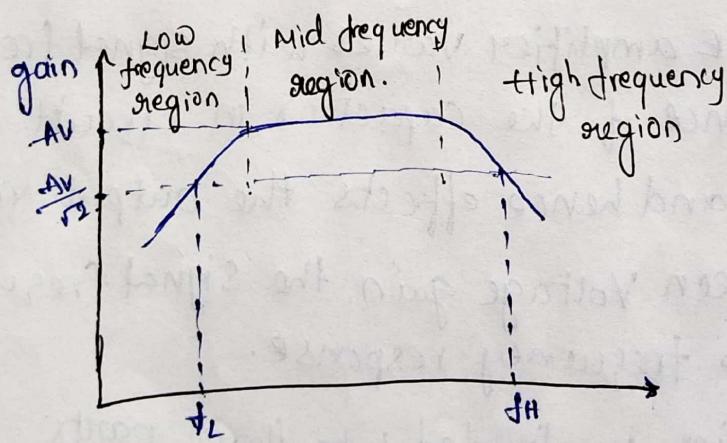
$$\text{Bandwidth} = f_H - f_L$$

$20 \log M = -3 \text{ dB}$  means power of the signal dropped to half of the original value. Voltage dropped to 70% of its value.

$M \approx 0.707$  Experimentally, we got lower-cutoff.

Lower cutoff frequency = 25 Hz

Higher cut-off frequency = 200 kHz



**Results verification sheet****Group No. 08****Experiment No. 2 : Two-Stage CE Amplifier**

All the testing is done with the two stages coupled, and source and load connected.

- Proceed if output has no distortion visible on oscilloscope up to  $\pm 1\text{V}$  at 1 kHz.

- First Stage:**

Designed values:  $I_C = I_E = 10.17\text{mA}$

$$V_C = 6\text{V} \dots$$

$$\text{Swamping resistance value (If required)} = 11.5\Omega$$

Measured values:

$$\text{a) Gain of first stage} = A_1 = \frac{V_{O1}}{V_S} = \frac{125\text{mV}}{5\text{mV}} = 25 \dots$$

$$(\text{The required gain of first stage} = A_1 = 20 \dots)$$

$$\text{b) Collector voltage } V_C \text{ of first stage} = 5.4\text{V} \dots$$

- Second Stage:**

Designed values:  $R_L = 4.7\text{k}\Omega$ ,  $R_{C2} = 560\Omega$

$$I_C = I_E = 10.17\text{mA}$$

$$V_C = 6\text{V} \dots$$

$$\text{Swamping resistance value (If required)} = 10.2\Omega \dots$$

Measured values:

$$\text{a) Gain of second stage} = A_2 = \frac{V_O}{V_{O1}} = \frac{400\text{mV}}{10\text{mV}} = 40 \dots$$

$$(\text{The required gain of second stage} = A_2 = 40 \dots)$$

$$\text{b) Collector voltage } V_C \text{ of second stage} = 6.2\text{V} \dots$$

- Frequency Response:**

Designed values:  $C_1 = 33\text{nF}$ ,  $C_2 = 100\text{nF}$ ,  $C_3 = 22\text{nF}$

$$C_{E1} = 1\text{mF} \dots, C_{E2} = 1\text{mF} \dots$$

Vary input frequency and find the 3 dB cut-off frequencies where output amplitude  $v_o$  drops to 70%.

$$\text{Lower cut-off frequency } (\leq 20 \text{ Hz}) = 25.17 \dots$$

$$\text{Higher cut-off frequency } (> 20 \text{ kHz}) = 200 \text{ kHz} \dots$$