# Computer Organization Lab 4: Pipelined CPU

Due: 2019/6/6

#### 1. Goal

Based on your Lab 3 CPU design, implement a pipelined CPU.

### 2. Homework Requirement

- a. Please use ModelSim or Xilinx as your HDL simulator.
- b. Please attach student IDs as comments at the top of each file.
- c. Please zip the Verilog files and the report and name it as "ID.zip".
- d. You must use the supplied Reg\_File.v
- e. In the top module, please change N to the value which is total lengths of input signal (include data and control) of pipeline register.

(google → verilog+parameter / parameterized modules / 參數式模組)

- f. Your CPU needs to support the following instructions: (80%)
  - i. ADD
  - ii. ADDI
  - iii. SUB
    - iv. AND
    - v. OR
  - vi. SLT
  - vii. SLTI
- viii. LW
  - ix. SW
  - x. BEQ
  - xi. MULT

mult rd, rs, rt; // rd=rs\*rt

0		rs	rt	rd	0	24
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g. Testbench ("CO\_P4\_test\_1.txt"):Use this testbench to test the basic instructions:

```
begin:
addi
          $1,$0,3;
                           // a = 3
          $2,$0,4;
                           // b = 4
addi
addi
          $3,$0,1;
                           // c = 1
                           // A[1] = 3
SW
          $1,4($0);
          $4,$1,$1;
                           // $4 = 2*a
add
          $6,$1,$2;
                           // e = a | b
or
          $7,$1,$3;
                           // f = a \& c
and
          $5,$4,$2;
                           // d = 2*a - b
sub
          $8,$1,$2;
                           // g = a < b
slt
          $1,$2,begin
beq
          $10,4($0);
                           // i = A[1]
lw
```

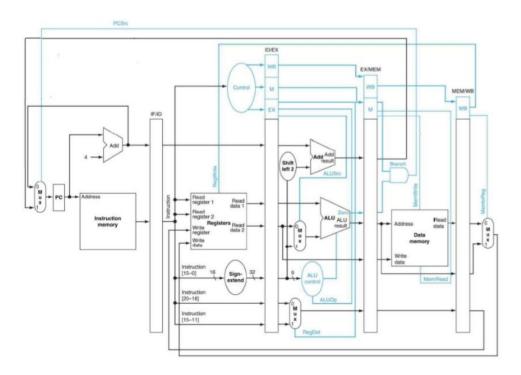
#### h. Bonus: Answer the question below and write it on your report. (20%)

Consider "CO\_P4\_test\_2.txt", try to solve the data hazard of I1/I2, I5/I6, and I8/I9 data dependency. Just modify the machine code of the testbench and test it on your pipeline CPU. (Write down the machine code and show the execution result in your report.)

```
I1:
     addi
                 $1, $0, 16
I2:
     addi
                 $2,$1,4
I3:
     addi
                 $3,$0,8
I4:
     SW
                 $1,4($0)
I5:
     lw
                 $4, 4($0)
I6:
                 $5, $4, $3
     sub
I7:
     add
                 $6,$3,$1
I8:
     addi
                 $7, $1, 10
I9:
     and
                 $8, $7, $3
I10: addi
                 $9,$0,100
```

Hint: You may (1) insert NOP or (2) reorder instructions.

# 3. Architecture Diagram



# 4. Report

- a. Your Architecture
- b. Hardware Module Analysis
- c. Problems You Met and Solutions
- d. Result
- e. Summary

## 5. Grade

- a. **Total:** 120 points (plagiarism will get 0 point)
- b. Report: 20 points (please use pdf format)
- c. Late submission: Score \* 0.8 before 6/13. After 6/13, you will get 0.

# 6. Q&A

If you have any question, it is recommended to ask in the <u>facebook discussion</u> forum.