register File design write regsel [2:0] With Decoder + write clecade[7:0] writedecodeto] writedewnder67 WY-en Wr-en M3-7W 16819 12916 Teg16 regib reg16 reg 16 [15:0] (0) TI Clk TrendoLHRO [15:0] readout K7 [15:0] read regsel Ferol Mux 2 read [0:5] read 2 data [15:0] read (data [15:0]

by Wenklan Mas Yunhe Liu 3/1/2016

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