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Base Band circuit design for ADPLL Synthesizers in nanometer technologies

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Introduction

The All-Digital Phase-Locked Loop (ADPLL) digital electronic circuit that are used in modern electronic communication systems like frequency synthesizer, modulator/demodulator is one of the principal research domains at the Huawei Nice Research Center in Sophia Antipolis.

With the fast evolution of 5G scenarios, important milestones in 5G research and development have been reached and standardization efforts are underway. We are working closely on ADPLL in order to get ready for the commercial launch of the next generation's mobile technology.

The aim of this internship is to leverage cutting edge research to improve the Base Band Digital section of ADPLL Synthesizers; Digital Time converters (DTCs), Time to Digital Converters, (TDC) ALL Digital Phase Frequency Detectors. The challenge is to correctly design and estimate electrical performances. This is an opportunity for R&D in a new advanced high-tech domain using digital processing and machine learning techniques.

CH1 CDR basic structure and principle analysis

1.1 Clock data recovery circuit and phase-locked loop principle

1.1.1 Basic principle of phase-locked loop

1.1.2 Clock data recovery circuit concept

Concept : There are two basic types of signals in digital communication systems: digital signals and clock signals. When the digital signal is clocked with a clock signal, the clock signal marks its signature on the digital signal, that is, the digital signal carries the clock. Figure 1-1 is a simple clock data recovery circuit schematic.

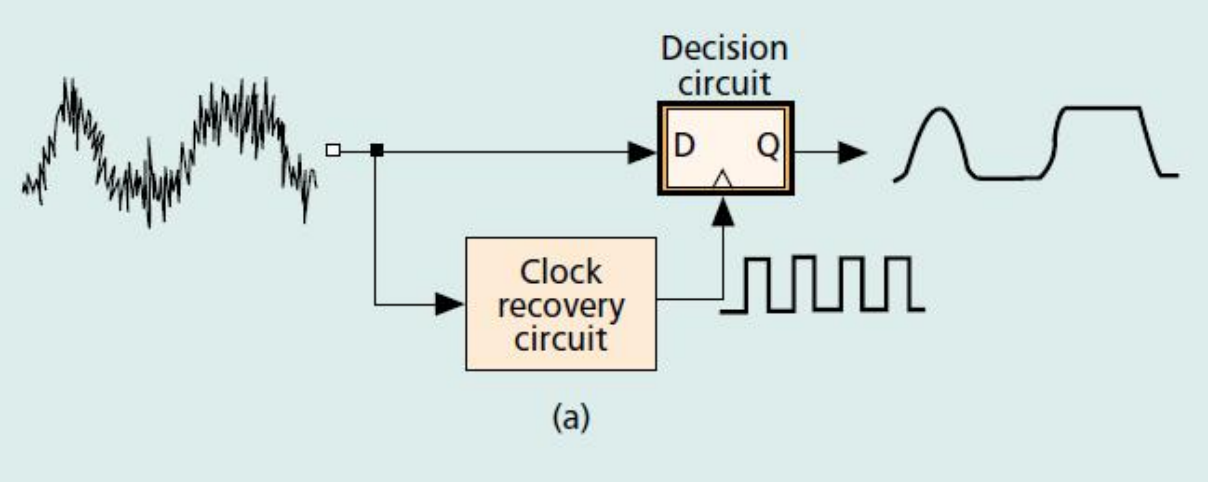

Fig.1-1 Function of CDR circuit

Function : The function of the clock data recovery circuit is the extraction of clock information and data retiming.

Implmentation : The input data first enters the phase detector, the phase detector generates a pulse output related to the difference between the two by comparing the phase relationship between the input data and the voltage controlled oscillator. The current is converted to a control voltage by a low-pass filter, causing the oscillator to change the oscillation frequency until the oscillator is synchronized with the input data, it is locked. The oscillation frequency of the oscillator when it is locked is the extracted clock signal, and the output of the phase detector when it is locked is the retiming data.

1.2 CDR main function module

1.2.1 Principle of phase detector

In the clock data recovery circuit, the phase detector compares the phase between the random input data and the clock signal generated by the voltage controlled oscillator to generate an error signal related to the phase error between the two.

Functions:
• Data transition detection
• Phase difference detection

Through the simple phase detector of the figure below, we can observe that signal B only jumps on the rising edge of the clock, so the output pulse of Y contains the phase error information of the clock and data.

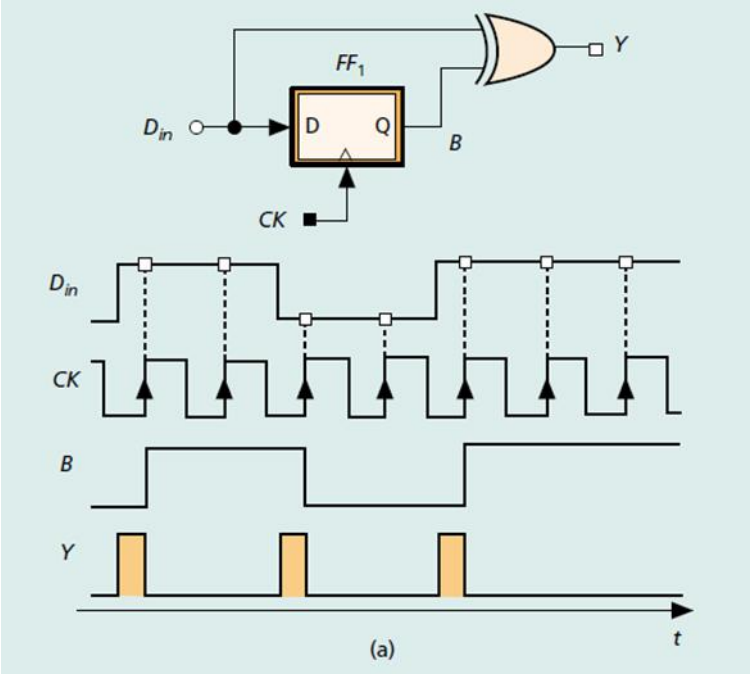

Fig.1-2 Function of phase detector

But its average output is a function of the input data hopping density, and it cannot uniquely represent the varying phase error. In other words, this structure may produce the same DC output level if the input phase changes. In order to overcome the problem of Y=Din⊕B output

and input data density, it needs a reference signal : it can generate a pulse at each data transition; Pulse width is independent of phase difference, independent of input data hopping density.

(1) Linear phase detector (The HOGGE phase detector)

The linear phase detector generates an output signal having a width equal to the phase error of the input data and the feedback clock by comparing the phase relationship. The basic linear phase detector is shown in Figure 1-3.

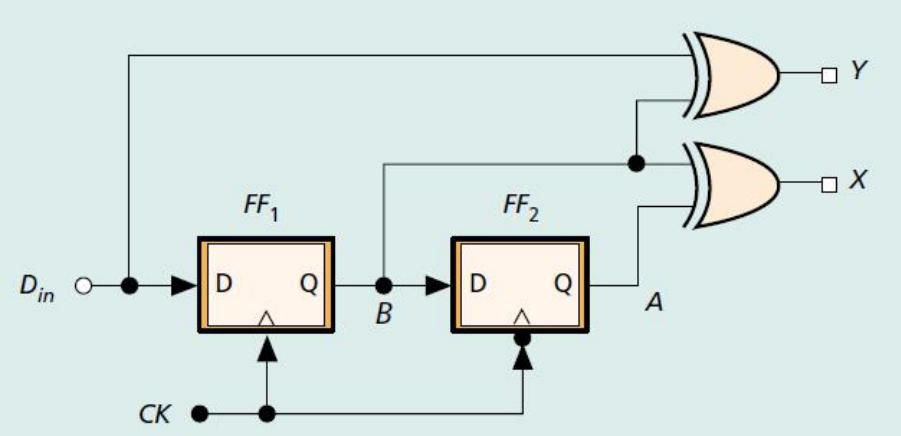

Fig.1-3 Topological structure of Hogge PD

Added a set of DFF and XOR gates, we use the exclusive OR of signal A and signal B as reference signals. The input data Din is XORed with the input data itself through two cascaded D flip-flops to generate a Y signal representing the phase difference and an X signal indicating the data hopping density. The working principle is as shown in Figure 1-4.

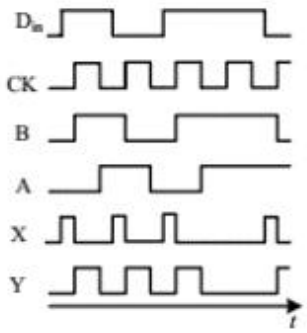

Fig.1-4 Output of Hogge PD

CH2 10Gbps clock data recovery circuit design

2.1 Phase detector design

2.1.1 Hogge phase detector design

According to the above structural diagram, we can know that the hogge phase detector consists of two D flip-flops and two XOR gates. The functionality of these modules is implemented by Verilog code.

```
//Verilog HDL for "STAGE", "DFF" "functional"


module DFF ( out, CK, D, VDD, VSS );

  output reg out;
  input wire D;
  input wire CK;
  inout wire VDD;
  inout wire VSS;


supply1 vdd;
supply0 gnd;

assign VDD = vdd;
assign VSS = gnd;

always@(posedge CK)

begin
out<=D;
end

endmodule
```

Fig.2-1 Verilog code of DFF

```
//Verilog HDL for "STAGE", "DFFinv" "functional"


module DFFinv (out, VDD, VSS, CK, D );
  output reg out;
  inout wire VDD;
  input wire D;
  inout wire VSS;
  input wire CK;


supply1 vdd;
supply0 gnd;

assign VDD = vdd;
assign VSS = gnd;

always@(negedge CK)

begin
out<=D;
end

endmodule
```

Fig.2-2 Verilog code of DFF Conversely

```
//Verilog HDL for "STAGE", "XOR" "functional"


module XOR ( Y, A, B );

  input wire A;
  output wire Y;
  input wire B;

assign Y = A^B;


endmodule
```

Fig.2-3 Verilog code of XOR gate

The modules are respectively generated corresponding symbols, and the modules are connected according to the topology map. The schema obtained is as follows.

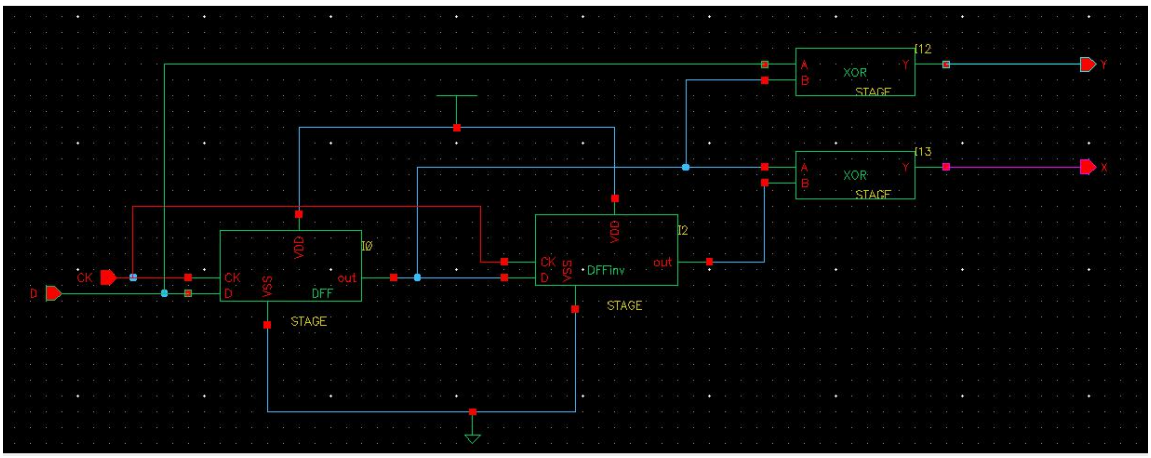

Fig.2-4 Schematic of Hogge phase detector

Next, the phase detector is also generated as a symbol and connects the two input, clock and data signals to the power supply.

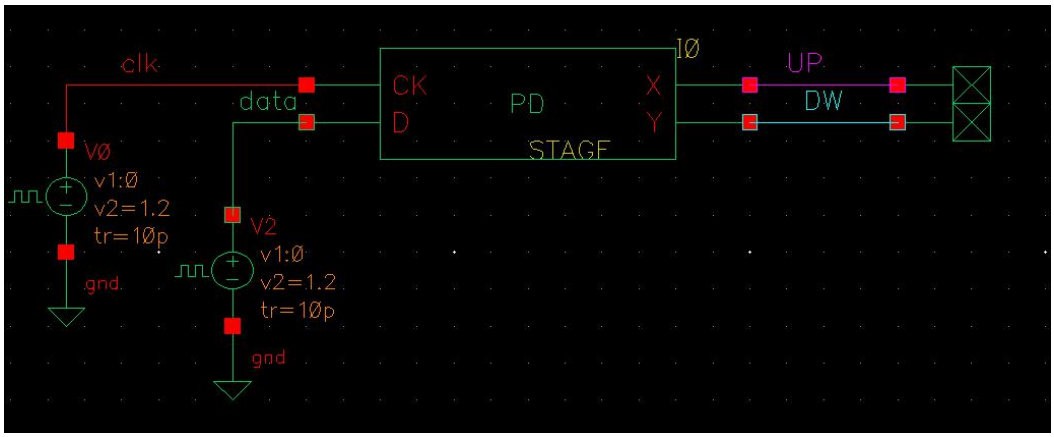

Fig.2-5 Schematic of the test of Hogge PD

The power supply is a pulse signal, the frequency of the data signal is 10Gbps, and their parameter settings are as follows.

Voltage 1	0 V
Voltage 2	1.2 V
Period	1/10e9/2 s
Delay time	10p+delay s
Rise time	10p s
Fall time	10p s
Pulse width	1/10e9/4-10p s

Fig.2-6 Parameters settings of clock signal

Voltage 1	0 V
Voltage 2	1.2 V
Period	1/10e9 s
Delay time	10p s
Rise time	10p s
Fall time	10p s
Pulse width	1/10e9/2-10p s

Fig.2-7 Parameters settings of data signal

Set the delay to 10ps, 50ps, and simulate, and get the following results.

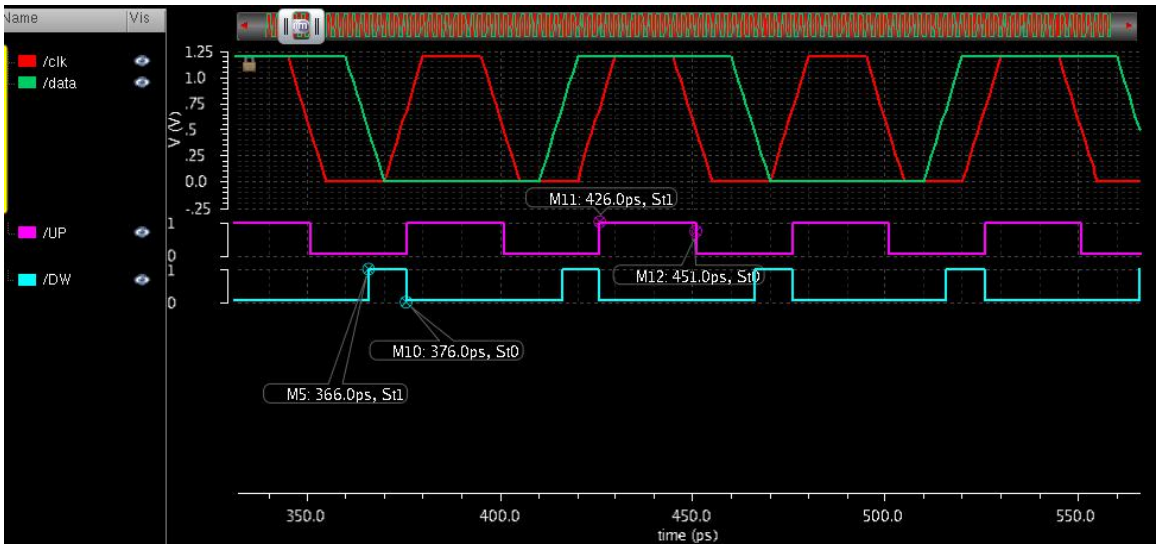

Fig.2-8 Result of simulation (delay = 10ps)

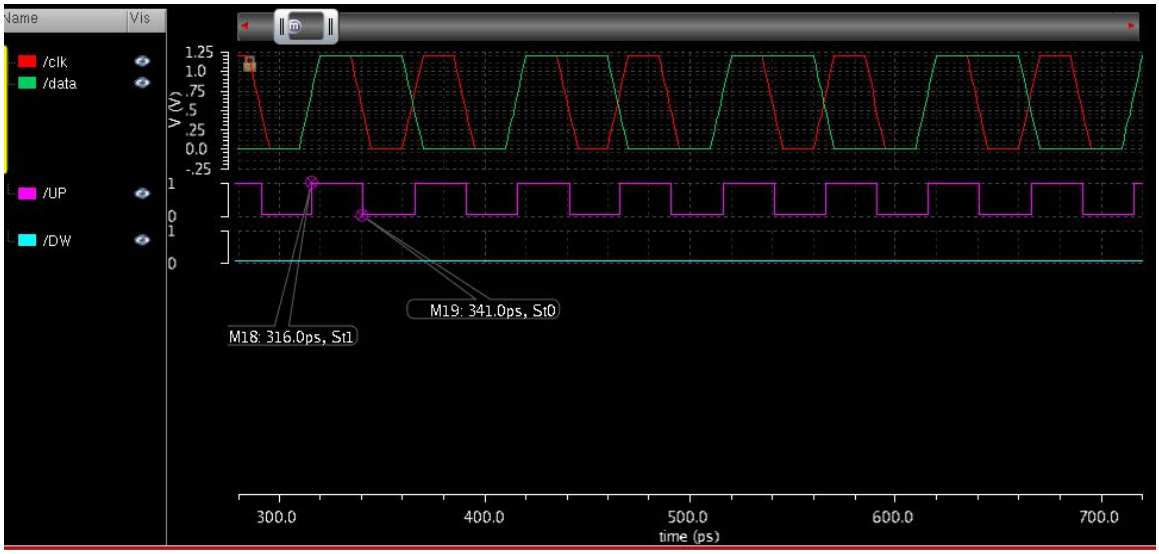

Fig.2-9 Result of simulation (delay = 50ps)

We can observe that the output DOWN is generated by data hopping, the pulse width is proportional to the phase difference between the clock and the data, and the other output UP pulse width is half of the clock period, which is 25ps.

Next I will design an alexander phase detector and a half rate phase detector to select the most suitable phase detector by comparing their performance.