

**MAO Yuqing**

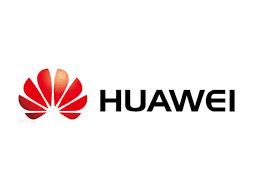
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**06410 BIOT**

Report of the Final Intership

**Base Band circuit design for ADPLL Synthesizers in nanometer technologies**



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**SUMMARY**

**THANKS**

I am grateful to the HUAWEI company for giving me such an internship opportunity, let me go to the society to get in touch with the knowledge of the school books, and let me grow my knowledges and open my eyes.

Thanks to my person in charge, Mr.Pasquale LAMANNA, who gave me the first experience in the industry and taught me a lot in digital circuit and other aspects during the work, help me master my work skills in such a fast time, solve problems, tolerate my mistakes and let me keep improving.

In addition, I would like thank Mr.Yoann Charlon and Mr.Leonardo Lizzi for the help and advice on the missions mentioned in this report.

I also thank the colleges from the Personnel department, the IT department, and the directors with all they can in their respective domains with patience .

Thanks to them, this internship was a rewarding experience from a professional but also personal point of view.

**INTRODUCTION**

1. **Introduction of the intership**

This internship was proposed by HUAWEI Nice Reserch Center. In this intership, i am closely integrated into a team of RF and Synthesizers experts and thus benefit from the knowledge and experience of the inter-disciplinary team based in Sophia Antipolis. The aim of this internship is to leverage cutting edge research to improve the Base Band Digital section of ADPLL Synthesizers; Digital Time converters (DTCs), Time to Digital Converters, (TDC) ALL Digital Phase Frequency Detectors. The challenge is to correctly design and estimate electrical performances. This is an opportunity for R&D in a new advanced high-tech domain using digital processing and machine learning techniques.

The All-Digital Phase-Locked Loop (ADPLL) digital electronic circuit that are used in modern electronic Communication systems like frequency synthesizer, modulator/ demodulator is one of the principal research domains at the Huawei Nice Research Center in Sophia Antipolis.

With the fast evolution of 5G scenarios, important milestones in 5G research and development have been reached and standardization efforts are underway. HUAWEI is working closely on ADPLL in order to get ready for the commercial launch of the next generation's mobile technology.

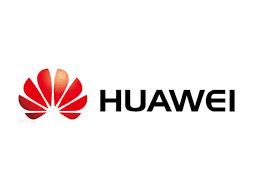
The specific internship contents of this time are :

* Design Base Band circuits for Digital Phase Detection
* Be responsible of top level validation of such circuits in the complete system Understand and root cause the observed issues
* Develop the layout for silicon foundry and take care of electrical characterization of circuits .

1. **Introduction of the company**

Founded in 1987, Huawei Technologies is a leading global information and communications technology (ICT) solutions provider. Driven by a commitment to sound operations, ongoing innovation, and open collaboration, we have established a competitive ICT portfolio of end-to-end solutions in telecom and enterprise networks, devices, and cloud technology and services. Our ICT solutions, products, and services are used in more than 170 countries and regions, serving over one-third of the world's population. With 180,000 employees, Huawei is committed to enabling the future information society, and building a Better Connected World. Huawei ranked 83th on the Global Fortune 500 based on its revenue in 2016. In 2016, the company’s revenue reached approximately USD 75.1 billion, with a 32% increase YOY and a solid increase in profits and cash flow.

Huawei provides customers with competitive, secure and reliable products, solutions and services in the fields of communication networks, IT, smart terminals and cloud services. It cooperates with eco partners to create value for customers, release personal potential and enrich families. Life, stimulate organizational innovation. Huawei insists on continuous innovation around customer needs, increases basic research investment, and accumulates the world's progress.



**3. CDR basic structure and principle analysis**

3.1 Basic principle of phase-locked loop

The phase-locked loop is a closed-loop automatic control system that tracks the phase of the input signal. It locks the input reference clock and outputs a series of frequency-stable clocks with modulation tracking for high-performance modulation and demodulation. The figure 3-1 is the most basic phase-locked loop block diagram and consists of three basic components: phase detector (PD), loop filter (LF) and voltage controlled oscillator (VCO).

Phase Detector

Loop Filter

Voltage Controlled Oscillator

Fig.3-1 Structure of basic PLL

The principle and function of each module are as follows :

1. The phase detector is a phase comparison device that compares the phase of the output signal with the reference signal to produce an error voltage for the instantaneous phase difference between the two signals.
2. The function of the loop filter is to filter out the high frequency components and noise of the error voltage to ensure the required performance and stability of the loop.
3. The voltage controlled oscillator is controlled by a voltage, and voltage causes the frequency of the voltage controlled oscillator to approach the reference frequency, that is, the difference between the two becomes smaller and smaller until the difference is eliminated and locked. The phase difference between the two signals after locking appears as a fixed stable value.

It can be seen that the phase tracking effect of the phase-locked loop can finally realize that the output signal is synchronized with the reference signal, and there is no frequency difference between the two.

3.2 Clock data recovery circuit

3.2.1 Clock data recovery circuit Concept

There are two basic types of signals in digital communication systems: digital signals and clock signals. When the digital signal is clocked with a clock signal, the clock signal marks its signature on the digital signal, that is, the digital signal carries the clock. Figure 3-2 is a simple clock data recovery circuit schematic.

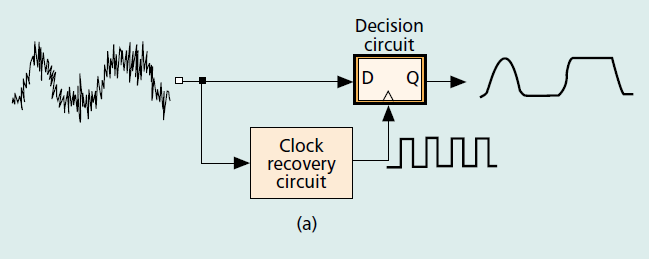
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Fig.3-2 Function of CDR circuit

Function : The function of the clock data recovery circuit is the extraction of clock information and data retiming.

3.2.2 Clock data recovery circuit implmentation

There are usually three ways to implement data recovery. The first is a phase-locked loop-based architecture, the second is a data oversampling based phase picking technique, and the third is a phase interpolation technique. This article uses a PLL-based clock recovery data circuit, so only a simple introduction to the PLL-based clock data recovery circuit. The circuit of Fig.3-3 operates as follows.

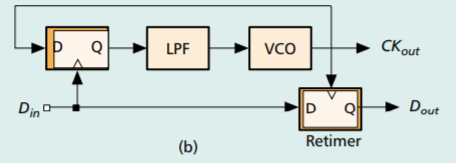


Fig.3-3 An example of CDR implmentation

The input data first enters the phase detector, the phase detector generates a pulse output related to the difference between the two by comparing the phase relationship between the input data and the voltage controlled oscillator. The current is converted to a control voltage by a low-pass filter, causing the oscillator to change the oscillation frequency until the oscillator is synchronized with the input data, it is locked. The oscillation frequency of the oscillator when it is locked is the extracted clock signal, and the output of the phase detector when it is locked is the retiming data.

3.3 Comparison of CDR and PLL

Compared with the phase-locked loop, the input of the clock data recovery circuit is a high-speed random data, and the whole circuit works at a high speed state, which makes the design of the clock data recovery circuit very complicated, which is mainly reflected in two aspects.

On the one hand, in the phase-locked loop circuit, the phase detector tracks a low-speed reference clock, and in the clock data recovery circuit, the phase detector tracks a high-speed random data; on the other hand, in order to accurately phase the random data, it is necessary to be able to detect the hopping of the data. At the same time, due to the randomness of the data, there may be a continuous sequence of 0 or 1 of the long sequence, which causes the VCO oscillation frequency to drift. Therefore, when there is no data transition, it should be ensured that the phase detector will not generate phase comparison information. The combination of the above aspects makes the design of the clock data recovery circuit extremely challenging.

3.4. CDR main function module --- Phase Detector

3.4.1 Principle of phase detector

In the clock data recovery circuit, the phase detector compares the phase between the random input data and the clock signal generated by the voltage controlled oscillator to generate an error signal related to the phase error between the two.

Functions:

• Data transition detection

• Phase difference detection

Through the simple phase detector of the figure.3-5 below, we can observe that signal B only jumps on the rising edge of the clock, so the output pulse of Y contains the phase error information of the clock and data.

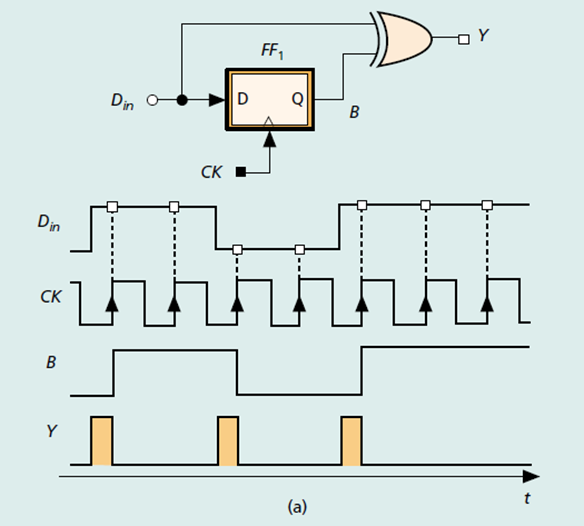


Fig.3-5 Function of phase detector

But its average output is a function of the input data hopping density, and it cannot uniquely represent the varying phase error. In other words, this structure may produce the same DC output level if the input phase changes. In order to overcome the problem of Y=Din⊕B output and input data density, it needs a reference signal : it can generate a pulse at each data transition; Pulse width is independent of phase difference, independent of input data hopping density.

* Linear phase detector (The HOGGE phase detector)

The linear phase detector generates an output signal having a width equal to the phase error of the input data and the feedback clock by comparing the phase relationship. The basic linear phase detector is shown in Figure 3-6.

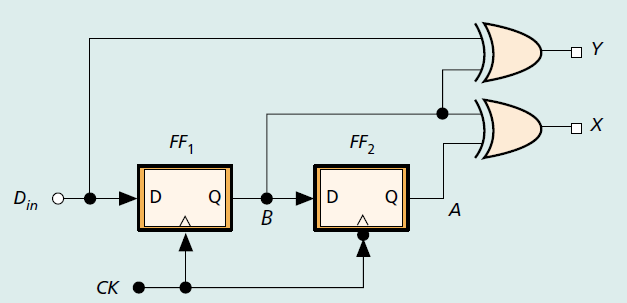


Fig.3-6 Topological structure of Hogge PD

The Hogge phase detector is a typical linear phase detector. As shown in the figure 3-6, the input NRZ signal passes through two D flip-flops. One of the D flip-flops samples the input data signal on the rising edge of the clock, and the other D flip-flop samples on the falling edge. According to the waveform diagram, the three signals, Din, A and Dout pass through two XOR gates, and the resulting signal has a linear phase detection characteristic. One of the output Y pulses is generated on the data transition edge, the pulse width is proportional to the phase difference between the clock and the data, and the other output X pulse width is half of the clock period. The working principle is as shown in Figure 3-7.

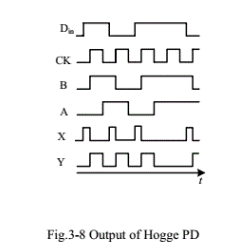
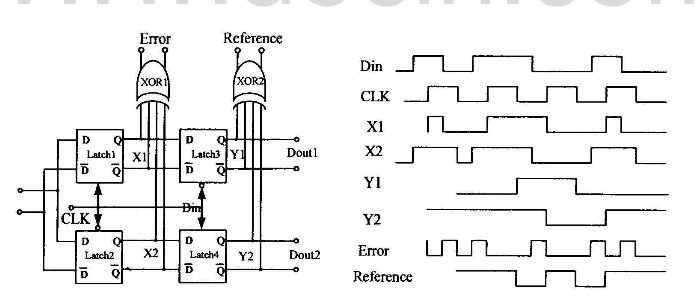
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Fig.3-7 Output of Hogge PD

**4. High-frequency Phase detector design**



1. (b)

Fig.4-1 Hogge Phase Detector

The circuit structure of the Hoggle phase detector is shown in Figure 4.1(a), which is the classic structure of the linear phase detector. The Hogge phase detector consists of four latches and two XOR gates. The operating timing is shown in Figure 4.14(b). The output of Latch l and the output of Latch 2 are XORed to obtain the error signal Error. The output of Latch 3 and the output of Latch 4 are XORed to obtain the reference signal Reference. The difference between the two signals can accurately reflect the phase difference between the clock and the input data.

4.1 Latch design

The circuit structure of the CML latch used in this design is shown in Figure 4-2. It consists of the input pair tube M1, M2, the differential clock pair tube M5, M6, the cross-coupling latch pair tube M3, M4, the tail current source Itail and two resistors with a resistance of R. The working principle of the latch is: when Clk+ is high and Clk- is low, M5 is turned on, M6 is turned off, and the input signal Din is output to Dout through M1 and M2, and the latch operates in the sampling state; When Clk+ is low and Clk- is high, M5 is turned off, M6 is turned on, Dout is not affected by Din, and M3 and M4 keep the output signal unchanged by positive feedback. At this time, the latch operates in the hold state.

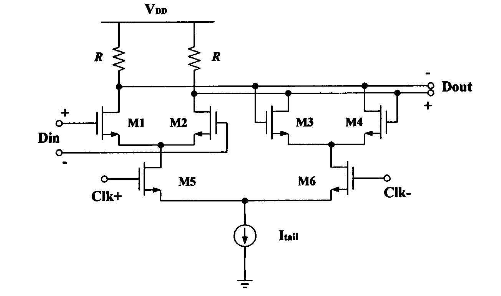


Fig.4-2 CML Latch circuit

The logic level of the CML register output is determined by the current Itail of the tail current source and the load resistance R. The high level VH is the power supply voltage VDD, and the low level VL is (VDD-Itail\*R). It is therefore possible to change the output logic level by changing Itail or R. In general, reducing the swing by reducing the resistance can increase the operating speed of the circuit, but this is not the case in circuits with particularly high speeds. The output logic level of the latch of this design is (0.8V-1.2V). Under the premise of ensuring the output logic level is unchanged, the operating speed of the circuit can be increased by increasing the current Itail of the tail current source and reducing the load resistance R, because this can reduce the RC time constant of the circuit and the pendulum of the output signal rate. The current Itail of the tail current source is not as large as possible. As the Itail increases, the working speed of the CML latch first becomes larger and then becomes smaller, and there is an optimum value. The Itail of this design is set to 500uA.

4.2 D Flip-flop design

The latch described above is actually a level trigger. When the clock is high, the latch samples: When the clock is low, the latch keeps the output voltage constant. The flip-flop is edge-triggered, which uses the rising or falling edge of the clock to sample the data and output it. The flip-flop used in this design consists of two master-slave connections, as shown in Figure 4-3, where the latch uses the CML circuit shown in Figure 4-2.

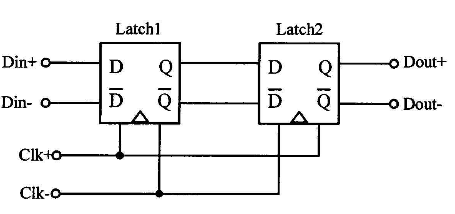


Fig.4-3 Structure of D Flip-flop

As can be seen from Figure 4-3, the input clock signals of the two latches are reversed, and their operation timing is shown in Figure 4-4. When the clock signal is high, Latch1 operates in the sampling state, Latch2 operates in the hold state, and the output signal remains unchanged. When the clock signal is low, Latch1 operates in the hold state, Latch2 operates in the sampling state, and the output voltage is Latch1. The voltage that is held, that is, the falling edge is triggered. The rising edge trigger can be realized by reversing the clock signals of Latch1 and Latch2.

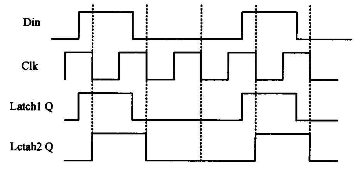


Fig.4-4 D Flip-flop diagram

4.3 High speed XOR gate design

The circuit structure of the high-speed XOR gate used in this design is shown in Figure 4-5. The XOR gate works as follows: When the input signal D1 is high level and D2 is high level, M1 and M4 are turned on, and M2 and M3 are turned off. At this time, both XA and XB are low level, and both M5 and M6 are off. At the cutoff, no current flows through the RL and the output is high. Similarly, when D1 is low and D2 is low, it outputs a high level. When the input signal D1 is high level and D2 is low level, M1 and M2 are turned on, and M3 and M4 are turned off. At this time, XA is low level, XB is high level, that is, M5 is turned off, M6 is turned on, and current is passed. RL, output low level. Similarly, when D1 is low and D2 is high, it outputs low. Therefore, when D1 and D2 are the same, no current passes through the resistor RL; when D1 and D2 are different, there is a current passing through the resistor RL, that is, the current through the resistor RL is in an exclusive OR relationship with the input signals D1 and D2.

Like the CML register, the logic level of the high-speed XOR gate output is determined by the current I of the tail current source and the load resistance R. The high level Vh is the power supply voltage VDD, and the low level V1 is (VDD-I\*RL). It is therefore possible to change the output logic level by changing I or RL.

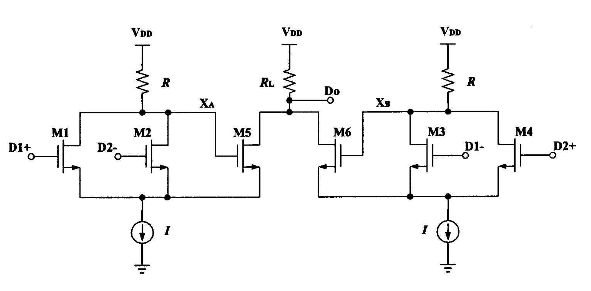


Fig. 4-5 High speed XOR gate circuit

2.1.1 Hogge phase detector design (10Gbps)

According to the above structural diagram, we can know that the hogge phase detector consists of two D flip-flops and two XOR gates. The functionality of these modules is implemented by Verilog code.

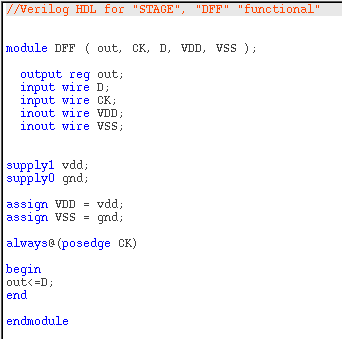


Fig.2-1 Verilog code of DFF

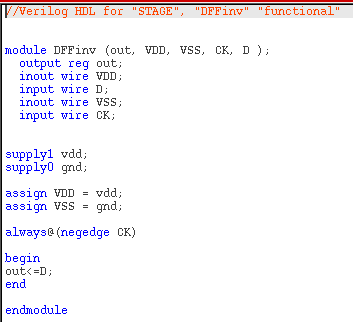


Fig.2-2 Verilog code of DFF Conversely

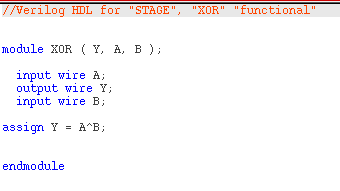


Fig.2-3 Verilog code of XOR gate

The modules are respectively generated corresponding symbols, and the modules are connected according to the topology map. The schema obtained is as follows.

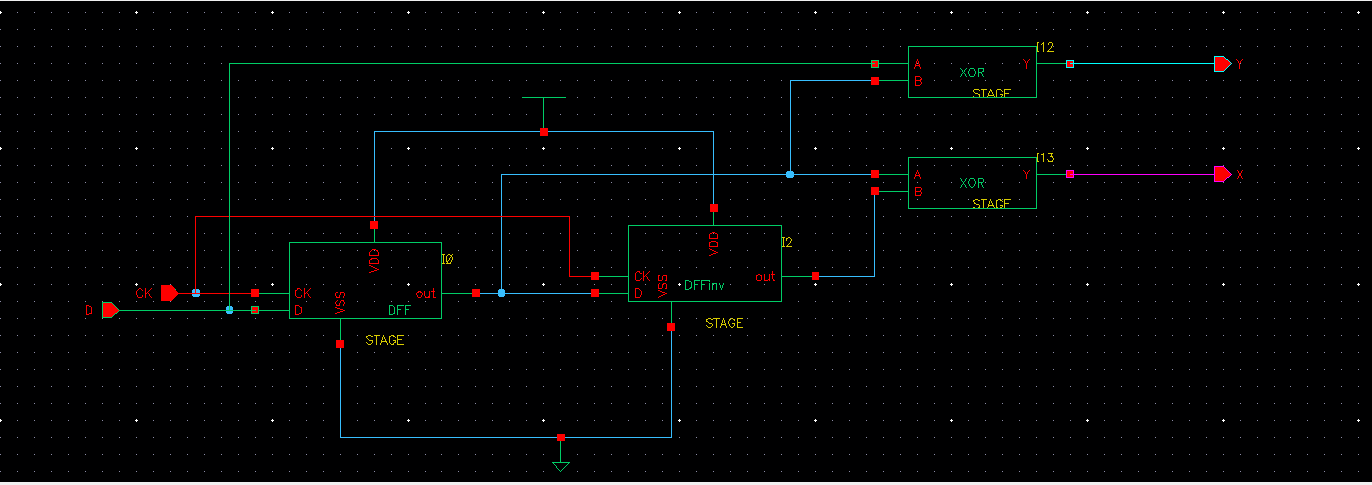


Fig.2-4 Schematic of Hogge phase detector

Next, the phase detector is also generated as a symbol and connects the two input, clock and data signals to the power supply.

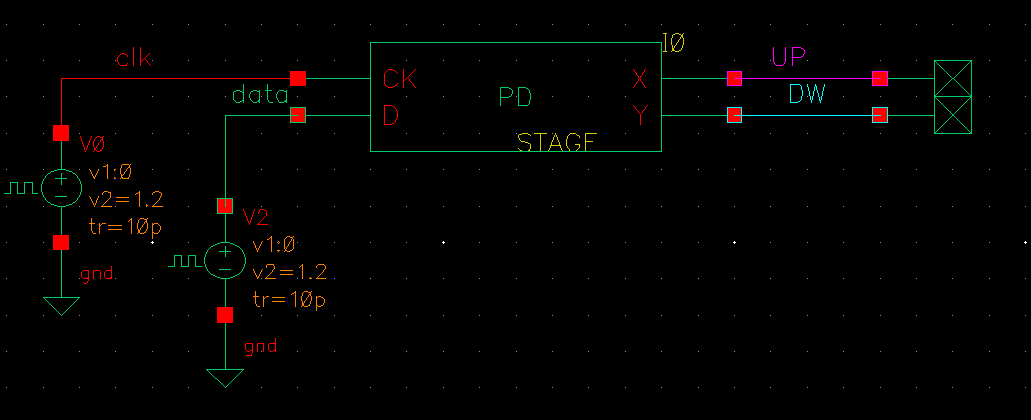


Fig.2-5 Schematic of the test of Hogge PD

The power supply is a pulse signal, the frequency of the data signal is 10Gbps, and their parameter settings are as follows.

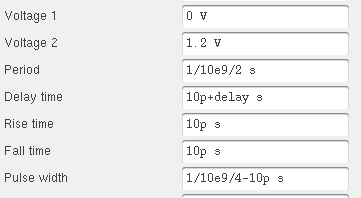
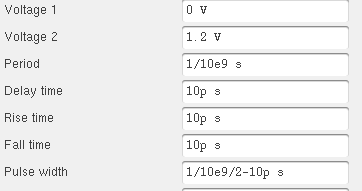
 

Fig.2-6 Parameters settings of clock signal Fig.2-7 Parameters settings of data signal

Set the delay to 10ps, 50ps, and simulate, and get the following results.

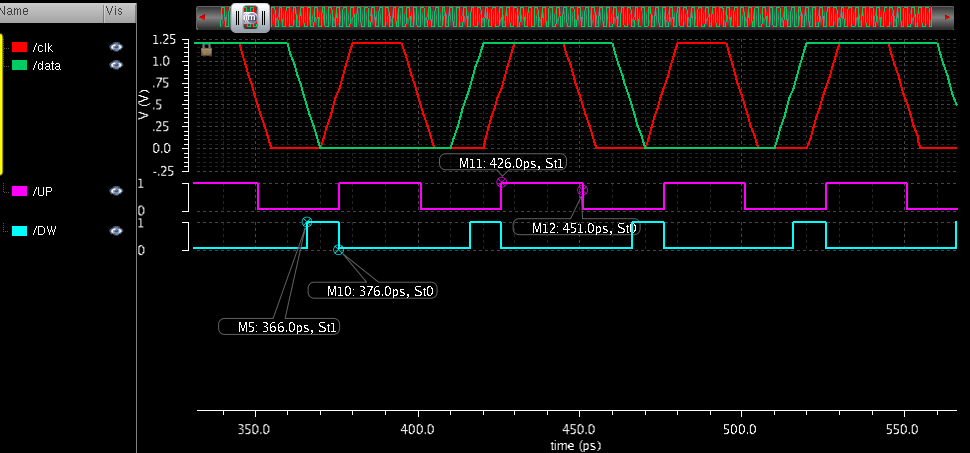


Fig.2-8 Result of simulation (delay = 10ps)

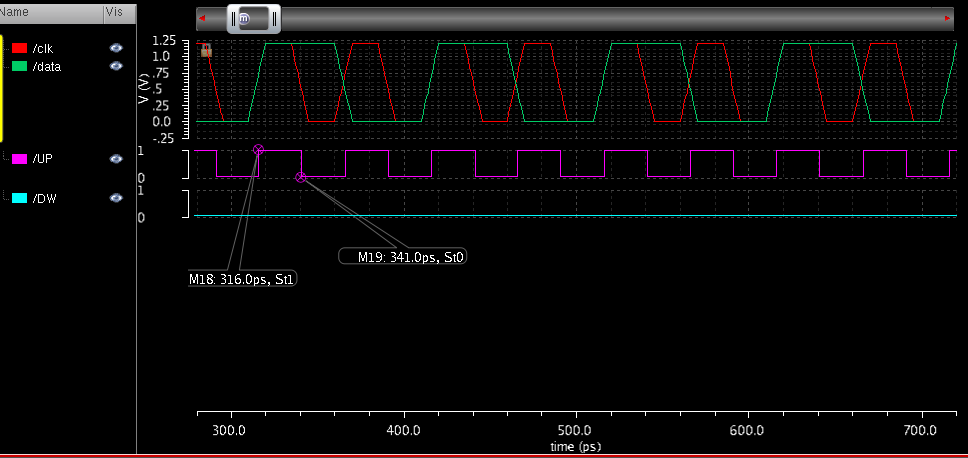


Fig.2-9 Result of simulation (delay = 50ps)

We can observe that the output DOWN is generated by data hopping, the pulse width is proportional to the phase difference between the clock and the data, and the other output UP pulse width is half of the clock period, which is 25ps.

However the Hogge phase detector suffers from a sensitivity to the data transition density, since each triangular pulse on the output of the loop integrator has positive net area, the presence or absence of such a pulse affects the average output of the loop integrator. The data dependent jitter thus introduced is often quite large. To reduce this problem it is possible to replace the triangular correction phase with “tri-waves” whose net area is zero when clock and data are aligned. As in Hogge detector, the width of output *up1* is dependent on the phase error between the delayed data and the clock, while the output *up2* and *down* are always a half clock cycle wide. The phase error can thus be obtained by comparing the variable width pulse from *up1* with the fixed pulses from *up2* and down.

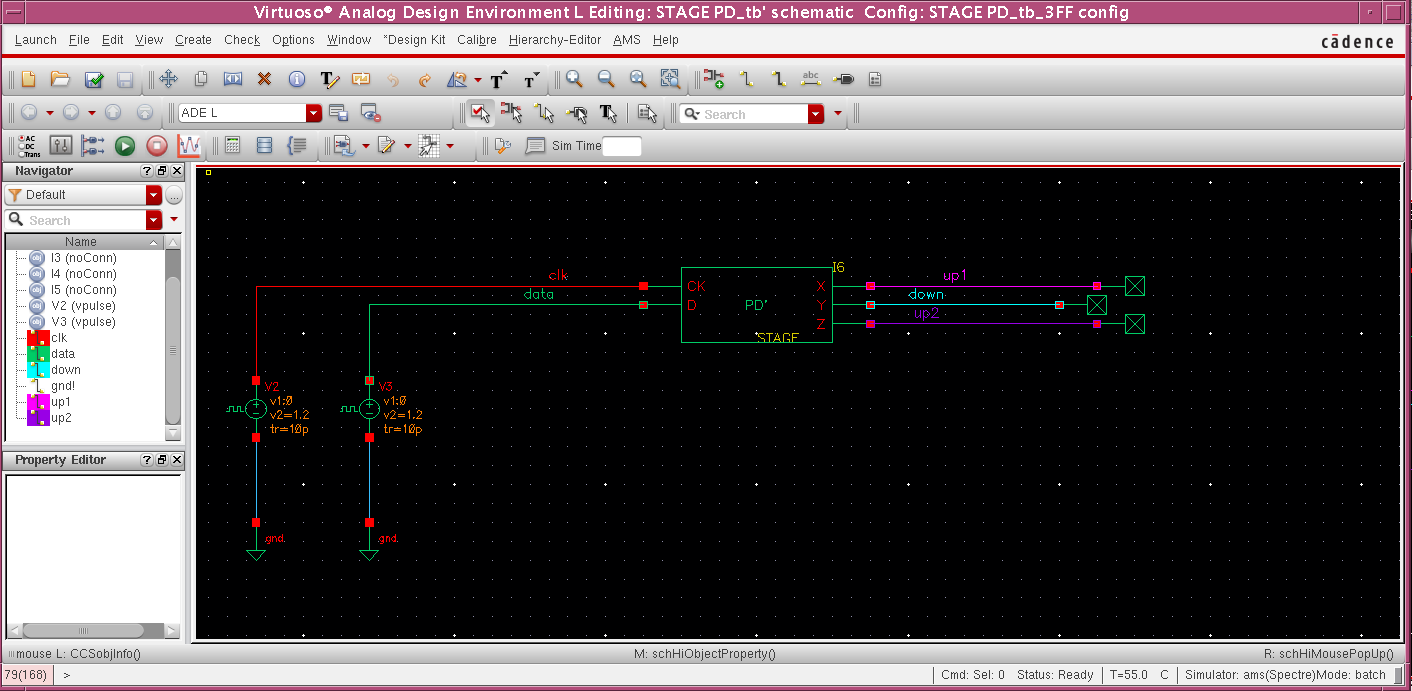


Fig.2-10 Schematic of the test of Hogge PD with 3FF

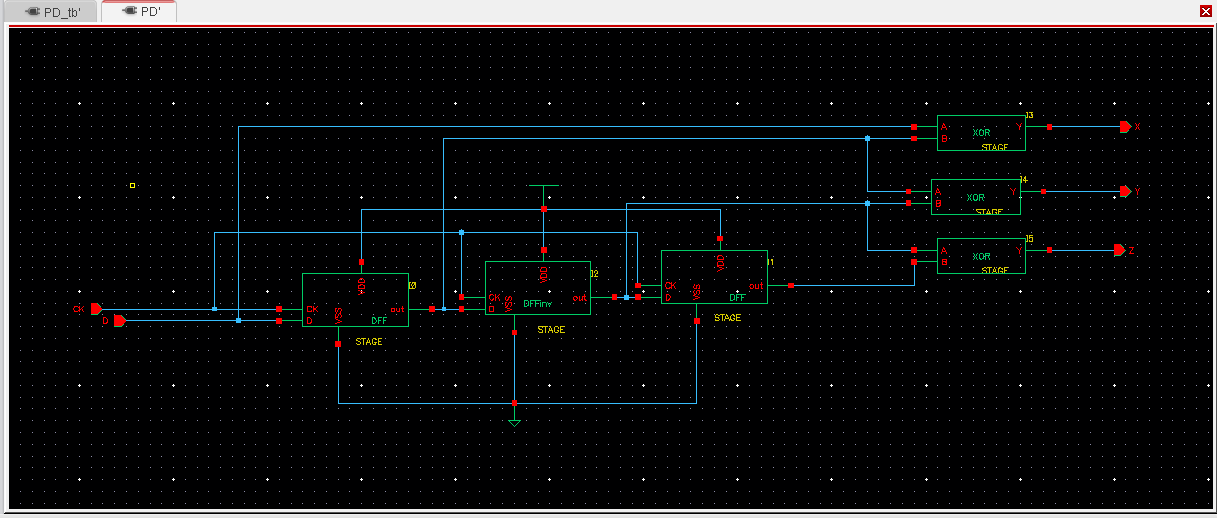


Fig.2-11 Schematic of Hogge phase detector with 3FF

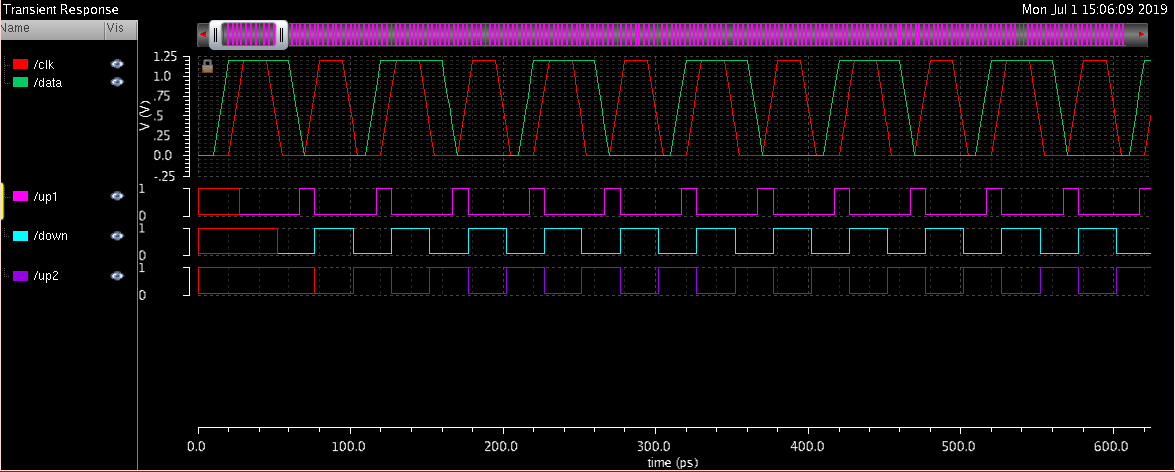


Fig.2-12 Result of simulation (delay = 10ps)

Note that each data transition initiates a three-sectioned transient (the tri-wave) on the output of the loop integrator, and that this tri-wave has zero area. Therefore, its presence or absence does not change the average output of the loop integrator. The tri-wave detector exhibits a much reduced sensitivity to data transition density.

The sensitivity to duty cycle can be restored to that of Hogge implementation with the simple modification shown in Figure.2-13.

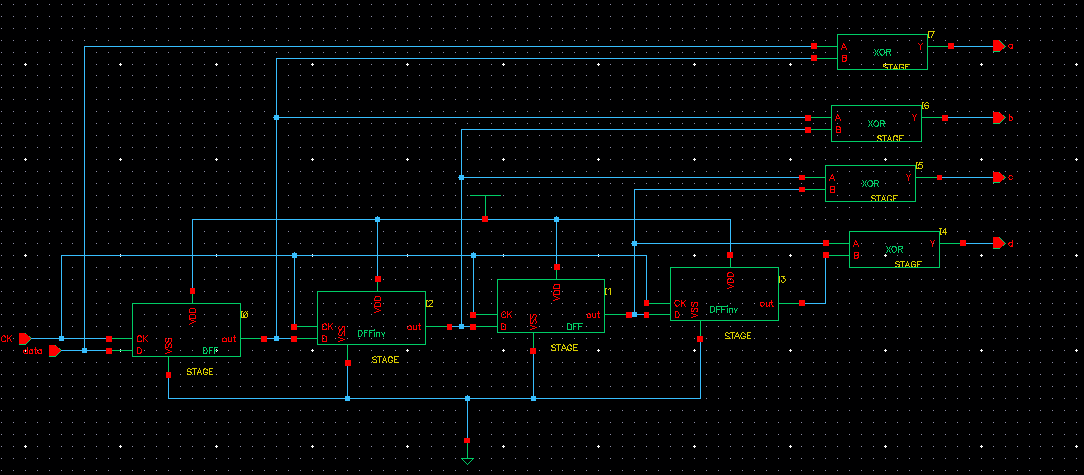


Fig.2-13 Schematic of Hogge phase detector with 4FF

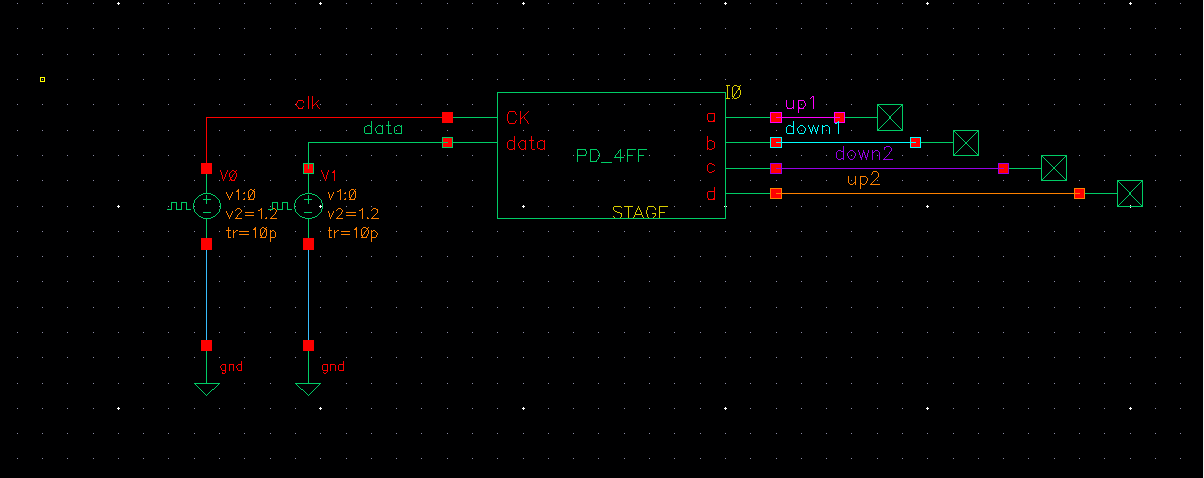


Fig.2-14 Schematic of the test of Hogge PD with 4FF

The modified tri-wave detector uses two distinct down-integration intervals clocked on opposite edges of the clock, rather than a single down integration of twice the strength clocked on a single clock edge. As a consequence, duty cycle effects are attenuated.

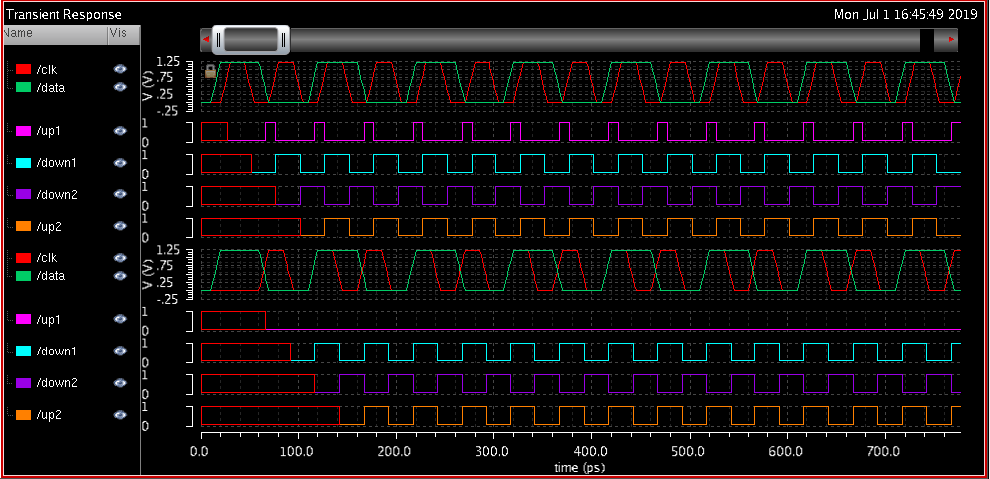
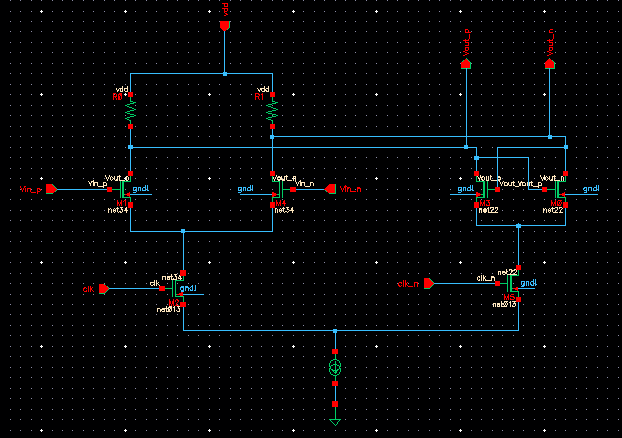
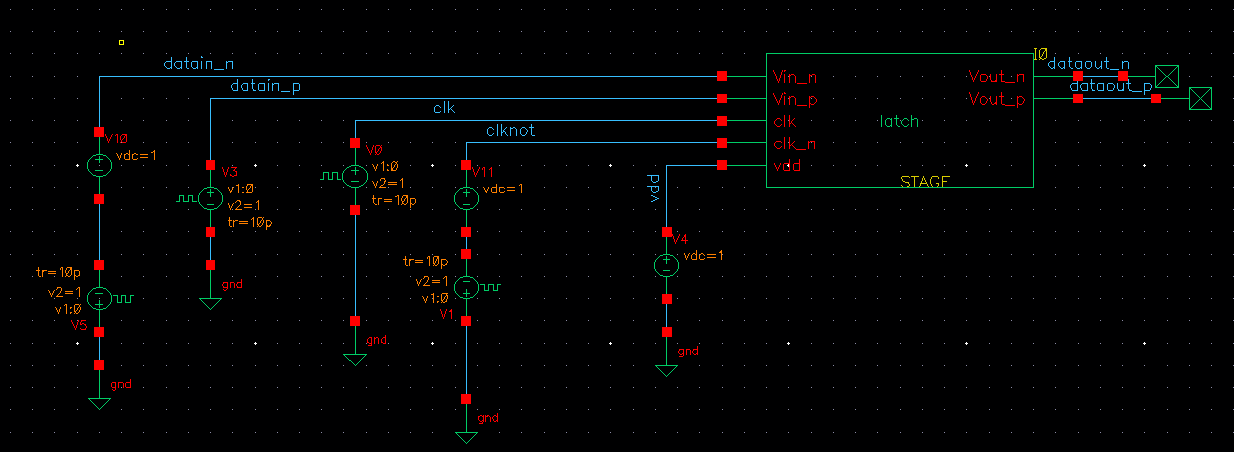


Fig.2-15 Result of simulation (delay = 15ps)

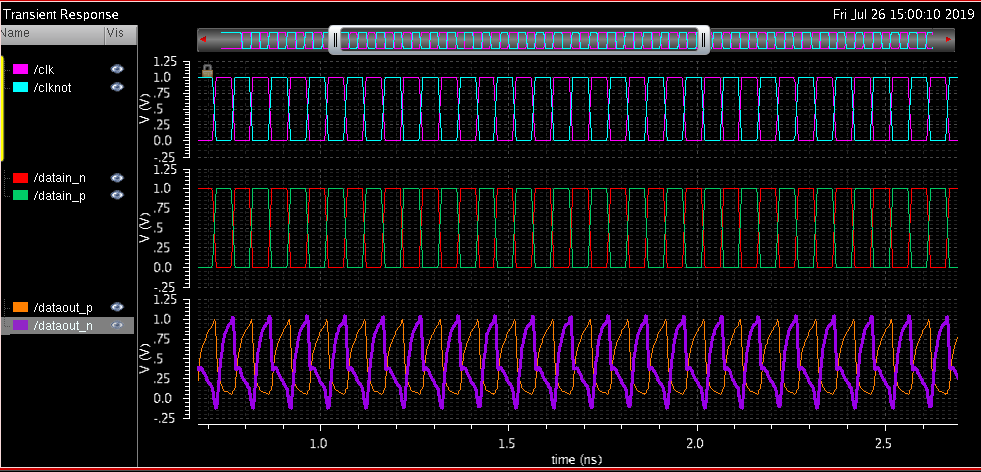
2.2 D Flip-Flop

After verifying successfully with the verilog level, the circuit implementation of the switching level is started. In order to design the D Flipflop, first design a Latch circuit. The circuit is implemented at the transistor level. To achieve an ideal circuit, first control the current of the ideal current source at 500uA. When the clock signal is 1, the circuit is in the transmission state; when the clock signal is 0, the circuit is in the holding state.

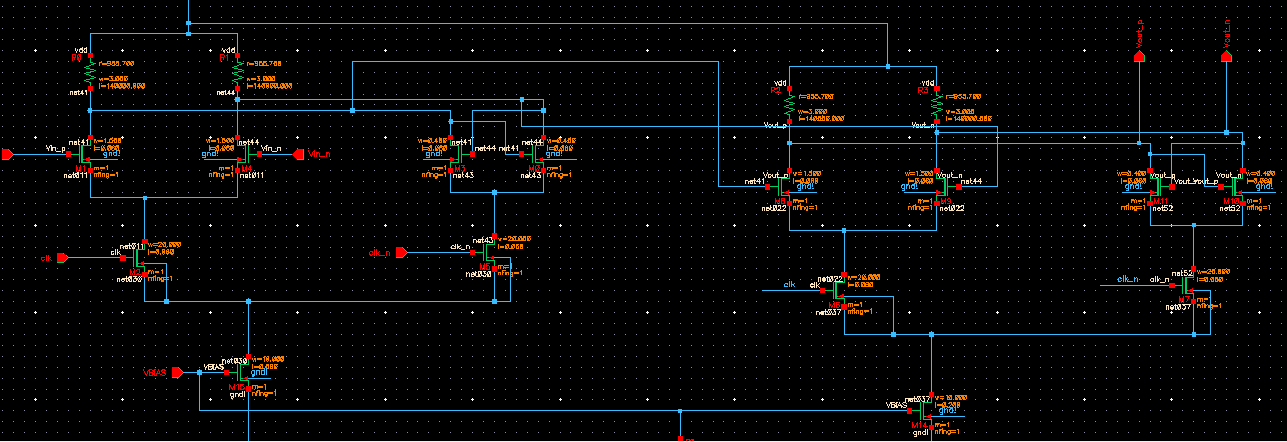




The simulated waveform of the CMOS latch is as follows.

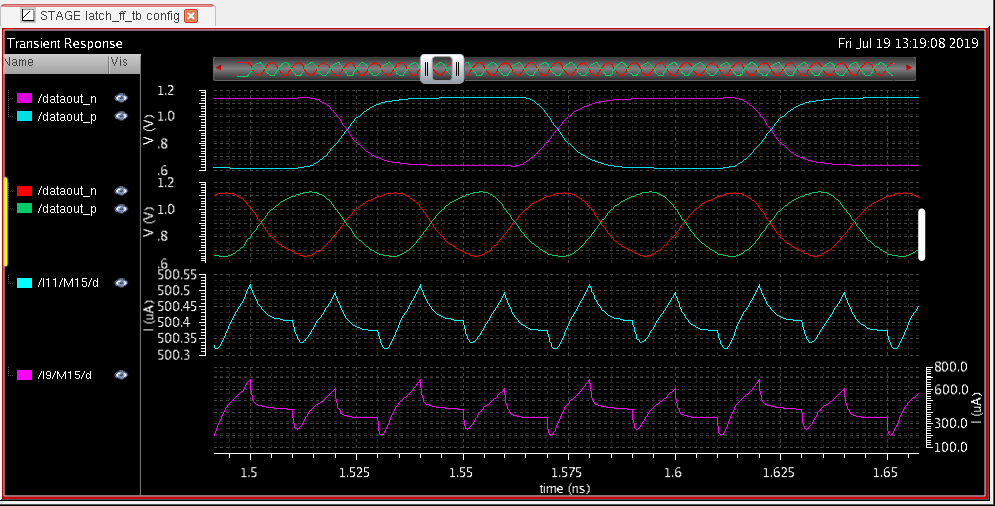


It can be seen that the output signal can follow the clock signal to latch the information of the input signal. Next, Connect two latches together to form a flipflop.(Up:10Ghz/down:25Ghz)

The simulation waveform of the CMOS flip-flop is as follows. The frequency of the above group is 10 GHz. In order to realize high-speed circuit, the frequency is increased to 28 GHz, as shown in the following group.

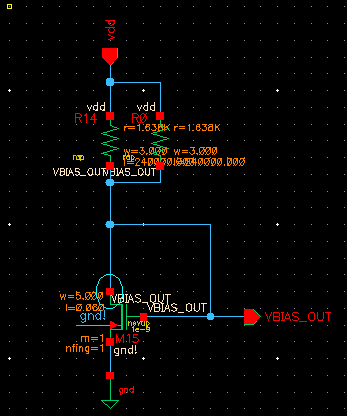
/9/M15/d

/11/M15/d

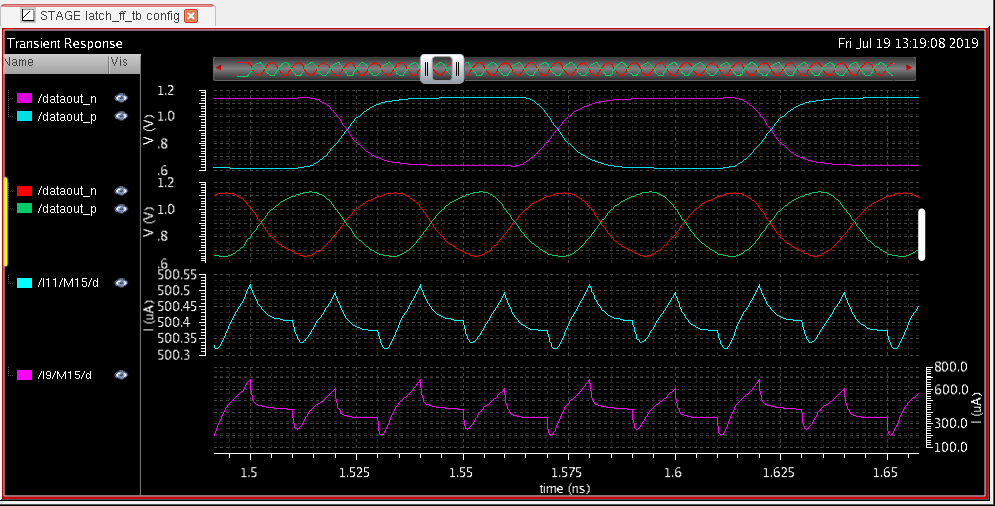


2.2.1 VBIAS

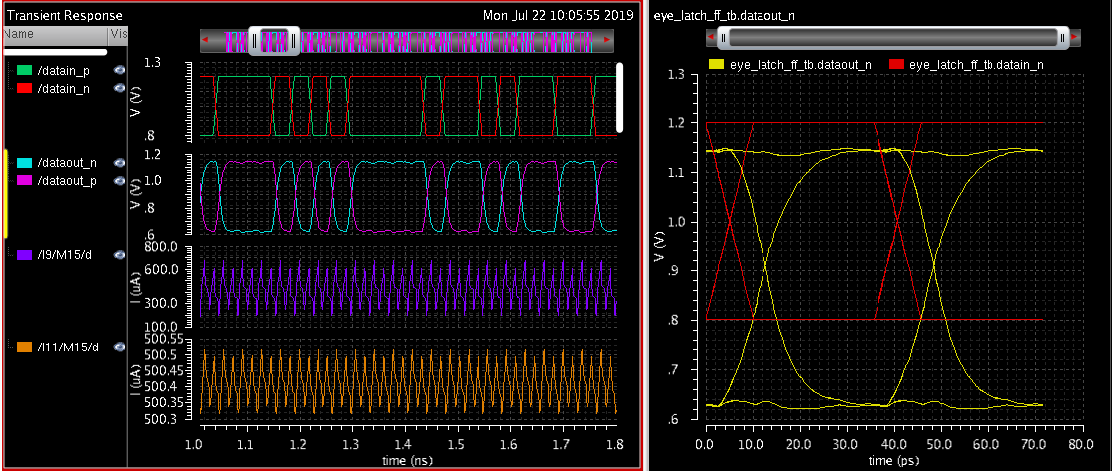
Just in the case of an ideal current source, now we add a bias circuit to make the current 500uA.



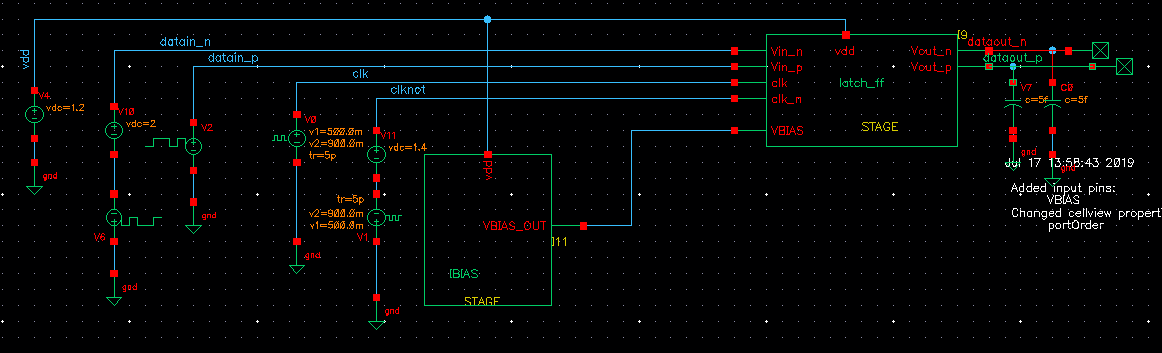
By observing the currents of different segments, it is found that the drain current of I9 is only 300uA-400uA, less than 500uA. This is because the following nmos tube does not reach the saturation region, and its width should be increased to 40um.

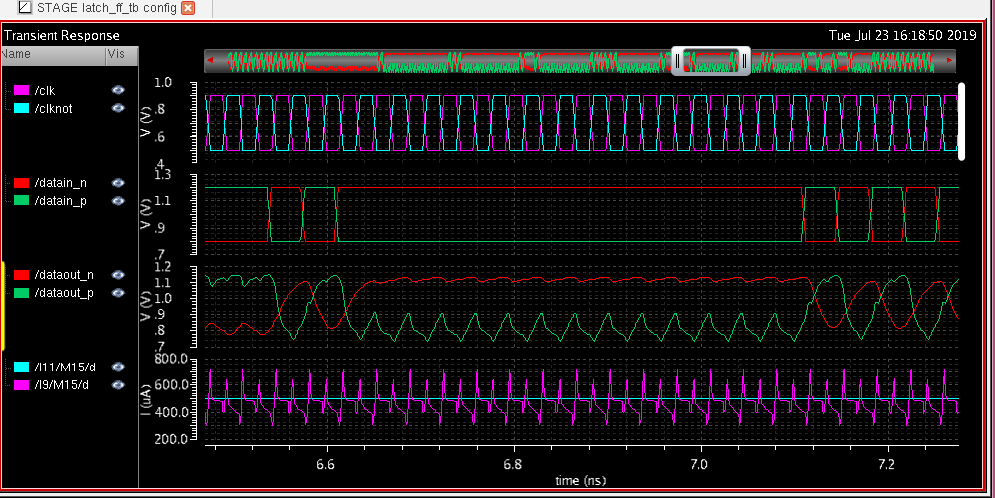


By adjusting the above parameters, the obtained simulation results are as follows, the output signal and the input signal are very close, the current is about 500uA, and the circuit performance can be seen through the eye diagram.

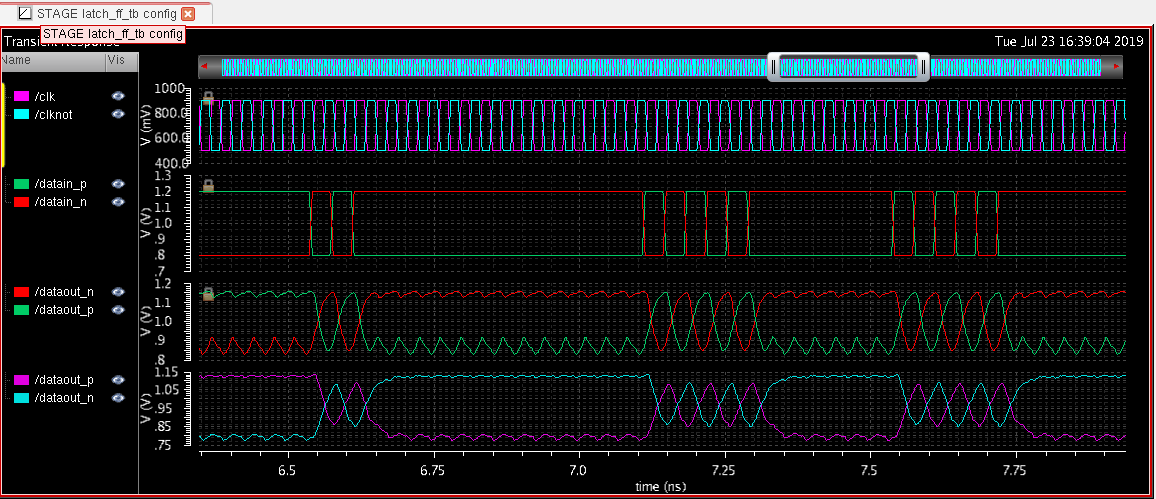


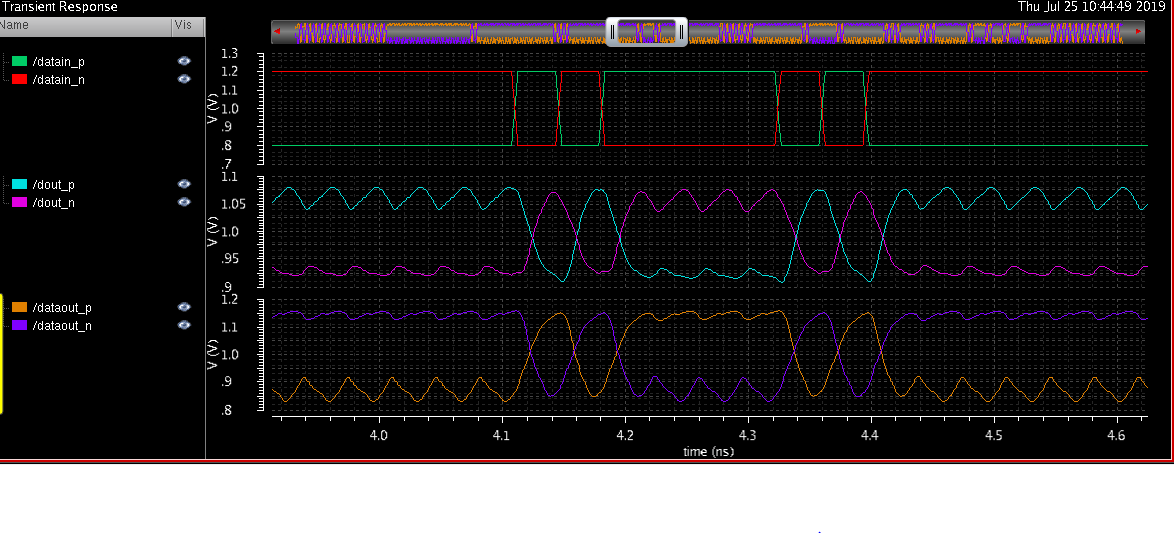
Next, add a decoupling capacitor to the testbench circuit to remove high frequency signal interference and energy storage. The overall circuit diagram is as follows





According to the frequency formula of the oscillation circuit f=1/2πRC, the required capacitance and resistance at a frequency of 28 GHz can be calculated. By continuously adjusting the values of the parameters, the final result is as follows.





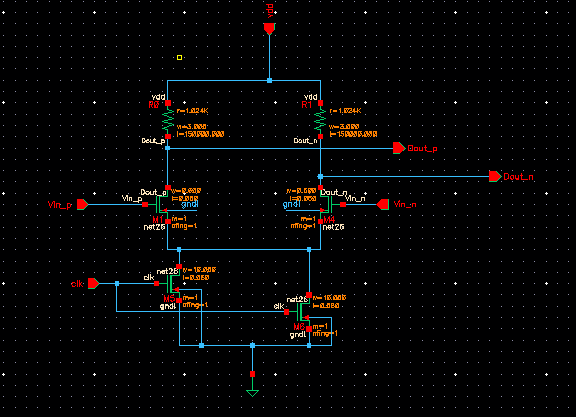
(中间的是新的 amplitude偏小 还需调)

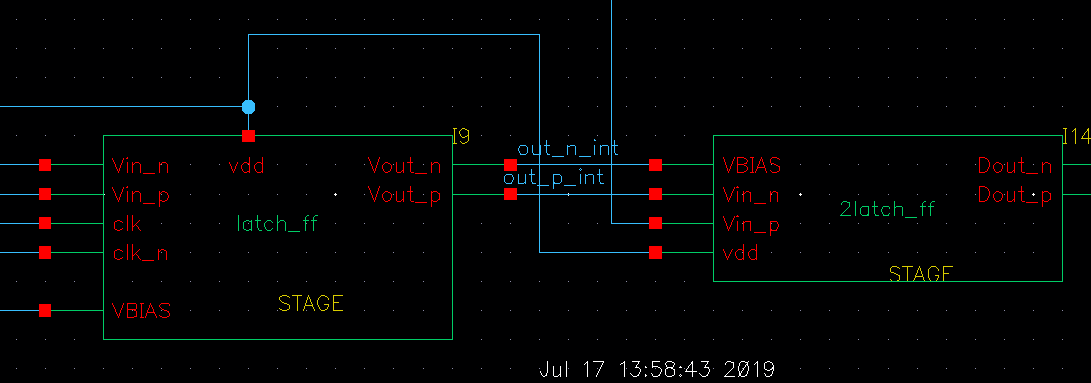
参数

Latch：r：1000欧左右（计算电阻由f=1/2πRC=28Ghz）左面nmos：1.5um 右边：0.4 下面 20um和10um

2.2.2 BUFFER

*2latch\_ff* is a buffer circuit to Improve drive capability  
The buffer is a mos tube with a large aspect ratio, and the large aspect ratio means large current and high driving capability.





By comparison, you can see that adding a buffer at the end of the circuit can effectively reduce the jitter.



2.3 XOR gate

