

CA1 – EXERCISE

REPORT

VIGNESH PRAKASAM | AO120541Y | MARCH 4, 2014

VIDEO DECODER:

Video decoder implementation has been done effectively. As per the design specifications posted, an efficient streaming of video packets to the display has achieved in this exercise as per the output frame rate of 24 ± 2 frames/second.

Assumptions:

1. Decoding is done in a separate decoding circuit
2. Processor is capable of handling multiple threads

Implementation details:

1. A timer has been used to send time out signal to display the frame for every 42ms. So as to reduce the frame rate violations.
2. Two buffers have been implemented. One is for collecting the correct packets to form a frame called Frame buffer and the other is to collect the decoded frames to display on a timeout signal called display buffer.
3. One thread has been created apart from main thread called the decoding thread. This thread performs the decoding and outputs to the display buffer.
4. Two FIFO queues has been initialized with a usage in decoding thread and in displaying method
5. First queue is implemented to store the Frames for the decoding thread to fetch it and process
6. Second queue is implemented to store the decoded frames fetched from it, to display as per the timer.
7. Decoder is designed in such way that the packets are received and put in the decoding queue in parallel with the decoding thread which processes it by decoding and puts in the display queue.
8. Another parallel process is to display the decoded frames with a continuous timer which alarms every 42ms.
9. A detailed flow chart of the implementation has been appended below

Note: The video is made to run for 30 seconds and terminates with the output stats. This time can be increased or decreased in the source code accordingly or a force exit (ctrl+c) can also be pushed at any point to show the output statistics.

The system produces a required average frame rate and minimum violation irrespective of the time of the video.

Video decoder

