MARCO APOLINARIO

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ABOUT

Machine Learning Researcher specializing in hardware-software co-design for brain-inspired AI systems. Proven expertise in developing scalable, energy-efficient neural models for real-time applications. Strong background in deep learning, neuromorphic computing, and energy-efficient neuro-inspired algorithms optimized for edge AI systems.

EDUCATION

Purdue University, Graduate School of Electrical and Computer Engineering West Lafayette, IN
Ph.D. in Electrical and Computer Engineering (Expected graduation: December 2025) January 2021-Present
Advisor: Prof. Kaushik Roy – Research Topic: Brain-Inspired Computing – GPA: 3.9

National University of Engineering, School of Electrical and Electronics Engineering Lima, Peru
B.Sc. in Electronics Engineering – GPA: 3.5 – Rank: 3/28 March 2013-December 2017

RESEARCH EXPERIENCE

Purdue University – Center for Brain-Inspired Computing (C-BRIC) West Lafayette, IN
Graduate Research Assistant August 2021-Present

- Conducted research on neuro-inspired machine learning algorithms for emerging hardware technologies, focusing on scalability and energy efficiency in neuromorphic systems.
- Designed a novel ADC-Less In-memory Computing Hardware, specifically optimized for Spiking Neural Networks, employing a collaborative HW/SW co-design approach. This resulted in remarkable energy savings of 2-7x and latency reductions of 9-24x when compared to traditional architectures.
- Proposed novel spatial, temporal, and fully local learning rules for artificial neural networks, including LLS, S-TLLR, and TESS, inspired by biologically plausible mechanisms such as spike-timing-dependent plasticity (STDP), neural activity synchronization, and eligibility traces. These methods achieved performance comparable to backpropagation while significantly reducing computational costs.

TU Delft – Cognitive Sensor Nodes and Systems (CogSys) Team Delft, Netherlands
Visiting Researcher September 2024-December 2024

- Conducted research on hardware-algorithm co-design with digital hardware accelerators for on-device learning using local learning rules in artificial neural networks, supported by the NSF AccelNet NeuroPAC Fellowship.

Texas Instruments – Kilby Labs Dallas, TX
Systems Engineering Intern May 2023-August 2023

- Conducted research into hardware-aware neural architecture and quantization search, leveraging evolutionary optimization algorithms to facilitate the deployment of deep learning models on low-power devices. Achieved a 10x reduction in model search time and a 5% increase in model performance for keyword spotting tasks.

National Institute for Research and Training in Telecommunications (INICTEL-UNI) Lima, Peru
Research Assistant in Computer Vision July 2017-December 2020

- Contributed to the development of various machine learning models for different applications, including timber species identification, underwater acoustic inversion, satellite cloud segmentation, and river level estimation.
- Integrated machine learning algorithms into low-power electronic systems to enable real-time inference capabilities for precision agriculture applications.
- Innovated by proposing a lightweight CNN model designed for recognizing timber species in microscope images, achieving accuracy rates exceeding 90%, even in scenarios with open-set conditions.
- Obtained three software copyrights, covering applications in remote sensing and health monitoring.
- Shared insights through scholarly contributions, including one journal paper and three conference papers.

SELECTED PUBLICATIONS

- **M. Apolinario**, K. Roy and C. Frenkel (Under Review, 2025). "TESS: A Scalable Temporally and Spatially Local Learning Rule for Spiking Neural Networks".
- **M. Apolinario** and K. Roy (2025). "S-TLLR: STDP-inspired Temporal Local Learning Rule for Spiking Neural Networks". Transactions on Machine Learning Research (TMLR).
- **M. Apolinario,** A. Roy and K. Roy (2025). "LLS: Local Learning Rule for Deep Neural Networks Inspired by Neural Activity Synchronization". IEEE/CVF Winter Conference on Applications of Computer Vision (WACV).
- **M. Apolinario,** and K. Roy (Under Review, 2024). "CODE-CL: Conceptor-Based Gradient Projection for Deep Continual Learning".
- S. Chowdhury, A. Kosta , D. Sharma , **M. Apolinario**, and K. Roy (2024). "Unearthing the Potential of Spiking Neural Networks". In Design, Automation & Test in Europe Conference & Exhibition (DATE).
- S. Biswas, A. Kosta, C. Liyanagedera, **M. Apolinario**, and K. Roy (2024). "HALSIE – Hybrid Approach to Learning Segmentation by Simultaneously Exploiting Image and Event Modalities". In Proceedings of the IEEE/CVF Winter Conference on Applications of Computer Vision (WACV).
- **M. Apolinario,** A. Kosta, U. Saxena, and K. Roy (2023). "Hardware/Software co-design with ADC-Less In-memory Computing Hardware for Spiking Neural Networks". IEEE Transactions on Emerging Topics in Computing.
- A. Kosta, **M. Apolinario**, and K. Roy (2023). "ANN vs SNN vs Hybrid Architectures for Event-based Real-time Gesture Recognition and Optical Flow Estimation". In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR) Workshops.
- **M. Apolinario,** D. Urcia, and S. Huaman (2019). "Open Set Recognition of Timber Species Using Deep Learning for Embedded Systems". In IEEE Latin America Transactions.
- **M. Apolinario,** S. Huamán, G. Morales, and D. Diaz (2019). "Estimation of 2D Velocity Model using Acoustic Signals and Convolutional Neural Networks". In IEEE INTERCON.

AWARDS

- **NSF AccelNet NeuroPAC Fellowship (2024):** Awarded for conducting research on a digital on-chip learning hardware accelerator at Delft University of Technology (TU Delft).
- **Graduate Peruvian Fellowship "Beca Generacion del Bicentenario" (2020):** Fully funded by the Peruvian Ministry of Education, recognizing outstanding professionals with high potential for innovation and research in graduate studies.
- **"Julio Urbina Arias" Award (2017):** Recognized for exceptional contributions to research and leadership within the IEEE Student Branch at the National University of Engineering, Lima, Peru.

TECHNICAL STRENGTHS

- **Programming and Hardware Description Languages:** Python, C/C++, VHDL/Verilog.
- **Machine Learning Frameworks:** Pytorch, Tensorflow/Keras.
- **EDA tools:** Cadence Virtuoso, Quartus Prime, and Eagle PCB.

RELEVANT COURSEWORK

- **Electronics courses:** Computer Architecture (Fall'23), System on Chip Design (Fall'22), Analog CMOS Design (Fall'22), Advanced VLSI Design (Spring'22), MOS VLSI Design (Fall'21), Solid State Devices (Spring'21).
- **Computer Science courses:** Applied Quantum Computing (Spring' 23), Optimization for Deep Learning (Fall'23), Computational Methods in Optimization (Spring'22), Artificial Intelligence (Fall'21).
- **2024 Telluride Neuromorphic Cognition Engineering Workshop:** Attended the workshop in-person and explored how to leverage different neuromodulation mechanisms for synaptic plasticity and reinforcement learning.
- **2021 Neuromatch Academy Computational Neuroscience Summer School:** Attended online, learn foundations of computational neuroscience and explore correlation between responses of artificial and vivo systems to visual stimuli.