

Marco Apolinario

📍 West Lafayette, IN 47906 ✉ mapolina@purdue.edu ☎ (765) 407-2732 🌐 mapolinario94.github.io
📄 marco-apolinario 📧 mapolinario94

About

Machine Learning Researcher specializing in hardware-software co-design for brain-inspired AI systems. Proven expertise in developing scalable, energy-efficient neural models for real-time applications. Strong background in deep learning, neuromorphic computing, and energy-efficient neuro-inspired algorithms optimized for edge AI systems.

Education

- Jan 2021 – present **Purdue University**, PhD in Electrical and Computer Engineering – West Lafayette, IN, USA
- Working on hardware-software co-design for brain-inspired AI systems
 - Advisor: Prof. Kaushik Roy - Expected graduation: December 2025
- Mar 2013 – Dec 2017 **National University of Engineering**, BS in Electronics Engineering – Lima, Peru
- GPA: 3.5/4.0, ranked 3rd out of 28 students
 - Awards: Outstanding member of the IEEE Student Branch

Experience

- Aug 2021 – present **Graduate Research Assistant**, Purdue University - Nanoelectronics Research Laboratory (NRL) – West Lafayette, IN, USA
- Conducted research on neuro-inspired machine learning algorithms for emerging hardware technologies, focusing on scalability and energy efficiency in neuromorphic systems.
 - Designed a novel ADC-Less In-memory Computing Hardware, specifically optimized for Spiking Neural Networks, employing a collaborative HW/SW co-design approach. This resulted in remarkable energy savings of 2-7x and latency reductions of 9-24x when compared to traditional architectures.
 - Proposed novel spatial, temporal, and fully local learning rules for artificial neural networks, including LLS, S-TLLR, and TESS, inspired by biologically plausible mechanisms such as spike-timing-dependent plasticity (STDP), neural activity synchronization, and eligibility traces. These methods achieved performance comparable to backpropagation while significantly reducing computational costs.
- Sept 2024 – Dec 2024 **Visiting Researcher**, Delft University of Technology (TU Delft) – Delft, Netherlands
- Conducted research on hardware-algorithm co-design with digital hardware accelerators for on-device learning using local learning rules in artificial neural networks, supported by the NSF AccelNet NeuroPAC Fellowship.
- May 2023 – Aug 2023 **Systems Engineering Intern**, Texas Instruments - Kilby Labs – Dallas, TX, USA
- Conducted research into hardware-aware neural architecture and quantization search, leveraging evolutionary optimization algorithms to facilitate the deployment of deep learning models on low-power devices. Achieved a 10x reduction in model search time and a 5% increase in model performance for keyword spotting tasks.
- July 2017 – Dec 2020 **Research Assistant in Computer Vision**, National Institute for Research and Training in Telecommunications (INICTEL-UNI) – Lima, Peru
- Developed energy-efficient machine learning models for different applications, including timber species identification, underwater acoustic inversion, satellite cloud segmentation, and river level estimation.
 - Integrated machine learning algorithms into low-power electronic systems to enable real-time inference capabilities for precision agriculture applications.

- Innovated by proposing a lightweight CNN model designed for recognizing timber species in microscope images, achieving accuracy rates exceeding 90%, even in scenarios with open-set conditions.
- Obtained three software copyrights, covering applications in remote sensing and health monitoring.
- Shared insights through scholarly contributions, including one journal paper and three conference papers.

Publications

- 2025 **CODE-CL: Conceptor-Based Gradient Projection for Deep Continual Learning**
Marco Apolinario, Sakshi Choudhary, Kaushik Roy. International Conference on Computer Vision (ICCV) ([10.48550/arXiv.2411.15235](https://arxiv.org/abs/10.48550/arXiv.2411.15235))
- 2025 **TESS: A Scalable Temporally and Spatially Local Learning Rule for Spiking Neural Networks**
Marco Apolinario, Kaushik Roy, Charlotte Frenkel. International Joint Conference on Neural Networks (IJCNN) ([10.48550/arXiv.2502.01837](https://arxiv.org/abs/10.48550/arXiv.2502.01837))
- 2025 **LLS: Local Learning Rule for Deep Neural Networks Inspired by Neural Activity Synchronization**
Marco Apolinario, Arani Roy, Kaushik Roy. IEEE/CVF Winter Conference on Applications of Computer Vision (WACV) ([10.1109/WACV61041.2025.00758](https://arxiv.org/abs/10.1109/WACV61041.2025.00758))
- 2025 **S-TLLR: STDP-inspired Temporal Local Learning Rule for Spiking Neural Networks**
Marco Apolinario, Kaushik Roy. Transactions on Machine Learning Research (TMLR) (openreview.net/forum?id=CNaiJRcX84)
- 2024 **Unearthing the Potential of Spiking Neural Networks**
Sayed Chowdhury, Adarsh Kosta, Deepika Sharma, Marco Apolinario, Kaushik Roy. Design, Automation & Test in Europe Conference & Exhibition (DATE) ([10.23919/DATE58400.2024.10546699](https://arxiv.org/abs/10.23919/DATE58400.2024.10546699))
- 2024 **HALSIE: Hybrid Approach to Learning Segmentation by Simultaneously Exploiting Image and Event Modalities**
Shristi Das Biswas, Adarsh Kosta, Chamika Liyanagedera, Marco Apolinario, Kaushik Roy. IEEE/CVF Winter Conference on Applications of Computer Vision (WACV) ([10.1109/WACV57701.2024.00586](https://arxiv.org/abs/10.1109/WACV57701.2024.00586))
- 2023 **Hardware/Software Co-Design With ADC-Less In-Memory Computing Hardware for Spiking Neural Networks**
Marco Apolinario, Adarsh Kosta, Utkarsh Saxena, Kaushik Roy. IEEE Transactions on Emerging Topics in Computing ([10.1109/TETC.2023.3316121](https://arxiv.org/abs/10.1109/TETC.2023.3316121))
- 2023 **Live Demonstration: ANN vs SNN vs Hybrid Architectures for Event-based Real-time Gesture Recognition and Optical Flow Estimation**
Adarsh Kosta, Marco Apolinario, Kaushik Roy. IEEE/CVF Conference on Computer Vision and Pattern Recognition Workshops (CVPRW) ([10.1109/CVPRW59228.2023.00436](https://arxiv.org/abs/10.1109/CVPRW59228.2023.00436))
- 2020 **Method of Estimating River Levels with Reflective Tapes Using Artificial Vision Techniques**
Lidia Lopez, Marco Apolinario, Samuel Huaman. Proceedings of the 5th Brazilian Technology Symposium ([10.1007/978-3-030-57566-3_19](https://arxiv.org/abs/10.1007/978-3-030-57566-3_19))
- 2019 **Open Set Recognition of Timber Species Using Deep Learning for Embedded Systems**
Marco Apolinario, Daniel Urcia, Samuel Huaman. IEEE Latin America Transactions ([10.1109/TLA.2019.9011545](https://arxiv.org/abs/10.1109/TLA.2019.9011545))
- 2019 **Estimation of 2D Velocity Model using Acoustic Signals and Convolutional Neural Networks**
Marco Apolinario, Samuel Huaman, Giorgio Morales, Daniel Diaz. IEEE International Conference on Electronics, Electrical Engineering and Computing (INTERCON) ([10.1109/INTERCON.2019.8853566](https://arxiv.org/abs/10.1109/INTERCON.2019.8853566))

- 2018 **Deep Learning Applied to Identification of Commercial Timber Species from Peru**
Marco Apolinario, Samuel Huaman, Gabriel Orellana. IEEE International Conference on Electronics, Electrical Engineering and Computing (INTERCON) ([10.1109/INTERCON.2018.8526457](https://doi.org/10.1109/INTERCON.2018.8526457))

Awards

- 2024 **NSF AccelNet NeuroPAC Fellowship**
Awarded for conducting research on a digital on-chip learning hardware accelerator at Delft University of Technology (TU Delft).
- 2020 **Graduate Peruvian Fellowship "Beca Generacion del Bicentenario"**
Fully funded by the Peruvian Ministry of Education, recognizing outstanding professionals with high potential for innovation and research in graduate studies.
- 2017 **"Julio Urbina Arias" Award**
Recognized for exceptional contributions to research and leadership within the IEEE Student Branch at the National University of Engineering, Lima, Peru.

Academic Service

Reviewer for Journals: IEEE Transactions on Image Processing, IEEE Transactions on Cognitive and Developmental Systems, IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), and IEEE Latin America Transactions

Reviewer for Conferences: International Conference on Machine Learning (ICML), International Conference on Computer Vision (ICCV), International Conference on Learning Representations (ICLR), Neural Information Processing Systems (NeurIPS), International Conference on Artificial Neural Networks (ICANN) and IEEE INTERCON

Invited Talks

- Apr 2025 **Energy-Efficient Brain-Inspired Learning in Deep Neural Networks**
Presented online at the IEEE Signal Processing Society student chapter at the National University of Engineering, Lima, Peru.
- Nov 2024 **Local Learning for Deep Neural Networks**
Presented at Data Management and Biometrics Group, University of Twente, Netherlands.
- July 2024 **Neuromodulation on Brain and Machines (Co-presented with Dr. Kathryn Simone)**
Presented at 2024 Telluride Neuromorphic Cognition Engineering Workshop, Telluride, CO, USA.
- June 2024 **Hardware/Software Co-design with ADC-Less In-Memory Computing for SNNs**
Presented at In-Memory Computing Applications Workshop at DAC 2024, San Francisco, CA, USA.

Relevant Coursework

Graduate electronics courses: AI Hardware (Spring'25), Computer Architecture (Fall'23), System on Chip Design (Fall'22), Analog CMOS Design (Fall'22), Advanced VLSI Design (Spring'22), MOS VLSI Design (Fall'21), Solid State Devices (Spring'21)

Graduate computer science courses: Applied Quantum Computing (Spring'23), Optimization for Deep Learning (Fall'23), Computational Methods in Optimization (Spring'22), Artificial Intelligence (Fall'21)

Professional Development

- 2024 **Telluride Neuromorphic Cognition Engineering Workshop**
Attended the workshop in-person and explored how to leverage different neuromodulation mechanisms for synaptic plasticity and reinforcement learning.
- 2024 **SRC TECHON**

Attended in person the annual conference hosted by the Semiconductor Research Corporation (SRC) at Austin, TX, USA.

2021 **Neuromatch Academy Computational Neuroscience Summer School**

Attended online, learn foundations of computational neuroscience and explore correlation between responses of artificial and vivo systems to visual stimuli.

Skills

Programming and Hardware Description Languages: Python, C/C++, VHDL/Verilog, and Git

EDA tools: Cadence Virtuoso, Quartus Prime, and Eagle PCB

Machine Learning Frameworks: Pytorch, Tensorflow/Keras

Languages: English (fluent), Spanish (native)