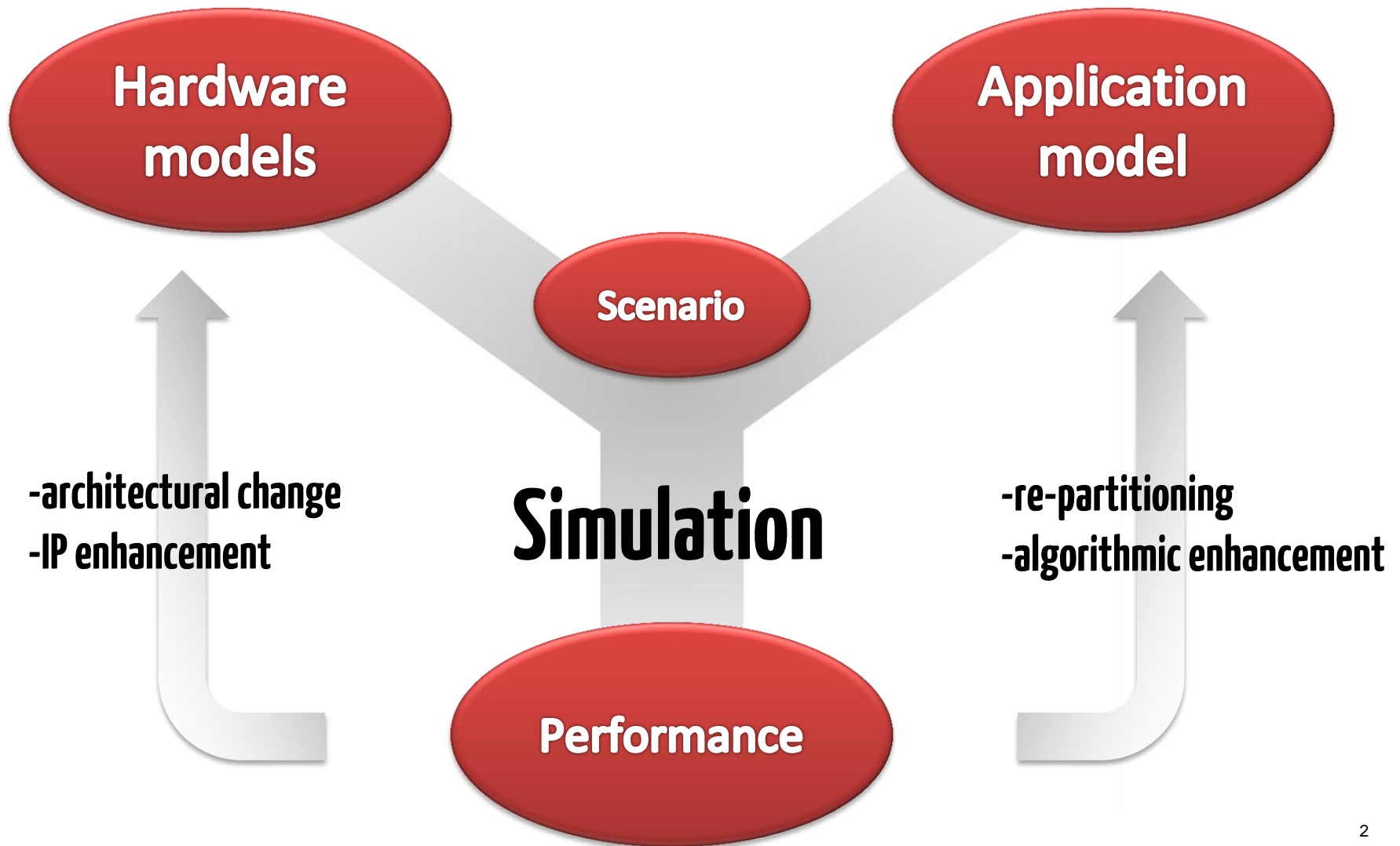


# ARM SoC exploration

Using gem5 for application specific  
system-on-chip architecture exploration

Alexandre Romaña & Abhilash Nair

# How we do architecture exploration



# The Case for gem5

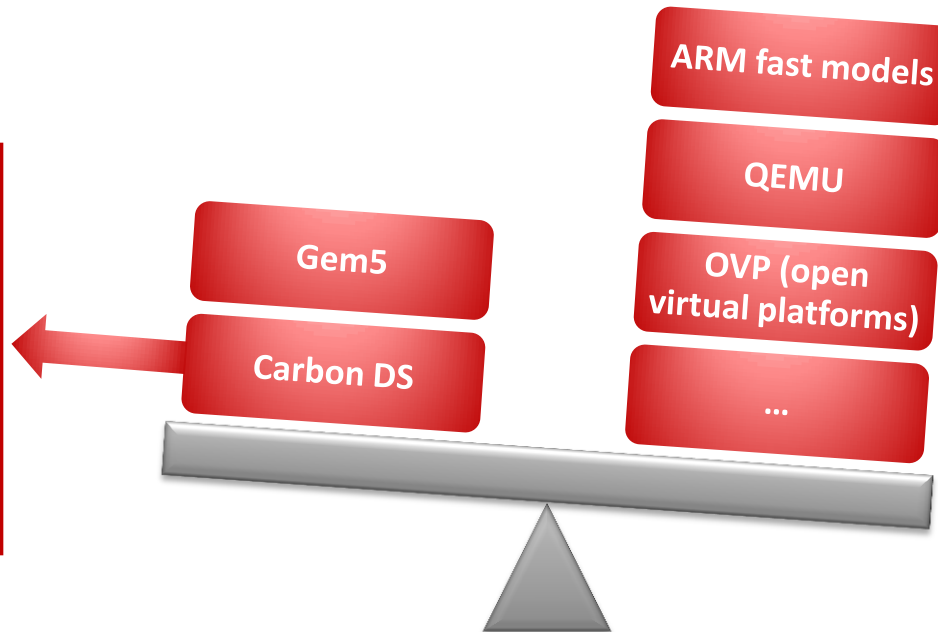
**Cycle  
accurate**

**Fast**


**Emulation**

**carbon**  
*Software before Silicon*

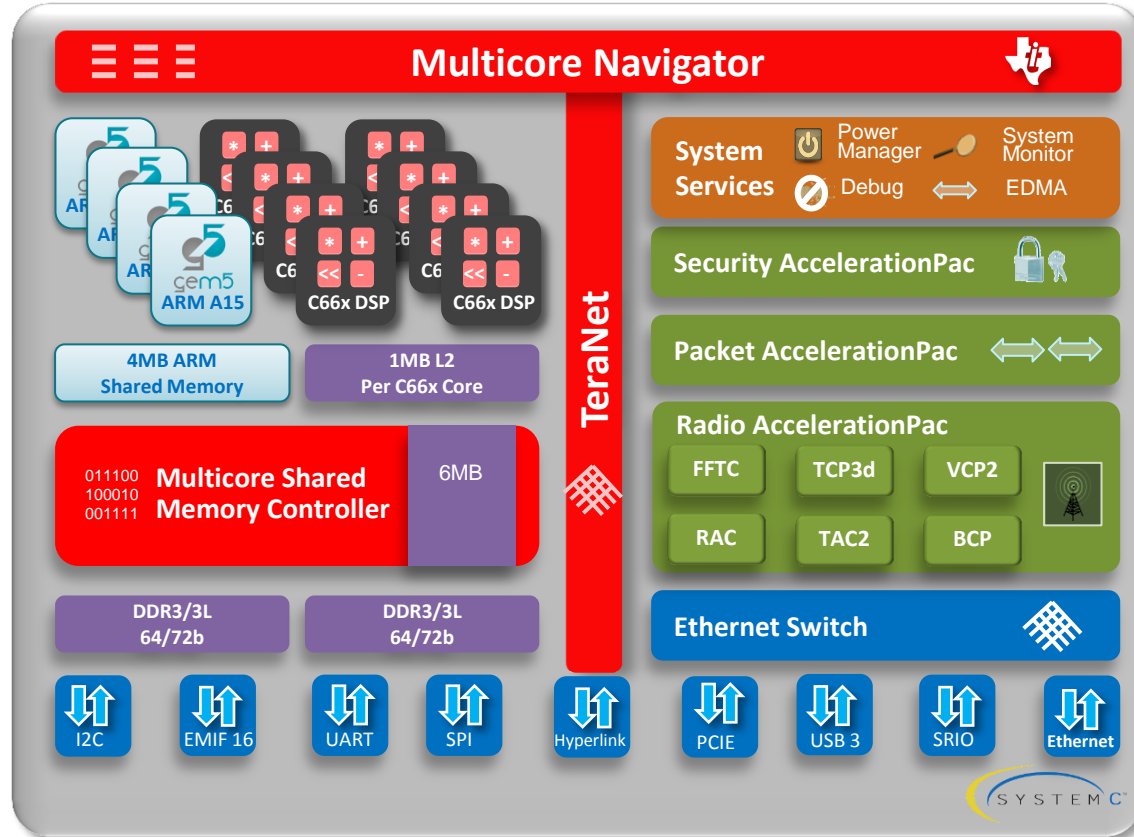
- **Late**
- **Expensive**
- **Slow**
- **Complex**



**Zebu**



# Architecture exploration for TCI6636K2H SoC for Small Cells (High End)

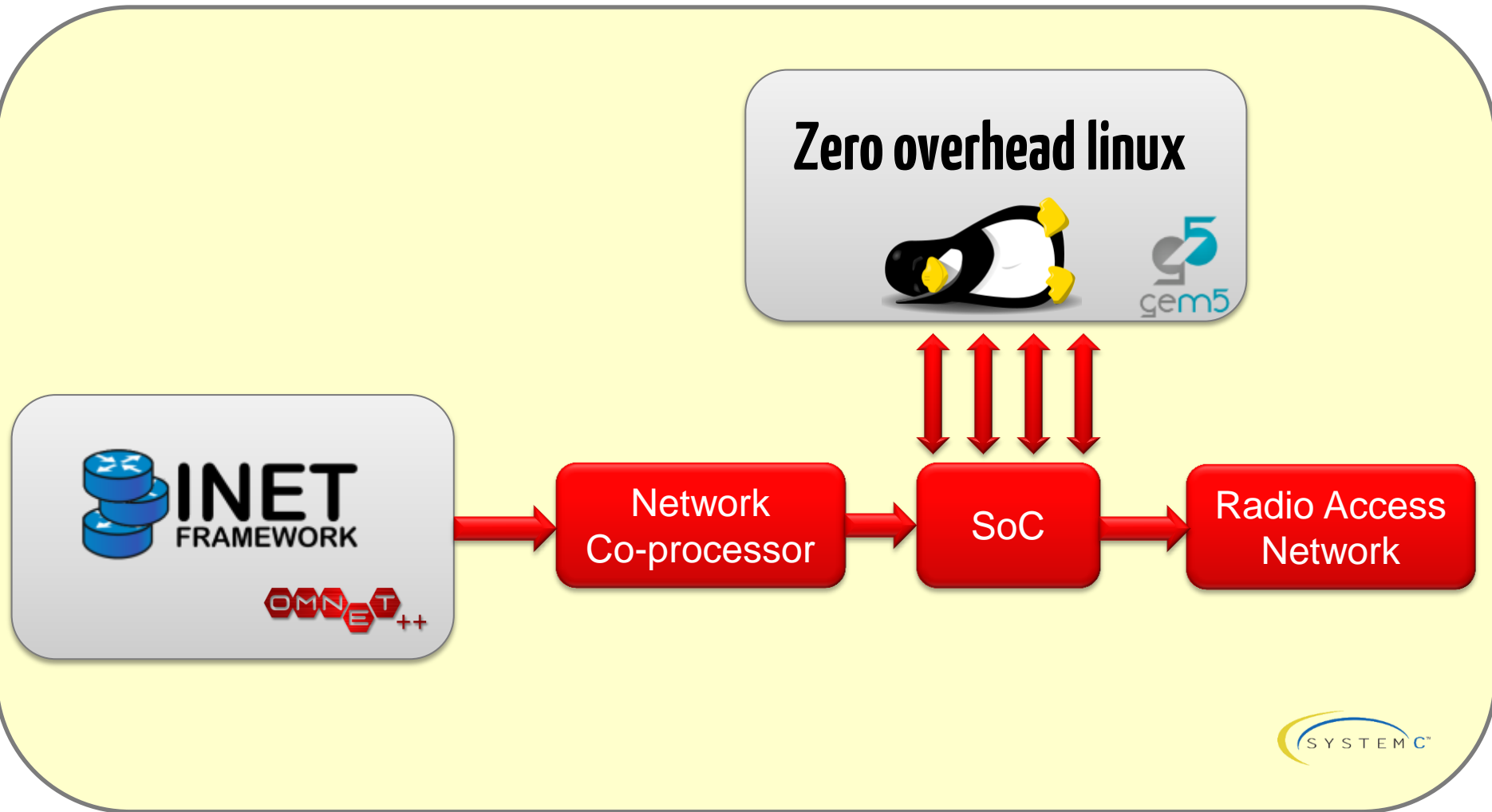


- First chip architected using gem5:
  - SL2\$ size
  - MSMC Coherency
  - Arbitration
  - ...

# System on a Chip components

- IPs in a SoC vs what gem5 supports:
  - ARM
  - DSP
  - Caches
  - Memories
  - Core Interconnect
  - Chip Interconnect
  - Hardware accelerators
  - External Interfaces
  - ...
- SystemC enabled full system benchmarking

# Use case example: Leveraging open source for linux fast path benchmarking



# The need for task partitioning

LTE PUCCH decoding **taskflow**

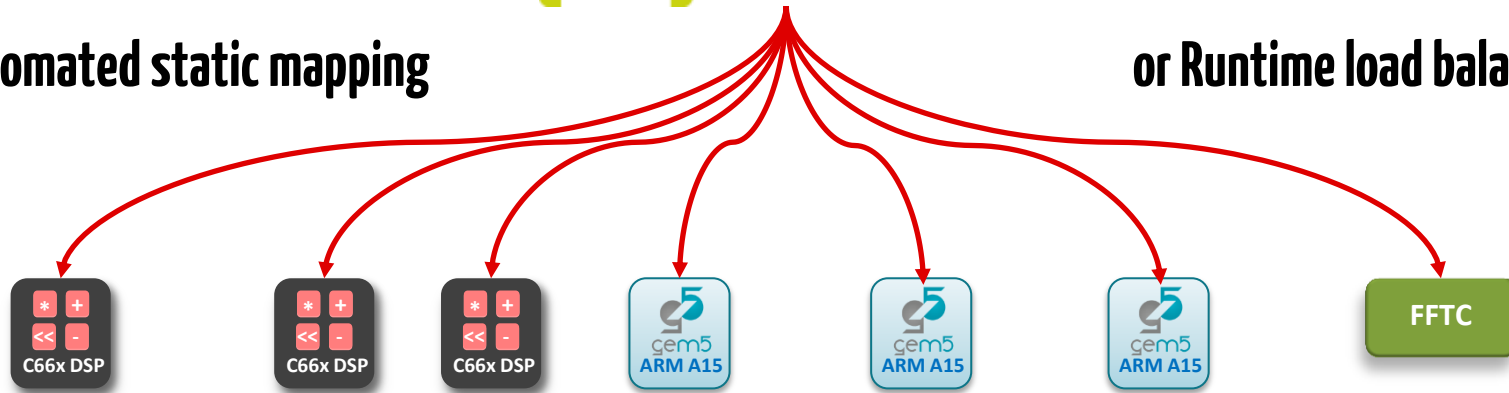


1000s of tasks



**Automated static mapping**

**or Runtime load balancing**



# Leveraging checkpointing

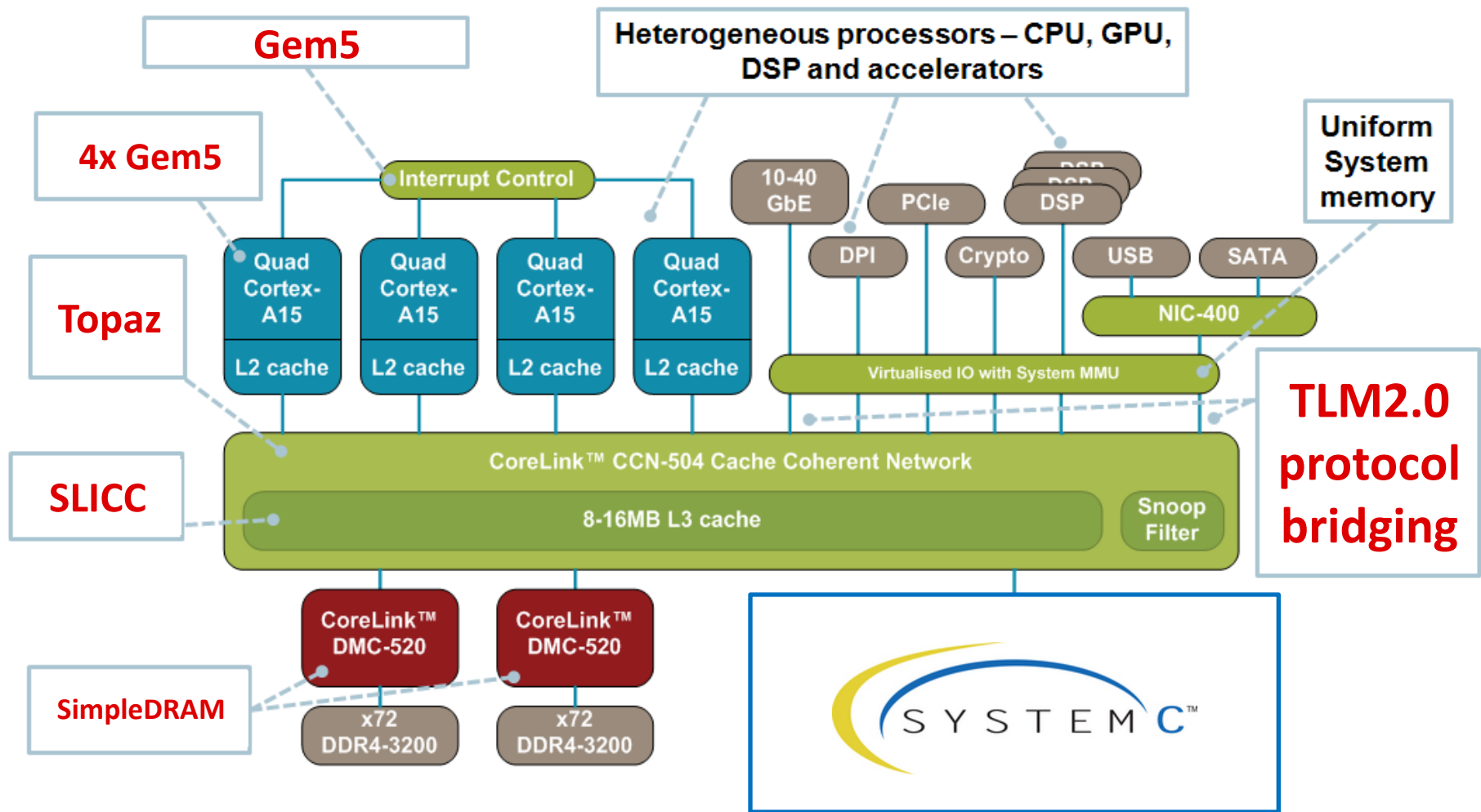


Useful for both bare metal and linux



# Modeling today's architectures

## ARM CCN-504



Source: [http://www.arm.com/images/CoreLink\\_CCN-504\\_system\\_large.png](http://www.arm.com/images/CoreLink_CCN-504_system_large.png)

**Thank You!**  
**Questions?**