JIS UNIVERSITY

Sr. No: 023/CSE/V/Set A

Roll Number | | | | | | | | | | |

END SEMESTER EXAMINATION – ODD 2023

YCS5004– Advanced Computer Architecture

Time: 2 Hrs. **Maximum Marks: 50**

Instructions to the candidate:

- ***Draw neat sketches and diagrams wherever necessary.***
- ***Attempt all sub-parts of a Question at one place.***

Part - A
Answer any ten (10x1=10 Marks)

1. What is the primary goal of performance evaluation in computer architecture? (1) CO3 L1

   a) To compare different computer systems
   b) To determine the cost of a computer system
   c) To predict the performance of a computer system
   d) To analyze the energy efficiency of a computer system

2. Amdahl's law is used to: (1) CO3 L1

   a) Measure the performance of a computer system
   b) Determine the speedup of a program on a parallel system
   c) Analyze the impact of memory hierarchy on performance
   d) Calculate the efficiency of a cache optimization technique

3. Which of the following is an example of a structural hazard? (1) CO3 L1

   a) Data dependency
   b) Resource conflict
   c) Branch prediction failure
   d) Instruction cache miss

4. Data forwarding is a technique used to: (1) CO3 L1

   a) Predict branch instructions
   b) Avoid data hazards in pipelined processors
   c) Improve memory hierarchy performance
   d) Increase the number of pipeline stages

5. Superscalar architecture is designed to: (1) CO L1

a) Execute multiple instructions simultaneously
b) Optimize memory access patterns
c) Increase the clock speed of the processor
d) Reduce the number of pipeline stages

6. What is the purpose of a Translation Lookaside Buffer (TLB)? (1) CO4 L1
a) To store virtual memory addresses
b) To cache recently accessed instructions
c) To manage memory coherency in a multiprocessor system
d) To translate virtual addresses to physical addresses

7. Which memory replacement policy aims to minimize the number of cache misses? (1) CO4 L1
a) Least Recently Used (LRU)
b) First-In-First Out (FIFO)
c) Random
d) Most Recently Used (MRU)

8. Uniform Memory Access (UMA) is characterized by: (1) CO4 L1
a) Equal access times to all memory locations
b) Varying access times to different memory locations
c) Separate address spaces for each processor
d) Low latency for local memory accesses

9. Which of the following is a characteristic of Non-Uniform Memory Access (NUMA)? (1) CO4 L1
a) All processors share a single memory space
b) Memory access times vary based on the location of the data
c) Each processor has its own private memory
d) Memory access is synchronized using a global clock

10. Which type of architecture is known for its efficient handling of parallel tasks with dedicated processing elements? (1) CO5 L1
a) Data flow computers
b) Superscalar architecture
c) Very Long Instruction Word (VLIW) architecture
d) Systolic architectures

11. Cache optimization techniques primarily aim to improve: (1) CO4 L1

a) Memory capacity
b) Memory access latency
c) Memory coherence
d) Memory hierarchy

12. Which of the following is a property of memory hierarchy? (1) CO4 L1

a) Low-level cache has a larger capacity than high-level cache
b) Data is always fetched from the highest level of cache
c) Locality of reference influences cache performance
d) Cache coherence is not a concern in memory hierarchy

Part - B
Answer any two (2x5=10 Marks)

Q. No		Question	Marks	CO	Bloom's Level
13.	a)	Explain Amdahl's law and provide an example illustrating its application in computer design.	(v)	CO3	L3
14.	a)	Define Instruction Level Parallelism (ILP) in computer architecture. Provide an example to illustrate ILP.	(v)	CO3	L2
15.	a)	Describe the concept of loosely coupled systems in computer architecture. Provide an example of a loosely coupled system and explain how it differs from a tightly coupled system.	(v)	CO2	L3
16.	a)	Consider a system with a 32-bit logical address space and a page size of 4 KB. If the system uses two-level paging, where the first-level page table has 512 entries and the second-level page table has 1024 entries, calculate the size of the first-level and second-level page tables in bytes.	(v)	CO4	L 3

Part - C
Answer any three (3x10=30 Marks)

Q. No	Question	Marks	CO	Bloom's Level

17.	a)	Explain the architecture of a Graphics Processing Unit (GPU) and discuss how it differs from a traditional CPU. Describe the key components and their functions in a GPU. Provide examples of tasks or applications that benefit significantly from GPU architecture.	(x)	CO5	L3
18.	a)	Identify and explain the three main types of hazards in pipelining: data hazard, structural hazard, and control hazard. Provide examples for each type and discuss the impact they can have on pipeline performance.	(x)	CO4	L3
19.	a)	Explain the principles behind Very Long Instruction Word (VLIW) Architecture. How does VLIW differ from Superscalar Architecture? Discuss the advantages and limitations of VLIW Architecture in comparison to Superscalar Architecture.	(x)	CO3	L 3
20.	a)	Describe the FIFO (First In, First Out) memory replacement policy. Given a memory with 4 frames and the following page reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Calculate the number of page faults using FIFO. Define Belady's anomaly.	(x)	CO4	L3
21.	a)	Explain the LRU (Least Recently Used) memory replacement policy. Consider a system that uses the Least Recently Used (LRU) page replacement policy. If a process references 10 pages in the order A, B, C, D, E, F, A, B, C, D, and a page fault occurs when referencing page F, determine the page that will be replaced.	(x)	CO4	L3

Course Outcomes:

CO1: To analyze and measure quantitative principles in computer science.
CO2: To design and analyze pipelining system.
CO3: To explain and analyze instruction level parallelism.
CO4: To analyze and design memory systems for higher bandwidth.
CO5: To categorize multiprocessor systems and analyze their performance.

Bloom's Level:

Remembering	Understanding	Applying	Analyzing	Evaluating	Creating
L1	L2	L3	L4	L5	L6