# COMP 103

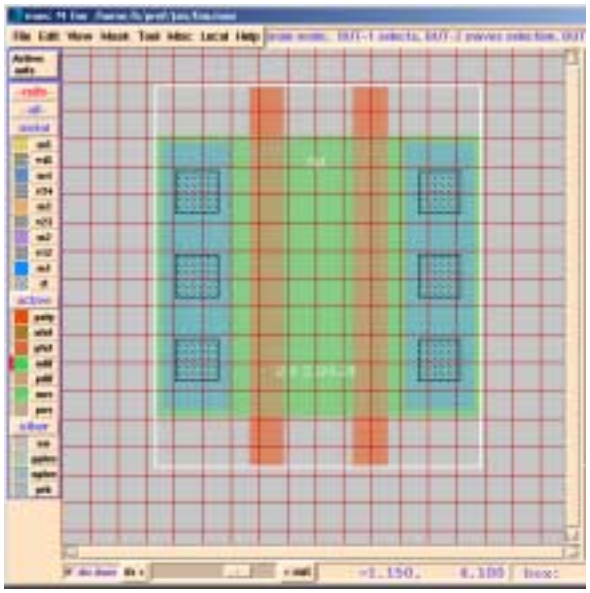
# Lecture 08

# Lab Prep: Design Rules & MOS Capacitance

[All lecture notes are adapted from Mary Jane Irwin, Penn State, which were adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]



## Layout Editor: *max* Design Frame

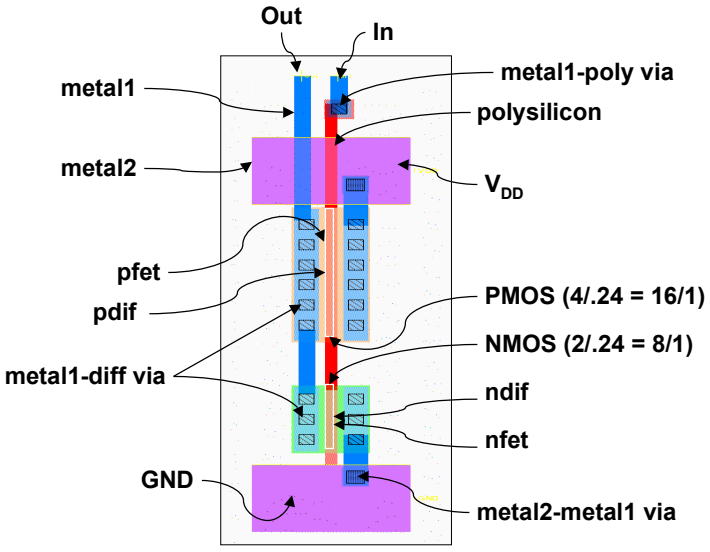


## *max* Layer Representation

- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support “stacked vias”
- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))
- Wells (nw) and other select areas (pplus, nplus, prb)

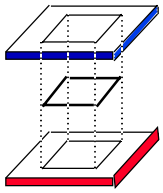


## CMOS Inverter Layout



## Simplified Layouts

- Online design rule checking (DRC)
- Automatic fet generation (just overlap poly and diffusion and it creates a transistor)
- Simplified via/contact generation
  - v12, v23, v34, v45
  - ct, nwc, pwc






## Design Rule Checker

## Design Rules

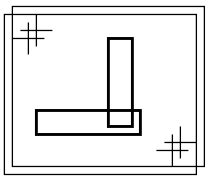
- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers



## Why Have Design Rules?

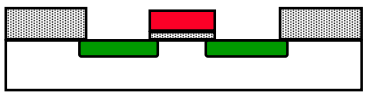
- To be able to tolerate some level of fabrication errors such as

- Mask misalignment



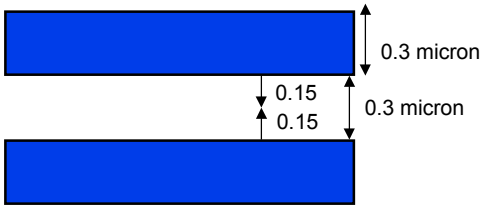
- Dust

- Process parameters (e.g., lateral diffusion)



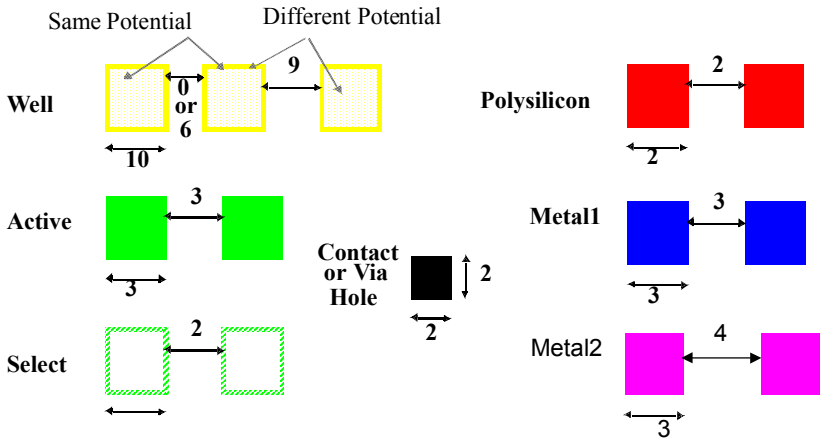
## Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab






## Intra-Layer Design Rules

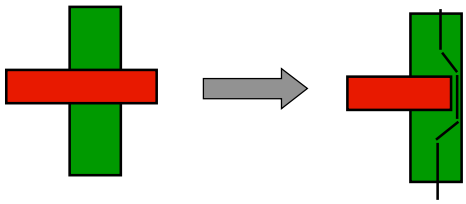



**Using Lambda Rules**

## Inter-Layer Design Rule Origins

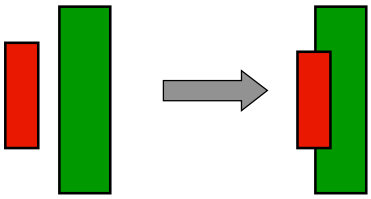
- Transistor rules – transistor formed by overlap of active and poly layers

Transistors



Catastrophic error

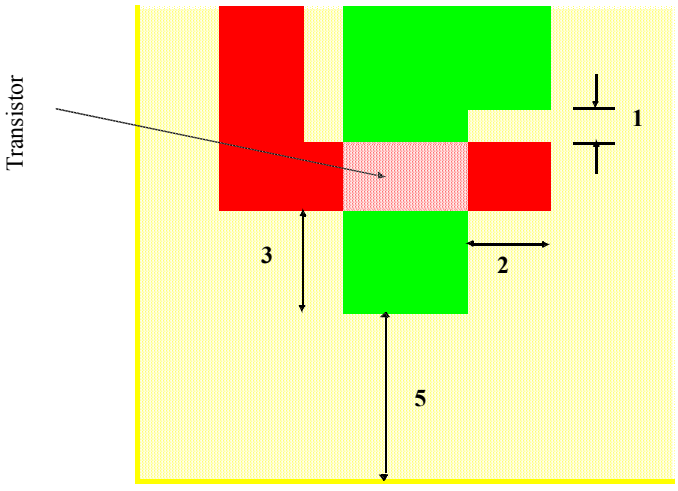
Unrelated Poly & Diffusion



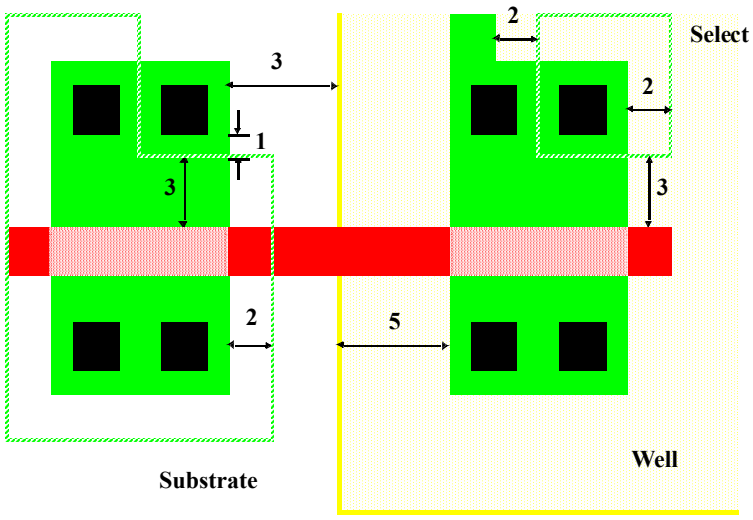
Thinner diffusion, but still working



## Transistor Layout



## Select Layer

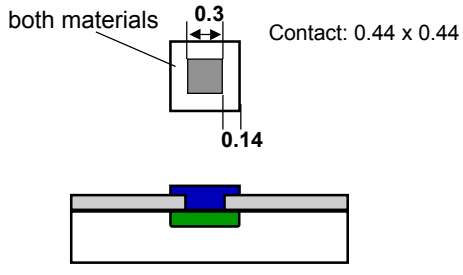




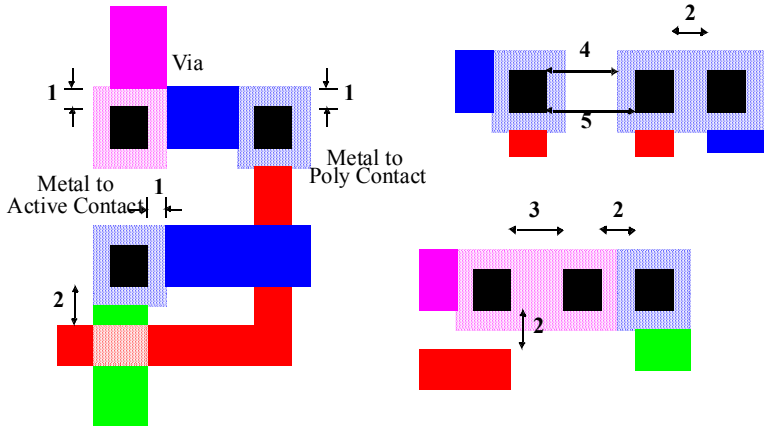

## Inter-Layer Design Rule Origins, Con't

- Contact and via rules

| | |
|---|---|
| M1 contact to p-diffusion<br>M1 contact to n-diffusion<br>M1 contact to poly | Contact Mask |
| Mx contact to My | Via Masks |



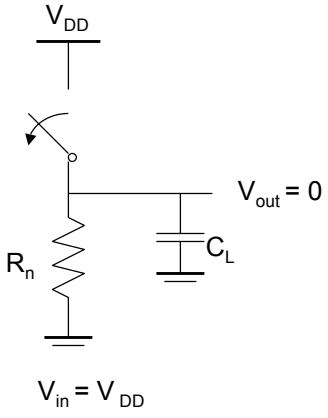
## Vias and Contacts






## CMOS Inverter: Dynamic

- Transient, or dynamic, response determines the maximum speed at which a device can be operated.

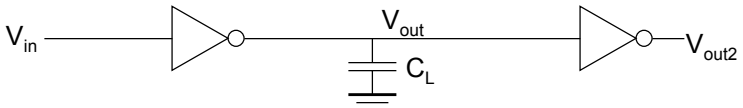



Today's focus

$t_{pHL} = f(R_n, C_L)$

Next lecture's focus

## Sources of Capacitance




intrinsic MOS transistor capacitances

extrinsic MOS transistor (fanout) capacitances

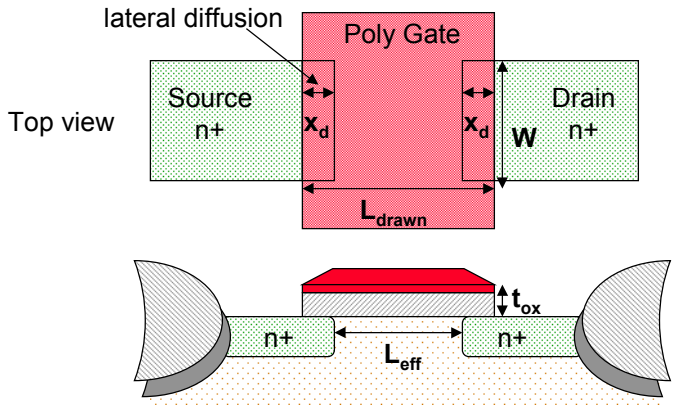
wiring (interconnect) capacitance



## MOS Intrinsic Capacitances

- Structure capacitances
- Channel capacitances
- Depletion regions of the reverse-biased *pn*-junctions of the drain and source

## MOS Structure Capacitances




Ignore the lateral diffusion

Overlap capacitance (linear) ignore this

$$C_{GSO} = C_{GDO} = C_{ox}\, x_d\, W = C_o\, W$$

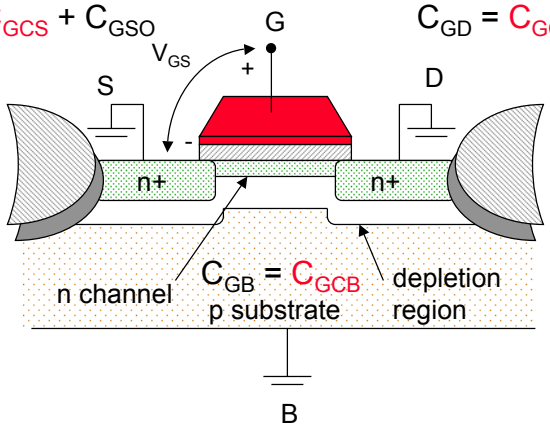
Cg = Cox WL Use this



## MOS Channel Capacitances

- The gate-to-channel capacitance depends upon the operating region and the terminal voltages

$C_{GS} = C_{GCS} + C_{GSO}$ $C_{GD} = C_{GCD} + C_{GDO}$



## Average Distribution of Channel Capacitance

| Operation Region | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ | $C_{GC}$ | $C_G$ |
|---|---|---|---|---|---|
| Cutoff | $C_{ox}WL$ | 0 | 0 | $C_{ox}WL$ | $C_{ox}WL + 2C_oW$ |
| Resistive | 0 | $C_{ox}WL/2$ | $C_{ox}WL/2$ | $C_{ox}WL$ | $C_{ox}WL + 2C_oW$ |
| Saturation | 0 | $(2/3)C_{ox}WL$ | 0 | $(2/3)C_{ox}WL$ | $(2/3)C_{ox}WL + 2C_oW$ |

- Channel capacitance components are nonlinear and vary with operating voltage
- Most important regions are cutoff and saturation since that is where the device spends most of its time

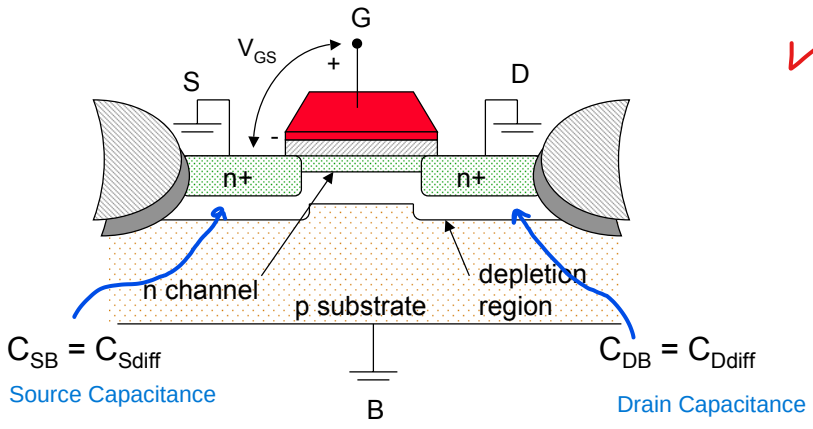
COMP103-L08.21

We do not want this slide

Ignore this slide

## MOS Diffusion Capacitances

- The junction (or diffusion) capacitance is from the reverse-biased source-body and drain-body pn-junctions.




$C_{SB} = C_{Sdiff}$

Source Capacitance

$C_{DB} = C_{Ddiff}$

Drain Capacitance

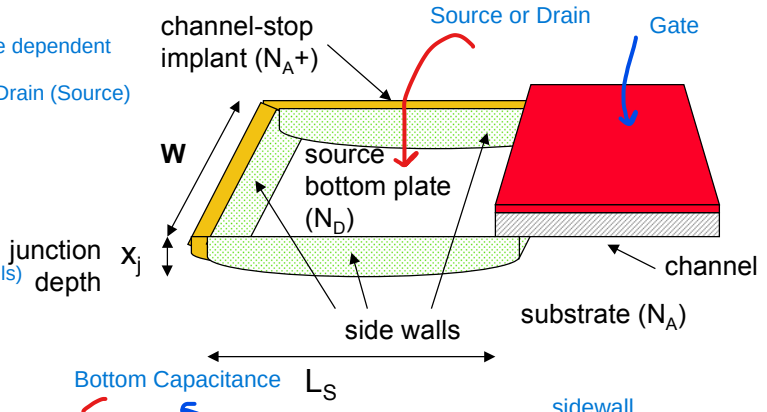
COMP103-L08.22

## Source Junction View

Drain and Source capacitances are Junction capacitance and are voltage dependent

The depend also on the Area of the Drain (Source) which forms the bottom capacitance

In old transistors and in DRAM transistors there is also Sidewall which depends on the perimeter and Xj ( area of sidewalls)




SW: Side Walls

sidewall

$$C_{diff} = C_{bp} + C_{sw} = C_j\, AREA + C_{jsw}\, PERIMETER$$

$$= C_j L_S W + C_{jsw}(2L_S + W)$$

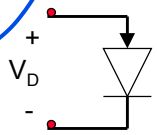
In new transistors the drain(or source) The transistor is not surrounded by (p) material but by insulator(SiO2), therefor no sidewall capacitance

Exists only in old transistors and in DRAM and some dynamic latches



## Reverse Bias Diode

- All diodes in MOS digital circuits are reverse biased; the dynamic response of the diode is determined by depletion-region charge or junction capacitance




Junction capacitance depends on voltage

$$C_j = C_{j0}/((1 - V_D)/\phi_0)^m$$

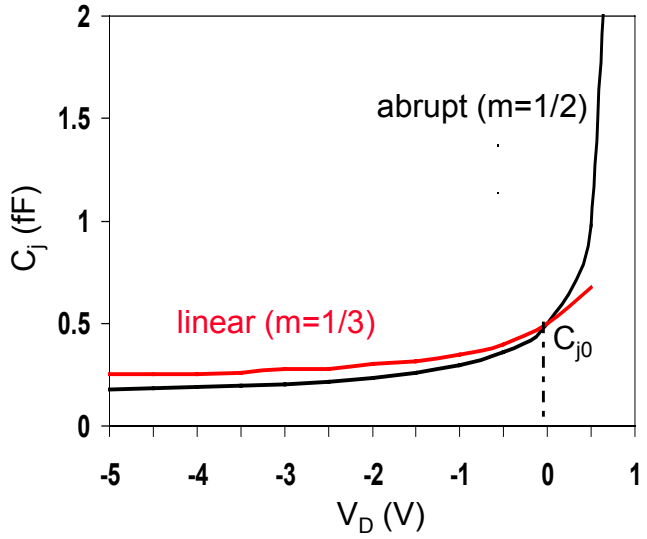
where $C_{j0}$ is the capacitance under zero-bias conditions (a function of physical parameters), $\phi_0$ is the built-in potential (a function of physical parameters and temperature)

and m is the grading coefficient

- m = ½ for an abrupt junction (transition from n to p-material is instantaneous)
- m = 1/3 for a linear (or graded) junction (transition is gradual)

- Nonlinear dependence (that decreases with increasing reverse bias)

## Reverse-Bias Diode Junction Capacitance






## Drain-Bulk Capacitance: $K_{eq}$'s (for 2.5 μm)

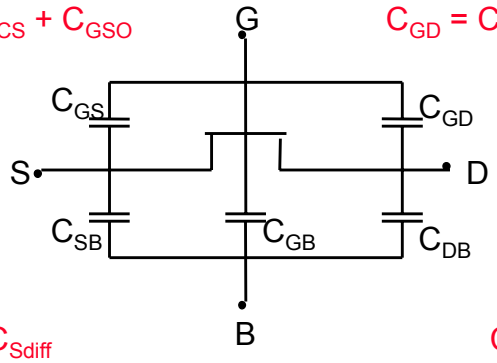
- We can simplify the diffusion capacitance calculations *even* further by using a $K_{eq}$ to relate the linearized capacitor to the value of the junction capacitance under zero-bias

$$C_{eq} = K_{eq}\, C_{j0}$$

| | high-to-low | | low-to-high | |
|---|---|---|---|---|
| | $K_{eqbp}$ | $K_{eqsw}$ | $K_{eqbp}$ | $K_{eqsw}$ |
| NMOS | 0.57 | 0.61 | 0.79 | 0.81 |
| PMOS | 0.79 | 0.86 | 0.59 | 0.7 |

## MOS Capacitance Model

$C_{GS} = C_{GCS} + C_{GSO}$ $C_{GD} = C_{GCD} + C_{GDO}$




$C_{SB} = C_{Sdiff}$ $C_{DB} = C_{Ddiff}$

$C_{GB} = C_{GCB}$



## Transistor Capacitance Values for 0.25µ

Example: For an NMOS with L = 0.24 µm, W = 0.36 µm, $L_D = L_S = 0.625$ µm

$C_{GSO} = C_{GDO} = C_{ox}\, x_d\, W = C_o\, W =$

$C_{GC} = C_{ox}\, WL =$

so $C_{gate\_cap} = C_{ox}WL + 2C_oW =$

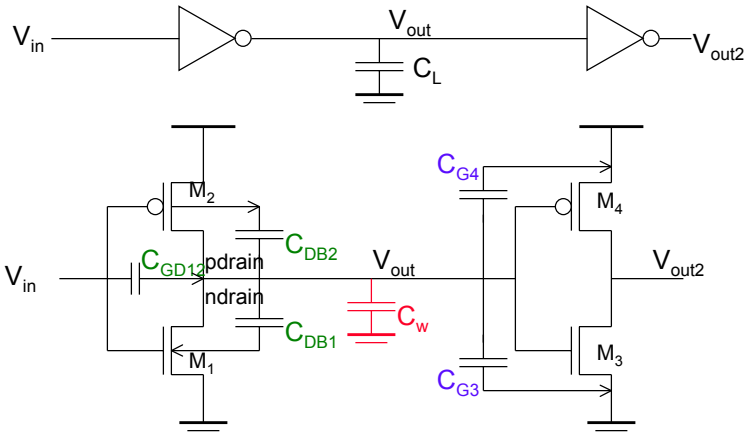
$C_{bp} = C_j\, L_S\, W =$

$C_{sw} = C_{jsw}\, (2L_S + W) =$

so $C_{diffusion\_cap} =$

| | $C_{ox}$ (fF/µm²) | $C_o$ (fF/µm) | $C_j$ (fF/µm²) | $m_j$ | $\phi_b$ (V) | $C_{jsw}$ (fF/µm) | $m_{jsw}$ | $\phi_{bsw}$ (V) |
|---|---|---|---|---|---|---|---|---|
| NMOS | 6 | 0.31 | 2 | 0.5 | 0.9 | 0.28 | 0.44 | 0.9 |
| PMOS | 6 | 0.27 | 1.9 | 0.48 | 0.9 | 0.22 | 0.32 | 0.9 |

## Review: Sources of Capacitance




intrinsic MOS transistor capacitances

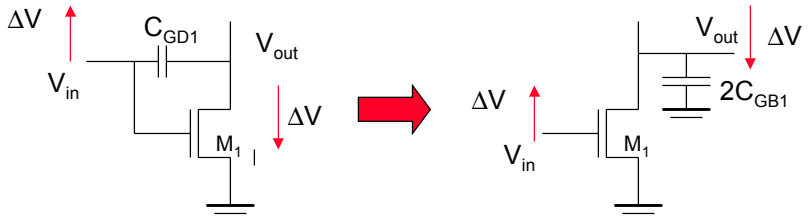
extrinsic MOS transistor (fanout) capacitances

wiring (interconnect) capacitance



## Gate-Drain Capacitance: The Miller Effect

- M1 and M2 are either in cut-off or in saturation.
- The floating gate-drain capacitor is replaced by a capacitance-to-ground (gate-bulk capacitor).




- A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground whose value is two times the original value

## Extrinsic (Fan-Out) Capacitance

- The extrinsic, or fan-out, capacitance is the total gate capacitance of the loading gates M3 and M4.

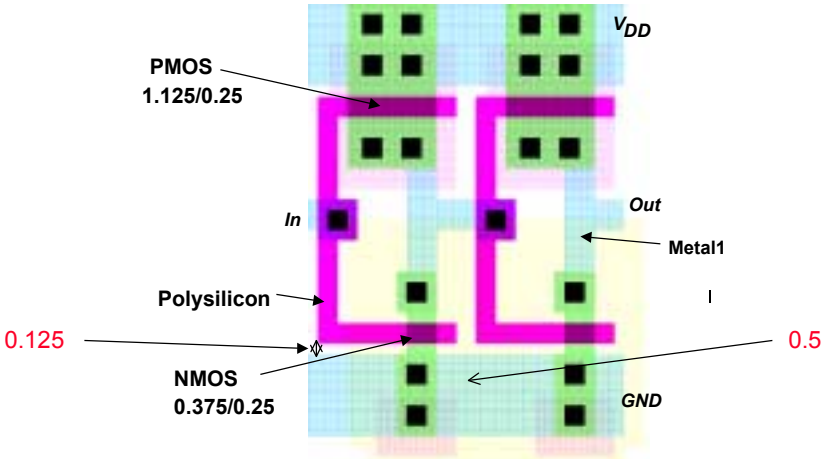
$$C_{fan\text{-}out} = C_{gate}\,(NMOS) + C_{gate}\,(PMOS)$$

$$= (C_{GSOn} + C_{GDOn} + W_n L_n C_{ox}) + (C_{GSOp} + C_{GDOp} + W_p L_p C_{ox})$$

- Simplification of the actual situation
  - Assumes all the components of $C_{gate}$ are between $V_{out}$ and GND (or $V_{DD}$)
  - Assumes the channel capacitances of the loading gates are constant



## Layout of Two Chained Inverters




| | W/L | AD (µm²) | PD (µm) | AS (µm²) | PS (µm) |
|---|---|---|---|---|---|
| NMOS | 0.375/0.25 | 0.3 | 1.875 | 0.3 | 1.875 |
| PMOS | 1.125/0.25 | 0.7 | 2.375 | 0.7 | 2.375 |

## Components of $C_L$ (0.25 µm)

| C Term | Expression | Value (fF) H→L | Value (fF) L→H |
|---|---|---|---|
| $C_{GD1}$ | $2\ C_{on}\ W_n$ | 0.23 | 0.23 |
| $C_{GD2}$ | $2\ C_{op}\ W_p$ | 0.61 | 0.61 |
| $C_{DB1}$ | $K_{eqbpn}AD_nC_j + K_{eqswn}PD_nC_{jsw}$ | 0.66 | 0.90 |
| $C_{DB2}$ | $K_{eqbpp}AD_pC_j + K_{eqswp}PD_pC_{jsw}$ | 1.5 | 1.15 |
| $C_{G3}$ | $(2\ C_{on})W_n + C_{ox}W_nL_n$ | 0.76 | 0.76 |
| $C_{G4}$ | $(2\ C_{op})W_p + C_{ox}W_pL_p$ | 2.28 | 2.28 |
| $C_w$ | from extraction | 0.12 | 0.12 |
| $C_L$ | $\Sigma$ | 6.1 | 6.0 |