IC Design

Homework # 3

(Due on 2022/11/24, 09:00. Verilog code and Report upload to NTU cool)

- ✧ Plagiarism is not allowed. 10% penalty for each day of delay.
- ✧ Any further questions, you can send e-mail to the TA (黃名善)
- ✧ TA email: r10943003@ntu.edu.tw , EE2-329

Specifications

In this homework, you are asked to design a **gate-level combinational circuit** that finds the Kendall rank coefficient of the four given pairs of numbers. Let (x0, y0), (x1, y1), (x2, y2), (x3, y3) be the four pairs of input data, and all the values of (xi) and (yi) are unique (ties are neglected for simplicity). Any pair of observations (xi, yi) and (xj, yj), where i < j, are said to be concordant if the comparison outcome of (xi, xj) and the comparison outcome of (yi, yj) are the same; otherwise, they are said to be discordant.

For example:

(1, 3) and (4, 2) are discordant pairs.

(1, 2) and (3, 4) are concordant pairs.

Then, the Kendall τ coefficient is defined as:

$$\tau = \frac{(\text{number of concordant pairs}) - (\text{number of discordant pairs})}{(\text{number of pairs})} = 1 - \frac{2(\text{number of discordant pairs})}{\binom{n}{2}}$$

The inputs of this circuit are **four pairs of 4-bit unsigned** digital values, denoted as *(i0_x, i0_y), (i1_x, i1_y), (i2_x, i2_y), (i3_x, i3_y)*. The output of the circuit denoted as ***kendall***, is a **4-bit signed number (round to the nearest number) represented with 2's complement and the last two digits are the fractional part**.

For example:

1101 will be -0.75 in floating point.

0101 will be 1.25 in floating point.

Below are some examples of the I/O:

Input								Output
i0_x	*i0_y*	*i1_x*	*i1_y*	*i2_x*	*i2_y*	*i3_x*	*i3_y*	*kendall*
0xb	0x7	0x6	0x2	0x5	0xb	0xd	0xc	0001
0xc	0xd	0x5	0x9	0x1	0x4	0x3	0x5	0100
0x7	0x5	0xc	0x6	0x1	0x4	0x5	0x2	0011
0x7	0x3	0xc	0xd	0x0	0x6	0x6	0x8	0001

There are some important things that you should notice:

- Your design should base on the **standard cells in the lib.v**. All logic operations in your design **MUST consist of the standard cells** instead of using the operands such as "+", "-", "&", "|", ">", and "<". **Note that the score of HW3 will be 0 if you use any of them.**
- Design your homework in the given "kendall.v" file. **You are NOT ALLOWED to change the filename and the header of the top module (i.e. the module name and the I/O ports)**.
- If your design contains more than one module, don't create new file for them, just put those modules in "kendall.v."
- The output waveform will be dumped to file "**kendall.fsdb."** You can use nWave to examine it.
- **For each set of input data, the test bench will allow your circuit to calculate outputs within 20ns.** Once exceeding 20ns or detecting the correct answer from your circuit, the test bench will soon provide the new data set to your design until all 10000 data sets have been simulated.

Grading

1. Gate-level design using Verilog (80%)

Your score will depend on both the correctness and performance of your design. We provide a "public" test bench with 10000 datasets. What follows is the grading policy:

Correctness & Performance	Score
Fail to pass the test bench.	40 * (1-err #/10000)
Functionally correct	40
Critical Path < 6ns	45
Critical Path < 5.5ns	50
Critical Path < 5ns	55
Critical Path < 4.5ns	60
Critical Path < 4ns	70
Critical Path < 3.5ns	80
Using operands, not standard cell logic	0
Plagiarism	0

Testbench will provide related information for grading:

```
Congratulations! Your critical path is below 4!
```

Critical Path <4ns

2. Report (20%)

You should also describe and discuss your design. Below are required items in your report.

- Circuit diagram (10%)
  Plot the circuit diagram of your design. You are encouraged to plot it hierarchically so that the reader can understand your design easily.
- Discussion (10%)
  Discuss about your design. For example, how do you find the concordant or discordant pair, how do you deal with the divider, and how do you improve your critical path.

Notification

Following are the files you will need (available on the class website)

HW3.zip includes

- **HW3_2022.pdf** : this document.
- **HW3_tutorial** Verilog introduction
- **kendall.v**:
  Dummy design file. Program the design in this file.
  The header of the top module and the declaration of the I/O ports are predefined in this file and you cannot change them.
- **lib.v**: standard cells.
- **tb_kendall.v**:
  Testbench for your design.
- **i0.dat, i1.dat, i2.dat, i3.dat:**
  Input patterns for the test bench. Put these files in the folder that contains **tb_ kendall.v** when doing simulation.
- **golden.dat:**
  Output patterns of correct answers for the test bench. Put this file in the folder that contains **tb_kendall.v** when doing the simulation.

- The following files should be compressed and uploaded to NTU cool by the due time.
  For example:
  HW3_r10943003.zip
  - HW3_r1094303 (folder)
    - Report (PDF format)
    - kendall.v

TA：黃名善，EE2-329

TA email: r10943003@gmail.com

HW3 Office hours: 11/22 14:00-16:00 @ 電二 329 室

11/23 14:00-16:00 @ 電二 329 室

If you have no time at office hours, you can email TA to discuss another time for an appointment.