IC Design HW4

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(a) simulation

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                Summary
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        Clock cycle:           10.5 ns
        Number of transistors: 6752
        Total excution cycle:  2378
        Correctness Score:     40.0
        Performance Score:     168590688.0
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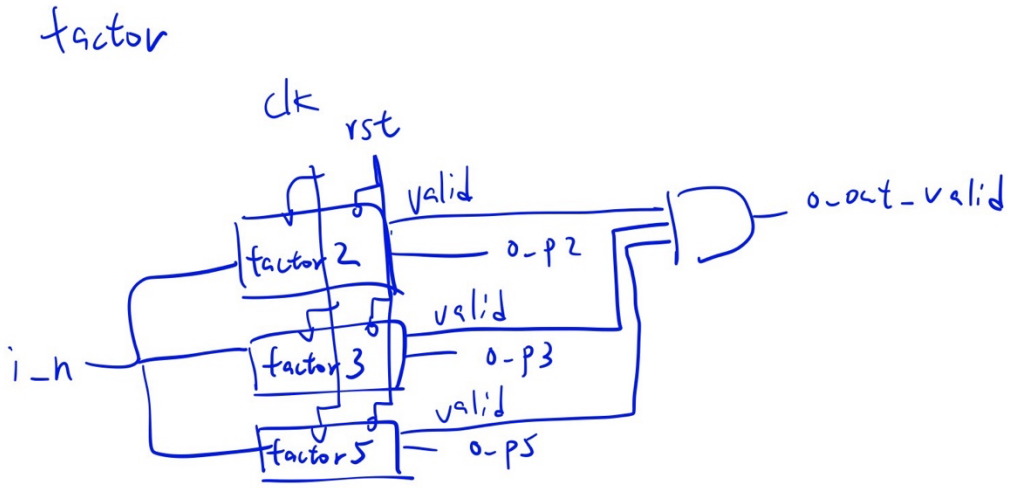
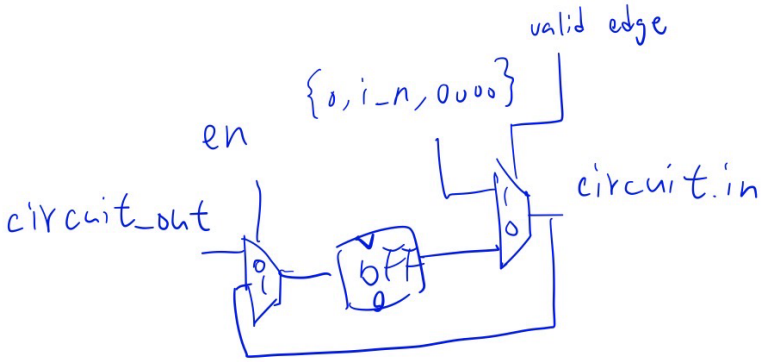
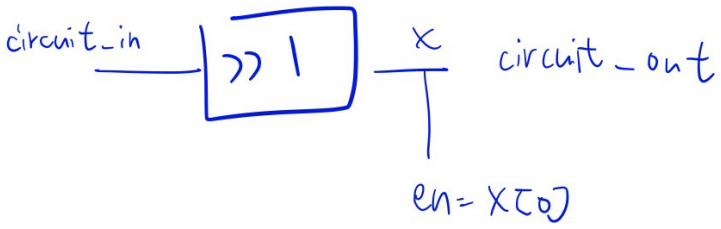
(b) circuit diagram

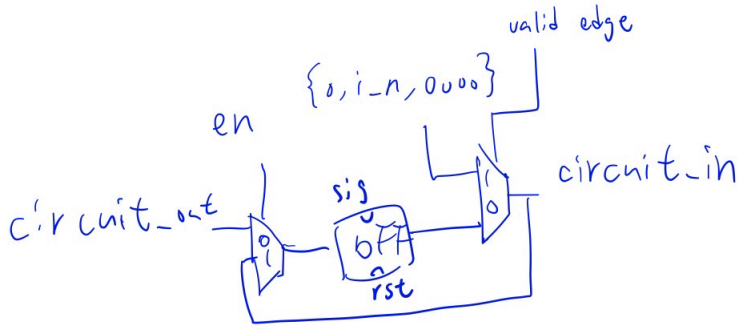


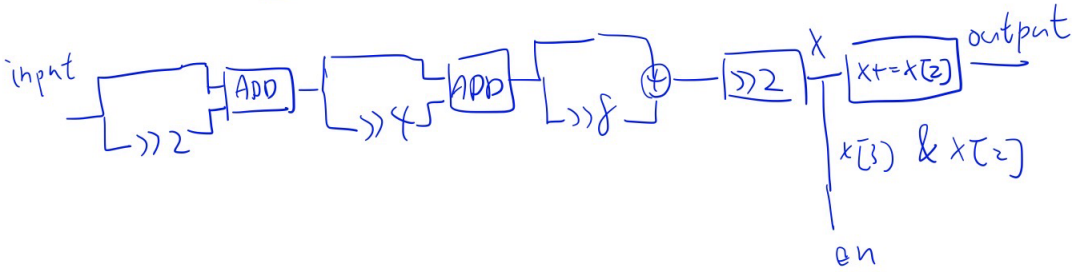
factor 2



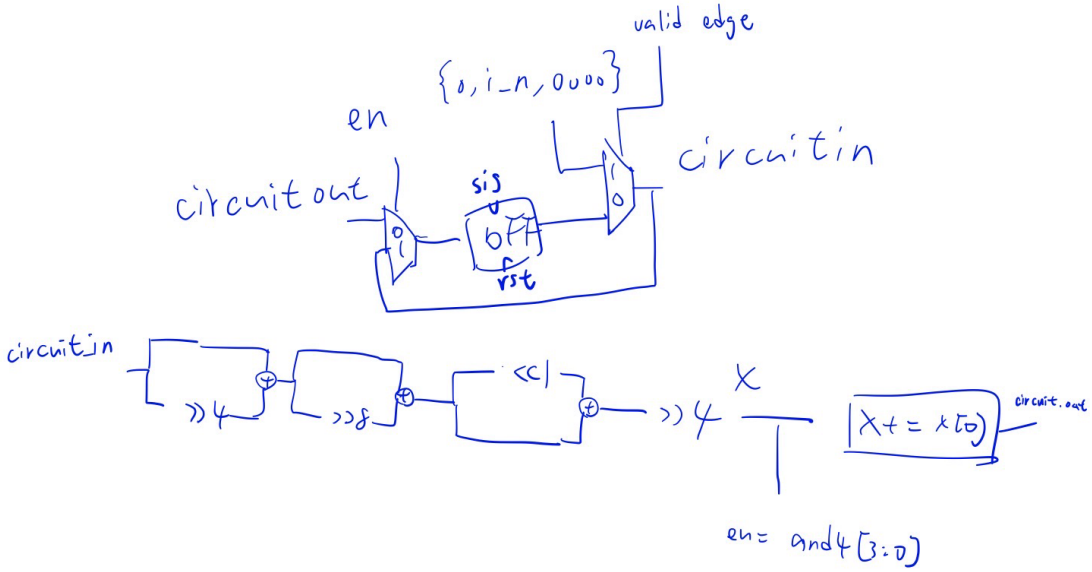


factor 3

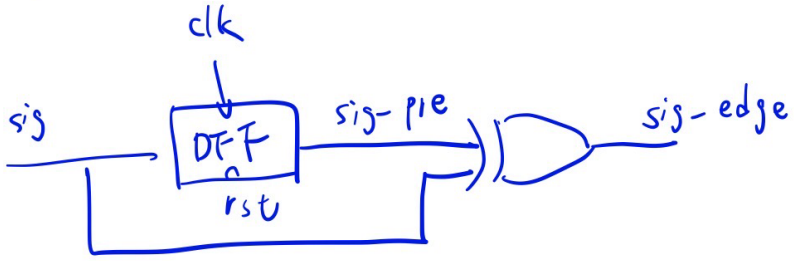




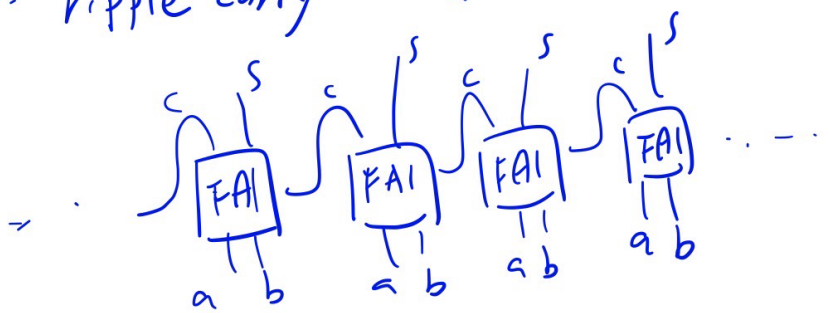
factor 5

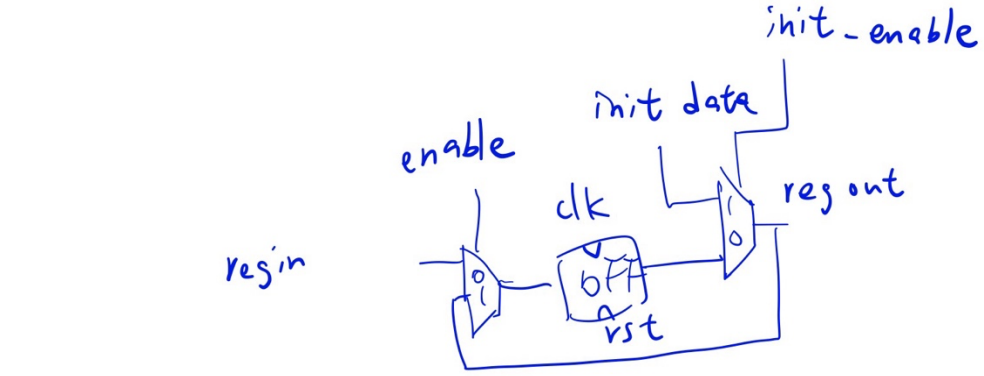


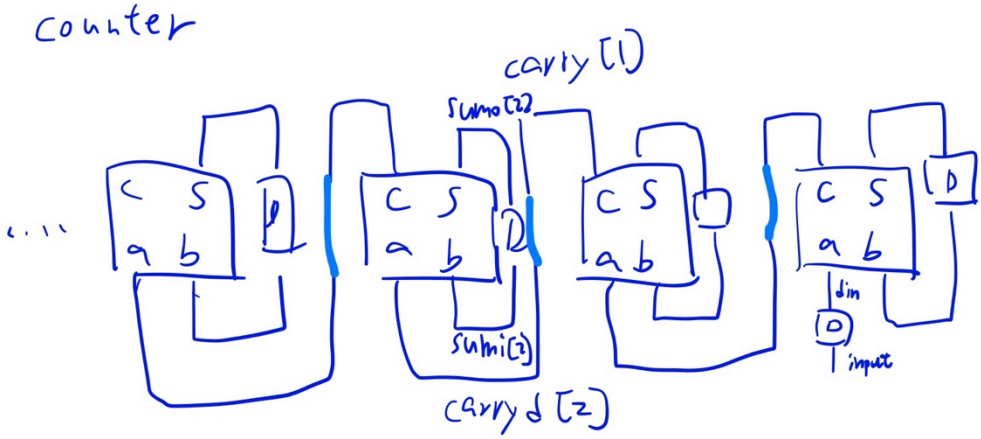
Sig to Edge



RCA: ripple carry adder







(c) discussion

My factor2 is designed by right shift the number at each clock if the LSB == 0, other output valid=1 and lock the value. The factor3 and factor is designed by an approximation: $\frac{x}{3} = x\left(1+\frac{1}{2^2}\right)\left(1+\frac{1}{2^4}\right)\left(1+\frac{1}{2^8}\right)\ldots$, and $\frac{x}{5} = 3x\left(1+\frac{1}{2^4}\right)\left(1+\frac{1}{2^8}\right)\left(1+\frac{1}{2^{16}}\right)\ldots$, to implement this algorithm, first add 2 bits at MSB and 4 bits at LSB, preventing overflow and provides the decimal part. The enable signal of factor3 is and2(regout[3],regout[2]), and that of factor5 is and4(regout[3],regout[2],regout[1],regout[0]). Because this is an approximation

method, the decimal part would be all 1s if it's real value should carryout 1 to integer part. I Also designed the common circuit part such as RegSet, which can control the loop and initialize, and the edge detector to generate the signal for initialize control. Then just brings the circuit diagram into code. I at first and misunderstood that it needs to output K, so I put them in a serial manner. The performance is nearly 2.5 times worse. And finally turned it into parallel and greatly reduced the critical path. In my perspective, this design is better than constructing a shifting divider because it not only needs to add much more times but also more complicated. Though the shift divider may have less transistors, it's still not worth it. As for the short come of this design, I think the most severe one is that the evaluation circuit takes a lot of time and only did in a single clock, which means the clock period is stuck by them. I think if I have more time on this problem, I would try to pipeline the combination circuit by more dffs to shorten the minimum clock period.