Operation Manual

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1440 HIGH VOLTAGE

WARRANTY

LeCROY CORPORATION warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1 year from the date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts and repairs are warranted for 90 days. This warranty extends only to the original purchaser and shall not apply to fuses, disposable batteries, or any product of parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within one year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions or operations, repairs will be billed at a nominal cost. In such cases, an estimate will be submitted before work is started, if requested.

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IN THE EVENT OF DAMAGE IN SHIPMENT to original purchaser the instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed Packing List. The manufacturer will not be responsible for shortages against the packing sheet unless notified promptly. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the LeCroy factory or the nearest service facility).

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ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily

answered by a member of our Engineering Services Department, telephone 914-578-6058 or your local distributor. You may address any correspondence to:

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A T T E N T I 0 N

SEE SECTION 2 FOR A GUIDE TO INSTALL, POWER AND INITIALLY OPERATE THE 1440 SYSTEM. MODULES SHOULD NOT BE REMOVED OR PLUGGED IN WHILE THE UNIT IS TURNED ON. DAMAGE MAY BE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

DO NOT OBSTRUCT AIR INTAKE.

IT IS IMPORTANT TO SET THE SIGN BIT FOR THE CORRECT POLARITY WHEN REQUESTING HIGH VOLTAGE. IF 2500 (INSTEAD OF -2500) IS REQUESTED FROM A NEGATIVE POLARITY UNIT THEN THERE WILL BE NO HIGH VOLTAGE OUTPUT.

SEE BACK POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

HV RESPONSE TO PROGRAMMING CHANGES IS IMMEDIATE WHEN HV IS ON. A CHANNEL CAN GO FROM 0 V OUTPUT TO 2500 V OUTPUT IN LESS THAN 40 MSEC.

A T T E N T I 0 N

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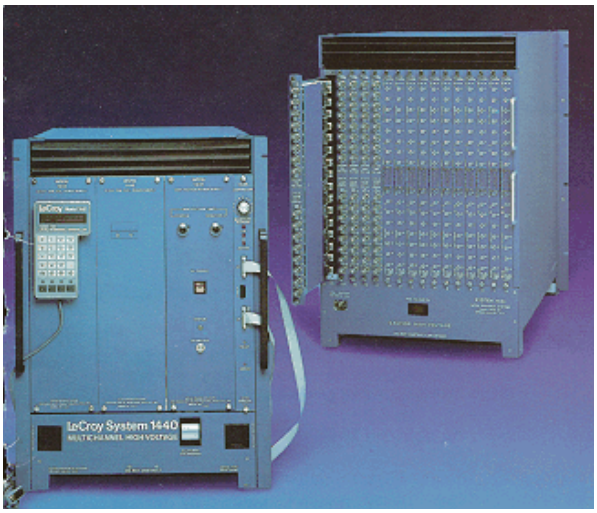
HIGH VOLTAGE SYSTEM

MULTIPLE CHANNEL, HIGHEST DENSITY **LeCroy**

SYSTEM 1440

WITH LOCAL REMOTE CONTROL



- Up to 256 Channels Per Mainframe
- Remote Control Via CAMAC or RS-232-C
- Lowest Cost Per Channel
- ± 2500 V, 2.5 mA Per Channel
- Slow HV Ramp-up and Ramp-down
- Short-circuit and Arc Protected
- TTL System Interlock/HV Status Output

FOR LARGE-SCALE PHOTOMULTIPLIER ARRAYS AND WIRE CHAMBER SPECTROMETERS

System 1440 is a multichannel programmable high voltage system designed for large scale applications where high reliability and performance are most important. The system provides up to 256 channels of high voltage in each 1449 chassis. Up to 16 chassis, or 4096 channels, may be controlled and monitored via a single daisy chain. Control may also be done from CAMAC via the LeCroy Model 2132 CAMAC/HV Interface.

FEATURES

Digital Voltage Sensing

A system ADC reads the actual output voltage, NOT the demand setting, with 12-bit precision. The output polarity is also reported.

Complete CAMAC Programmability

All the operations which may be performed from the TTY are available through the Model 2132 CAMAC interface. A simple binary control word scheme makes programming easy.

Thermal Protection

A temperature monitor on each of the low voltage power supplies shuts off the high voltage in the event of overheating that can result from excessive loading, clogged fan filters, or high ambient temperatures.

Continuous Memory
Battery backup protects the integrity of internal memory for 24 hours. This makes the memory immune to occasional power failures. The batteries are continuously recharged whenever AC power is available.

FUNCTIONAL DESCRIPTION

System 1440 employs high efficiency switching supplies. As a fourth generation design, the HV supplies offer cool and reliable operation. The system reliability is further enhanced by the design of the mainframe which provides excellent cooling and a minimum of interconnects. Convenience, versatility and serviceability have been achieved through the use of modular construction. The microprocessor circuit, the power unit, two 31 V DC supplies and up to sixteen 16-channel HV supplies plug into the 1449 mainframe. As a result, the system can provide negative outputs, positive outputs, or both. Systems of less than 256 channels may be easily established. A more economical low power chassis, Model 1449E, is also possible for those applications which require less than the full power output of the unit. For details, see the ordering information listed below.

System 1440 provides many features to protect its costly loads against HV damage. The HV run-up and run-down rates may be selected by a jumper option on the control unit. Rates of 0.5 -- 3.0 kV/sec are available. Rapid shutdown (panic-off) of all channels is provided locally by a pushbutton and also from a remote sensor via TTL System Interlock input. The 1449 chassis provides a clamp-to-ground output to indicate that the HV is on. The 1443/12 HV module provides an interlock to disable all 16 channels when the Card Interlock contacts are opened (available on block connector-type modules only).
The 1449 mainframe has two vernier potentiometers to provide separate hardware limits to set the maximum voltage output of the positive and negative channels. Two 8-bit registers are available to provide separate software limits for setting the output current limit threshold of the positive and negative channels. The 1443/12 Series modules are available for both polarities. To avoid problems caused by the use of modules of the wrong polarity, the 1443/12 treats a demand voltage of the wrong polarity as a 0 V demand. As a second safeguard, output polarity indication is provided in the voltage monitor readback.
System 1440 contains a 13-bit ADC (12 bits plus sign) to allow the output voltage of all channels to be measured. The accuracy of the monitor is +(0.1%+1.5 V). The voltage programmability of the HV modules is 12 bits (plus sign bit).
The maximum output voltage available from the 1443/12 Series card is 2500 V. The full scale of the system programming may be jumper selected to be 2500 V, 2047 V, 1500 V and 4095 V (2500 V maximum allowable demand value). This allows the range and resolution of System 1440 to be matched to the experiment requirement.

ORDERING INFORMATION

Mainframe 1449/1449E

To order a System 1440, it is first necessary to determine the total HV power required for the application. For those systems requiring less than 256 channels or those requiring less than full voltage and current, the low power mainframe, 1449E, may suffice. If not, order the Model 1449 mainframe. Both versions include all logic and control units required for use with up to 256 HV channels. The 1449 provides a total of 1.6 kW to the 1443/12 HV cards. The Model 1449E provides 0.8 kW. For each 1443/12 card in excess of eight, 15 W must be deducted from the available 1449E power.

Example: A system consisting of 176 channels, operating at 2 kV, each with a load of 2 mA must provide: 176 x 2 kV x 2 mA = 704 W. Since 11 cards are required, 755 W are available from the 1449E so the lower priced 1449E may be selected.

If the 1449E must be upgraded for 1600 W operation, a Model 1442 DC Supply must be ordered. The time required to install and test the addition is less than 1 hour. No special tools are required.

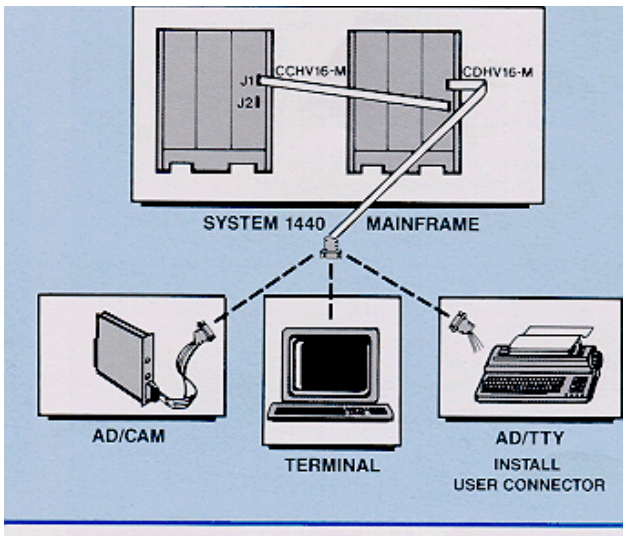
16-Channel IIV Modules 1443 Series
HV modules provide 16 outputs of up to 2.5 mA at 2500 V. Modules of positive and negative output

are available and are denoted by P and N suffixes, respectively.
The HV modules employ front-panel block connectors for the 16 HV outputs. Also available is the SHV connector by specifying an F suffix.

Model 1443N/12	Negative, block connector
Model 1443P/12	Positive, block connector
Model 1443NF/12	Negative, SHV connectors
Model 1443PF/12	Positive, SHV connectors
Model 1440X	Extender for 1443/12 Series HV module and 1445 microprocessor unit. Intended as a service tool.
Model 1441	Power module. Spare part. Included in 1449 Series.
Model 1442	DC supply. Included in 1449 Series.
Model 1445	Microprocessor unit. Included in 1449 Series.
Model 1447	Handheld TTY.
Model 2132	Interface to CAMAC

CONNECTORS

Model HVCK20FB	Female bulkhead type (used on 1443/12 front panel).
Model HVCK20MB	Male bulkhead type.
Model HVCK20FC	Female cable type.
Model HVCK20MC	Male cable type (mates with 1443/12 front panel).



ACCESSORIES

CCHV16-M A data cable used to connect the 1440 chassis to each other. M is the length of the cable in meters.

CDHV16 M A data cable used to connect the 1440 chain to a controller. A standard RS-232-C 25-pin "D" connector is employed at the controller end. M is the length of the cable in meters. See below for "D" connector to adapter options.

AD/TTY Mates with CHV16 cable. Provides pigtails suitable for direct connection to a Teletype.

AD/CAM Mates with CDHV16 cable. Provides the correct connector for connection to the Model 2132 Interface to CAMAC.

Handheld Controller

Optional Model 1447 handheld controller allows local control of a 1449 chassis. By plugging the Model 1447 into the Auxiliary Control connector of the 1449 chassis, commands can be issued to the chassis without interruption of the other chassis in the control daisy chain.

Panic-Off
A front-panel pushbutton shuts down all supplies promptly for protection against the unexpected.

HV Status Output
A front-panel Lemo output used to indicate HV present at rear connectors. May be used for personnel safety interlocks or as an independent indicator.

Interlock

A front-panel BNC input accepts a TTL input, triggering a panic-off. Internal programming jumper allows user assignment of logic levels, allowing the input to be used as a failsafe interlock or a remote panic-off.

Error Indicator

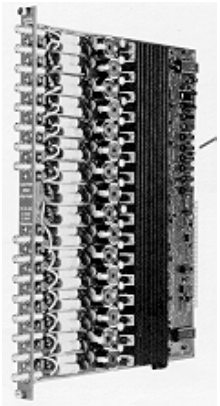
A front-panel Lemo connector used to indicate that all HV channels are operating within 1.5% (of F.S.). An error condition produces a TTL clamp-to-ground. Empty stations within the mainframe are ignored for this diagnostic. If the error is corrected, the Error Indicator output returns to its quiescent open circuit condition.

Voltage Limit

Two front-panel adjustments set hardware limits separately for positive and negative channels.

Model 1443 16-CHANNEL HV MODULE

Each 1443 card has 16 independently controlled High Voltage outputs. These cards may be ordered with block connectors or with SHV connectors (F suffix) for the High Voltage outputs.



Sophisticated Interactive TTY Operation
A simple, easy to understand mnemonic language allows all of the features of System 1440 to be exercised. This includes setting, measuring and adjusting any channel or all channels. The language offers iterative command execution similar to a **FORTRAN DO Loop**, allowing commands to operate on groups of channels. The system can offer a status report and print out an array of measurements of all outputs within the mainframe. Each mainframe must be assigned a unique address. This allows commands to be referred to each chassis. Special shorthand allows the addressing to be skipped after the first reference. An RS-232-C type interface is used.

Intelligent Daisy Chain
Up to 16 mainframes may be operated remotely. Serial Transmit and Receive lines are used. An identifier line allows the system to differentiate between **CAMAC** and **TTY** modes. This allows for **ASCII** coding for **TTY** operation and binary coding for **CAMAC** operation. Binary coding greatly simplifies programming. The 1440 system automatically knows which remote device is active.

Fault Indicator
A front-panel connector signals a fault by a clamp-to-ground. A fault condition is generated by a failure of any of the DC power supplies. The most common causes are over-temperature or over-current conditions.

SPECIFICATIONS

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Model 1449/1449E HV

CONTROL MAINFRAME
GENERAL
HV Modules/Mainframe: Up to 16

Channels/Mainframe: U p to 256

Maximum HV Output Power: 1.6 kW for Model 1449. 800 W for Model 1449E. For each 1443/12 in excess of eight, deduct 15 W from the 800 W available.

DISPLAY

HV ON Indicators: Yellow lamp indicates HV is enabled for turn on, i.e., HV DISABLE is not actuated and INTERLOCK is not asserted. Integral with front-panel HV ON indicator (red lamp) and HV DISABLE button. Rear-panel indicator lamp.

LVPS Status: Two LED's indicate presence of -- 15 V and + 5 V. Ready lit by + 15 V.

System Active: Front-panel LED indicates 1443/12 Cards enabled for generating HV.

MECHANICAL

Packaging: 19" rack-mount chassis, 17" wide x 22" deep x 261/4" high.

(Add 3" to depth to include handle protrusion.)

Input Power: 180-260 V AC 50/60 Hz <15 A.

Ambient Humidity: 0 to 85% relative humidity.

Operating Temperature: 10 to 40ºC ambient.

Shipping Weight: 210 lbs. (95 kg).

Model 1443

16-CHANNEL HV MODULE

Channels/Module: 16

Output Voltage: 0 to 2500 V; > 500 V for rated performance. Polarity indicated by

N or P suffix.

Voltage Regulation: 0.05% of full scale, line and load.

Full Scale: 2500 V, 2047 V, 1500 V; 4095 V also available

(limited to 2500 V max.) mainframe jumper option.

Programming Step: 0.025% of full scale.

Programming Accuracy: <+0.2% + 2 V) for demand voltages > 500 V.

Programming Reproducibility: < 1 V at a constant load and temperature

after 10-minute warmup.

Voltage Monitor Accuracy: +(0.1% + 1.5 V) channel-to-channel.

Monitor Long-Term Stability: <1.5 V/wk at constant load and temperature.

Output Long-Term Stability: <2 V/wk at constant load and temperature.

Monitor Temperature Coefficient: Typically 0.005%/§C. Max., 0.01%/§C

form 500 V to 2500 V (10ºC to 40ºC ambient).

Output Ripple: Typically <50 mV peak-to-peak; <250 mV peak-to-peak maximum.

Current Output: Up to 2.5 mA per channel.

Output Protection: Fully protected against arcs at load, short circuit and overload.

Output Connector Type: Multiconductor block-type connectors. SHV connectors

specified by F suffix.

Model 1443 16

CHANNEL HV MODULE
BLOCK CONNECTOR DATA

PIN ASSIGNMENTS

PIN	FUNCTION
1	HV Output Channel 0
2	HV Output Channel 1
3	HV Output Channel 2

4	HV Output Channel	3
5	HV Output Channel	4
6	HV Output Channel	5
7	HV Output Channel	6
8	HV Output Channel	7
9	HV Output Channel	8
10	HV Output Channel	9
11	HV Output Channel	10
12	HV Output Channel	11
13	HV Output Channel	12
14	HV Output Channel	13
15	HV Output Channel	14
16	HV Output Channel	15
17	Ground Return	--
18	Ground Return	--
19	Interlock (short to 20 for enable)	--
20	Interlock (short to 19 for enable)	--

SECTION 2
OPERATING THE 1440

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2.1 Installation and Setup

2.1.1 Uncrating and Inspection

The packaging for the 1440 System consists of a heavy cardboard box and a wooden pallet held together by two steel bands. The 1440 container should always be oriented with the pallet down. The package is custom made for the system and should be saved for any subsequent shipments which may be required. Rebanding requires the use of a banding machine, commonly available in Shipping and Receiving departments.

To open the box, cut the two bands and lift the cardboard box off of the unit. The 1440 can be lifted off of the pallet, allowing the package to be saved. Discard the bands.

Inspect the 1440 System for signs of damage. If problems are found, contact your nearest LeCroy office for assistance. The 1440 System employs modular construction to aid in service and enhance system flexibility. Check each of the subassemblies to be sure that it is seated in place and that its captive securing screws are snug. The subassemblies that should be checked are summarized in the following sections.

2.1.2 Front Panel Assemblies (See Figure 2.1)

2.1.2.1 Model 1449 or 1449E are the model numbers of the mainframe including power supplies and control. The 1449-Series does not include the plug-in HV cards. Inspect the structure for mechanical integrity. Front panel units may be inspected by loosening their retaining screws. The assembly will then pivot on its lower edge as shown in Figure 2.2 and 2.3. A "catch" will hold the unit in the open position. The "catch" must be released before closing the unit.

2.1.2.2 Model 1445 is the controller for the unit. It is located in the rightmost position in the front of the 1449. It is a plug-in module. The front panel of the unit (see Figure 2.4) provides communication connectors (both the control daisy chain and the optional hand held controller), Fault and Error diagnostic outputs, power supply and microprocessor pilot lights and a mainframe address selection switch. On-board jumpers allow the user to select the communication BAUD RATE, the voltage programming full scale and the voltage readback full scale. When the unit leaves the factory, these values are set to 1200 BAUD, 4095 V and 4095 V respectively. For details on reprogramming, see Figure 2.8.

2.1.2.3 Model 1441 is the Supply and Control module. It is located to the left of the Controller. The Model 1441 provides +15 V and +5 V. High voltage limit circuits for both positive and negative supplies voltage run up and run down circuitry, safety-interlock functions and the line voltage monitor. The 1441 is hinged at the bottom and may be accessed by unfastening the top two screws and pivoting it out.

The front panel of the Model 1441 includes voltage limit vernier potentiometers, and HV ENABLE (safety) button, an HV STATUS indicator (TTL compatible) output and a pilot light and an INTERLOCK input.

The Model 1441 contains jumpers to set the voltage run-up rate, voltage run-down rate and the Interlock polarity. These are factory set, respectively, to 1 KV/sec, 1 KV/sec and normal (not asserted when open). For details on reprogramming, see Figure 2.5.

2.1.2.4 Model 1442 is a 1 KW DC supply used to provide power to the 1443 high voltage plug-in cards. The Model 1449 contains two of these units, located in the left two compartments of the front of the unit. The right (center) 1442 station is vacant in the 1449E. The 1442 subassembly does not include the front panel. Separately ordered 1442 for spares will be supplied without the front panel which is part of the mainframe.

2.1.2.5 Model 1447 is a hand-held controller (see Figure 2.6) intended for local operation of the 1440 system. It is an optional accessory not included in the 1449/1449E package. When plugged into the 1447 input of the Model 1445, it overrides the control daisy chain to this unit only. Other mainframes are unaffected by the installation of the 1447.

2.1.3 Rear Panel Assemblies

2.1.3.1 Description

Up to sixteen of the 1443-Series sixteen-channel high voltage cards plug into the 1449 or 1449E mainframe. Cards designed to provide outputs of negative or positive polarity may be plugged into the unit without regard to position in the chassis.

2.1.3.2 Calibration of 1443 Cards

Field calibration of the 1443 series HV Cards is easily done with the panel accessable potentiometer on each HV channel. The action of the potentiometer is to change the monitor reading reported by the 1445 controller. Turning the adjustment clockwise increases the magnitude of the HV output. Typically the potentiometer allows about ± 30 volts of adjustment.

The following procedure applies for each channel to be calibrated.

1. Program a Demand voltage of ± 2500 volts (depending on card polarity).
2. Read actual output of the channel through the mainframe monitor and note reading.
3. Measure actual HV output with an external metering scheme and while monitoring adjust panel accessable potentiometer to set the reading on the external metering scheme to agree with that of the internal ADC Monitor as done in step 2.

This assures that the internal ADC monitor agrees with the actual HV output. By using the Update feature of the 1440 system, accuracy of the HV outputs can be improved almost to the accuracy level of the internal monitor.

2.1.4 Power

2.1.4.1 Supply Voltage -- The 1449 mainframe requires input voltage from the line between 208 to 240 VAC 50 to 60 Hz.

This voltage can be applied either line-to-line or line-to-neutral. Input line variations over the range of 180 to 260 VAC will be tolerated by the mainframe. A low line detector in the 1441 disables internal power supplies if the line drops below 180 VAC and internal varistors clamp the input line from exceeding 265 VAC.

A fully loaded 1449 mainframe consums 2500 W from the

input line. Normally the maximum current drawn from the line at full power varies from 9 to 13A, depending upon input line voltage. A 16A circuit breaker is integral to the main AC power switch on the front panel. It is suggested that each 1449 mainframe be connected to its own 20A power feed.

At 50 Hz output ripple specs will be met above 190 VAC.

At full rated power below 190 VAC the line frequency ripple will grow and may exceed normal p-p ripple specs. Mainframe will still shut down at 180 VAC.

2.1.4.2 **Connecting the AC Line Cord** -- The 1449 mainframe is

supplied with a 3 conductor detachable 3 meter line cord. Each conductor is 14 AWG. A foil shield surrounds the 3 conductors and is attached to the ground wire in the mainframe via the light gauge uninsulated wire. A line plug is attached to the end of the power cord with screw terminals. If it is necessary to change the line plug, remove the 2 screws holding the plug together and remove all three wires from the plug.

The 3 wires in the line cord are designated as follows:

BLUE	LINE
BROWN	NEUTRAL OR LINE
GREEN/YELLOW	GROUND

Note that the ground wire is also connected to the foil

shield to suppress radiated noise from the power cord.

2.1.4.3 **Grounding** -- Proper grounding of the mainframe is

essential for proper mainframe and multi-mainframe system operation. The High Voltage outputs and the RS232C communications interface are referenced to the 1449 mainframe chassis. The ground wire of the line cord is also connected to the mainframe chassis. Ground loops could cause spurious communications or excessive line noise at the HV outputs. It is possible to have substantial ground differences in an experimental lab environment between different power feeds and or the experimental high voltage load grounds. Three phase power distribution systems are especially susceptible to this phenomenon.

All 1449 mainframes, the CAMAC or RS232C communication

device and the HV load ground should be grounded together with a good low inductance high current capability conductor. The entire system should then be tied to a good earth ground. The ground connection of the line plug should be attached to the input power outlet if it is essentially "clean" with respect to the system ground established above. If the power outlet ground is "dirty" with respect to the system ground then large ground currents could flow and it would be advisable to not make connection of the line cord ground to the wall outlet ground.

2.1.4.4 **Initial Power Up** -- Once the line cord has been properly

installed to the wall outlet and the system has been properly grounded, the system can be powered up and checked out.

Turn on the AC main power switch by pressing the top

half of the rocker in. The switch should become illuminated and the fans should be heard immediately. A 2 second delay is implemented before the supply voltages of the 1441 are allowed to turn on. After this initial delay the "READY" portion of the HV ENABLE switch on the 1441 and the 3 LEDS on the 1445 (-15, +5, ACTIVE) should all be lit.

Note that the HV on light is off. The 1440 always powers

up with high voltage off. Depress the HV enable switch (a push-push type) and both the READY and ACTIVE lights should go out. Depress the HV enable switch again and both lights should turn back on.

2.2 Communications with the 1440

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2.2.1 BAUD Rate

The **BAUD** rate of the 1440 system is factory set to 1200 **BAUD.** Any standard rate can be selected over the range 75 to 9600 **BAUD**. It should be set to match the computer port or terminal to be used The **BAUD** rate is set by a jumper within the Model 1445. See Figure 2.8. Our RS232C format uses the following characteristics:

8 Bits,*

1 Stop Bit and
No Parity

*Note: was 7 bits for Prom versions 1.4 or lower

2.2.2 Cabling

A system containing multiple 1449 mainframes employs the CCHV16-M

cable to interconnect This cable must run from J2 on one 1440 to J1 on the next as shown in Figure 2.9. These connectors are located on the Model 1445. This cable consists of standard ribbon cable terminated at each end with 8-pair connectors. Here M is the length of the cable in meters. See Figure 2.10.

An RS232 port on a computer or a standard terminal usually employs

a standard D type connector. To aid in connecting the 1440 System to such a device, a CDHV16-M (M = length in meters "able is available. This is a cable identical to the CCHV16-M at one end but terminated in a mating D connector at the other end (see Figure 2.11).

The total length of all of the cables in the control daisy chain

should be limited to 150M (500 feet).

To connect the control daisy chain to a Model 2132 interface or to a

teletype adapters are available as Models AD/CAM and AD/TTY respectively (see Figures 2.12 and 2.13). The AD/TTY cable makes system 1440 compatible with terminals using a 20 mA loop.

The high voltage outputs of the 1443 cards may be either SHV or

block connectors Parts for both the male (HVCK-20MC) and female HVCK-20FC) block connectors are available from LeCroy (see Figures 2.14 and 2.15). A summary of the parts contained in these kits and cross references with AMP part numbers is contained in the following table.

2.2.3 Sign On Messages

In the ASCII communication mode the 1445 will generate a sign on

message when the internal microprocessor is initialized. If a 1447 is plugged in this message is "1447 OPERATIONAL"; the normal message via the daisy chain is "LeCROY SYSTEM 1440". The messages are normally generated on AC power up. Also any time that the 1441 detects more than 1 missing AC line cycle it will recycle the internal power supplies and generate the sign on message. Whenever the internal power supplies are cycled the microprocessor sets the HV status to OFF. This is a useful indication that the AC power line is noisy and the situation should be investigated.

In the unlikely event that the microprocessor stops properly executing it's microprogram a hardware circuit will reset the microprocessor and a sign on message will be generated. Since this reboot was not caused by a loss of AC power no change in the operating status of the 1440 system will occur (HV will remain on if it was on for example) except that the mainframe select command may have to be reissued. The Z command (system reboot) has the same

actions as those just described.

HV BLOCK CONNECTOR PARTS AVAILABLE

	LRS #	AMP #
Male Connector Pin (1)	405-463-003	201330-1
Connector Block (1)	405-463-003	203908-2
Male Guide Pin (2)	405-213-001	200833-4
Female Guide Pin (2)	405-343-004	200835-4
Male Jackscrew (2)	405-260-001	226654-2
Female Jackscrew (2)	405-370-001	226655-1
Shield (Special) (2)		201846-1
Shield (Standard) (2)	405-691-008	201571-1
Connector Block (3)	405-152-002	203909-2
Female Connector Pin (3)	405-545-001	201328-1

(1) For use on male connectors only (mates with 1443 front panel)

(2) For use on either male or female connector ends

(3) For use on female connectors only

Parts (1) and (2) are contained in connector kit HVCK-20MC. Parts (2) and (3) are

contained in kit HVCK-20FC.
Recommended HV wire (3 kV rating): LRS #589-601-124

ITT #VU1029-9-C

2.3 Startup Hints for the 1440

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2.3.1 Default Settings

As delivered, the 1440 will be set to:

l. **Range** -- 4095 V full scale which corresponds to 1 V/count. If demand exceeds 2500 V, the hardware voltage limit will override. Note: some modules have 12-bit DACs and some have

10-bit, however all programming is done to 12-bits. For 10-bit channels, the two LSB's -are ignored by the HV card. Therefore High Voltage will be incremented in minimum steps of 4 volts (4V/4 counts rather than 1V/1 count) in 10-bit modules.

2. **BAUD rate** -- 1200 BAUD. When communicating with either the

Model 1447 optional hand held controller or with the Model 2132 CAMAC interface, the 1440 System automatically adjusts its BAUD rate accordingly. With other terminals, check that the BAUD rate matches the terminal. See Figure 2.8. This unit uses RS232C so it is directly compatible with most commercial terminals. The pin outs of the communication daisy chain connectors on the 1445 are shown in Figure 2.16.

3. **Run-up and run-down rates** set to 1 KV/sec.

2.3.2 **Control daisy chain** -- uses 16-wire ribbon cable. See Figures 2.9, 2.10

2.11, 2.12, 2.13. Last mainframe need not be terminated.

2.3.3 **Power and Cooling** -- Operates off nominal 208 or 220 V, 50 or 60 Hz.

Filters for fans which cool the system are easily removed for cleaning as shown in Figure 2.17.

2.3.4 **Optional hand held controller, Model 1447,** -- when plugged in,

overrides that 1449 mainframe but others in chain remain active.

2.3.5 Front and Rear Panel Indicators of System 1440 Operating Status

2.3.5.1 **INTERLOCK: TTL level input, edge triggered.** Polarity is

user selectable. When triggered INTERLOCK immediately stops the 1443 cards from generating voltage. Shortly thereafter the processor will turn off the 31 V supplies and return the system to the OFF state.

2.3.5.2 **STATUS: TTL level output.** Open collector, diode isolated

(high impedance when AC off). HV on is indicated by a clamp to ground.

2.3.5.3 **ERROR: TTL level output.** Open collector, diode isolated.

The processor monitors the actual output from all channels in the mainframe (only while HV is on). If any channel is in error by more than 64 counts the ERROR output is clamped to ground, when the channel(s) are no longer in error the output is released. This condition will always exist during a HV turnon and the release of ERROR may be used to indicate end of turn on.

2.3.5.4 **FAULT: TTL level output.** Open collector, diode isolated.

The clamp to ground indicates that one or more of the AC supplies is shut down. This condition may be caused by overtemperature, overcurrent, or other reasons. The processor attempts to clear all but a fault from the +5 volt supply. The +5 supply will try to clear itself. As a result of the processors attempts to clear a fault, the output may be pulsed. This is due to the interactive nature of the fault and reset conditions. When the reset is issued the supply will attempt to turn on. During this time it may not be in fault. For example, overcurrent will not exist until a certain output voltage is achieved, whereas over-temperature may exist for a long time.

2.3.5.5 **HV ENABLE/PANIC OFF:** Push button "flip flop" switch.

Pushing the switch initiates the same sequence as INTERLOCK. However, in order for the 1440 to resume

generating voltage, the switch must be pushed a second time. The yellow HV READY light will be lit when the unit is able to generate voltage.

2.3.5.6 Pilot Lights: The 1440 System contains several pilot lights which give a visual indication of certain operating conditions.

+5 LED -- Indicates +5 is functional.

-15 LED -- Indicates -15 is functional. +15 operation can be verified by the HV READY lamp. Both +15 and -15 should be tracking with both on or both off.

ACTIVE LED -- Indicates that 1443s are receiving sync pulses. The 1443s cannot generate voltage without a sync pulse.

READY -- Indicates that HV may turned on. When off HV cannot be turned on.

HV ON Lamp -- Indicates that controller has enabled 31 V supplies and that HV is on.

31 V Pilot lamp -- Located on the rear of the unit. Provides a visual indication that the 31 V supply is operating.

2.3.6 TTY -- getting started:

Steps 1 and 2 should be omitted when using the 1447.

1. Set and note mainframe address to XX via rotary switch on 1445. No specific value is required.
2. Enter " MXX (CR) " to select unit MXX.
3. Enter " W2500 CO A (CR) ". This writes a demand of +2500 V to All channels. Insert a "-" sign after the "W" if negative high voltage is desired. Here A indicates All. Addressing of the Demand register is caused by reference to CO.
4. Enter " ON (CR) " Turn on HV
5. Enter " R E A (CR) " note spaces between R, E and E, A. Read out Every value for All channels i.e., measured voltage and Demand and Backup programming registers voltages for all channels. (Note cntl C aborts if you get impatient).
6. If the desired high voltage does not appear on the outputs, check:
   a. Actual and Demand Polarities (check the printout from Step 5) must match (see Step 3). Cards will not generate voltage if the wrong polarity is requested.
   b. If the 1443 cards supplied with the system, have block connectors, the HV Interlock must be grounded to generate high voltage (Pin 19 connected to Pin 20 -- see Figure 2.18). For testing and tutorial a 10 G 1/4 watt resistor may be used on card 0 (caution HV will be exposed).
   c. Current limit must be programmed to provide current

sufficient for any loads plugged into the 1443 cards (see TTY instructions SECTION 3).

d. 1441 front panel voltage limits (positive and negative)

must be set high enough to allow the programmed voltage.

e. HV must be enabled. Yellow Ready light should be lit.

If not, push switch.

f. Verify light on rear panel is on. If not check setup of 31.5 V supplies. The back plane power bus is split such that each 1442 supplies 8 cards. The 1449E has both buses connected together. Verify appropriate connectors for the number of 1442's by removing 1443 card 7 and visually inspecting (as shown in Figure 2.19). The jumpers may be installed, if needed, by top soldering. Clearance behind the board is only .25 inches.

2.4 Tutorial

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Start up 1440 as discussed in Section 2.1. All channels should be at + or

-- 2500 V. No sensitive equipment should be connected until the user is familiar with the system.

The following commands demonstrate some of the features of the 1440.

1. **Enter "CO U N(CR)"**. Copy the Demand to the Backup and uses the Backup

to compensate (Update) for tolerances in the Backup Demand.

The N reports any channels that do not meet allowable tolerance. The

unit should respond with "NONE".

2. **Enter "R F V CO,ODO16(CR)"**. Unit will respond with actual voltage

readings for all channels on card 0. Substituting P for V in this command would cause a response showing the Demand Programmed Voltages.

3. **Enter "W 1400 C5DO4(CR)"**. If the first 1443 card is an N model, the

command should be "W-1400C5DO4(CR)". This will set 4 channels (5, 6, 7 and 8) to 1400 volts. This may be verified by entering "R P DO4(CR)". The channel number does not need to be respecified. The Demand buffer will be read since it was operated on by the previous command.

4. **Enter "I1000C7DO10R(CR)"**. Unit will respond with "Reading Channel

C17 DEM XXXX" which means that channels 7-16 have been set to 1000 V, channel 17 is left at voltage XXXX and the pointer is at Channel 17. This is the most convenient method to sequentially set all voltages in a system to differing values.

At this point it is recommended that the user read Section 3 and

practice the commands.

2.5 1445 Full Scale Programming Options

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See Figure2.8.

Full Scale (approx)	Volts/Count* (Exact)	10 Bit Card Programming Step
4095	1.000	4 V
2500	0.625	2.5 V
2048	0.500	2.0 V

1500 0.375 1.5 V

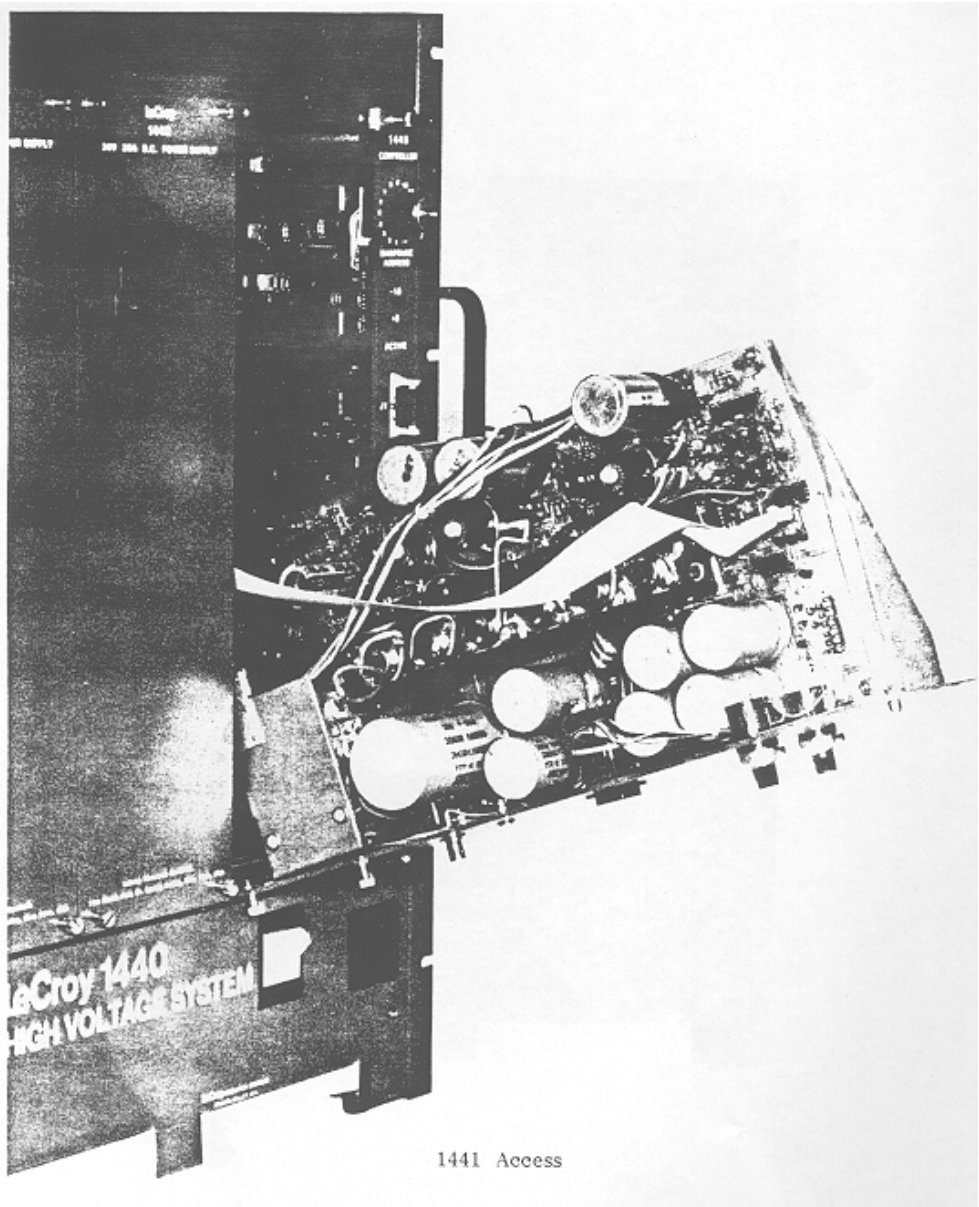
*12 Bit System Programming

Example of 10 Bit vs 12 Bit Programming at 1.000 Volts/Count

10 Bit

Programmed Demand	**Voltage Monitor**
2046	2044
2047	2044
2048	2048
2049	2048
2050	2048

Figure 2.1



1441 Access

Figure 2.2

Figure 2.3

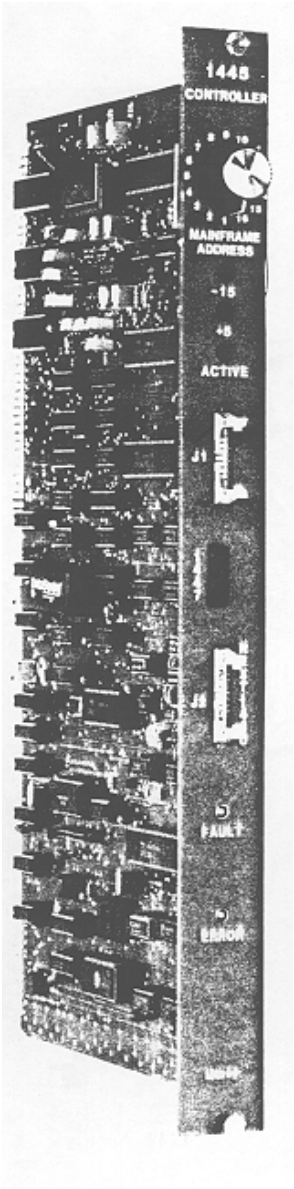
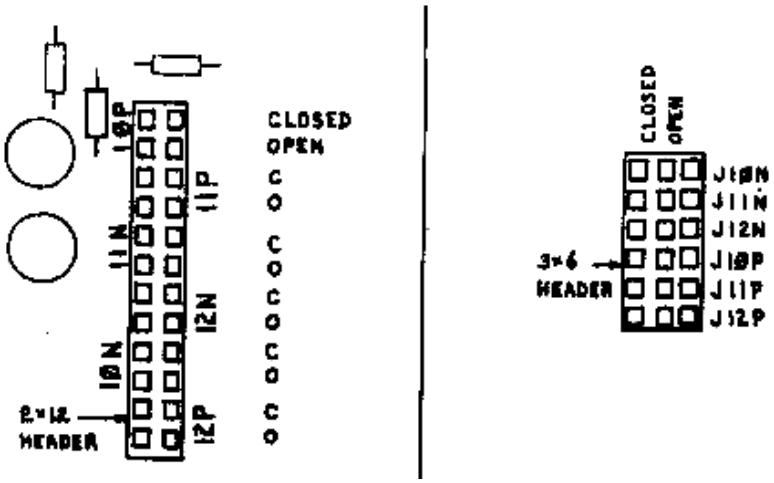

1440
CONTROLLER
MAINFRAME
ADDRESS
-15
+5
ACTIVE
J1
J2
FAULT
ERROR

Figure 2.4

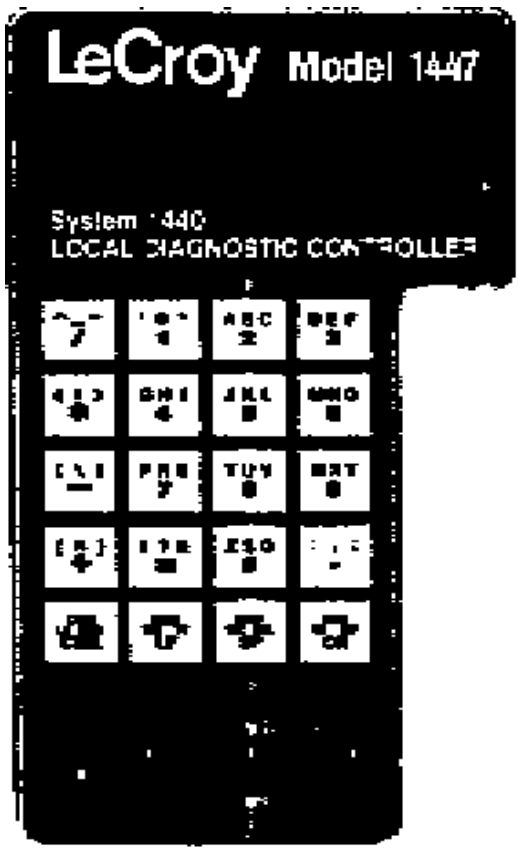

CLOSED
OPEN
10P
11P
11N
12N
10N
12P
2×12
HEADER
CLOSED
OPEN
J10N
J11N
J12N
J10P
J11P
J12P
3×6
HEADER

REV B **REV C**

This corner of the 1441 assembly drawing shows the position of the 24-pin or 18 pin header which may be used to program the HV Run up/Run down rates. These rates as a function of the position of jumpers in this header are:

		J10N	**J11N**	**J12N**	**(Negative High Voltage)**
Run Up	**Run Down**	**J10P**	**J11P**	**J12P**	**(Positive High Voltage)**
500 V/sec	500 V/sec	Open	Closed	Open	
1 kV/sec	1 kV/sec	Open	Closed	Open	
1 kV/sec	1 kV/sec	Closed	Closed	Closed	
2 kV/sec	2 kV/sec	Closed	Open	Closed	
500 V/sec	1.5 kV/sec	Open	Closed	Closed	
1 kV/sec	3 kV/sec	Open	Open	Closed	
l kV/sec	-0-	Closed	Closed	Open	Illegal
2 kV/sec	-0-	Closed	Open	Open	Illegal

Figure 2.5



Hand Held Controller

Figure 2.6

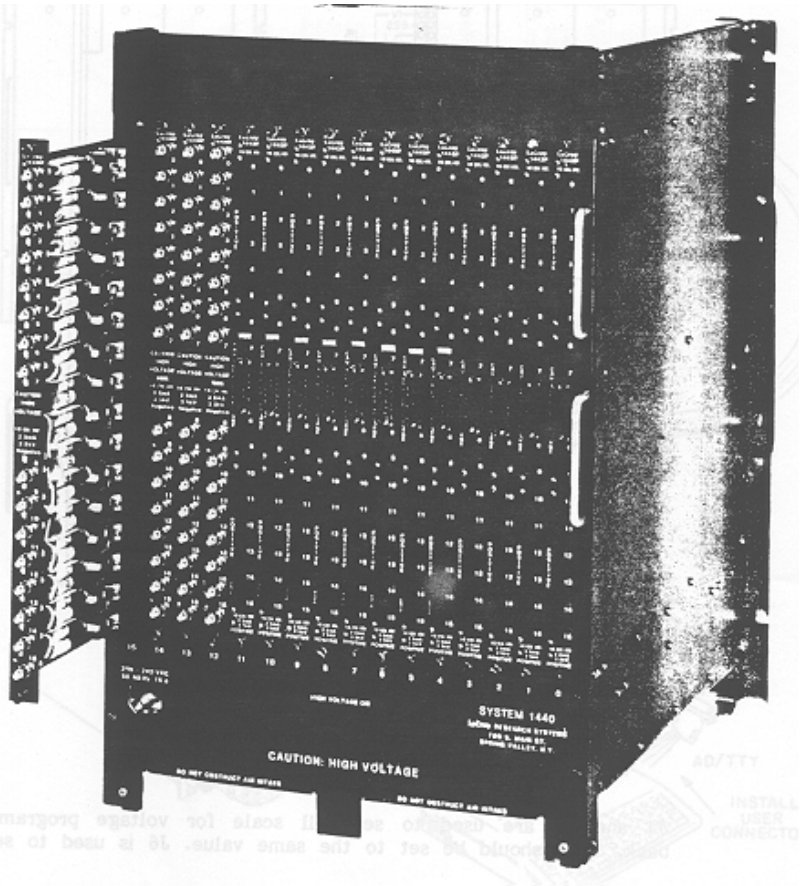
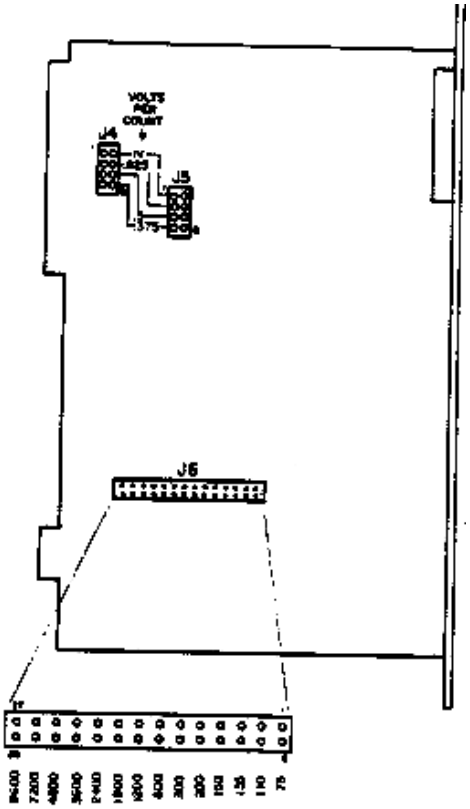


Figure 2.7



1445

J4 and J5 are used to set full scale for voltage programming and voltage back. They should be set to the same value. J6 is used to set BAUD rate.

Figure 2.8

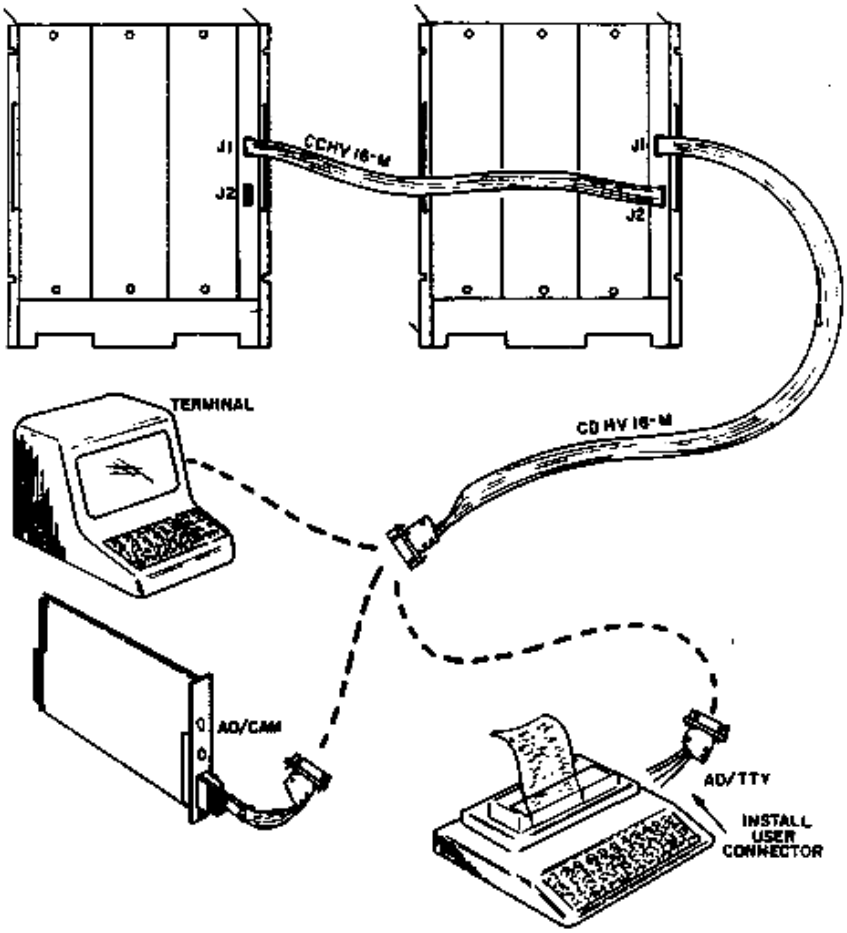

J1
J2
CCHV 16-M
J1
J2
J1
TERMINAL
CD HV 16-M
AD/CMM
AD/TTY
INSTALL
USER
CONNECTOR

Figure 2.9

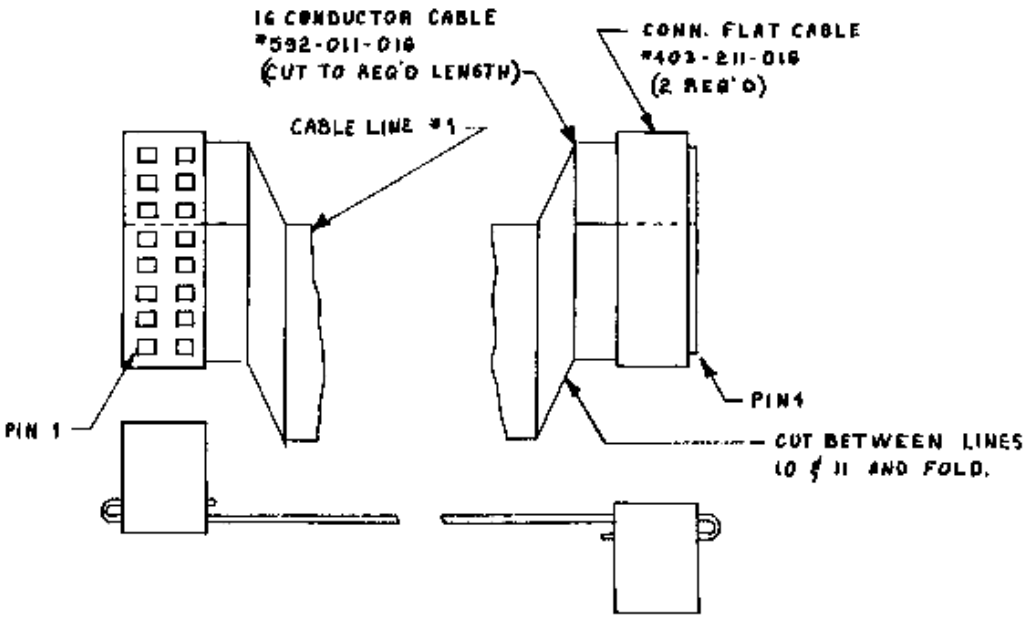


Figure 2.10
CCHV16-M

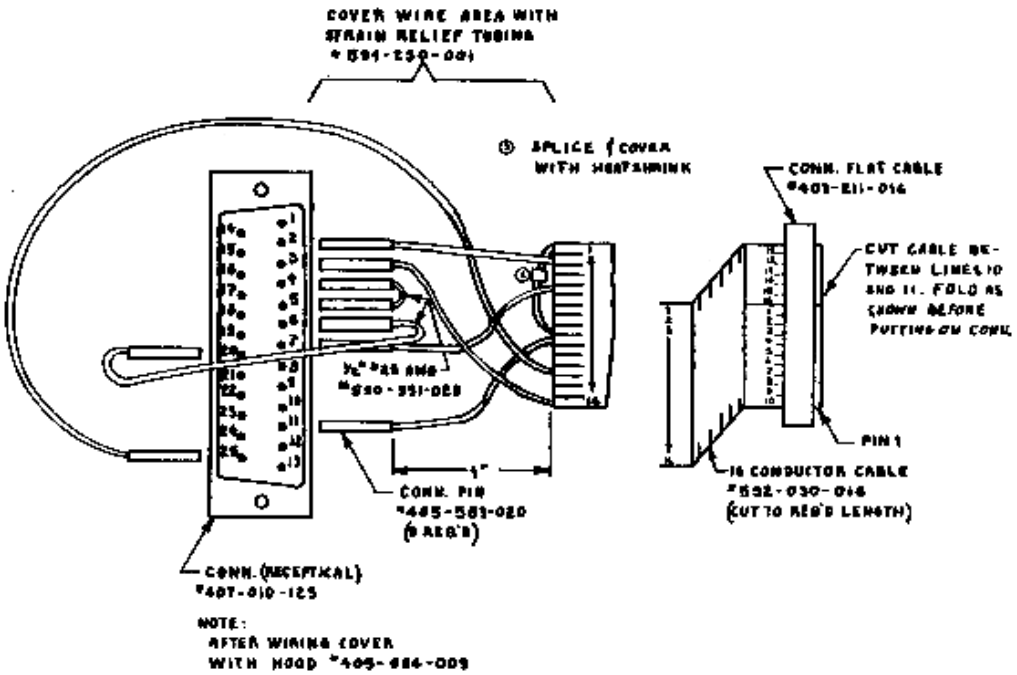
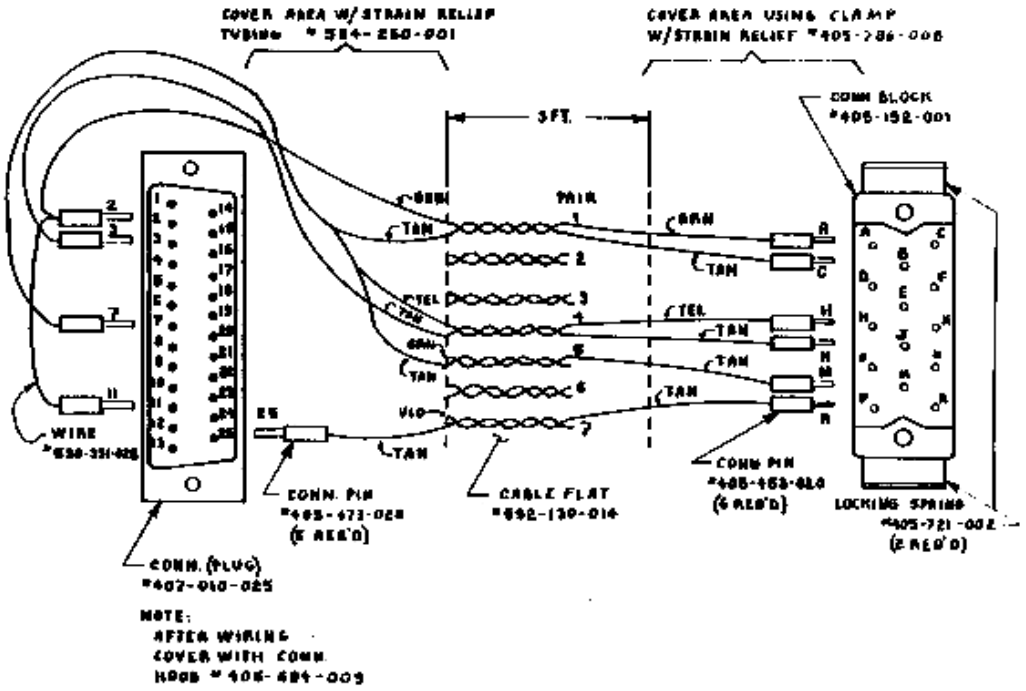
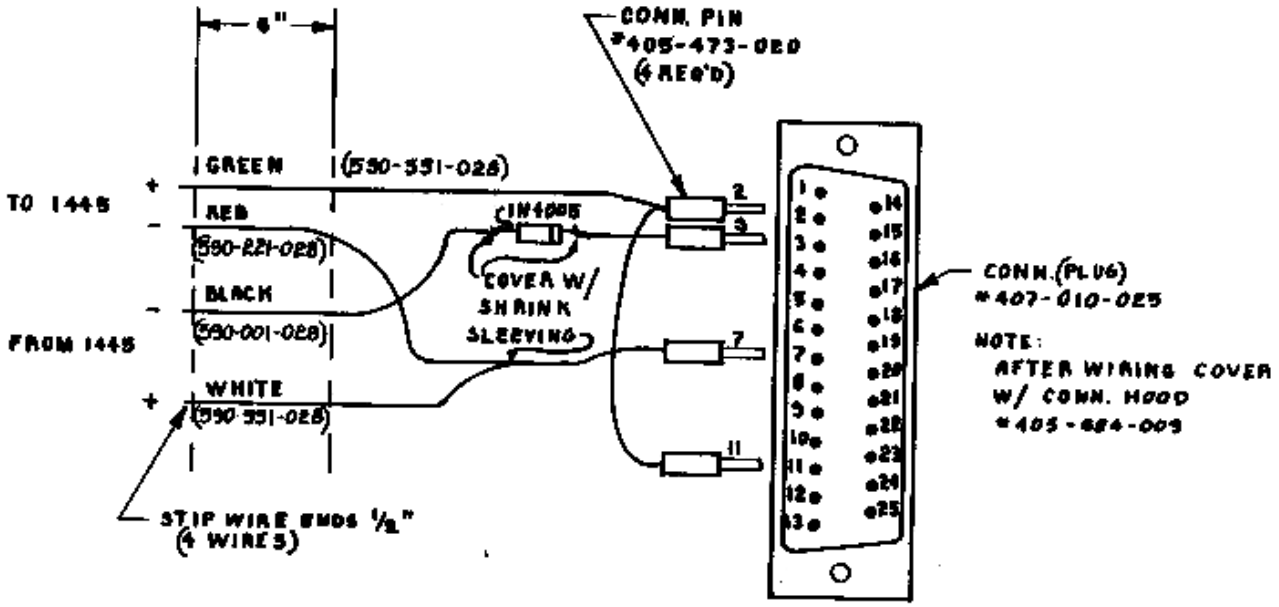


Figure 2.11
CDHV16-M



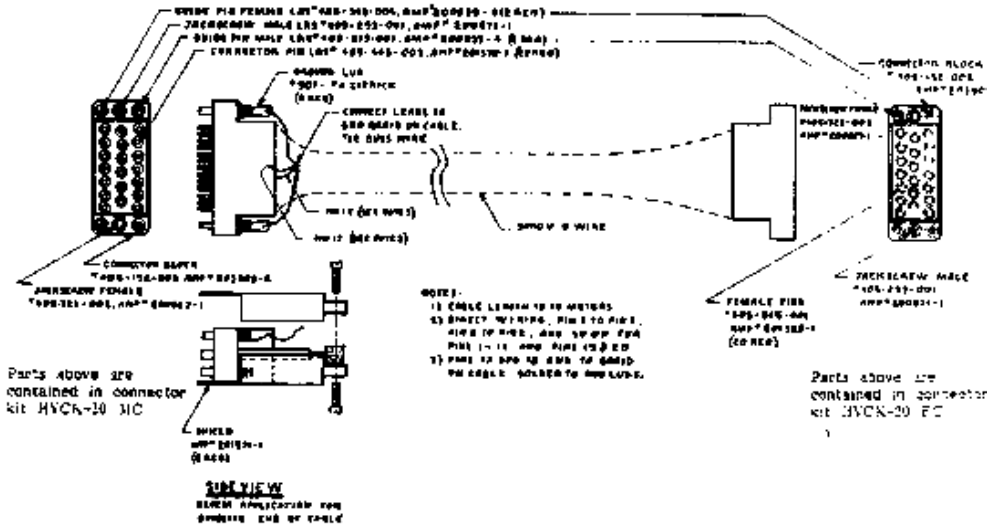
AD/CAM

Figure 2.12



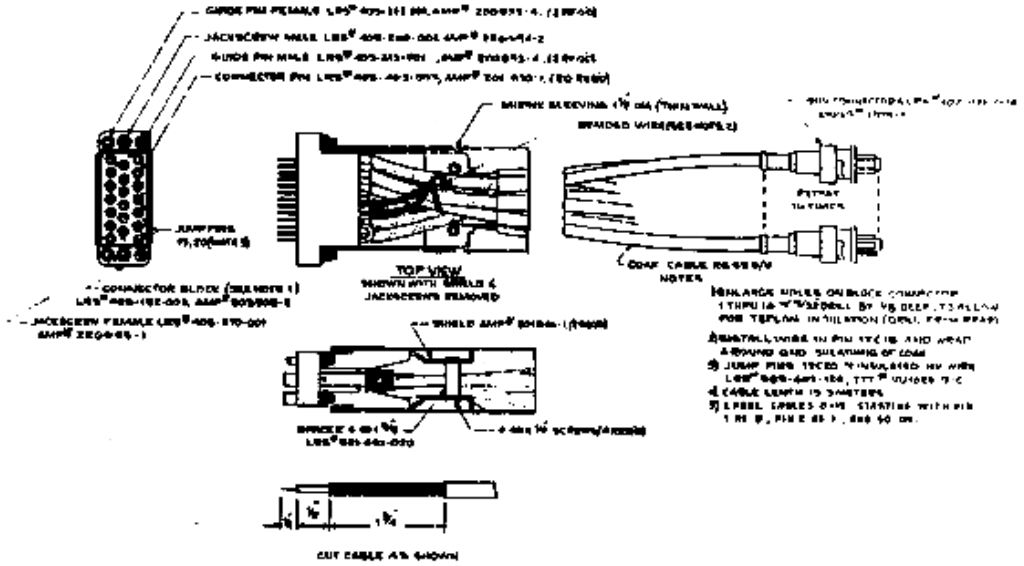
AD/TTY
20 mA Current Loop

Figure 2.13



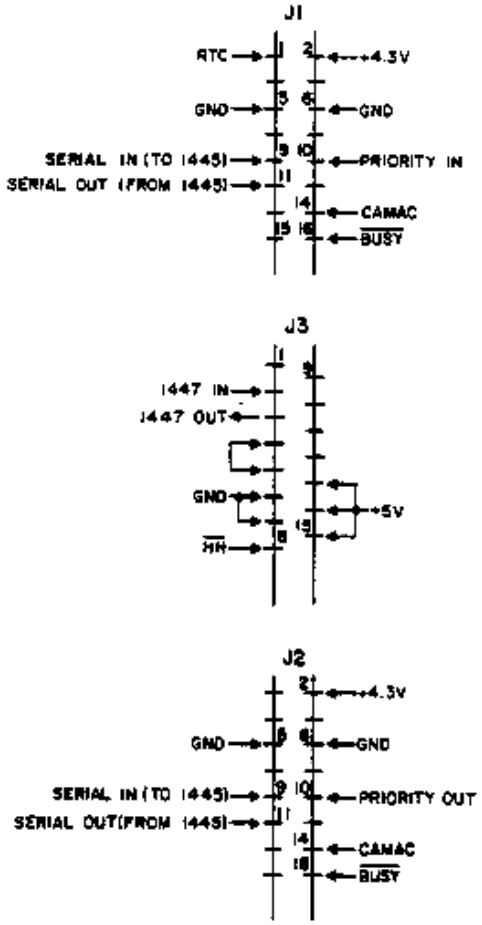
CFB/MB-M

Figure 2.14



AB/SHV

Figure 2.15



1445 FRONT PANEL PINOUT

Figure2.16

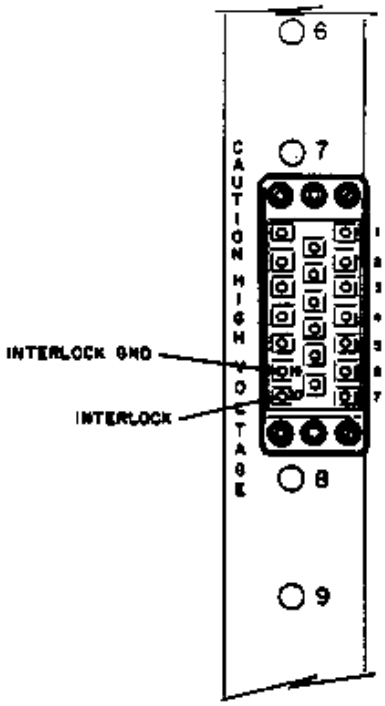


Figure 2.18

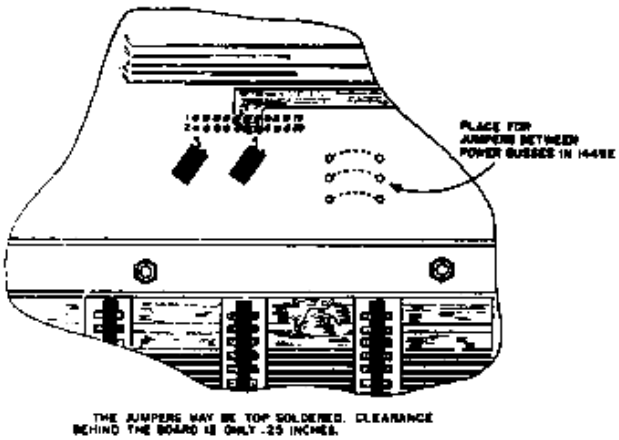


Figure 2.19

SECTION 3 CAMAC AND TTY CONTROL OF THE 1440

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3.1 System 1440 ASCII Syntax of Command Lines

System 1440 instructions are grouped into 3 categories: COMMANDS, MODIFIERS and CONTROL CHARACTERS

Several instructions form an instruction group, and many instruction groups may be entered on a single command line. A command line is terminated by a carriage return. Instruction execution begins after the carriage return is entered.

Instruction groups are executed in the order that they are received: from left to right.

Instruction Groups:

1. A new instruction group begins at the beginning of each command line. The

first instruction group on a command line need not begin with a command.

2. All successive instruction groups on the command line begin with a command and may be followed by modifiers.

3. An instruction group ends when a new group starts (with a command) or a carriage return terminates the command line.

4. Execution of instructions within an instruction group is from right to left. The command starting the group is executed last, after ANY modifiers.

Note that this causes "W1000C5B(CR)" and "W1000C5" to be identical since the "B" modifier was overridden by the "C5" modification.

In the following examples -

M indicates a Modifier Instruction
C indicates a Command Instruction
I.G indicates an Instruction Group

	I.G.	**I.G.**	**I.G.**	**I.G.**
	M M	C M M	C	C M (CR)
Execution Sequence after carriage return	2 1	5 4 3	6	8 7

Commands requiring that a number follow the command are not executed if the number is not entered. A "Missing Number" message is returned. Note that the abortion of one command group may change the action of following command groups.

3.2 ASCII Line Parsing

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ASCII characters are divided into 4 groups: Letters, Numbers, Control and Delimiters. Any printable characters not in the first 3 groups is a delimiter. Words are groups of consecutive letters terminated by a delimiter or number. The word may be any length. Only enough characters to make it unique are checked, the rest are ignored. The semi-colon is a special delimiter since it causes all the following characters up to, and including, the next semi-colon to be ignored.

Values are a set of consecutive numbers (inc. '-' and',') terminated by a Letter or Delimiter. This makes for a flexible input line.

Ex: "WRITE 1000; VOLTS, TO; CHANNEL 5 (CR)" is identical to "W1000C5(CR)"

Note that spaces were not necessary since the numbers are letters terminate each other.

3.3 Programmable Pointers

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The 1445 maintains a set of "pointers". These are:

1. Channel
2. Demand/Backup
3. Programmed/Actual
4. Selected Mainframe

Their values are altered by the appropriate commands. They remain valid so that every command does not need them to be specified. Pointers are only modified by commands which intentionally affect their value (for example, update does not affect any pointers).

The mainframe pointer is important to the System 1440 communication protocol. The 1440 system will echo back all keyboard entries even if no mainframe is selected, however, no action will occur in response to the commands until a mainframe or all mainframes are selected. All mainframes are deselected upon power up and must be selected after power up with a M command. Communication mode changes also deselect mainframes. If a 2132 CAMAC interface is connected after a mainframe was selected by an ASCII terminal the mainframe will deselect itself. When changing from terminal to hand-held mode the mainframe is selected automatically. When returning to the terminal mode the mainframe is automatically deselected and must be readdressed with an M command before commands will be acted upon. Use of the A (all) modifier will not deselect a selected mainframe.

A "mainframe # responding" response will be generated when a unit which was not selected becomes selected. Note that readdressing the same mainframe will not cause another response since the mainframe was already selected.

Although no restrictions are placed on the setting of the units mainframe address switch, the switch is only checked by the mainframe when a mainframe select command is issued. If Ml is selected and -it's switch is changed to M2 it will continue to remain selected. Furthermore if a M2 command is then issued no "mainframe # responding" response will be generated since the mainframe was already selected.

1 = Number Required
2 = Works With ALL Channels or Mainframes
3 = Works With D0
4 = Affects Channel Pointer
5 = Affects Demand Reg. Pointer
6 = Affects I/O Reader Pointer

3.4 ASCII Instruction Set

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3.4.1 COMMANDS

Single Mainframe Oriented

M	Mainframe Specifier	1

1 = Number Required
2 = Works With ALL Channels or Mainframes
3 = Works With D0
4 = Affects Channel Pointer
5 = Affects Demand Reg. Pointer
6 = Affects I/O Reader Pointer

ST	STatus Request	
EM	EMpty HV Card Slot Request	
N	Non Updated Channel Request	
RL	Read and Report both Current Limits	
VER	Prints Version # of Firmware	

Channel Oriented

R	Read	2,3

W	Write	1,2,3
I	Write with Auto Increment of Channel Pointer	1,2,3,4

General

ON	Turn HV ON	2
OF	Turn HV OFF	2
LI	Current LImit Specifier (+ depending on data)	1,2
SW	SWap Demand and Backup Program Buffers	2
CO	COPY Demand into Backup Program Buffers	2
U	Update (Demand = Demand + Backup - Actual)	2
CL	CLear Faults	2

3.4 ASCII Instruction Set

3.4.2 MODIFIERS

Pointer Oriented

C	Channel Specifier, also selects Demand Programming Buffer	1,4,5
B	Backup Programming Buffer Selector - Note that if both "B" and "C" modifiers are within the same instruction group the "B" must preeced the "C"	5

1 = Number Required
2 = Works With ALL Channels or Mainframes
3 = Works With D0
4 = Affects Channel Pointer
5 = Affects Demand Reg. Pointer
6 = Affects I/O Reader Pointer

P	Specifies Read from either Programming Buffer	6
V	Specifies Read out actual HV output Value	6

Iterative Modifiers

A	Modifies Command to function on ALL Channel or Mainframes	
DO	Specifies the Total number of successive Channels on which a Read or Write Command Operates	1

Read Format Modifiers

F	FORMATS read response into 8 Columns of data	2,3
E	Causes a 3 Column response for a read Command that includes EVERY pertinent value for a	2,3

Channel. i.e., Demand, Backup and actual

CONTROL CHARACTERS

C	Abort Last Command
X	Abort Command Line
H	Rubout
S	Stop - Halt operations and printout until Q received
Q	Resume printout
Z	Reboot
;	Ignore rest of line until next ";" or (CR)
,	Multiply preceding No. by 16 and add following No. i.e. C5,11=C91

3.5 Operations on Buffer Memories (Common to CAMAC and ASCII)

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The 1445 contains two sets of programming memory. They are physically independent and are referenced by their logical names. One buffer is called the Demand buffer. This buffer contains the data that is sent to the HV cards The other is called the Backup buffer. Its data is simply held in reserve. Both buffers may be accessed independently with the appropriate commands. There are several commands to manipulate these buffers in their entirety. These commands are identical in either CAMAC of ASCII modes-

3.5.1 COPY - This command copies the contents of the Demand buffer into the Backup buffer.

3.5.2 SWAP - This command exchanges the logical reference to the memories This may change the data that is sent to the cards. It appears to the user as an exchange of the contents of Demand and Backup buffers although there is no movement of data. The change in programming occurs "instantly" and each channel will receive its new data in one timing loop.

3.5.3 UPDATE - To provide the use with a convenient method of compensating errors due to specified programming accuracy, the UPDATE command is provided. This will ease the task of providing maximum channel to channel matching when needed. There are certain restrictions placed upon programming if this command is desired. The update function requires that the backup buffer be designated as the desired output voltage. The microprocessor in conjunction with the ADC is then able to adjust the programming of the Demand buffer to yield the desired output. This adjustment is done upon receiving the update command and is not a continuous process.

When the UPDATE command is issued it acts upon all 256 channels (unless there are empty slots The formal definition of the action taken is

New Demand = Backup -- measured + Old Demand
If and only if the absolute magnitude of
New Demand - Backup is less than 64

Before performing this calculation, the firmware checks to see that each of the three values (Backup, measured and Old Demand is either zero or of the same sign as the other two values. If a sign difference is found then the UPDATE is not performed and the channel is flagged in memory. This prevents the use of values which have an incorrect polarity when calculating the New Demand. During the above calculation all voltage values are unsigned (the sign bit is masked After the New Demand is calculated and checked, its range is clipped to between 0 and 4095. Then the sign of the measured voltage is appended. If any channel cannot meet the allowed error it will be flagged in memory and no change in the Demand buffer occurs The non-updateable command may then be used to obtain a report

The update procedure will not alter the demand by + 1 count.
This prevents "wandering" during successive update's.

When using the UPDATE command it is recommended that the COPY and SWAP commands be avoided. Also note that if it is desired to turn off channels, either both buffers (for the appropriate channels) should be cleared or the Demand cleared and the UPDATE command avoided until the channels are to be restored

3.6 CAMAC Control

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3.6.1 Commands - short form

TAG	FORMATS	DESCRIPTION
0	C C C C C C C C M M M M X 0 0 0	Mainframe Ch. used in turn on
1	C C C C C C C C X X X I 0 0 0 1	Channel write Demand
	1	Backup
		Ch. pointer after write
	0	no change
	1	increment
2	1 V V V V V V V V V V V V 0 1 0	Voltage data positive
	0	negative
3	C C C C C C C C A A A X X 0 1 1	General read command
	0 0 0	Demand of ch. C
	0 0 1	Backup of ch. C
	0 1 0	Measured voltage ch. C
		Mainframe requests
	X X X X X X X X 0 1 1	Non-updated ch.
	1 0 0	Current limit pos.
	1 0 1	Current limit neg.
	1 1 0	Empty slots
	1 1 1	Status
4	D D D D D D D D X X X X X 1 0 0	Count (Data of 0 means 256)
5	D D D D D D D D 0 X X F X 1 0 1	Current limit negative
	1	positive
6	X X X X X X X X A A A F Z 1 1 0	Command specifier
	0 0 0 0	Turn off HV
	0 0 1 0	Turn on HV
	0 1 0 0	Clear faults
	0 1 1 0	Disable finished res.
	1 0 0 0	Swap (see programming
	1 0 1 0	Copy buffer
	1 1 0 0	Updated operations)
	1 1 1 0	Enabled finished res.
	X X X X X X X X X X X 1 1 1 0	System reboot
7		Nop

M = mainframe V = voltage D = data C = channel

F = 1 for all units 0 for selected unit **I = increment**
A = subtag

Most significant bit to the left for all numbers.

3.6.2 Commands - Detailed Description

TAG **FORMAT AND DETAILS**

0 **CCCCCCCCMMMMX000**

Selects mainframe MMMM as receiver for further commands. Sets channel C as the channel to be used in determining end of HV turnon. Turnon is considered complete when dv/dt of ch. C is zero. MMMM of 0 means mainframe 16. Note that a change in communication mode or an AC power down will deselect the mainframe. See Sec. 3.3 for further details.

1 **CCCCCCCCXXXIB001**

Write to channel C. B indicates Demand (0) or Backup (1) buffer. I indicates status of channel pointer after write occurs (0 = no change, 1 increment). Write data is in tag 2 commands immediately following. This command need only be sent once and may be used in conjunction with the count option. The following combinations are possible.

No count followed by tag 1 I = 0
All following tag 2's go to same ch. Proper data makes this a ramp up/down of single specified channel.

No count followed by tag 1 I = 1
All following tag 2's go to successively increasing channels. Useful for programming entire box.

Count followed by tag 1 I = 0
(Not intended to be used). First following tag 2 goes to channel CCC Command will execute once since repetition is redundant. Any further tag 2's will be ignored.

Count followed by tag 1 I = 1
First following tag 2 will be used to program channel CCC and then increment ch. pointer. Since command is executed count times this forms a preset command to a common voltage. Any further tag 2 commands are ignored.

2 **SVVVVVVVVVVVV010**

Voltage write data. S indicates polarity of VYV (1 = positive). Receipt of tag 2 causes write to occur if previous commands are syntactically correct. Note that programming is not in 2's complement notation. Use of wrong polarity will set HV output to zero.

3 **CCCCCCCCAAAXX011**

General read command. AAA indicates source of readback. CCC indicates ch. where appropriate. Channel readbacks may be used with count specifier and occur on "count" sequential channels starting with channel CCC. (Note see Tag 7).

4 **DDDDDDDDXXXXX100**

Count specifier. Causes following commands to execute DDD times where appropriate. Data of 0 is equivalent to 256. Count of 1 permitted, major effect is to generate channel i.d. in response to read command (see tag 3 and 4 responses).

5 **DDDDDDDDSXXFX101**

Current limit. S indicates polarity (1 = positive). F=l flags all units to respond.

6 **XXXXXXXXAAAFZ110**

Command specifier. F flags all units to respond. AAA indicates action requested. Note

that enabling the finished response generates a finished response and disabling it will not generate one. Z=l causes system reboot and overrides rest of word.

7 NOP

The only effect is to break the chain of syntax checks. The sequence of Tag 1, Tag 2, Tag 3 (with any subtag 3-7) will generate a syntax error when in fact the sequence is correct. Inserting a Tag 7 before the Tag 3 will eliminate the syntax error message.

3.6.3 Responses -- Short Form

TAG	FORMAT	DESCRIPTION
0	0 0 0 B B B B B M M M M 0 0 0 0	Status (one response)
		Bit encoding
	b	1=HV on/0=off
	b	1=enabled/0=disabled
	b	0=1441 operating
	b	0=1442 low operating (Left)
	b	0=1442 high operating (Right/Center)
1	0 0 0 0 0 A A A M M M M 0 0 0 1	Finished response to tag 6 subtag A A A
2	1 V V V V V V V V V V V V 0 1 0	Voltage read positive
	0	negative
3	C C C C C C C C M M M M 0 0 1 1	Buffer i.d. Demand
	1	Backup
4	C C C C C C C C M M M M 0 1 0 0	Measured data i.d.
	0 0 0 0 1	Empty slot report
	1 1 1 1 1 l 1 1 1	No empty slots
5	D D D D D D D D M M M M 0 1 0 1	Current limit negative
	1	positive
6	C C C C C C C C M M M M 0 1 1 0	Non-updatable ch. #
	D D D D D D D D 1	Total # of channels
7	0 0 0 0 0 0 0 E M M M M 0 1 1 1	Receiver error 1440
	X X X X X X X X X X X X 1 1 1 1	2132

M = mainframe V = voltage D = data C = channel
B = Bit, encoded status information

Most significant, bit, to the left, for all numbers

Lam 1 set/Lam 2 clear for all responses

3.6.4 Responses - Detailed Description

TAG FORMAT AND DISCUSSION

0 000BBBBBMMMM0000

Status response from mainframe MMM. B represents binary encoded operating conditions.

1 **00000AAAMMMM0001**

Finished response to tag 6 subtag AAA commands from mainframe MMMM. Note that when using the F flag all units will act upon the command identically up to the point of transmitting the response. At that point only the selected mainframe continues, if no units are selected it is possible for no response to occur.

2 **SVVVVVVYVVVVV010**

Voltage read data. S indicates polarity

3 **CCCCCCCCMMMMB011**

Programming buffer i.d. from mainframe MMMM in response to tag 3 subtag 0 or 1. B indicates Demand/Backup. Sent following tag 2 data words when count option is used (Count = 1 may be used to generate this response on single channel read). Provides verification of complete transfer. CCC is last channel sent.

4 **CCCCCCCCMMMMT100**

T=O. Measured voltage i.d. Same as above for tag 3 subtag 2

T=l. Response to empty card slot request. CCC is lowest ch. on empty slot (i.e. 4 LSB's = 0). If unit is full CCC will be 255 (i.e. 4 LSB's not 0).

5 **DDDDDDDDMMMMS101**

Current limit read back from mainframe MMMM. S indicates polarity (1 = positive).

6 **CCCCCCCCMMMMT110**

T=l CCC is total number of non-updateable channels in unit. Note that unit reports C of 255 for both 255 and 256. If CCC is non-zero responses with T=0 will follow.

T=O CCC is channel that cannot be updated. Max. of 31 responses generated (note empty slots not included).

7 **0000000EMMMMT111**

Error indicator. If T=l error is caused by 2132 receiver and all other bits are invalid. If T=O error is caused by 1440 receiver in mainframe MMMM. E will then indicate hardware (0) or syntax (1) error.

3.7 General Notes on Using System 1440 with 2132 CAMAC Interface

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3.7.1 Transmitting to System 1440

The data received by System 1440 is buffered to a depth of 40 commands. All mainframes receive all commands independently whether they are selected or not. Those units not selected will not act upon the command. This means that consideration of the buffer depth does not include mainframe selection. The depth of the buffer has been set to accommodate the expected size of command - bursts. For instance, in a setup of multiple units a burst of status requests may be issued without waiting for any response (buffer depth max. of 16). Since the size of the 2132 input and output buffers is also 40 there should be no difficulties involved. If the buffer size is ignored and the computer manages to overflow it any following commands will be lost.

3.7.2 Responses from System 1440

Output from System 1440 to the 2132 is only generated in response to a request. There is no spontaneous transmission. When requesting information from 1440 the buffersize of the 2132 must be taken into account. The count option in the commands to the 1445 can generate a block response of up to 257 words. The demand and measured i.d.

responses have been included to assist in verifying that no data responses are lost. The suggested mode of operation is to limit the count to 39 (39 channels + 1 i.d. word fills 2132). If this is not done the 2132 must be read out fast enough to prevent overflow. This might be a reasonable approach if the LAM is used as an interrupt.

3.7.3 CAMAC Programming

Computer interface to System 1440 is accomplished with a LeCroy 2132. The language linking them has been designed to minimize programming problems, however there are certain nuances that should not be forgotten.

l. The mainframe select command is residual. It remains active until another mainframe command is received. Obviously if power is turned off the 1440 will not be able to respond, it will also lose its selected status when power is restored. Computer programs that are waiting for responses should expect this situation and be able to cope with it. Do not forget the mainframe select command when trying to re-establish communications. This situation can also occur if the 1447 is plugged in, the 2132 cable is disconnected, or the 2132 is turned off.

2. The 1440 may have mixed polarity and/or empty slots. This should be taken into account since programming a card to the wrong voltage will result in zero output. It is suggested that programming be done by card or single channel. These are convenient sizes to be compatible with both the 2132 buffer and the necessity to handle polarity and empty slots.

3. To aid in determining the mainframe configuration, the unit will generate a list of empty cards upon request. If the unit is full, a response indicating that it is full will be sent. If not full the response will be a variable length list (depending on setup). When is the list ended? There are two ways to handle this. One is to consider that it is certain to take less than 160 msec, between words. The other would be to issue some other command (enable finished response for example) and use that command's response as the list terminator.

4. LAMs. The 1440 generates an L1 with every transmission. This can be used to indicate that the 2132 has received data. Unfortunately the LAM and the amount of data are uncorrelated. This raises the question of when to clear the LAM. This can be difficult since transfers occur in different sizes and the 2132 may be simultaneously issuing new commands. If polling is acceptable it is recommended that the LAM be ignored and allow the Q response from an F(2) to indicate valid data. Note that L2 is NEVER generated.

5. Fifos. Both the 2132 and the 1445 are fifo buffered. This allows a burst of data to be transmitted at high speed, but then necessitates a delay to allow processing of that data. The 2132 will indicate fifo full during an F16 by not returning a Q response. The 1445, being isolated from the host computer cannot give such an indication. Its buffer length exceeds that of the 2132 giving on level of protection. The best way to ensure that no data is lost is to transmit data in a handshaking mode. This means that data sent to the 1445 should be in blocks of less than 40 words, the last word being a command that generates a response. This response will then have the additional meaning of "fifos empty", thus ensuring proper operation. Normal program flow will generally, but not always, accomplish this. If necessary, the ENABLE FINISHED RESPONSE command is a handy way to get a response when nothing more than indicating fifo empty is desired. The most likely situation to cause concern is down loading a set of voltages. This is where programming in card increments is convenient. The sequence of COUNT, WRITE, 16 voltages, ENABLE FINISHED RESPONSE, will fit into the 2132 buffer twice. First send one block of writes, then loop sending blocks followed by a wait for finished response. This gives maximum throughput while maintaining handshaking. Note that if this loop is to cross mainframes the mainframe select command should be included.

3.7.4 Summary of CAMAC Function Codes for 2132 Interface

F(0) (A(0)+A(1)) N	Read LAM Register (Rl=L1, R2=L2)
F(2) (A(0)+A(1)) N	Read and advance input buffer (data valid if Q=1)
F(9) A(0) N	Clear buffers, Ll and L2
F(16) N	Write into output buffer (Q=l if word is accepted at output buffer. Data

	transfer will then proceed to the HV)
F(27) (A0) N	Test Ll.
F(27) A(1) N	Test L2
F(10) A(0) N	Clear Ll
F(10) A(1) N	Clear L2
F(10) A(0) N	Enable Ll
F(26) A(1) N	Enable L2
F(24) A(0) N	Disable L1
F(24) A(1) N	Disable L2
Z S2	Clear Ll, clear L2, clear buffers, enable Ll, disable L2
C S2	Clear Ll, clear L2, clear buffers

Note: The 1440 system does not utilize L2. All responses generate Ll.

SYSTEM 1440 FIRMWARE UPDATE

PROM FIRMWARE VERSION 1.3 CHANGES FROM EARLIER VERSIONS:

l. The "Copy" command has been changed to Copy the "Demand" programming registers contents into the "Backup" programming register.

2. The name of the programming register actually controlling the HV output has been changed from "Active" to "Demand".

3. CAMAC mode HV Monitor read back accuracy was made consistent with ASCII mode accuracy by internally allowing a slightly longer settling time before executing the ADC Read command.

4. CAMAC response to a "Turn On" command while the front panel "HV Enable" is disabling the HV turn on function is an immediate "Finished Response". Earlier Prom versions generated several meaningless response words in this situation. It is advisable to verify a proper HV Turn On with a Status Request to check if the HV was disabled.

5. Version 1.3. will not perform the Update function on a channel if the polarity of the Actual, Demand and Backup registers is not the same. This avoids undesirable new Demand values caused by incorrect polarities.

6. The Version 1.3 firmware can properly report in response to a "Status" request that a Fault condition exists.

7. To aid in setting polarity programming, in the ASCII mode only, a command is available to allow the firmware to automatically set the polarity of Write command data on that command line. If the first character of a command line is an * (asterisk), then all write commands will be stored with proper polarity until the CR terminates the *.

PROM FIRMWARE VERSION 1.4 CHANGE FROM 1.3

l. The finished response to HV turn may have been generated before HV turn on ramping was completed in earlier versions. Version 1.4 reliably generates the finished response after HV turn on is completed and output voltage is stable.

PROM FIRMWARE VERSION 1.5 CHANGES FROM VERSION 1.4

1. The programming of the 1445's UART was changed. The old RS232 format was: 7 bits, 1 stop bit and no parity. The new RS232 format is: 8 bits, 1 stop bit and no parity. This change should not affect users with terminals, however if the 1440 is directly interfaced to a computer, the software for the computer may have to be changed to properly recognize data from the 1440 system.

PROM FIRMWARE VERSION 1.7 CHANGES FROM VERSION 1.5

l. Upon AC power up older prom versions would load the positive current limit register with the data for the negative current limit; the negative current limit register would be loaded with the data for the positive current limit. This may not have been noticed if both positive and negative current limit registers were loaded with the same value. Version 1.7 correctly loads the .current limit registers on AC power up.

2. In the ASClI (RS232) mode of communication the Status Request response was enhanced. With version 1.7 the 1440 will report that there are non regulating channels, using the message: "CH ERROR". If all channels are regulating; no additional message is given.

3. The error limit for determining if a channel was "Non Updatable" was reduced from 128 ADC counts to 64 ADC counts.

SECTION 4

TECHNICAL DESCRIPTION

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The block diagram in Figure 4.2 may be useful in tracing the interaction of the 1440 subassemblies described in this Section.

4.1 Controller

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The 1445 is a microprocessor based controller designed to provide the necessary control signals for the various subsystems of System 1440 and to provide for interface to terminals or computers. The circuitry is divided into four main areas as follows:

Processor -- The processing system is composed of an 8085 microprocessor together with an 8251 USART, 8255 parallel interface (3), a 16 bit latch formed from four LS1l3's, memory and miscellaneous medium scale IC's. The interconnection of these devices is straight forward and provides the 8085 with over 90 I/0 lines and serial communications capability. The 8085 generates the system clocks to which all devices in the system are synchronized.

RS232C Interface -- The 1445 uses a parallel bus for reception and transmission together with a serial line for protocol. The input is referred to as Jl and continues from J2 to the next 1440. This allows up to 16 mainframes to be daisy chained together under one control device. For local control of the units a 1447 may be plugged into a separate connector. When used, the 1447 will override Jl and cause the unit to "disappear" from the daisy chain.

The receiver from J1 is an LM311 used for its high input impedance to prevent excessive loading on the control device. The receiver from the 1447 is an LM339 and is wire-ored with the 311 to override input from Jl.

The output from the 1445 through J1 is a tri-state driver consisting of Q4,Q5,Q6, and part of U55, Zener diodes are used to drop the +15 and -15 to the 12 volts required by RS232C, Output to the 1447 is picked off prior to the tri-state driver and buffered by a TTL inverter. Although this signal only goes from 0 to +5 volts it is compatable with RS232C over the short lengths encountered when using the 1447.

Two lines provide for bus arbitration to insure that one and only one driver is active at a time, these are CTS and PI. CTS is an open collector line used to indicate that a unit is in control of the bus. This line is set/cleared in response to mainframe addressing commands. In the event that no unit is selected the PI line will determine which unit is to terminate the bus and echo terminal input. This line is a serial daisy chain from the first unit on down to the end. It consists of Q3,Q8, and part of U12. The first unit in a chain will have PI connected to +4 (Jl-2) providing that unit with priority, U12 and Q3 are used to defeat priority to succeeding units. This type of circuit allows the priority to be passed to the next unit in the chain if power is turned off.

Battery -- The random access memory on the 1445 is battery backed up. To provide for a clean transistion from normal power to battery, a threshold detector Q2, is used to generate an on board power down signal. This is used to defeat the chip select for the RAM and generate a reset pulse to the 8055.

Normal AC power down will generate a power signal on the 1441. This interrupts the 8085 which then sets a flag in memory. When power is restored this flag indicates that HV should be off and the mainframe deselected. In case of a transient on the +5 (primarily due to power on insertion of HV cards), the on board power down detect will protect the memory and reset the 8085. Since no indication of a normal AC off is present the processor will continue as if nothing happened.

Card Interface -- The main areas interfacing the processor to high voltage cards are the ADC, DAC's and digital programming memory.

The ADC is a unipolar device and the proper polarity can be selected through multiplexer U26 according to card type. The card's readback is buffered through a variable gain amplifier (U14, jumper selectable) and the desired card is selected through mux Ul.

The DACs are simply connected to provide the programming current limit for the cards. The LSB weighting is 10 pA so that a programmed current limit of 100 corresponds to a current limit of about 1 mA.

The reference output from the ADC is used to generate Negative Full Scale (NFS) and Positive Full Scale (PFS). It is first raised to +10 V by U14 then selectively divided through a resistor network and jumper J5 to generate four selectable full scale ranges. This voltage is buffered by U38 to supply NFS to the cards. NFS is inverted by U38 to supply PFS to the cards.

The digital programming is sent to the cards in four bit words. These are then latched on

the card to form a 16 bit word (12 bits data, 1 sign, 3 zeros). These are stored sequentially in memory and three free running LS161's generate the addressing. The addressing is also sent to the cards and decoded to form the CSEL lines. To provide access for writing new values to the RAM a synchronizing circuit compares the free running address to the desired channel requested by the processor. When the channel "comes around" the write line to the RAM is asserted and the latched output from the processor is multiplexed onto the databus and the write to all four locations occurs "on the fly". There are two individual RAM chips that are addressed in parallel. Which of these two devices is written, read from, or sent to the cards is controlled by the appropriate multiplexers and demultiplexers. The read back of programmed voltages is done by latching (U44 -- U47) the four words of a channel's data as they appear in the normal addressing loop.
Note that demand voltage programming is not ramped or rate limited in any way. The HV cards will respond to these demand changes immediately.

4.2 1443 High Voltage Cards

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The 1443 Series of High Voltage Plug in cards are designed to convert a digital demand value to a HV output independently for each of 16 HV channels. The basic functions implemented on the card are digital data bus decoding and latching, digital to analog conversion of demand values and demultiplexing, high voltage generation and regulation, and multiplexing of readback voltages to be feedback to the 1445 controller.
The digital data for a single channel is encoded in four successive 4-bit bytes on the data bus DB0 to DB3 allowing 16 bits per channel. The first byte contains the MSBs of the 16 bit data word of which the MSB is indicative of card polarity. The remaining 3 bytes contain the 12 bits of HV demand programming. The CSEL signal operates the "Timing Generator" circuit and is asserted when the Most Significant Byte for a channel on this HV card is presented on the Data Bus. The timing generator then clocks the data into latches. If the first byte contains incorrect coding of polarity the "Control Data Accumulator" latches will be held in the cleared state resulting in a demand value of zero. The 12 bit output of the latches are available to the DAC circuits.
Two programming resolution HV cards are available. The standard HV card utilizes a 10 bit DAC and the optional /12 suffix cards are equipped with a 12 bit DAC. Since the pinouts of the two DACs are not compatible, a separate socket is provided for each. The only notable difference is that the 10 bit DACs are not connected, and do not respond, to the 2 LSBs of the 12 bit programming word.
The DAC is supplied with an external Full Scale Reference Voltage which is set by the programming gain jumpers on the 1445 controller. The output current of the DAC is converted to a demand voltage via U13 which has a gain adjustment to allow calibration of the programming accuracy of the HV card. The output from U13 corresponds to 1/410 of the resultant HV to be generated. The analog control voltage is then demultiplexed by U14 which, in conjunction with a "hold" capacitor on each channel, provides a DC control voltage on each of its 16 outputs.
A new channel of the HV card is updated by the data bus every 32 psec. The 4 bytes of data and the channel on card address (CA2 - CA5), which address the control voltage demultiplexer, are latched within the first 2 haec. During this time the demultiplexer is disabled to allow for DAC settling time. During the remaining 30 psec the demultiplexer is connecting U13 to the hold capacitor for the addressed channel. The remaining 15 HV card slots are also updated during this time.
The systems sequence for updating HV channels is to start at channel 0 of card 0 and then update channel 0 of card 1, 2, ..., 15 and then moves to channel 1 of card 0 etc. This cycle is controlled by hardware on the 1445 controller and causes every HV channel to be updated every 512 sec.
High Voltage generation is accomplished through a fixed frequency, pulse width modulated switching circuit. The switch transistor "kicks" the primary circuit of the set-up transformer. The width of the drive pulse affects the sinusoidal voltage swing of the primary circuit which is symmetrical about the 31.5 V baseline. The secondary circuit of the transformer is capacitively tuned to be resonant at 62.5 KHz. The transformer provides voltage gain with a set-up turns ratio of 1:43. Additional gain is provided by a voltage doubler. The output of the voltage doubler is smoothed by a multistage filter network.
Each HV output is monitored by the HD140 divider network in series with a panel accessable HV output adjustment pot. The "Error Amplifier" monitors the feedback from the HD140 as well as the DC control voltage from the hold capacitor and adjusts its output to null the error between its two inputs. The error amplifier output is the reference level to the 311 comparitor. The other comparitor input is a ramp that, when compared to the error amplifier output, determines the switch transistor drive pulse width. There are 4 Ramp Generator circuits each producing a differently phased ramp from the 4 digital sync inputs. Adjacent channels are connected to different ramp generators to minimize crosstalk effects.

The common node of the high voltage output stage is tied to ground through a resistor which provides a voltage level corresponding to the average high voltage output current. Q21 acts as a current limiter by comparing the resistors voltage to the reference supplied by the 1445 controller. If output current increases beyond the limit threshold, Q21 is biased on and reduces the error amplifier input from the control voltage hold capacitor. See Figure 4.1.

The center tap of the HD140 is also used for readback monitoring to the system ADC. A buffer is inserted into the readback oath to isolate the HD140 and the local error amplifier from noise that can be caused by the readback multiplexer switching. The readback monitor is within the feedback loop of the voltage regulator. This causes the operation of the HV Output Adjustment pot to adjust only the HV output and not the readback value.

The sixteen readback buffers are multiplexed onto a single readback line (VFB). A readback address (FAO -- FA3) plus a decoded card select (FSEL) controls the readback multiplexer. The readback addresses are under total control of the Processor and are not associated with the demand data addressing scheme. When the HV card is selected for readback the polarity of the card is returned to the controller by a clamp to ground on either the POS or NEG lines. Empty card slots are identified by neither polarity ID line being asserted.

The HV output digital means. limited by the about 7 W is transistor. In increase to a frequency. In a frequency of stage maximum output voltage is not limited to 2500 V by The maximum voltage produceable is about 2900 V and is voltage limits (PVL or NVL). The maximum output power of limited by the maximum drive pulse width to the switch either of these limit modes the ripple of the HV output will volt or more with a frequency of twice the AC line the current limit mode the ripple may increase to a volt with several KHz.

A certain amount of crosstalk between adjacent channels on a card is caused by stray capacitive coupling. This coupling does not affect the monitor circuits but is injected into the HV output stage. It is most noticable by setting a channel to 0 V while it's neighbors are at maximum voltage. The zeroed channel may be at 120 V unloaded or as low as 30 V if loaded with 1 M Q, This low level output when the demand value for a channel is set to zero poses no danger to the user since it contains very little energy.

Note that this crosstalk effect does not cause additive errors in the regulator circuit. If the channel is at 50 V output and the demand is between 0 and 50 V the output will remain at 50 V since the regulator is not responsiblefor the error. Increasing the demand to 60 V will allow the regulator to operate properly to produce about 60 V. Due to this crosstalk, large voltage changes may cause brief transient effects on adjacent channels.

4.3 1442 Technical Description

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The 1442 is an off-line switching power supply. The input AC is rectified and filtered to supply the switching stage. Power switching is a full-wave bridge consisting of Q1 -- Q4. The secondary of the power transformer is full-wave rectified to produce 31.5 V.

The supply is pulse width modulated by a TL494C (U4). The outputs of U4 driving the base transformer. This transformer has four secondary windings and a regenerative feedback winding from the power transformer. The "turn on" of the power transistors is aided by this regenerative signal. The base drive circuit then provides the "turn off" power.

All necessary auxiliary circuits are provided by the rest of the 1449 system. Power supplies (+15, +5) come from the 1441 and the control signal (clock, HV UP, fault reset) are generated on the 1445.

The circuit is protected locally against several fault conditions. The power transformer primary current is rectified and filtered to monitor output current. A thermostat mounted on the heat sink provides temperature protection (set for 90 degrees C). Overvoltage is checked by an OP amp (U6), and the presence of a clock from the 1445 is guaranteed by missing pulse detector U5. This is necessary since the 1442 is synchronized to the rest of the system. This prevents beat frequencies from occurring. These fault conditions are diode or'ed together to set a flip-flop and turn the supply off if necessary. The fault out line will indicate this condition to the 1445. The 1445 can then take appropriate action and attempt to reset the 1442.

Whenever the 1442 is "turned on", a ramp is supplied to it's dead time control (U4 pin 4) by a resistor and capacitor. This "soft start" prevents extreme current surges.

4.4 1441 Technical Description

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The 1441 is a combined low voltage power supply and auxiliary control unit.

POWER SUPPLIES

The 1441 is an off-line switching power supply. independent circuits to generate +15, -15, and +5.3. similar circuits so only one will be described.
The 220 nominal input AC is rectified and filtered to provide approximately 350 V DC to the switching stage. Both the output from, and the control to, the switching transistors are transformer coupled. This provides complete line isolation. The power stage is a half-wave configuration. One end of the main power transformer primary is connected to 1/2 of the input DC through a capacitive divider. The other end is driven through a push-pull transistor pair (2N6543s). The secondary of the transformer is full wave rectified and filtered through an LC network to provide the output voltage. Operation of the power stage is fixed frequency, pulse width modulated, and controlled by an SG3524 switching regulator IC. The SC3524 compares the output voltage (divided down) with its reference (pins 1,2) and accordingly regulates its outputs (pins 12,13). Each output drives a pulse transformer through a transistor buffer. The base drive transformer is a dual secondary. Part of the signal is used to generate a voltage source for switching the power transistors (half-wave rectified into a 47 uf cap.). Two buffers are used (2N2907 and 2N3053) to provide clean base drives for the power transistors.
The SG3524 synchronizes its output to the clock provided by the 1445 (pin 3). It can also be turned off by the S.D. control signal (pin 10). When resistor/capacitor provides a ramp up (soft start).
The output current is sensed by a .025 3W resistor. This is then converted by an OP amp into an overcurrent signal.
The outputs are proteced from overvoltage by transorbs mounted on the backplane.

POWER SUPPLY CONTROL

To run the power supplies an auxiliary transformer is used to provide +12 (LM7812), -12 (LM7912), and +5 (TIP31C). This transformer is also used to detect low line and power down conditions. The negative peak of the secondary is balanced against +5. If the peak is of sufficient amplitude Ul (LM311) will trigger monostable U2 (96S02). This missing pulse detector is used to shut down all three supplies.
One half of U3 is in control of the +5.3 V supply. It has a 2 second time constant and is fired from either the power down detect or the +5.3 overcurrent detect. The capacitor on it's trigger is to ensure proper power on sequencing. The other half of U3 is in control of the +15, -15 shut down. It is configured as a flip-flop with a clock and clear. Clocking the flop releases the shut down and soft start for +15 and -15. This is the end of the 2 second turn on delay (capacitively coupled), the fault reset, or the power down detect (for proper turn on when not in mainframe). Clearing the flop turns of f +15, and -15 and generates the fault out to the 1445. The clear is the "or" of +15 overcurrent, -15 overcurrent or overtemperature.
Since +5.3 is necessary for the 1445 and 1443 control circuits, a fault on this line also brings down +15 and -15. It will continually try to reset itself at 2 second intervals. The +15 and -15 are the supplies to most analog circuits and are interlocked to prevent erratic high voltage operation, however they will not bring down the +5.3. The 1445 will take care of issuing the fault reset for these supplies.

AUXILIARY CIRCUITS

HV ON LAMP -- The control signal for the 1442 supplies is buffered and drives a lamp controlled by the 1445.
HV DISABLE, INTERLOCK, and READY LAMP -- the HV disable and interlock are or'ed together and the results are buffered to drive the ready lamp. This signal is send back to the 1445.
STATUS LEMO -- The open collector buffered output from the HV UP signal.
VOLTAGE LIMIT and RUN UP/DOWN CIRCUITS -- The HV UP signal is generated on the 1445 in response to turn on/off commands. The 1441 generates the signals PVL and NVL. These are used by the 1443 cards to limit their maximum output voltage. The maximum value of these signals is set by two front panel potentiometers. The minimum is fixed. When the HV UP signal changes from logical 0 to 1 (turn on), both NVL and PVL are ramped up to their maximum value. During turn off (HV UP goes to 0), both limits are ramped to their minimum.

TESTING

The 1441 has been designed to operate in a stand alone mode. By removing the control cable and DC power connector (leaving only the AC line cord) it can be tested independent of the system. Note that this is for the power supplies only, without the control signals the auxiliary circuits cannot be controlled. This is absolutely safe, its just that their states may not be predicted. Note the READY lamp is driven from +15 V. It the lamp does not light press the switch (it's a mechanial flip-flop). This is a simple "life test". Since the +15 is interlocked to the -15, and both are defeated if there is no +5.3 V, the READY

lamp is a reasonable indication that the unit is operational.

4.5 Output Current Characteristics

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The current limit circuit on the 1443 is a simple transistor design. This is the reason for the loose tolerance in the current limit specifications. Also, the HV sense resistor is part of the measured load. To guarantee full output current the circuit is designed (and checked) to have its error on the PLUS side. The current limit circuitry is there to protect the load not the 1443. Current limited operation is not an intended mode of use.

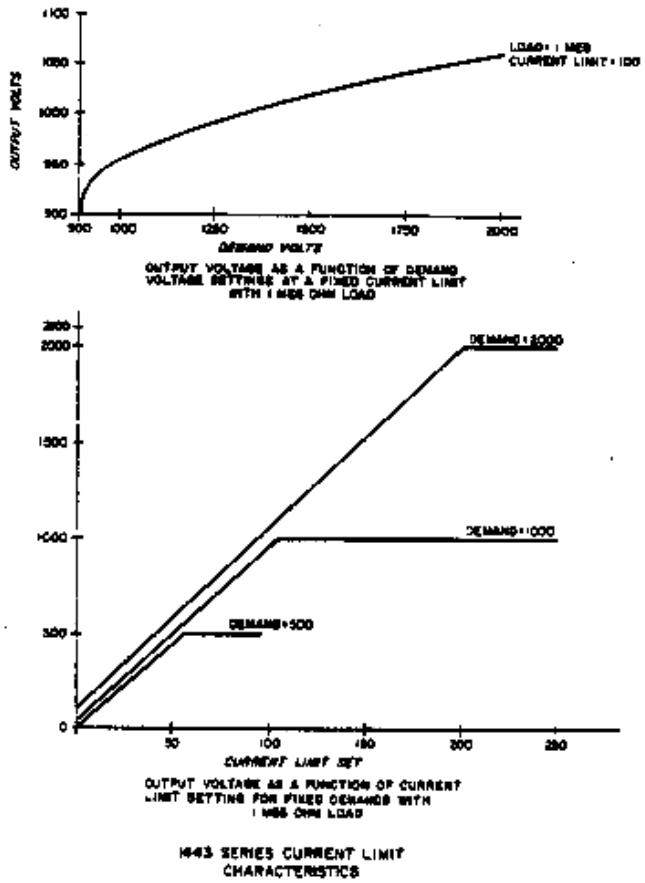

Figure 4.1