UNIVERSITAT POLITÈCNICA DE CATALUNYA
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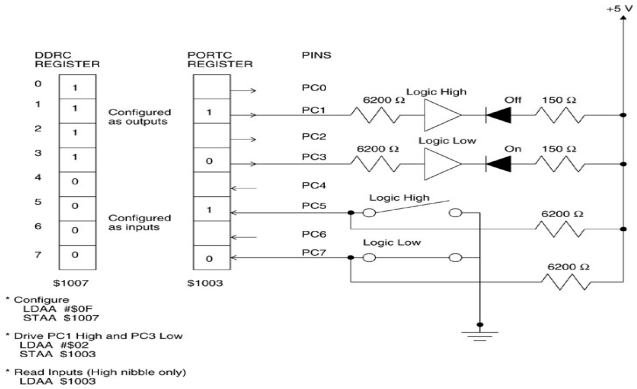
I/O Ports

Dpt. Enginyeria de Sistemes, Automàtica i Informàtica Industrial

Need of I/O ports

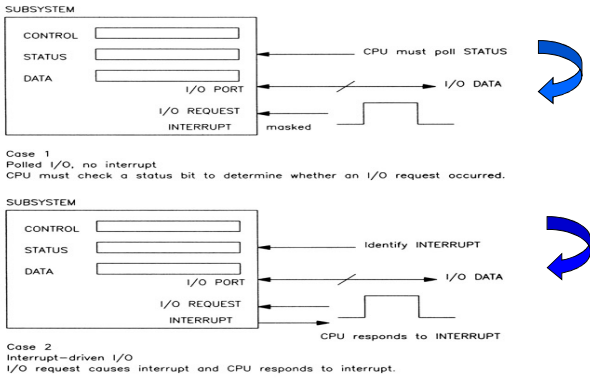
- Several applications require interfacing an MCU with Light Emitting Diodes, Switches, Liquid Crystal Display, Seven Segment Displays.
- I/O ports therefore have to be programmed to handle input/output signals.



I/O Port Structure

1. Data Register: for data in transit
2. Control Register: Hold commands from processor to port
3. Status Register: Used to monitor I/O activity

Principle functionality is serve as way station for data in transit between the computer and external world.

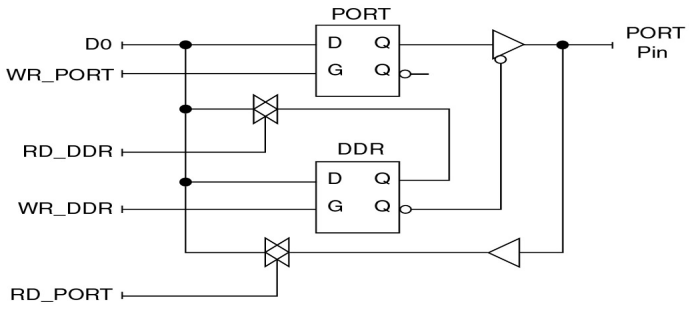


Polling

Interrupt Driven

General Purpose I/O: Bidirectional

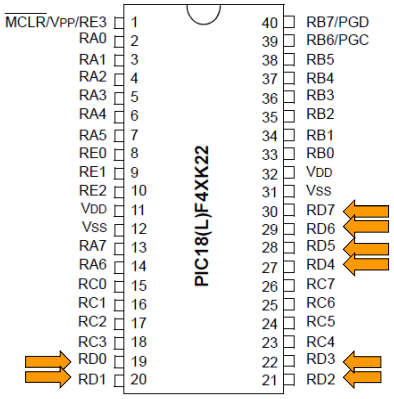
- Most GPIO pins on the MCU can be programmed for use in either direction.
- Two registers: the data register PORT and data direction register DDR.
  - The DDR determines the direction of the port pin.
    - If the DDR = 1 then the port is an output and
    - if the DDR = 0 the data register output is disabled and the port pin is placed in high impedance state.



Overview of the PIC18 Parallel I/O Ports

- **I/O pins are often grouped into** ports**.**
- **A port consists of up to 8 pins, a data direction register (**TRISx**), a latch register (**LATx**) , and a data register (**PORTx**); where, x = A…H, J, K.**

- Data to be output is written into the latch, which in turn drives the output pins.
- **An I/O port is often** multiplexed **with one or more peripheral functions.**
- **When a peripheral function is enabled, the I/O pins cannot be used for general purpose I/O.**
- **A PIC18 may have as many as 10 I/O ports.**



Example: PORTD pins D{0..7}

Overview of the PIC18 Parallel I/O Ports

Table 3 (reference manual, page 7) fully describes the functionality of all device pins.

TABLE 3: PIC18(L)F4XK22 PIN SUMMARY

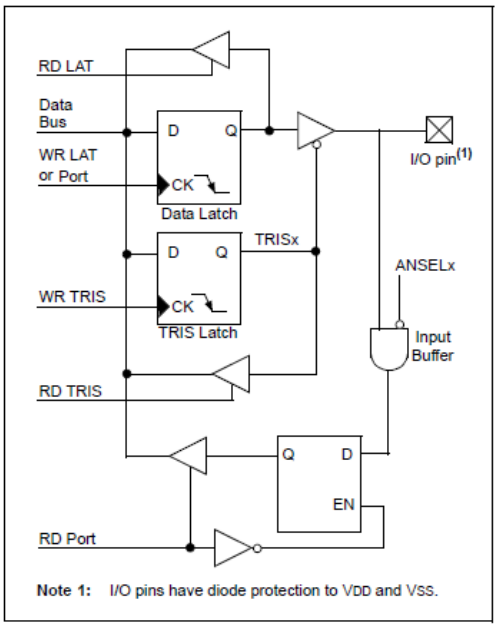
40-PDIP	40-UQFN	44-TQFP	44-QFN	I/O	Analog	Comparator	CTMU	SR Latch	Reference	(E)CCP	EUSART	MSSP	Timers	Interrupts	Pull-up	Basic
2	17	19	19	RA0	AN0	C12IN0-										
3	18	20	20	RA1	AN1	C12IN1-										
4	19	21	21	RA2	AN2	C2IN+			VREF- DACOUT							
5	20	22	22	RA3	AN3	C1IN+			VREF+							
6	21	23	23	RA4		C1OUT		SRQ					T0CKI			
7	22	24	24	RA5	AN4	C2OUT		SRNQ	HLVDIN			$\overline{SS}$1				
14	29	31	33	RA6												OSC2 CLKO
13	28	30	32	RA7												OSC1 CLKI
33	8	8	9	RB0	AN12			SRI		FLT0				INT0	Y	
34	9	9	10	RB1	AN10	C12IN3-								INT1	Y	
35	10	10	11	RB2	AN8		CTED1							INT2	Y	
36	11	11	12	RB3	AN9	C12IN2-	CTED2			CCP2 P2A(1)					Y	
37	12	14	14	RB4	AN11								T5G	IOC	Y	
38	13	15	15	RB5	AN13					CCP3 P3A(3)			T1G T3CKI(2)	IOC	Y	
39	14	16	16	RB6										IOC	Y	PGC
40	15	17	17	RB7										IOC	Y	PGD
15	30	32	34	RC0						P2B(4)			SOSCO T1CKI T3CKI(2) T3G			
16	31	35	35	RC1						CCP2(1) P2A			SOSCI			

.....

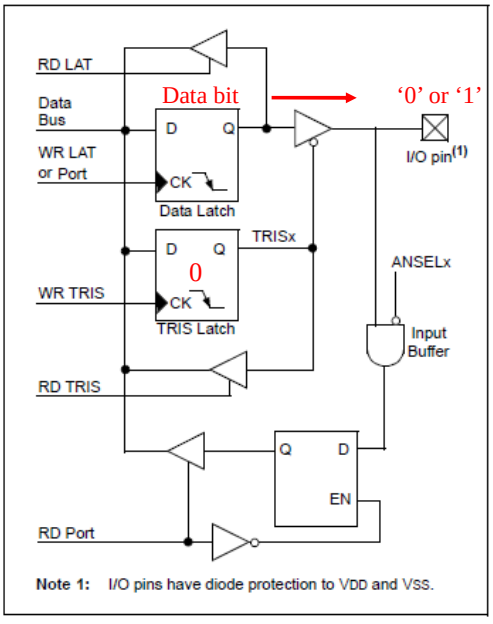
PIC18 I/O port operation

- **TRISx register (data direction register. 1 Input 0 Output)**
- **PORTx register (reads the levels on the pins of the device)**
- **LATx register (output latch)**
- **ANSELx register (analog input control.** 0 Digital / 1 Analog**)**

x = {A, B, C, D}

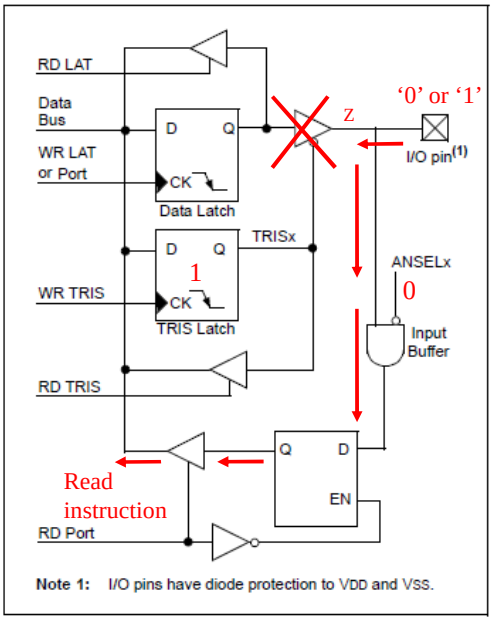


PIC18 I/O port operation



Output

PIC18 I/O port operation



Input

PORTA

- **PORTA is an 8-bit wide, bidirectional port.**
- **Pins RA6 and RA7 are multiplexed with the main oscillator pins.**
- **The operation of pins RA<3:0> and RA5 as analog is selected by setting the ANSELA<5, 3:0> bits in the ANSELA register which is the default setting after a Power-on Reset.**

Note: **On a Power-on Reset, RA5 and RA<3:0> are configured as analog inputs and read as '0'. RA4 is configured as a digital input.**

PORTA

There is a table (e.g. PORTA pag. 128) showing all the possible functions and the required configuration settings for every pin.

TABLE 10-1: PORTA I/O SUMMARY

Pin Name	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RA0/C12IN0-/AN0	RA0	0	0	O	DIG	LATA<0> data output; not affected by analog input.
		1	0	I	TTL	PORTA<0> data input; disabled when analog input enabled.
	C12IN0-	1	1	I	AN	Comparators C1 and C2 inverting input.
	AN0	1	1	I	AN	Analog input 0.
RA1/C12IN1-/AN1	RA1	0	0	O	DIG	LATA<1> data output; not affected by analog input.
		1	0	I	TTL	PORTA<1> data input; disabled when analog input enabled.
	C12IN1-	1	1	I	AN	Comparators C1 and C2 inverting input.
	AN1	1	1	I	AN	Analog input 1.
RA2/C2IN+/AN2/ DACOUT/VREF-	RA2	0	0	O	DIG	LATA<2> data output; not affected by analog input; disabled when DACOUT enabled.
		1	0	I	TTL	PORTA<2> data input; disabled when analog input enabled; disabled when DACOUT enabled.
	C2IN+	1	1	I	AN	Comparator C2 non-inverting input.
	AN2	1	1	I	AN	Analog output 2.
	DACOUT	x	1	O	AN	DAC Reference output.
	VREF-	1	1	I	AN	A/D reference voltage (low) input.
RA3/C1IN+/AN3/ VREF+	RA3	0		O	DIG	LATA<3> data output; not affected by analog input.
		1	0	I	TTL	PORTA<3> data input; disabled when analog input enabled.
	C1IN+	1	1	I	AN	Comparator C1 non-inverting input.
	AN3	1	1	I	AN	Analog input 3.
	VREF+	1	1	I	AN	A/D reference voltage (high) input.

PORTA

There is a table (e.g. PORTA pag. 128) showing all the possible functions and the required configuration settings for every pin.

RA4/CCP5/C1OUT/ SRQ/T0CKI	RA4	0	—	O	DIG	LATA<4> data output.
		1	—	I	ST	PORTA<4> data input; default configuration on POR.
	CCP5	0	—	O	DIG	CCP5 Compare output/PWM output, takes priority over RA4 output.
		1	—	I	ST	Capture 5 input/Compare 5 output/ PWM 5 output.
	C1OUT	0	—	O	DIG	Comparator C1 output.
	SRQ	0	—	O	DIG	SR latch Q output; take priority over CCP 5 output.
	T0CKI	1	—	I	ST	Timer0 external clock input.
RA5/C2OUT/SRNQ/ SS1/ HLVDIN/AN4	RA5	0	0	O	DIG	LATA<5> data output; not affected by analog input.
		1	0	I	TTL	PORTA<5> data input; disabled when analog input enabled.
	C2OUT	0	0	O	DIG	Comparator C2 output.
	SRNQ	0	0	O	DIG	SR latch $\overline{Q}$ output.
	$\overline{SS1}$	1	0	I	TTL	SPI slave select input (MSSP1).
	HLVDIN	1	1	I	AN	High/Low-Voltage Detect input.
	AN4	1	1	I	AN	A/D input 4.
RA6/CLKO/OSC2	RA6	0	—	O	DIG	LATA<6> data output; enabled in INTOSC modes when CLKO is not enabled.
		1	—	I	TTL	PORTA<6> data input; enabled in INTOSC modes when CLKO is not enabled.
	CLKO	x	—	O	DIG	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
	OSC2	x	—	O	XTAL	Oscillator crystal output; connects to crystal or resonator in Crystal Oscillator mode.
RA7/CLKI/OSC1	RA7	0	—	O	DIG	LATA<7> data output; disabled in external oscillator modes.
		1	—	I	TTL	PORTA<7> data input; disabled in external oscillator modes.
	CLKI	x	—	I	AN	External clock source input; always associated with pin function OSC1.
	OSC1	x	—	I	XTAL	Oscillator crystal input or external clock source input ST buffer when configured in RC mode; CMOS otherwise.

TABLE 10-2: REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	—	ANSA3	ANSA2	ANSA1	ANSA0	149
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH<1:0>		308
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH<1:0>		308
LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	152
VREFCON1	DACEN	DACLPS	DACOE	—	DACPSS<1:0>		—	DACNSS	335
VREFCON2	—	—	—	DACR<4:0>					336
HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL<3:0>				337
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	148
SLRCON	—	—	—	SLRE	SLRD	SLRC	SLRB	SLRA	153
SRCON0	SRLEN	SRCLK<2:0>			SRQEN	SRNQEN	SRPS	SRPR	329
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				253
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS<2:0>			154
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	151

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for PORTA.

TABLE 10-3: CONFIGURATION REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONFIG1H	IESO	FCMEN	PRICLKEN	PLLCFG	FOSC<3:0>				345

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for PORTA.

Example: Initializing PORTA

```
MOVLB 0xF          ; Set BSR for banked SFRs
CLRF PORTA,1       ; Initialize PORTA by
                   ; clearing output
                   ; data latches
CLRF LATA,1        ; Alternate method
                   ; to clear output
                   ; data latches
MOVLW C0h          ; Configure I/O
MOVWF ANSELA,1     ; for digital inputs
MOVLW 0CFh         ; Value used to
                   ; initialize data
                   ; direction
MOVWF TRISA,1      ; Set RA<3:0> as inputs
                   ; RA<5:4> as outputs. A6 and A7 are OSC!!
```

Example: C programming

```
#include <p18f45k22.h>
#include "config.h"

void main()
{
    ANSELA = 0xC0    //A5-A0:DIGITAL, Pin A6 and A7? OSC or IO
    ANSELB = 0x00     // B DIGITAL
    TRISA=0xFF;       // PORTA INPUT
    TRISB=0x00;       // PORTB OUTPUT
    PORTB=0x00;

    while (1) {
        PORTB=PORTA;
    };
}
```

PORTB

- **PORTB is an 8-bit wide, bidirectional port.**
- **All pins may be used as Digital or Analog Pins**
- **The pins RB<2:0> may bes used for external interrupts (Int0, Int1 and Int2).**
- **Four of the PORTB pins (RB<7:4>) are individually configurable as interrupt-on-change pins**

Note: **On a Power-on Reset, RB<5:0> are configured as analog inputs by default and read as '0'; RB<7:6> are configured as digital inputs.**

When the PBADEN Configuration bit is set to '1', RB<5:0> will alternatively be configured as digital inputs on POR.

PORTC

- **PORTC is an 8-bit wide, bidirectional port.**
- **RC2..RC7 may be used as Analog Pins. On a Power-on Reset, these pins are configured as analog inputs.**

PORTD

- **PORTD is an 8-bit wide, bidirectional port.**
- **All the pins may be used as Analog Pins. On a Power-on Reset, these pins are configured as analog inputs.**

PORTE

- **PORTE is an** 4-bit **wide, bidirectional port.**
- **RE0..RE2 may be used as Analog Pins. On a Power-on Reset, these pins are configured as analog inputs.**
- **RE3 = MASTER CLEAR. On a Power-on Reset, RE3 is enabled as a digital input only if Master Clear functionality is disabled.**

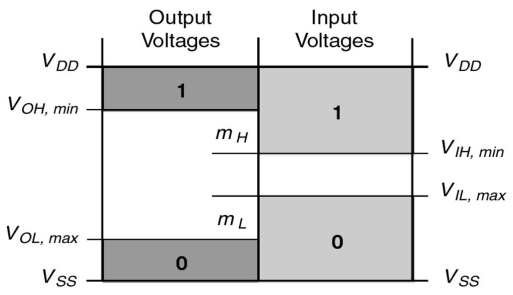
Interfacing: Voltage Parameters

- **Like any digital device, before we can connect something to an input or output, we need to know the specification for the interface parameter.**
- **The first parameter to consider are the input and output voltage levels and corresponding noise margins.**

VDD and VSS are supply voltages. The output voltage parameters are V_{OL} and V_{OH}.

The input voltage parameters are V_{IL} and V_{IH}.

For a digital system to work correctly, the output high voltage always must be between $V_{IH,min}$ and VDD.



Noise Margin?

Interfacing: Current Parameters

- **The interface current parameters are the output currents, I_{OH} and I_{OL}, and the input leakage current I_{IN}.**
  1. **I_{OH} is the current ***flowing out*** of a ***high output***.**
  2. **I_{OL} is the current ***flowing out*** of a ***low output***.**
  3. **I_{IN} is the leakage current that flows into or out of an input pin.**

- **These currents are used to determine the ***static fanout of a device*****, that is, the number of inputs that can be connected to one output while preserving the required voltage margins.**
  1. **Static fanout for a low output is: $n_L = | I_{OL,max} |/| I_{In} |$**
  2. **Static fanout for a high output is: $n_H = | I_{OH,max} |/| I_{In} |$**
  3. **$n = \min [n_H, n_L]$**

Absolute maximum ratings

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD}, and $\overline{MCLR}$)	-0.3V to (V_{DD} + 0.3V)
Total power dissipation **(Note 1)**	1.0W
Maximum current out of V_{SS} pin (-40°C to +85°C)	300 mA
Maximum current out of V_{SS} pin (+85°C to +125°C)	125 mA
Maximum current into V_{DD} pin (-40°C to +85°C)	200 mA
Maximum current into V_{DD} pin (+85°C to +125°C)	85 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports (-40°C to +85°C)	200 mA
Maximum current sunk by all ports (+85°C to +125°C)	110 mA
Maximum current sourced by all ports (-40°C to +85°C)	185 mA
Maximum current sourced by all ports (+85°C to +125°C)	70 mA

Maximum I_{OX} for the PIC18F45K22 is +/- 25mA.

This Maximum ratings give the value that if exceeded may destroy the part.

DC Characteristics. Supply Voltage

27.1 DC Characteristics: Supply Voltage, PIC18(L)F2X/4XK22

PIC18(L)F2X/4XK22				Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	PIC18LF2X/4XK22	1.8	—	3.6	V	
			PIC18F2X/4XK22	2.3	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage**(1)		1.5	—	—	V	
D003	VPOR	VDD **Start Voltage** to ensure internal Power-on Reset signal		—	—	0.7	V	See section on Power-on Reset for details
D004	SVDD	VDD **Rise Rate** to ensure internal Power-on Reset signal		0.05	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	**Brown-out Reset Voltage**						
		BORV<1:0> = 11(2)		1.75	1.9	2.05	V	
		BORV<1:0> = 10		2.05	2.2	2.35	V	
		BORV<1:0> = 01		2.35	2.5	2.65	V	
		BORV<1:0> = 00(3)		2.65	2.85	3.05	V	

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: On PIC18(L)F2X/4XK22 devices with BOR enabled, operation is supported until a BOR occurs. This is valid although VDD may be below the minimum rated supply voltage.

3: With BOR enabled, full-speed operation (FOSC = 64 MHz or 48 MHz) is supported until a BOR occurs. This is valid although VDD may be below the minimum voltage for this frequency.

Input characteristics

27.8 DC Characteristics: Input/Output Characteristics, PIC18(L)F2X/4XK22

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O PORT:					
D140		with TTL buffer	—	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D140A			—	—	0.15 VDD	V	1.8V ≤ VDD ≤ 4.5V
D141		with Schmitt Trigger buffer	—	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
		with I2C levels	—	—	0.3 VDD	V	
		with SMBus levels	—	—	0.8	V	2.7V ≤ VDD ≤ 5.5V
D142		MCLR, OSC1 (RC mode)(1)	—	—	0.2 VDD	V	
D142A		OSC1 (HS mode)	—	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:		—	—		
D147		with TTL buffer	2.0	—	—	V	4.5V ≤ VDD ≤ 5.5V
D147A			0.25 VDD + 0.8	—	—	V	1.8V ≤ VDD ≤ 4.5V
D148		with Schmitt Trigger buffer	0.8 VDD	—	—	V	2.0V ≤ VDD ≤ 5.5V
		with I2C levels	0.7 VDD	—	—	V	
		with SMBus levels	2.1	—	—	V	2.7V ≤ VDD ≤ 5.5V
D149		MCLR	0.8 VDD	—	—	V	
D150A		OSC1 (HS mode)	0.7 VDD	—	—	V	
D150B		OSC1 (RC mode)(1)	0.9 VDD	—	—	V	
	IIL	**Input Leakage I/O and MCLR**(2),(3)					VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D155		I/O ports and MCLR	—	0.1	50	nA	≤ +25°C(4)
			—	0.7	100	nA	+60°C
			—	4	200	nA	+85°C
			—	35	1000	nA	+125°C

Interpretation:
if the power supply (VDD) is between 4,5V and 5,5V then $V_{IL\,MAX}$ = 0,8V

$V_{IL\,MAX}$ = 0,8V (voltage input low maximum) means that any voltage under 0,8V put on an input pin will always be read as a logical '0'

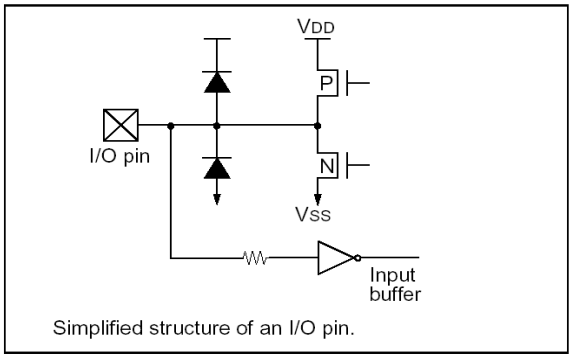
Output characteristics

27.8 DC Characteristics: Input/Output Characteristics, PIC18(L)F2X/4XK22 (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D159	VOL	**Output Low Voltage** I/O ports	—	—	0.6	V	IOL = 8 mA, VDD = 5V IOL = 6 mA, VDD = 3.3V IOL = 1.8 mA, VDD = 1.8V
D161	VOH	**Output High Voltage**(3) I/O ports	VDD - 0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 1 mA, VDD = 1.8V

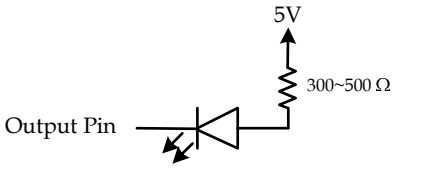
$V_{OL\,MAX}$ = 0,6V (voltage output low maximum) means that even in the worst conditions, a logical '0' will always be output as a voltage less than 0,6V

Protection diodes

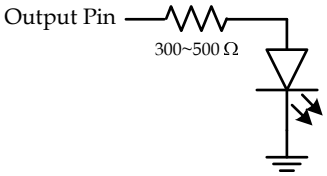


Simplified structure of an I/O pin.

Interfacing with LEDs



(a) low voltage on output pin lights LED



(b) high voltage on output pin lights LED

A LED emits light when current flows through it in the positive direction i.e. when the voltage on the anode side is made higher than the voltage on the cathode side.

The forward voltage across the LED is typically about 1.5 to 2 Volts.
We need to add a resistor to limit the current.

Connecting a LED to an Output Port

- Using a 5-volt supply and assuming that the LED has a 2.0 V drop across it, what resistor value will limit the current to 10mA?
- Answer:
  - $5V = 2.0V + I_{Rx} \times Rx$
  - Setting I_{Rx} to 10mA the resistor Rx is solved to be 300 Ohm.

Seven Segment Displays

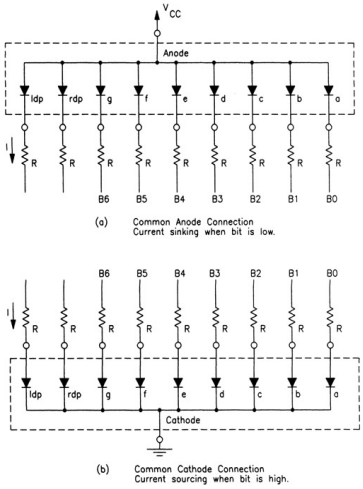
- Common Anode:

1. All anodes are tied in common.
2. Segment will be lit whenever a low voltage is applied.

- Common Cathode:

1. all cathodes are tied in common.
2. Segment will be lit whenever a high voltage is applied.

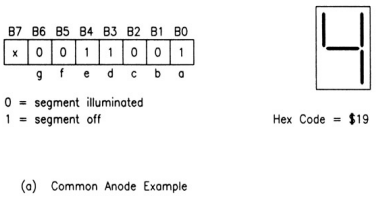
- Current limiting resistors must be included or else you might damage display.

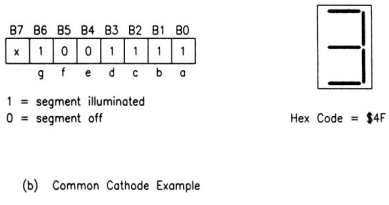


Seven Segment Displays: Examples

- **Depending on the type of display used a different hex code is generated by the MCU.**

1. **Common Anode: sending a ``0" will illuminate the segment.**
2. **Common Cathode: sending a ``1" will illuminate the segment.**





Interfacing with DIP Switches

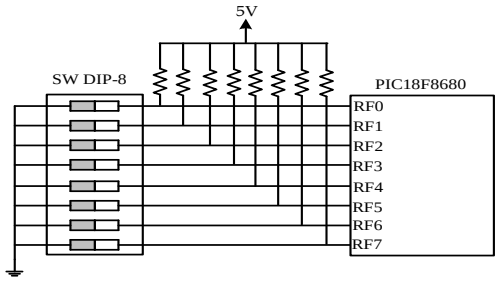


Figure 7.24b Connecting a set of eight DIP switches to port F of the PIC18F8680

Reading a byte from the DIP switches to WREG

```
movlw   0xFF    ; configure port F for input
movwf   TRISF   ;       “
movf    PORTF,W         ; read portF
```

Interfacing with Keypad

Types of Key Switches

1. Membrane: A plastic or rubber membrane presses one conductor onto another.
2. Capacitive: Two parallel plates. Pressing the plates changes the distance between the plates and changes the capacitance.
3. Hall effect: The motion of the magnetic flux lines of a permanent magnet perpendicular to a crystal is detected as voltage appearing between the two faces of the crystal.
4. Mechanical: Two metal contacts are brought together to complete an electrical circuit.

Mechanical Keypads and Keyboard

- **Low cost and strength of construction**
- **Most popular**
- **Pressing the key switch generates a series of pulses instead of a single clean output**
- **Human being cannot press and release the key switch 20 ms**
- **A debouncing process is required for correct operation**

Keypad Input Program

Keypad Input Program **Consists of Three Parts**

1. Keypad scanning
2. Key switch debouncing
3. Table lookup

Keypad Scanning

- **Performed to detect which key is being pressed**
- **Performed row by row or column by column**
- **The rows and columns of a keypad are simply conductors**
- **The row to be scanned is pulled to low. Other rows are pulled high.**
- **When a key is pressed, the corresponding row and column are shorted together and is detected low.**
- **The diodes in Figure 7.26b provide**

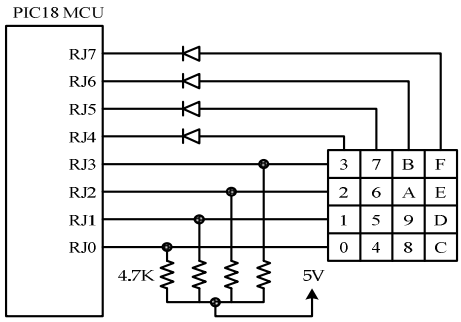


Figure 7.26b Sixteen-key keypad connected to PIC18 (used in all SSE demo boards)

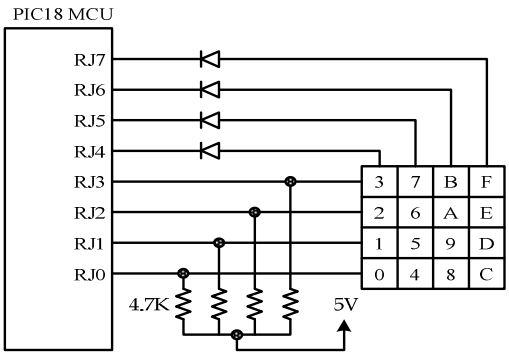
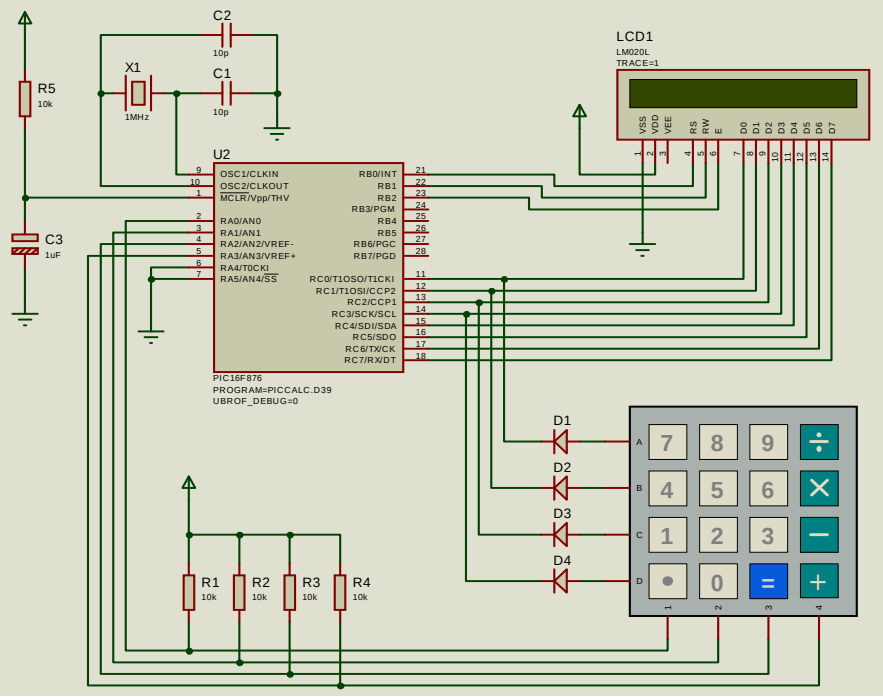


Figure 7.26b Sixteen-key keypad connected to PIC18 (used in all SSE demo boards)



Keypad Debouncing

- **When a key is pressed, the voltage of the key switch falls and rises a few times within a period of about 5 ms as a contact bounces.**
- **A debouncer will recognize that the switch is closed after the voltage is low for about 10 ms and will recognize that the switch is open after the voltage is high for about 10 ms.**
- **Both hardware and software debouncing solutions are available.**
- **The simplest and most popular software solution is** wait-and-see. **The program simply waits for 10 ms after detecting a key switch is closed and re-examines the same key.**
- **Three hardware debouncing techniques are shown in Figure 7.27.**

ASCII Code Lookup

- **The keypad input subroutine returns the ASCII code to the caller.**

Keypad Debouncing

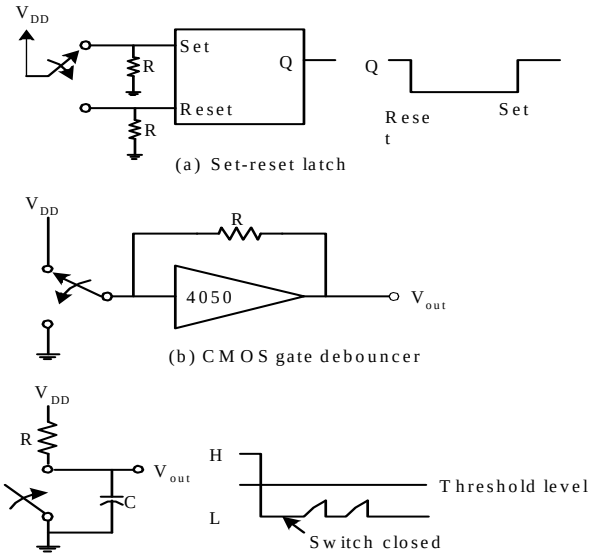
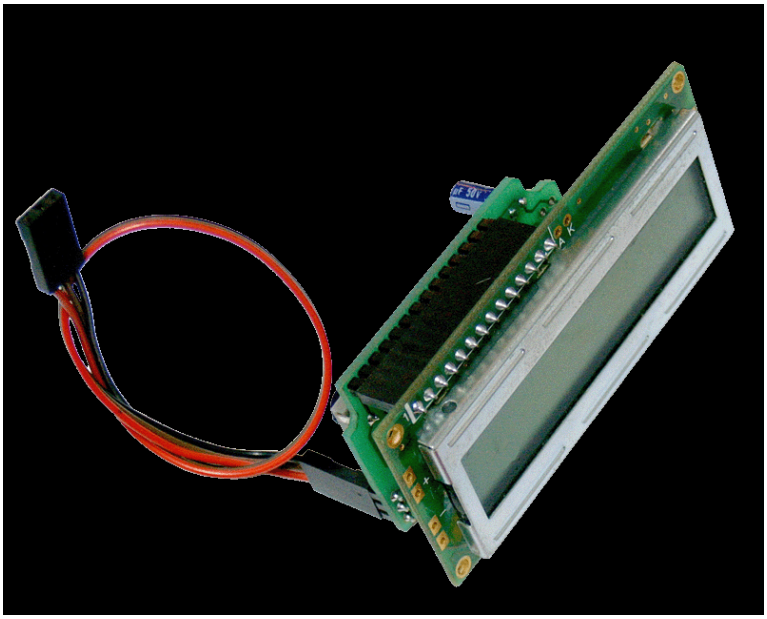


Figure 7.27 Hardware debouncing techniques

Keypad debouncing

```
#include     <p18F8680.h>
#define  keypad_dir  TRISJ
#define  keypad      PORTJ
void wait_10ms(void);
…
unsigned char get_key (void)
{
keypad_dir = 0x0F;              /* configure RJ7..RJ4 for output */
keypad |= 0xF0;                 /*  RJ3..RJ0 for input */
while (1) {
     keypad &= 0xEF;            /* set RJ4 to low to scan the first row */
     if (!(keypadbits.RB0)) {
          wait_10ms( );
          if (!(keypadbits.RB0))
               return 0x30;/* return the ASCII code of 0 */
     }
     if (!(keypadbits.RB1)) {
          wait_10ms( );
          if (!(keypadbits.RB1))
               return 0x31;/* return the ASCII code of 1 */
…
}
```

Interfacing to LCD



Interfacing to LCD

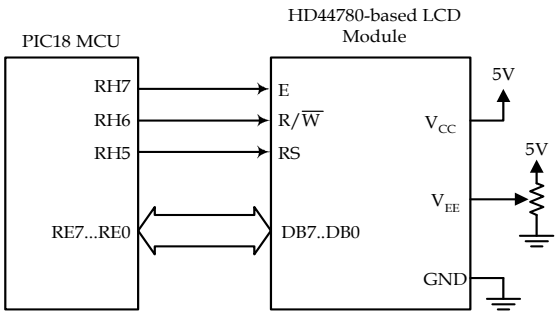


Figure 7.21a LCD interface example (8-bit bus)

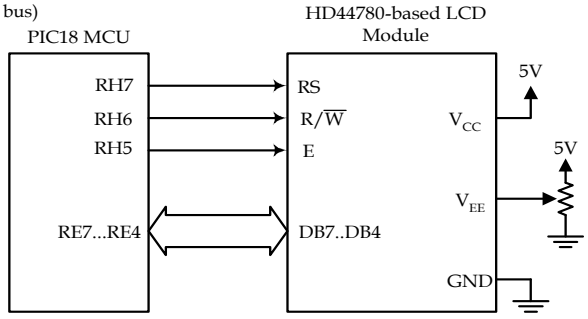


Figure 7.21b LCD interface example (4-bit bus)

DDRAM

Display data RAM

16 x 8-bit characters

Table 7.8b DDRAM address usage for a 2-line LCD

Display size	Visible	
	character positions	DDRAM addresses
2 * 16	00..15	0x00..0x0F + 0x40..0x4F
2 * 20	00..19	0x00..0x13 + 0x40..0x53
2 * 24	00..23	0x00..0x17 + 0x40..0x57
2 * 32	00..31	0x00..0x1F + 0x40..0x5F
2 * 40	00..39	0x00..0x27 + 0x40..0x67

CGROM

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)

Note: The user can specify any pattern for character-generator RAM.

CGRAM

Character generator RAM

Eight character patterns can be written

5 x 8 pixel fonts

The selection of DDRAM or CGRAM is determined by the instruction.

User-defined char code (for using character)	RAM position (for defining character
0x00* or 0x08	**0x00 to 0x07**
0x01 or 0x09	**0x08 to 0x0F**
0x02 or 0x0A	**0x10 to 0x17**
0x03 or 0x0B	**0x18 to 0x1F**
0x04 or 0x0C	**0x20 to 0x27**
0x05 or 0x0D	**0x28 to 0x2F**
0x06 or 0x0E	**0x30 to 0x37**
0x07 or 0x0F	**0x38 to 0x3F**

A3	A2	A1	A0	O4	O3	O2	O1	LSB O0	
0	0	0	0	1	0	0	0	0	
0	0	0	1	1	0	0	0	0	
0	0	1	0	1	0	1	1	0	
0	0	1	1	1	1	0	0	1	
0	1	0	0	1	0	0	0	1	
0	1	0	1	1	0	0	0	1	
0	1	1	0	1	1	1	1	0	
0	1	1	1	0	0	0	0	0	← Cursor position

*** 0x00 should not be used. Reserved for end-of-string.**

LCD instructions

Table 7.6 HD44780 instruction set

Instruction	Code										Description	Execution time
	RS	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears display and returns cursor to the home position (address 0).	1.64 ms
Cursor home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position (address 0). Also returns display being shifted to the original position. DDRAM contents remain unchanged.	1.64 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Set cursor move direction (I/D), specifies to shift the display (S). These operations are performed during data read / write.	40 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets on/off of all display (D), cursor on/off (C) and blink of cursor position character (B).	40 µs
Cursor /display shift	0	0	0	0	0	1	S/C	R/L	*	*	Sets cursor-move or display-(S/C), shift direction (R/L). DDRAM contents remains unchanged.	40 µs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display line (N) and character font (F).	40 µs
Set CGRAM address	0	0	0	1	CGRAM address						Sets the CGRAM address. CGRAM data is sent and received after this setting.	40 µs
Set DDRAM address	0	0	1	DDRAM address							Sets the DDRAM address. DDRAM data is sent and received after this setting.	40 µs
Read busy flag and address counter	0	1	BF	CGRAM/DDRAM address							Reads busy flag (BF) indicating internal operation is being performed and reads CGRAM or DDRAM address counter contents (depending on previous instruction).	0 µs
Write to CGRAM or DDRAM	1	0	write data								Writes data to CGRAM or DDRAM.	40 µs
Read from CGRAM or DDRAM	1	1	read data								Reads data from CGRAM or DDRAM.	40 µs

LCD instruction bit names

Table 7.7 LCD instruction bit names

Bit name	Settings	
I/D	0 = decrement cursor position.	1 = increment cursor position
S	0 = no display shift.	1 = display shift
D	0 = display off	1 = display on
C	0 = cursor off	1 = cursor on
B	0 = cursor blink off	1 = cursor blink on
S/C	0 = move cursor	1 = shift display
R/L	0 = shift left	1 = shift right
DL	0 = 4-bit interface	1 = 8-bit interface
N	0 = 1/8 or 1/11 duty (1 line)	1 = 1/16 duty (2 lines)
F	0 = 5x7 dots	1 = 5 x 10 dots
BF	0 = can accept instruction	1 = internal operation in progress

HD44780 Commands

1. Clear display **(0x01). This command clears the LCD screen, sets the address counter to 0, sets the cursor to the upper left corner of the LCD screen, and also sets the I/D bit to 1 in entry mode.**

2. Return Home **(0x02). Sets DDRAM address 0 into address counter, move cursor to the upper left corner of the display but does not change the contents of the DDRAM.**

3. Entry Mode Set. **The I/D bit of this command controls the incrementing or decrementing of the DDRAM address. The display will shift if the S bit is 1 when the DDRAM is being written into.**

4. Display On/Off Control**. This command can turn on the display (D = 1), turn on the cursor (C = 1), and turn on the cursor blinking (B = 1).**

5. Cursor or Display Shift. **This command determines to shift the cursor (S/C = 0 bit) or display (S/C bit = 1) to the right (R/L bit = 1) or to the left (R/L bit = 0).**

HD44780 Commands

6. Function Set. **This command allows the user to set the interface data length, select the number of lines, and the font size:**
DL **bit. When set to 1, data is exchanged in 8-bit length. Otherwise, data is exchanged in 4-bit length.**
N **bit. When set to 1, two-line display is selected. Otherwise, 1-line display is selected.**
F **bit. When set to 0, the 5 × 7 font is selected. Otherwise, 5 × 10 font is selected.**

7. Set CGRAM Address**. This command contains the CGRAM address to be set into the address counter.**

8. Set DDRAM Address**. This command allows to set the DDRAM address into the address counter.**

9. Read Busy Flag and Address. **This instruction reads the busy flag (BF) and the address counter. The BF flag indicates whether the LCD controller is still executing the previously received command.**

LCD registers

The Data Register
- **The data to be written into the DDRAM or CGRAM is written into this register.**
- **To read data from DDRAM or CGRAM, the microcontroller reads from this register.**

The Instruction Register
Stores instruction codes

RS signal selects IR or DR register

Table 7.9 Register selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DDRAM or CGRAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

Timing Consideration for the LCD

- Certain timing parameters must be satisfied in order to successfully access the LCD.

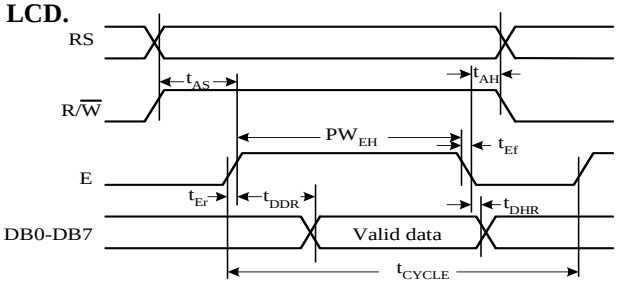


Figure 7.22 HD44780 LCD controller read timing diagram

Table 7.12 HD44780 bus timing parameters (2 MHz operation)

Symbol	Meaning	Min	Typ	Max.	Unit
t_{CYCLE}	Enable cycle time	500	-	-	ns
PW_{EH}	Enable pulse width (high level)	230	-	-	ns
t_{Er}, t_{Ef}	Enable rise and decay time	-	-	20	ns
t_{AS}	Address setup time, RS, R/W, E	40	-	-	ns
t_{DDR}	Data delay time	-	-	160	ns
t_{DSW}	Data setup time	80	-	-	ns
t_{H}	Data hold time (write)	10	-	-	ns
t_{DHR}	Data hold time (read)	5	-	-	ns
t_{AH}	Address hold time	10	-	-	ns

Timing Consideration for the LCD

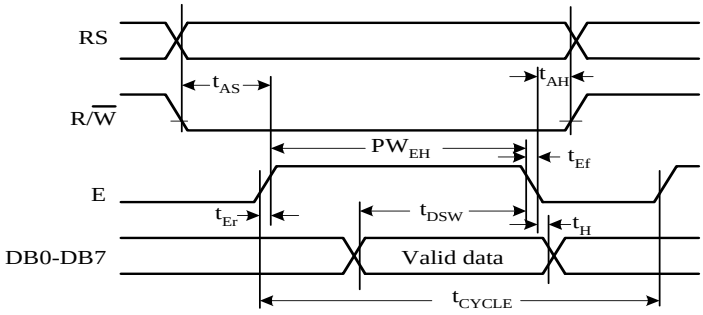


Figure 7.23 HD44780 LCD controller write timing diagram

Table 7.12 HD44780 bus timing parameters (2 MHz operation)

Symbol	Meaning	Min	Typ	Max.	Unit
t_{CYCLE}	Enable cycle time	500	-	-	ns
PW_{EH}	Enable pulse width (high level)	230	-	-	ns
t_{Er}, t_{Ef}	Enable rise and decay time	-	-	20	ns
t_{AS}	Address setup time, RS, R/W, E	40	-	-	ns
t_{DDR}	Data delay time	-	-	160	ns
t_{DSW}	Data setup time	80	-	-	ns
t_{H}	Data hold time (write)	10	-	-	ns
t_{DHR}	Data hold time (read)	5	-	-	ns
t_{AH}	Address hold time	10	-	-	ns

Procedure for Writing a Byte **into the** IR register

Step 1
Pull the RS and the E signals to low.
Step 2
Pull the R/W signal to low.
Step 3
Pull the E signal to high.
Step 4
Output data to the output port attached to the LCD data bus. (Need to configure port for output).
Step 5
Pull the E signal to low.

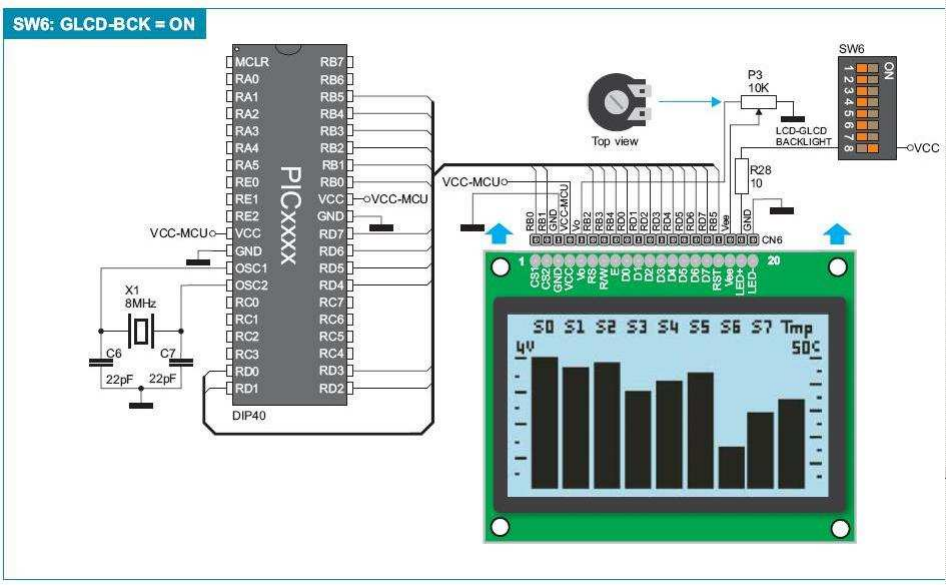
Procedure for Reading a Byte **from the** IR register

Step 1
Pull the RS and the E signals to low.
Step 2
Pull the R/W signal to high.
Step 3
Pull the E signal to high.
Step 4
Read the value of the LCD data bus. (need to configure port E for input)
Step 5
Pull the E signal to low.

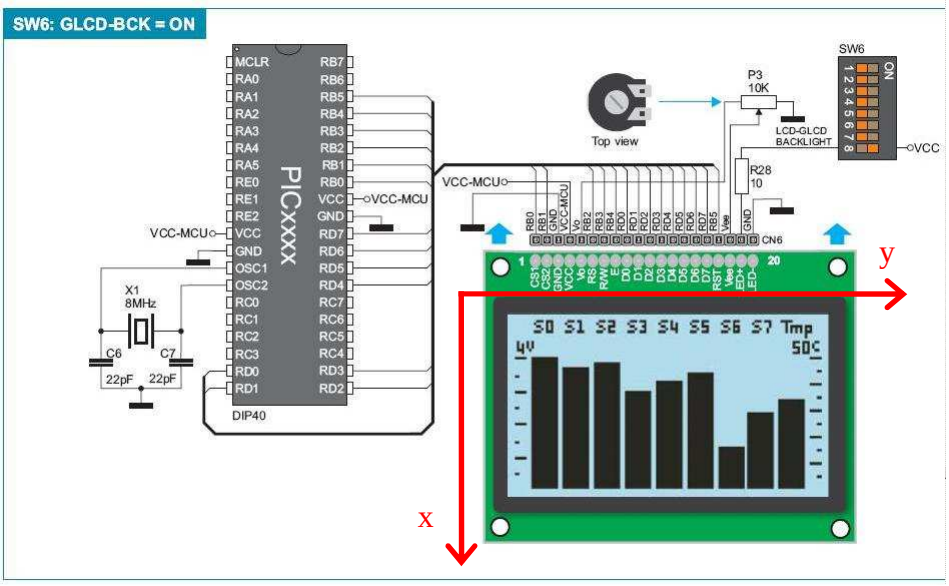
Procedure for Writing a Byte **into the** LCD data register

Step 1
Pull the RS signal to high and pull the E signals to low.
Step 2
Pull the R/W signal to low.
Step 3
Pull the E signal to high.
Step 4
Output data to the I/O port attached to the LCD data bus.
Step 5
Pull the E signal to low.

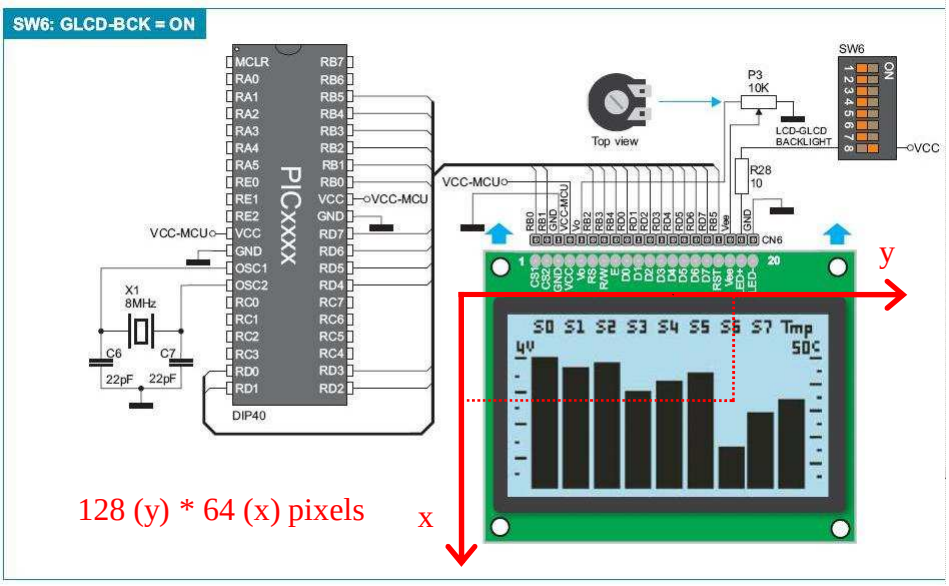
El GLCD



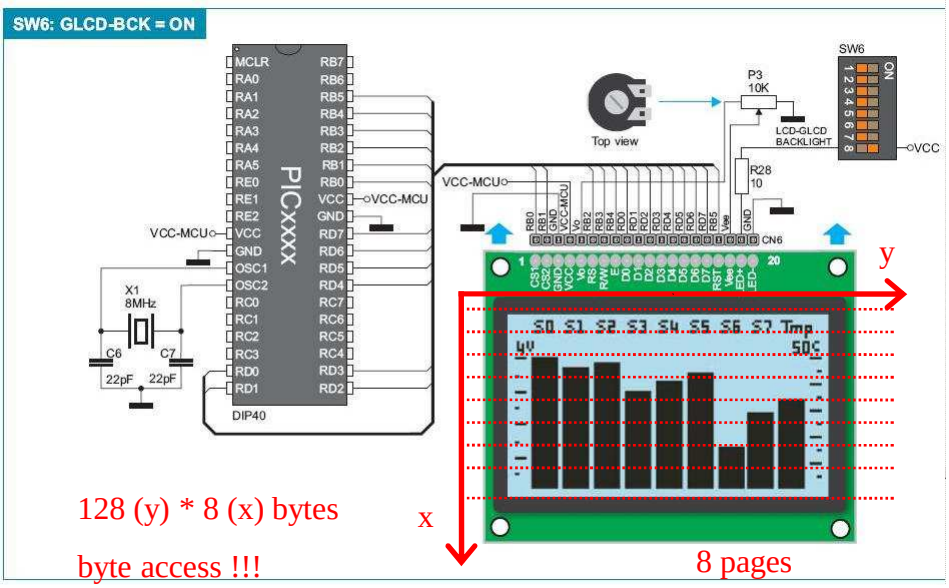
El GLCD



El GLCD



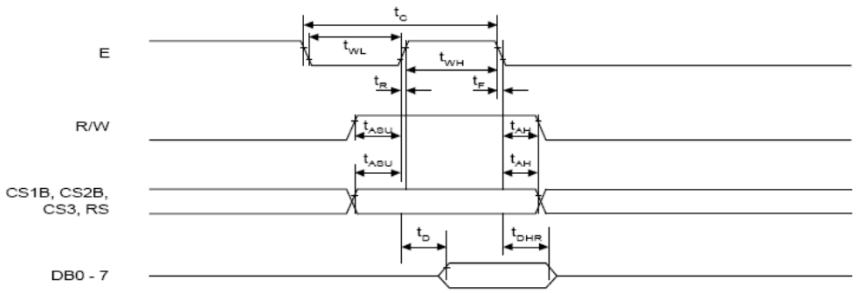
El GLCD



GLCD. Instruction set

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L: OFF, H: ON
Set address (Y address)	L	L	L	H	Y address (0 - 63)						Sets the Y address in the Y address counter.
Set page (X address)	L	L	H	L	H	H	H	Page (0 - 7)			Sets the X address at the X address register.
Display start line (Z address)	L	L	H	H	Display start line (0 - 63)						Indicates the display data RAM displayed at the top of the screen.
Status read	L	H	Busy	L	On / Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write display data	H	L	Write data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read display data	H	H	Read data								Reads data (DB0:7) from display data RAM to the data bus.

GLCD. Read timing



Characteristic	Symbol	Min	Typ	Max	Unit
E cycle	t_C	1000	-	-	ns
E high level width	t_{WH}	450	-	-	ns
E low level width	t_{WL}	450	-	-	ns
E rise time	t_R	-	-	25	ns
E fall time	t_F	-	-	25	ns
Address set-up time	t_{ASU}	140	-	-	ns
Address hold time	t_{AH}	10	-	-	ns
Data set-up time	t_{DSU}	200	-	-	ns
Data delay time	t_D	-	-	320	ns
Data hold time (write)	t_{DHW}	10	-	-	ns
Data hold time (read)	t_{DHR}	20	-	-	ns

GLCD. Write timing