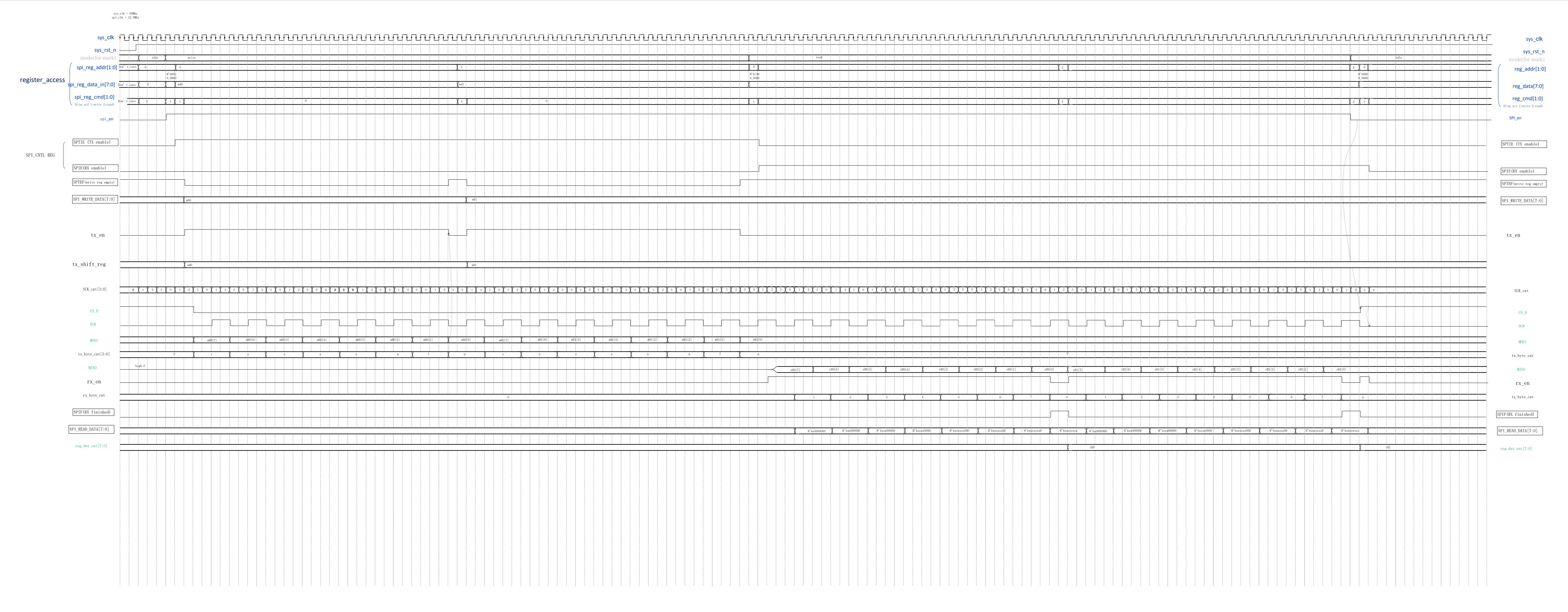
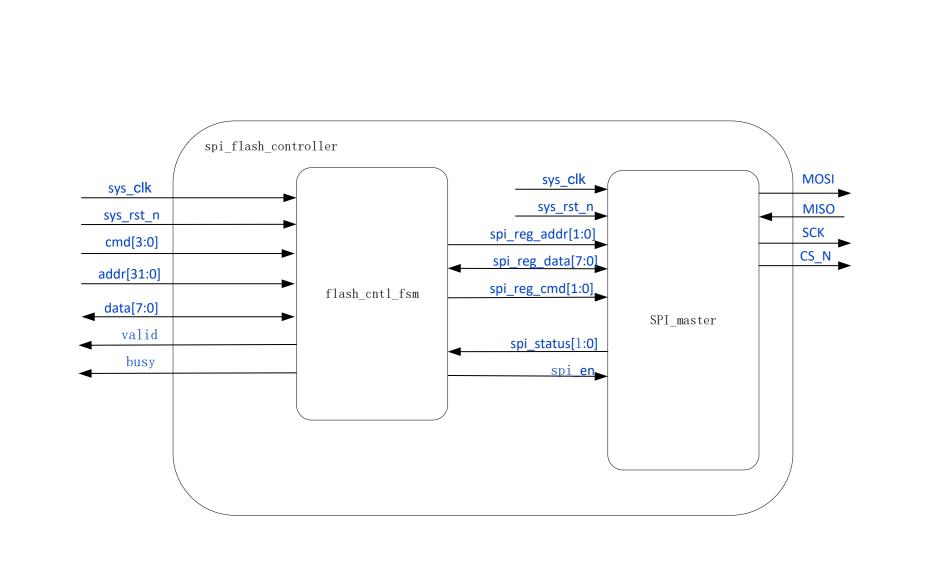


			SPI re	eigsters defination						
0	SPI_CNTL (r/w)	7	6	5	4	3	2	1	0	
		SPIE(RX enable)	SPE (Global enable) SPTIE (TX enable)		MSTR	CPOL	СРНА		LSBFE	
					0	0	0		0	
1	SPI_STATUS (read only)	7	6	5	4	3	2	1	(
		SPIF(RX finished)		SPTEF(TX reg empty)						
		0		1						
2	SPI_READ_DA	7	6	5	4	3	2	1	(
	TA			SPI read data						
	(read only)									
3	SPI_WRITE_D	7	6	5	4	3	2	1	(
	ATA	SPI read data								
	(write only)									





4' b0000 n flach cntl fem 4' b0001 s	ector erase age program ead				
IDLE: 4'b0000 WE: 4'b0001 WRITE: 4'b0011 READ: 4'b0010 sys_clk tPP = 3ms tCE = 400s tSE = 400ms tSHSL = 50ns tBP1= 50us WE sys_rst_n cmd[3:0			Total addr		
tBP2 = 12us data_in[7: cmd_reg[3: addr_reg[31: instruction_reg [7:0] data_byte_cd spi_tx_data_buffer[7:0] [0:255]		X 8' h02			
fsm_n_s busy spi_reg_addr[1:0]	IDLE	WRITE WRITE 3 3 reset the cntl reg w switch to idle 8' h02 a0 dn-1	IDLE	X 0 8' b100 0 0000 X X	X IDLE
spi_reg_cmd[1:0] spi_en spi_disable_pulse spi_status[1](write empty write_finished_pulse					
<pre>spi_status[0](read ready byte_read_done_pulse</pre>		(0 (1) (\(\frac{1}{\text{rd0}}\)	
writen_byte_max read_byte_cnt read_byte_max valid		= (data_byte_cnt-1) + 4	\(\text{rd_num} \)	1 rdn-1 x rdn	X 0
data_out[7:0 wait_cnt tW	t SHSL	1 \(\tw \) \(\	tw X 0	\(\text{rd0} \) \(\text{rd-1} \) \(\text{1} \)	w−

