1. Description

1.1. Project

Project Name	StrRob
Board Name	STM32L476G-DISCO
Generated with:	STM32CubeMX 6.0.0
Date	04/04/2022

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

|	
Core(s)	Arm Cortex-M4

2. Pinout Configuration
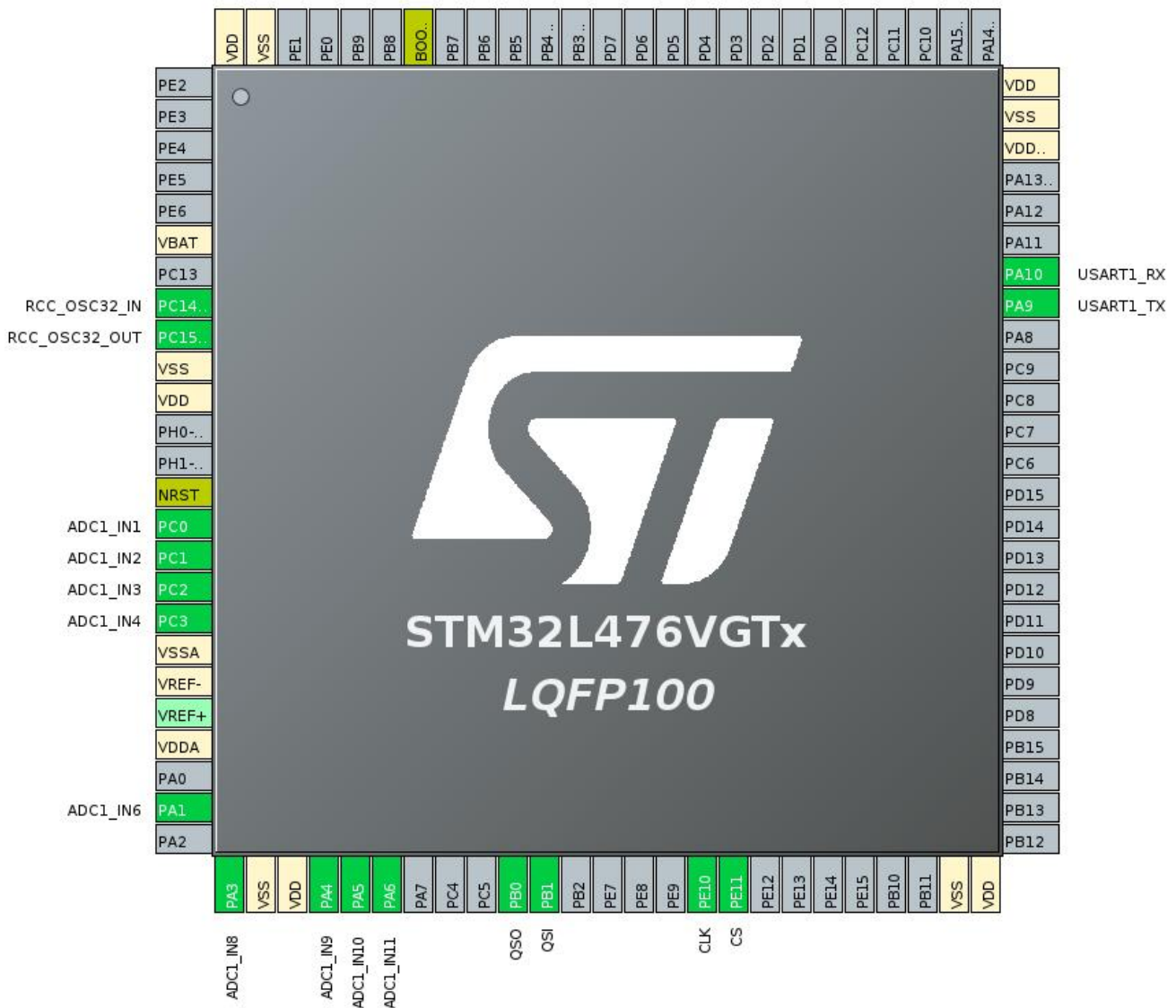
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
14	NRST	Reset		
15	PC0	I/O	ADC1_IN1	
16	PC1	I/O	ADC1_IN2	
17	PC2	I/O	ADC1_IN3	
18	PC3	I/O	ADC1_IN4	
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
24	PA1	I/O	ADC1_IN6	
26	PA3	I/O	ADC1_IN8	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN9	
30	PA5	I/O	ADC1_IN10	
31	PA6	I/O	ADC1_IN11	
35	PB0	I/O	QUADSPI_BK1_IO1	QSO
36	PB1	I/O	QUADSPI_BK1_IO0	QSI
41	PE10	I/O	QUADSPI_CLK	CLK
42	PE11	I/O	QUADSPI_NCS	CS
49	VSS	Power		
50	VDD	Power		
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

4. Clock Tree Configuration
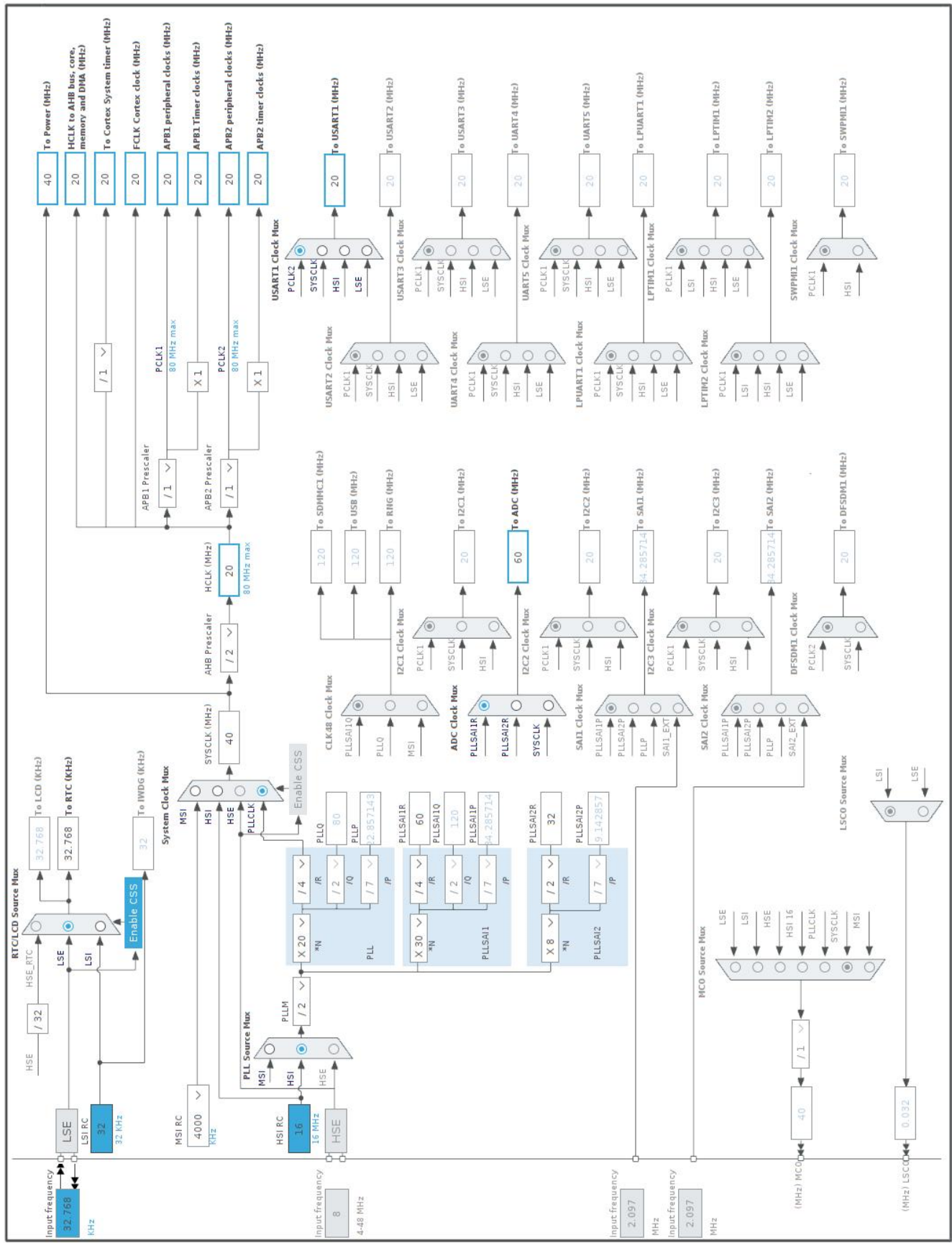
5. Software Project

5.1. Project Settings

Name	Value
Project Name	StrRob
Project Folder	/home/marcel/Documents/semestrVI/SterRob/stmProject/StrRob
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.16.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_QUADSPI_Init	QUADSPI
5	MX_ADC1_Init	ADC1
6	MX_RTC_Init	RTC
7	MX_TIM2_Init	TIM2
8	MX_USART1_UART_Init	USART1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476VGTx
Datasheet	DS10198_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.65	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart
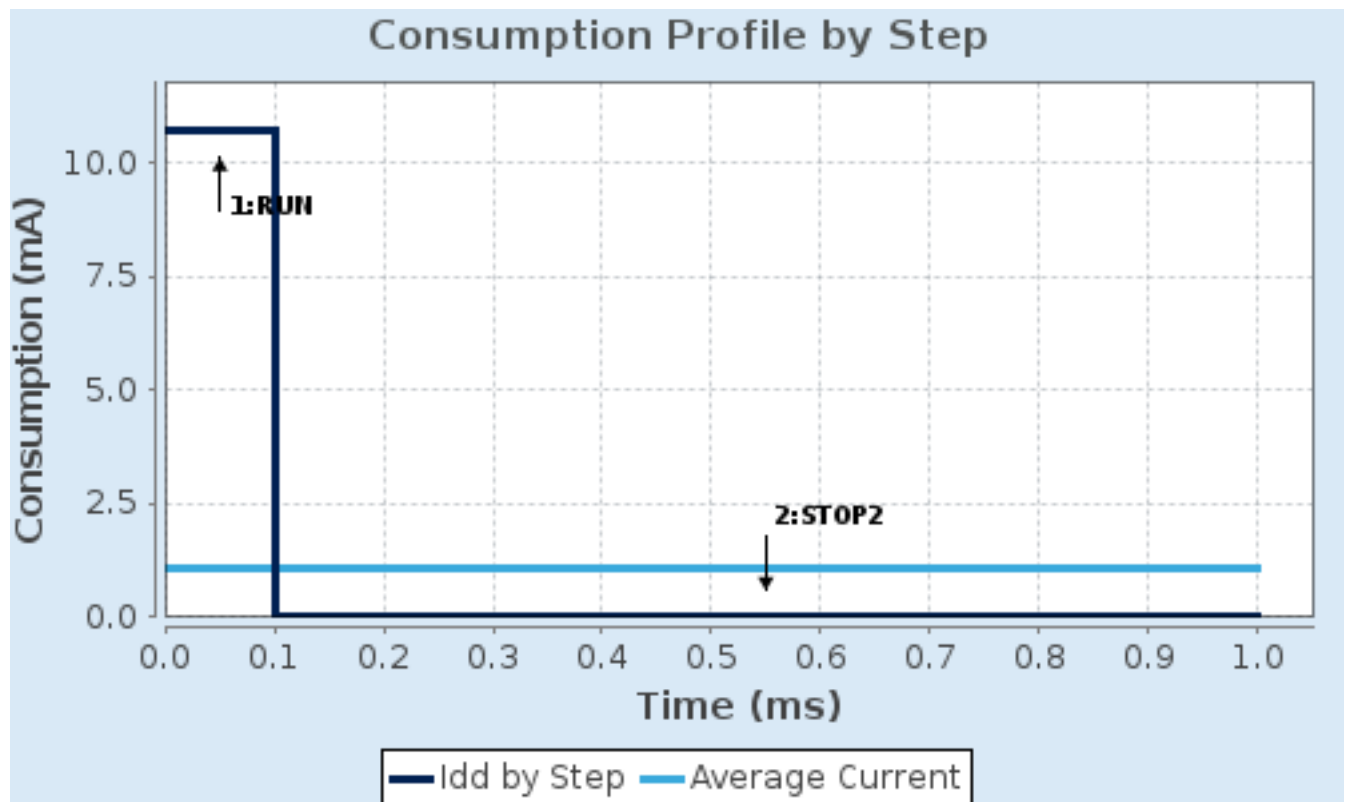
7. IPs and Middleware Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN6: IN6 Single-ended

IN8: IN8 Single-ended

IN9: IN9 Single-ended

IN10: IN10 Single-ended

IN11: IN11 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 8-bit resolution ***
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**9 ***
External Trigger Conversion Source	**Timer 1 Trigger Out event 2 ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**2 ***
Channel	Channel 1

Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**3 ***
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**4 ***
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**5 ***
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**6 ***
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**7 ***
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**8 ***
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Rank	**9 ***
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. GPIO

7.3. QUADSPI
Single Bank: Single/Dual SPI Line
7.3.1. Parameter Settings:

General Parameters:

Clock Prescaler	**1 ***
Fifo Threshold	**4 ***
Sample Shifting	**Sample Shifting Half Cycle ***
Flash Size	**20 ***
Chip Select High Time	1 Cycle
Clock Mode	Low

7.4. RCC
Low Speed Clock (LSE) : Crystal/Ceramic Resonator
7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.5. RTC
mode: Activate Clock Source
mode: Activate Calendar
7.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	**Binary data format ***
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.6. SYS
Timebase Source: SysTick

7.7. TIM2
Clock Source   : Internal Clock
7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**19999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	

Update Event *

7.8. USART1
Mode: Asynchronous
7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN2	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN4	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN6	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN8	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN9	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN10	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN11	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
QUADSPI	PB0	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	QSO
	PB1	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	QSI
	PE10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	CLK
	PE11	QUADSPI_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	CS
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode: **Circular ***

Peripheral Increment: Disable

Memory Increment: **Enable ***

Peripheral Data Width: Half Word

Memory Data Width: Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
ADC1 and ADC2 interrupts	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
USART1 global interrupt	unused		
QUADSPI global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Prefetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
DMA1 channel1 global interrupt	true	true	true
ADC1 and ADC2 interrupts	true	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓	ADC1 ✓	RTC ✓	QUADSPI ✓			
GPIO ✓		TIM2 ✓	USART1 ✓			
NVIC ✓						
RCC ✓						
SYS ✓						

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00108832.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00083560.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00111498.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156964.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209748.pdf

Application note   http://www.st.com/resource/en/application_note/DM00125306.pdf

Application note   http://www.st.com/resource/en/application_note/DM00141025.pdf

Application note   http://www.st.com/resource/en/application_note/DM00144612.pdf

Application note   http://www.st.com/resource/en/application_note/DM00148033.pdf

Application note   http://www.st.com/resource/en/application_note/DM00209768.pdf

Application note   http://www.st.com/resource/en/application_note/DM00216518.pdf

Application note   http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note   http://www.st.com/resource/en/application_note/DM00228015.pdf

Application note   http://www.st.com/resource/en/application_note/DM00227538.pdf

Application note   http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note   http://www.st.com/resource/en/application_note/DM00269143.pdf

Application note   http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note   http://www.st.com/resource/en/application_note/DM00223574.pdf

Application note   http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note   http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note   http://www.st.com/resource/en/application_note/DM00260952.pdf

Application note   http://www.st.com/resource/en/application_note/DM00263732.pdf

Application note   http://www.st.com/resource/en/application_note/DM00269146.pdf

Application note   http://www.st.com/resource/en/application_note/DM00296349.pdf

Application note   http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note   http://www.st.com/resource/en/application_note/DM00264868.pdf

Application note   http://www.st.com/resource/en/application_note/DM00355687.pdf

Application note   http://www.st.com/resource/en/application_note/DM00311483.pdf

Application note   http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note   http://www.st.com/resource/en/application_note/DM00367673.pdf

Application note   http://www.st.com/resource/en/application_note/DM00373474.pdf

Application note   http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note   http://www.st.com/resource/en/application_note/DM00371863.pdf

Application note   http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note   http://www.st.com/resource/en/application_note/DM00354333.pdf

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Application note   http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note   http://www.st.com/resource/en/application_note/DM00536349.pdf

Application note   http://www.st.com/resource/en/application_note/DM00209772.pdf

Application note   http://www.st.com/resource/en/application_note/DM00476869.pdf

Application note   http://www.st.com/resource/en/application_note/DM00660597.pdf

Application note   http://www.st.com/resource/en/application_note/DM00725181.pdf