

# Laboratório de Sistemas Digitais

## Aula Teórico-Prática 13

Ano Letivo 2017/18

Utilização de recursos da FPGA

Restrições e análise temporal

A interface JTAG para programação e  
depuração

# Conteúdo

- Exemplo de utilização de recursos usados por um projeto implementado numa FPGA
- Restrições e análise temporal
  - Exemplo prático com especificação de restrições temporais e avaliação da frequência máxima de funcionamento
- Programação e depuração de FPGAs: a interface JTAG
  - A cadeia JTAG da placa DE2-115
  - A memória FLASH para armazenamento de configurações da FPGA de forma não volátil
  - Criação de ficheiros para programação da memória FLASH

Quartus Prime Lite Edition - C:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/CombMultDiv - CombMultDiv

File Edit View Project Assignments Processing Tools Window Help

CombMultDiv

Project Navigator

Files

- CombMultDiv.srf
- CombMultDiv.sdc
- CombMultDiv.frf
- CombMultDiv.vhd

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Edit Settings
- View Report
- Chip Planner
- Technology Map Viewer (Post-Fitting)
- Design Assistant (Post-Fitting)
- Assembler (Generate programming)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Compilation Report - CombMultDiv

CombMultDiv.vhd

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.all;
3 use IEEE.NUMERIC_STD.all;
4
5 entity CombMultDiv is
6     port(CLOCK_50 : in std_logic;
7         SW : in std_logic_vector(17 downto 0);
8         LEDR : out std_logic_vector(15 downto 0));
9 end CombMultDiv;
10
11 architecture Behavioral of CombMultDiv is
12
13     signal s_sw : std_logic_vector(17 downto 0);
14     signal s_multResult : std_logic_vector(15 downto 0);
15     signal s_divQuotient : std_logic_vector(7 downto 0);
16     signal s_divRemainder : std_logic_vector(7 downto 0);
17
18     begin
19         process(CLOCK_50)
20         begin
21             if (rising_edge(CLOCK_50)) then
22                 s_sw <= SW;
23             end if;
24         end process;
25
26         s_multResult <= std_logic_vector(unsigned(s_sw(7 downto 0)) * unsigned(s_sw(15 downto 8)));
27
28         s_divQuotient <= std_logic_vector(unsigned(s_sw(7 downto 0)) / unsigned(s_sw(15 downto 8)));
29         s_divRemainder <= std_logic_vector(unsigned(s_sw(7 downto 0)) rem unsigned(s_sw(15 downto 8)));
30
31         process(CLOCK_50)
32         begin
33             if (rising_edge(CLOCK_50)) then
34                 if (s_sw(17) = '1') then
35                     LEDR <= s_multResult;
36                 else
37                     LEDR <= s_divRemainder & s_divQuotient;
38                 end if;
39             end if;
40         end process;
41     end Behavioral;
42 end
```

Messages

Type	ID	Message
Information		Quartus Prime Shell was successful. 0 errors, 0 warnings

System Processing (8)

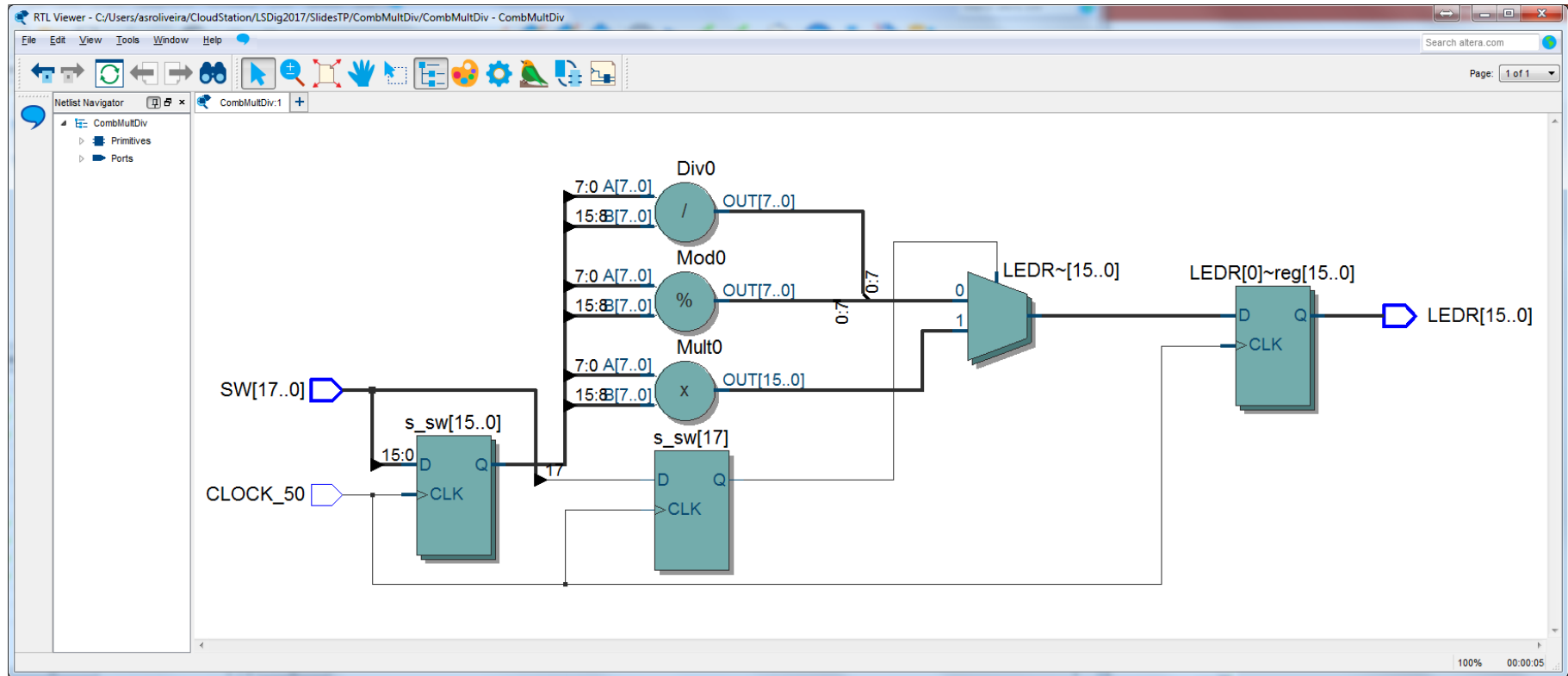
100% 00:00:05

Ficheiros do projeto: VHD, SDC, FRF, SRF (+QSF)

Exemplo de um projeto com multiplicador/divisor combinacional, sem sinal

Entradas e saídas registadas melhora comportamento temporal e facilita análise

# RTL View



# Recursos da FPGA Utilizados

Quartus Prime Lite Edition - C:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/CombMultDiv - CombMultDiv

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator

Files

- CombMultDiv.srf
- CombMultDiv.sdc
- CombMultDiv.frf
- CombMultDiv.vhd

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
  - Summary
  - Settings
  - Parallel Compilation
  - Source Files Read
  - Resource Usage Summary
  - Resource Utilization by Entity
  - DSP Block Usage Summary
  - Optimization Results
  - Parameter Settings by Entity Instance

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Edit Settings
- View Report

Compilation Report - CombMultDiv

Analysis & Synthesis Resource Utilization by Entity

Compilation Hierarchy Node	LC Combinationals	LC Registers	Memory Bits	DSP Elements	DSP 9x9	DSP 18x18	Pins
1  CombMultDiv	164 (24)	33 (33)	0	1	1	0	35
1  lpm_divide:Div0	74 (0)	0 (0)	0	0	0	0	0
1  lpm_divide_nhm:auto_generated	74 (0)	0 (0)	0	0	0	0	0
1  sign_div_unsign_fkh:divider	74 (0)	0 (0)	0	0	0	0	0
1  alt_u_div_i4f:divider	74 (73)	0 (0)	0	0	0	0	0
1  add_sub_8pc:add_sub_1	1 (1)	0 (0)	0	0	0	0	0
2  lpm_divide:Mod0	66 (0)	0 (0)	0	0	0	0	0
1  lpm_divide_q9m:auto_generated	66 (0)	0 (0)	0	0	0	0	0
1  sign_div_unsign_fkh:divider	66 (0)	0 (0)	0	0	0	0	0
1  alt_u_div_i4f:divider	66 (66)	0 (0)	0	0	0	0	0
3  lpm_mult:Mult0	0 (0)	0 (0)	0	1	1	0	0
1  mult_aat:auto_generated	0 (0)	0 (0)	0	1	1	0	0

Note: For table entries with two numbers listed, the numbers in parentheses indicate the number of resources of the given type used by the specific entity alone. The numbers listed outside of parentheses indicate the total resources of the given type used by the specific entity and all of its sub-entities in the hierarchy.

Messages

Type ID Message

- 204019 Generated file CombMultDiv.vho in folder "c:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/simulation/modelsim/" for EDA simulation tool
- 204019 Generated file CombMultDiv\_7\_1200mv\_85c\_vhd\_slow.sdo in folder "c:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/simulation/modelsim/" for EDA simulation tool
- 204019 Generated file CombMultDiv\_7\_1200mv\_0c\_vhd\_slow.sdo in folder "c:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/simulation/modelsim/" for EDA simulation tool
- 204019 Generated file CombMultDiv\_min\_1200mv\_0c\_vhd\_fast.sdo in folder "c:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/simulation/modelsim/" for EDA simulation tool
- 204019 Generated file CombMultDiv\_vhd.sdo in folder "c:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/simulation/modelsim/" for EDA simulation tool
- Quartus Prime EDA Netlist writer was successful. 0 errors, 0 warnings
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 102 warnings

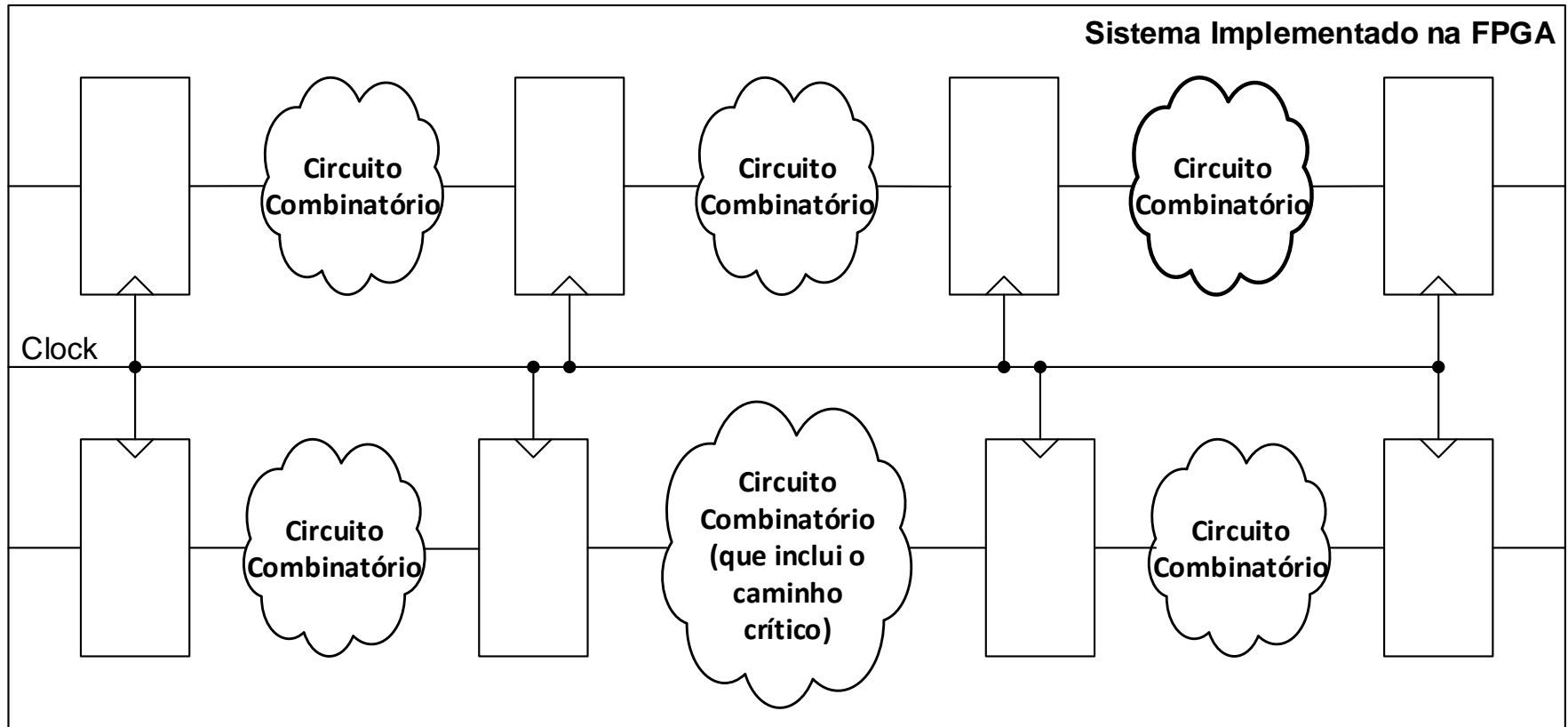
System Processing (231)

100% 00:01:45

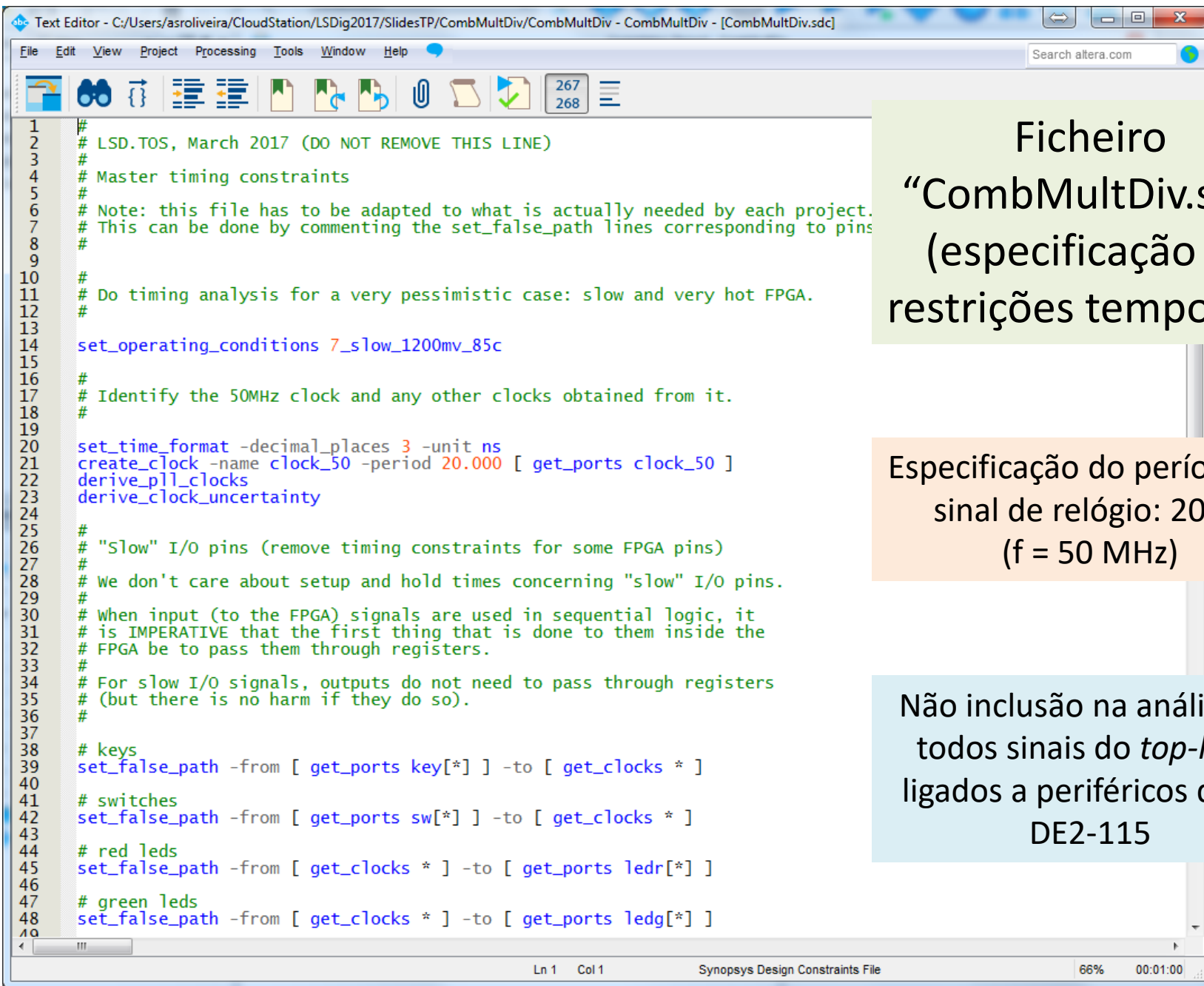
# Análise Temporal

- Questões
  - Como podemos saber se um determinado sistema pode operar com um sinal de relógio com uma dada frequência?
  - Como determinar a frequência máxima de funcionamento de um sistema?
- Resposta
  - Especificar restrições temporais e realizar a análise temporal após a implementação (compilação) do sistema
- Pressupostos e simplificações consideradas em LSDig
  - Todo o sistema opera com um único sinal de relógio
  - Todas as entradas e saídas do sistema (*top-level*) são registadas
  - Os *timings* (incluindo os tempos de *setup* e de *hold*) dos sinais de entrada e saída externos (*top-level*) são ignorados – simplificação útil, embora questionável e só possível devido à natureza dos sinais de interface com os periféricos do *kit* DE2-115

# Estrutura Conceptual do Sistema e Caminho Crítico



- Todo o sistema opera com um único sinal de relógio
- Todas as entradas e saídas do sistema (*top-level*) são registadas
- Os *timings* (incluindo os tempos de *setup* e de *hold*) dos sinais de entrada e saída externos (*top-level*) são ignorados



```
1 #
2 # LSD.TOS, March 2017 (DO NOT REMOVE THIS LINE)
3 #
4 # Master timing constraints
5 #
6 # Note: this file has to be adapted to what is actually needed by each project.
7 # This can be done by commenting the set_false_path lines corresponding to pins
8 #
9
10 #
11 # Do timing analysis for a very pessimistic case: slow and very hot FPGA.
12 #
13
14 set_operating_conditions 7_slow_1200mv_85c
15
16 #
17 # Identify the 50MHz clock and any other clocks obtained from it.
18 #
19
20 set_time_format -decimal_places 3 -unit ns
21 create_clock -name clock_50 -period 20.000 [ get_ports clock_50 ]
22 derive_pll_clocks
23 derive_clock_uncertainty
24
25 #
26 # "slow" I/O pins (remove timing constraints for some FPGA pins)
27 #
28 # We don't care about setup and hold times concerning "slow" I/O pins.
29 #
30 # When input (to the FPGA) signals are used in sequential logic, it
31 # is IMPERATIVE that the first thing that is done to them inside the
32 # FPGA be to pass them through registers.
33 #
34 # For slow I/O signals, outputs do not need to pass through registers
35 # (but there is no harm if they do so).
36 #
37
38 # keys
39 set_false_path -from [ get_ports key[*] ] -to [ get_clocks * ]
40
41 # switches
42 set_false_path -from [ get_ports sw[*] ] -to [ get_clocks * ]
43
44 # red leds
45 set_false_path -from [ get_clocks * ] -to [ get_ports ledr[*] ]
46
47 # green leds
48 set_false_path -from [ get_clocks * ] -to [ get_ports ledg[*] ]
49
50
```

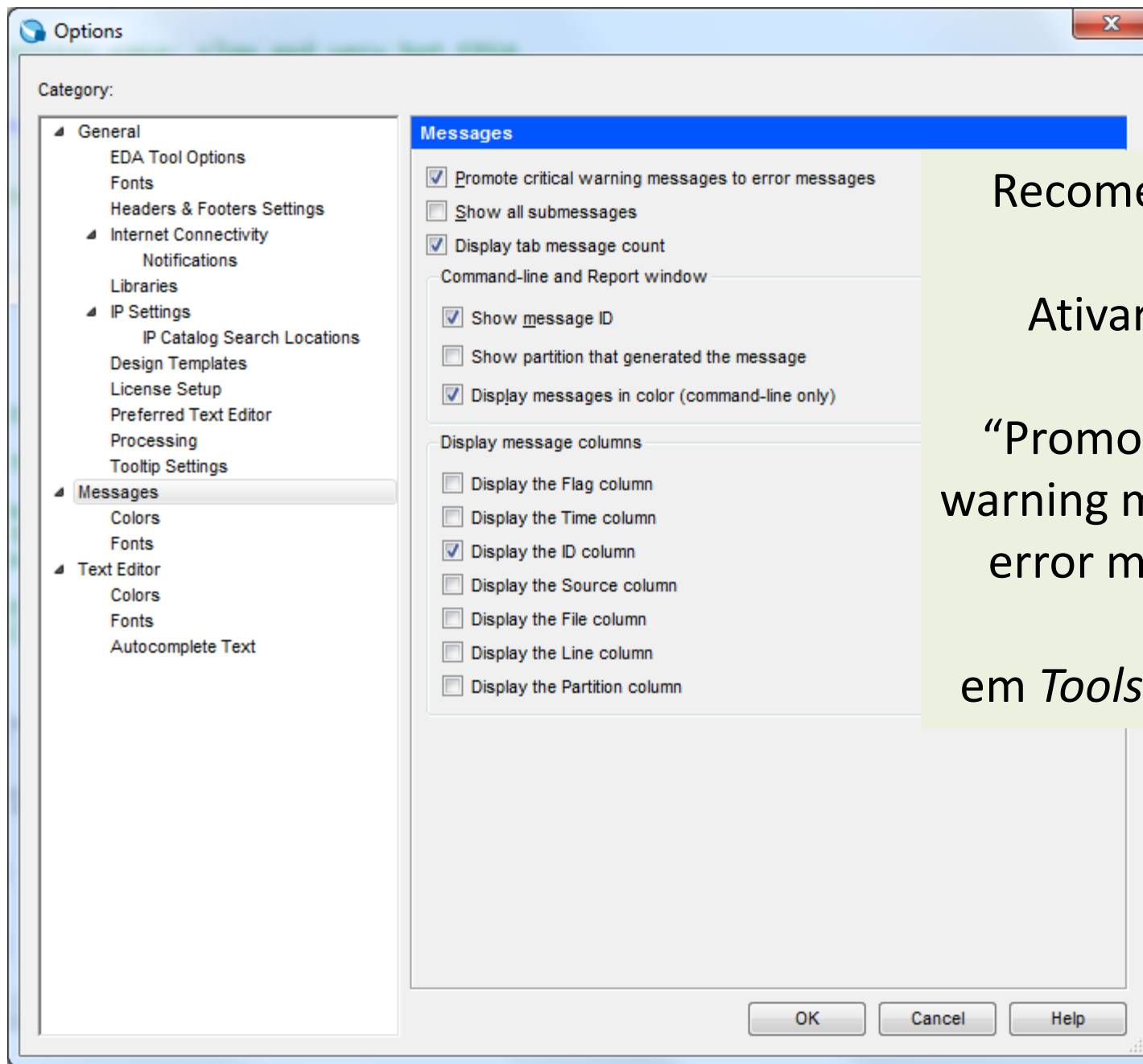
Ficheiro  
“CombMultDiv.sdc”  
(especificação de  
restrições temporais)

Especificação do período do  
sinal de relógio: 20 ns  
(f = 50 MHz)

Não inclusão na análise de  
todos sinais do *top-level*  
ligados a periféricos do kit  
DE2-115







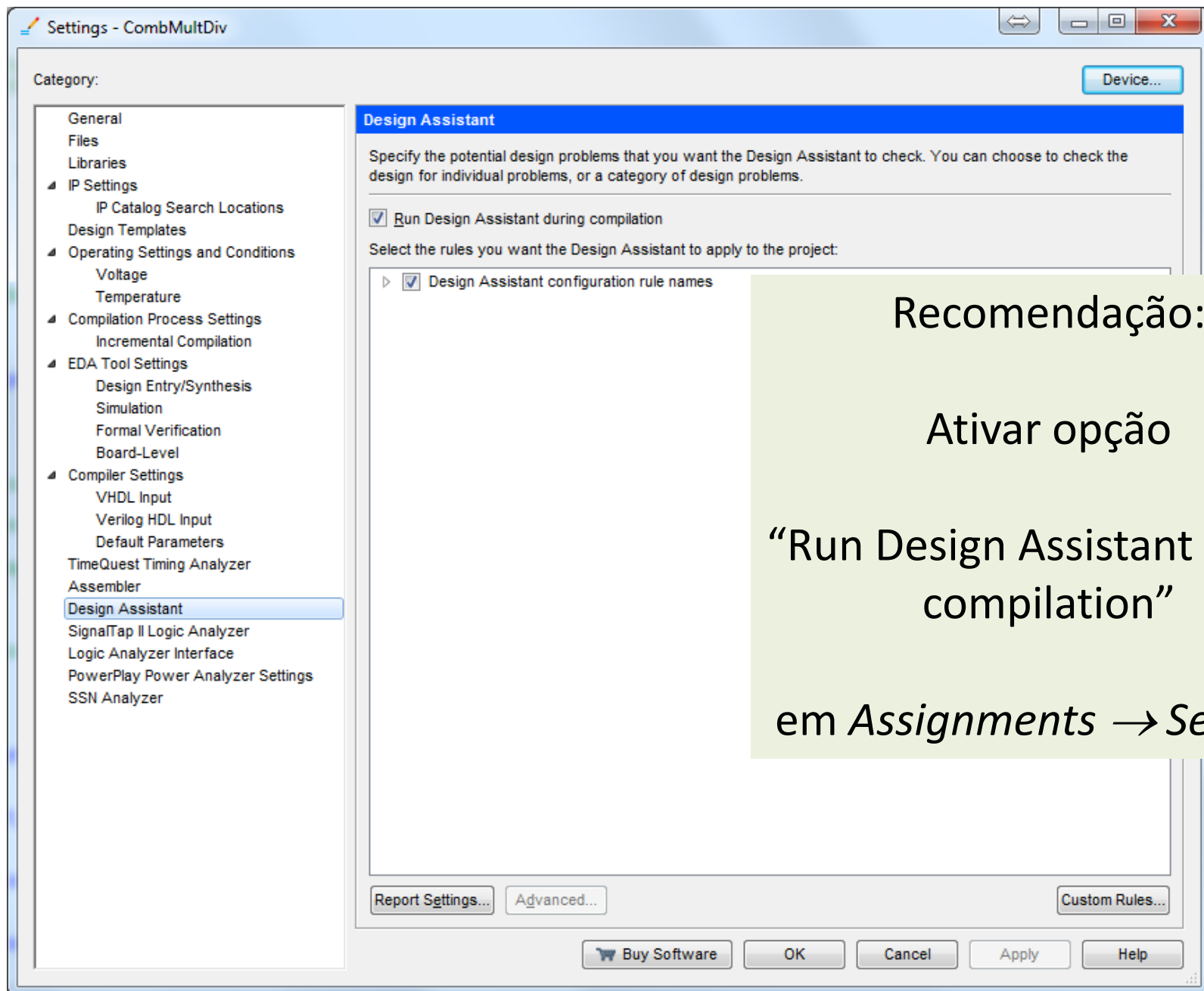
Recomendação:

Ativar opção

“Promote critical  
warning messages to  
error messages”

em *Tools* → *Options*





Recomendação:

Ativar opção

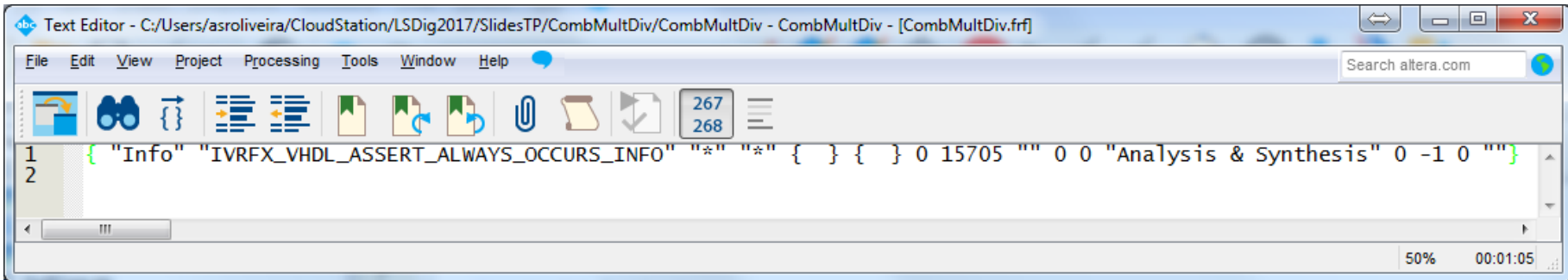
“Run Design Assistant during compilation”

em *Assignments* → *Settings*



# Ficheiros FRF e SRF

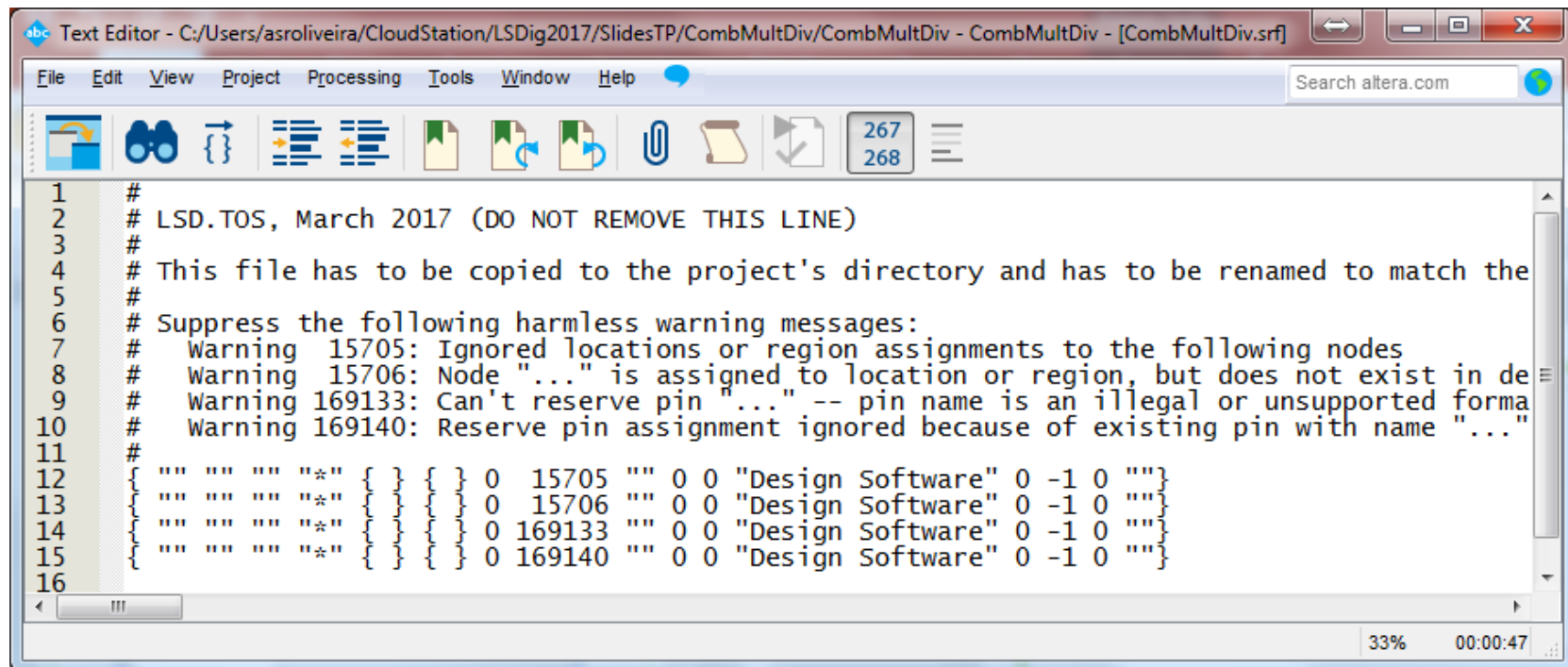
## (supressão seletiva de *warnings*)



Text Editor - C:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/CombMultDiv - CombMultDiv - [CombMultDiv.frf]

```
1 { "Info" "IVRFX_VHDL_ASSERT_ALWAYS_OCCURS_INFO" "*" "*" { } { } 0 15705 "" 0 0 "Analysis & Synthesis" 0 -1 0 "" }
```

50% 00:01:05



Text Editor - C:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/CombMultDiv - CombMultDiv - [CombMultDiv.frf]

```
1 #
2 # LSD.TOS, March 2017 (DO NOT REMOVE THIS LINE)
3 #
4 # This file has to be copied to the project's directory and has to be renamed to match the
5 #
6 # Suppress the following harmless warning messages:
7 #   Warning 15705: Ignored locations or region assignments to the following nodes
8 #   Warning 15706: Node "..." is assigned to location or region, but does not exist in de
9 #   Warning 169133: Can't reserve pin "..." -- pin name is an illegal or unsupported forma
10 #   Warning 169140: Reserve pin assignment ignored because of existing pin with name "..."
11 #
12 { "" "" "" "*" { } { } 0 15705 "" 0 0 "Design Software" 0 -1 0 "" }
13 { "" "" "" "*" { } { } 0 15706 "" 0 0 "Design Software" 0 -1 0 "" }
14 { "" "" "" "*" { } { } 0 169133 "" 0 0 "Design Software" 0 -1 0 "" }
15 { "" "" "" "*" { } { } 0 169140 "" 0 0 "Design Software" 0 -1 0 "" }
16 }
```

33% 00:00:47

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CombMultDiv

Project Navigator

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- CombMultDiv.frf
- CombMultDiv.vhd

Tasks

Compilation

- Task
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- Design Assistant (Post-Fitting)
- Assembler (Generate programming)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Compilation Report - CombMultDiv

CombMultDiv.vhd

CombMultDiv.sdc\*

267  
268

```

1 #
2 # LSD.TOS, March 2017 (DO NOT REMOVE THIS LINE)
3 #
4 # Master timing constraints
5 #
6 # Note: this file has to be adapted to what is actually needed b
7 # This can be done by commenting the set_false_path lines corres
8 #
9 #
10 #
11 # Do timing analysis for a very pessimistic case: slow and very
12 #
13 set_operating_conditions 7_slow_1200mv_85c
14
15 #
16 # Identify the 50MHz clock and any other clocks obtained from it
17 #
18
19
20 set_time_format -decimal_places 3 -unit ns
21 create_clock -name clock_50 -period 10.000 [ get_ports clock_50 ]
22 derive_pll_clocks
23 derive_clock_uncertainty
24
25 #
26 # "slow" I/O pins (remove timing constraints for some FPGA pins)
27 #
28 # We don't care about setup and hold times concerning "slow" I/O pins.
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30 # When input (to the FPGA) signals are used in sequential logic, it
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32 # FPGA be to pass them through registers.
33 #
34 # For slow I/O signals, outputs do not need to pass through registers
35 # (but there is no harm if they do so).
36 #
37
38 # keys
39 set_false_path -from [ get_ports key[*] ] -to [ get_clocks * ]
40
41 # switches
42 set_false_path -from [ get_ports sw[*] ] -to [ get_clocks * ]

```

Messages

All Find... Find Next

Type ID Message

Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 0 warnings

System Processing (235)

Ln 21 Col 43 Synopsys Design Constraints File 100% 00:00:05

Será que o projeto funciona com um sinal de relógio de 100 MHz?

The screenshot shows the TimeQuest Timing Analyzer interface. The 'Set Operating Conditions' panel on the left has 'Slow 1200mV 85C Model' selected. The 'Report' panel shows a tree structure with 'Summary (Setup)' expanded, and 'Slow 1200mV 85C Model' selected. The 'Tasks' panel shows a list of tasks, with 'Report Setup Summary' checked. The 'Console' panel at the bottom shows the command `tcl> create_timing_summary -setup -panel_name "summary (setup)" -multi_corner` and a red error message: `promoted from critical warning: Timing requirements not met`.

**Slow 1200mV 85C Model**

	Clock	Slack	End Point TNS
1	clock_50	-6.685	-63.247

**Report**

- TimeQuest Timing Analyzer Summary
- Advanced I/O Timing
- SDC File List
- Summary (Setup)
  - Slow 1200mV 85C Model
  - Slow 1200mV 0C Model
  - Fast 1200mV 0C Model

**Tasks**

- Open Project...
- Netlist Setup
- Create Timing Netlist
- Read SDC File
- Update Timing Netlist
- Reset Design
- Set Operating Conditions...
- Reports
  - Slack
    - Report Setup Summary
    - Report Hold Summary
    - Report Recovery Summary

**Console**

```
tcl> create_timing_summary -setup -panel_name "summary (setup)" -multi_corner
promoted from critical warning: Timing requirements not met
tcl>
```

0% 00:00:00 Ready

## NÃO!

Com um sinal de relógio com um período de 10 ns, a folga (*slack*) é negativa (-6,685 ns). Assim, o período mínimo do sinal de relógio é cerca de  $10 + 16,685 = 16,685$  ns ( $f_{\max} = 59,9$  MHz)

$$(T_{\min} = T_{\text{especificadoSDC}} - T_{\text{slack}})$$

(análise realizada pela ferramenta “TimeQuest Timing Analyser”, disponível no menu *Tools*, após a implementação/compilação do projeto)

# Caminho Crítico e Frequência Máxima

TimeQuest Timing Analyzer - C:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/CombMultDiv - CombMultDiv

File View Netlist Constraints Reports Script Tools Window Help

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Set Operating Conditions

- ☒ Slow 1200mV 85C Model
- ☐ Slow 1200mV 0C Model
- ☐ Fast 1200mV 0C Model

Report

- DDR
- Summary (Metastability)
- Clock Summary Tree
- Clock Transfers
- Unconstrained Paths
- SDC Assignments

Tasks

- Report Timing Closure Recommendation
- Macros
  - Report All Summaries
  - ☒ Report Top Failing Paths
  - Report All IO Timings
  - Report All Core Timings
  - Create All Clock Histograms
- Write SDC File...

Slow 1200mV 85C Model

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-6.685	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	17.024
2	-6.657	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.997
3	-6.644	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.983
4	-6.638	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.977
5	-6.619	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.958
6	-6.616	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.956
7	-6.610	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.950
8	-6.606	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.945
9	-6.597	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.936
10	-6.591	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.931
11	-6.587	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.926
12	-6.578	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.917
13	-6.578	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.918
14	-6.578	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.917
15	-6.575	s_sw[10]~_Duplicate_1	LEDR[8]~reg0	clock_50	clock_50	10.000	0.342	16.915
16	-6.572	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.911
17	-6.569	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.909
18	-6.568	s_sw[10]~_Duplicate_1	LEDR[10]~reg0	clock_50	clock_50	10.000	0.342	16.908
19	-6.565	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.904
20	-6.563	s_sw[10]~_Duplicate_1	LEDR[11]~reg0	clock_50	clock_50	10.000	0.342	16.903
21	-6.560	s_sw[10]~_Duplicate_1	LEDR[9]~reg0	clock_50	clock_50	10.000	0.342	16.900
22	-6.559	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.899
23	-6.550	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.890
24	-6.550	s_sw[14]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.342	16.890
25	-6.547	s_sw[14]~_Duplicate_1	LEDR[8]~reg0	clock_50	clock_50	10.000	0.343	16.888
26	-6.546	s_sw[10]~_Duplicate_1	LEDR[13]~reg0	clock_50	clock_50	10.000	0.341	16.885

No fmax paths to report  
No fmax paths to report

tcl>

Console History

0% 00:00:00 Ready

```
abc Text Editor - C:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/CombMultDiv - CombMultDiv - [CombMultDiv.vhd]
File Edit View Project Processing Tools Window Help Search altera.com
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.all;
3 use IEEE.NUMERIC_STD.all;
4
5 entity CombMultDiv is
6 port(CLOCK_50 : in std_logic;
7      SW : in std_logic_vector(17 downto 0);
8      LEDR : out std_logic_vector(15 downto 0));
9 end CombMultDiv;
10
11 architecture Behavioral of CombMultDiv is
12
13     signal s_sw : std_logic_vector(17 downto 0);
14     signal s_multResult : std_logic_vector(15 downto 0);
15     signal s_divQuotient : std_logic_vector(7 downto 0);
16     signal s_divRemainder : std_logic_vector(7 downto 0);
17
18 begin
19     process(CLOCK_50)
20     begin
21         if (rising_edge(CLOCK_50)) then
22             s_sw <= SW;
23         end if;
24     end process;
25
26     s_multResult <= std_logic_vector(unsigned(s_sw(7 downto 0)) * unsigned(s_sw(15 downto 8)));
27
28     --s_divQuotient <= std_logic_vector(unsigned(s_sw(7 downto 0)) / unsigned(s_sw(15 downto 8)));
29     --s_divRemainder <= std_logic_vector(unsigned(s_sw(7 downto 0)) rem unsigned(s_sw(15 downto 8)));
30
31     process(CLOCK_50)
32     begin
33         if (rising_edge(CLOCK_50)) then
34             if (s_sw(17) = '1') then
35                 LEDR <= s_multResult;
36             else
37                 LEDR <= s_divRemainder & s_divQuotient;
38             end if;
39         end if;
40     end process;
41 end Behavioral;
42
```

E se o projeto incluir apenas o multiplicador (isto é, se o divisor for removido), qual o período mínimo/frequência máxima do sinal de relógio?



TimeQuest Timing Analyzer - C:/Users/asroliveira/CloudStation/LSDig2017/SlidesTP/CombMultDiv/CombMultDiv - CombMultDiv

File View Netlist Constraints Reports Script Tools Window Help

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Set Operating Conditions

☒ Slow 1200mV 85C Model  
☐ Slow 1200mV 0C Model  
☐ Fast 1200mV 0C Model

Report

TimeQuest Timing Analyzer Summary

Advanced I/O Timing

SDC File List

Summary (Setup)

Slow 1200mV 85C Model

Slow 1200mV 0C Model

Fast 1200mV 0C Model

Tasks

Open Project...

Netlist Setup

Create Timing Netlist

Read SDC File

Update Timing Netlist

Reset Design

Set Operating Conditions...

Reports

Slack

Report Setup Summary

Report Hold Summary

Report Recovery Summary

Deriving Clock Uncertainty. Please refer to report\_sdc in TimeQuest to see clock uncertainties.

tcl> create\_timing\_summary -setup -panel\_name "summary (setup)" -multi\_corner

tcl>

Console History

100% 00:01:16 Ready

	Clock	Slack	End Point TNS
1	clock_50	6.933	0.000

Resposta: 3,067 ns

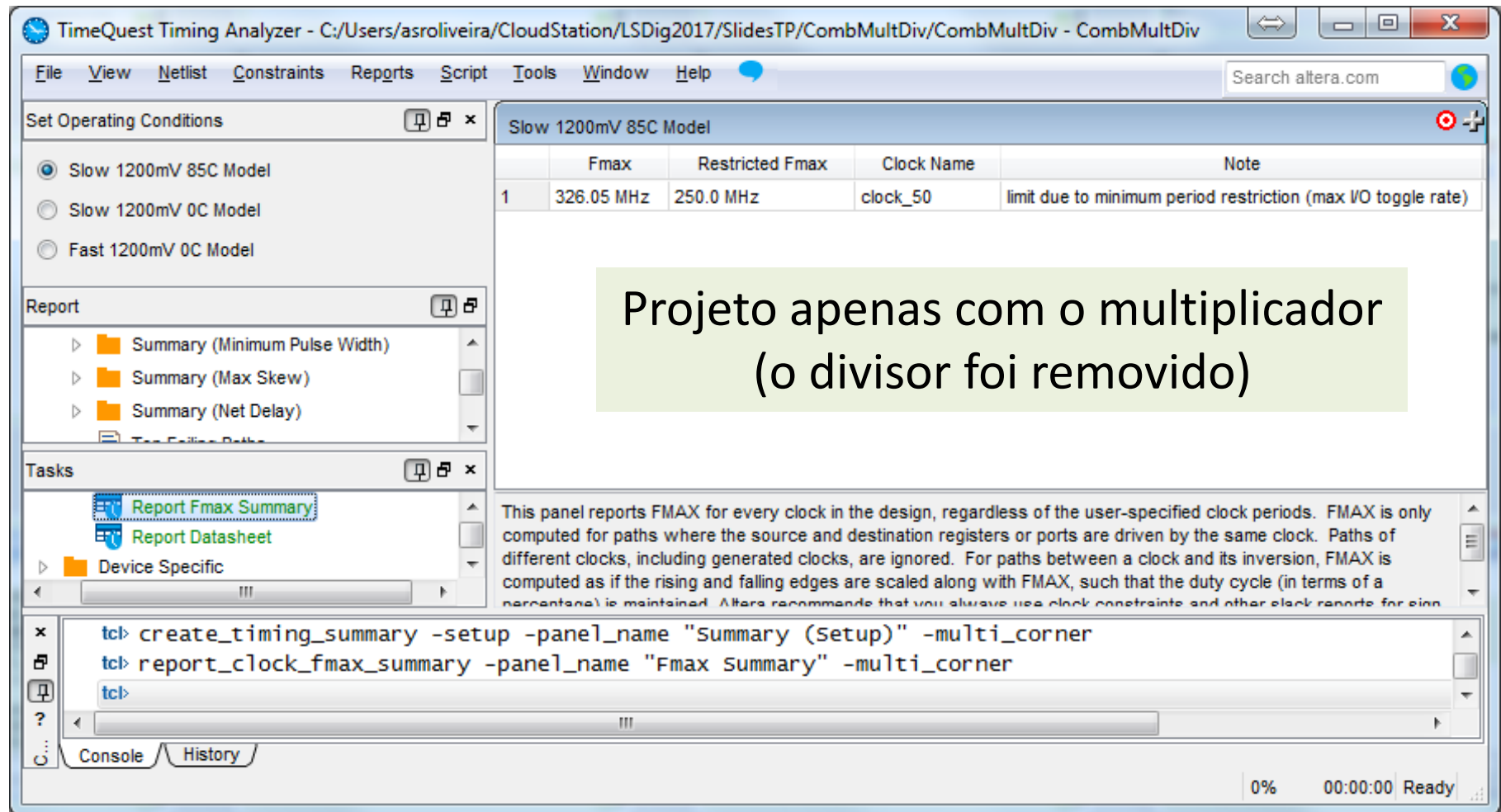
$$T_{\min} = T_{\text{especificadoSDC}} - T_{\text{slack}} = 10 - 6,933 = 3,067 \text{ ns}$$

( $f_{\max} = 326 \text{ MHz}$ )

Projeto apenas com o multiplicador  
(o divisor foi removido)



# Caminho Crítico e Frequência Máxima



The screenshot shows the TimeQuest Timing Analyzer interface. The 'Set Operating Conditions' panel on the left has 'Slow 1200mV 85C Model' selected. The 'Report' panel shows a tree structure with 'Summary (Minimum Pulse Width)', 'Summary (Max Skew)', and 'Summary (Net Delay)'. The 'Tasks' panel has 'Report Fmax Summary' and 'Report Datasheet' highlighted. The main window displays a table titled 'Slow 1200mV 85C Model' with the following data:

	Fmax	Restricted Fmax	Clock Name	Note
1	326.05 MHz	250.0 MHz	clock_50	limit due to minimum period restriction (max I/O toggle rate)

A green text box is overlaid on the table with the text: 'Projeto apenas com o multiplicador (o divisor foi removido)'.

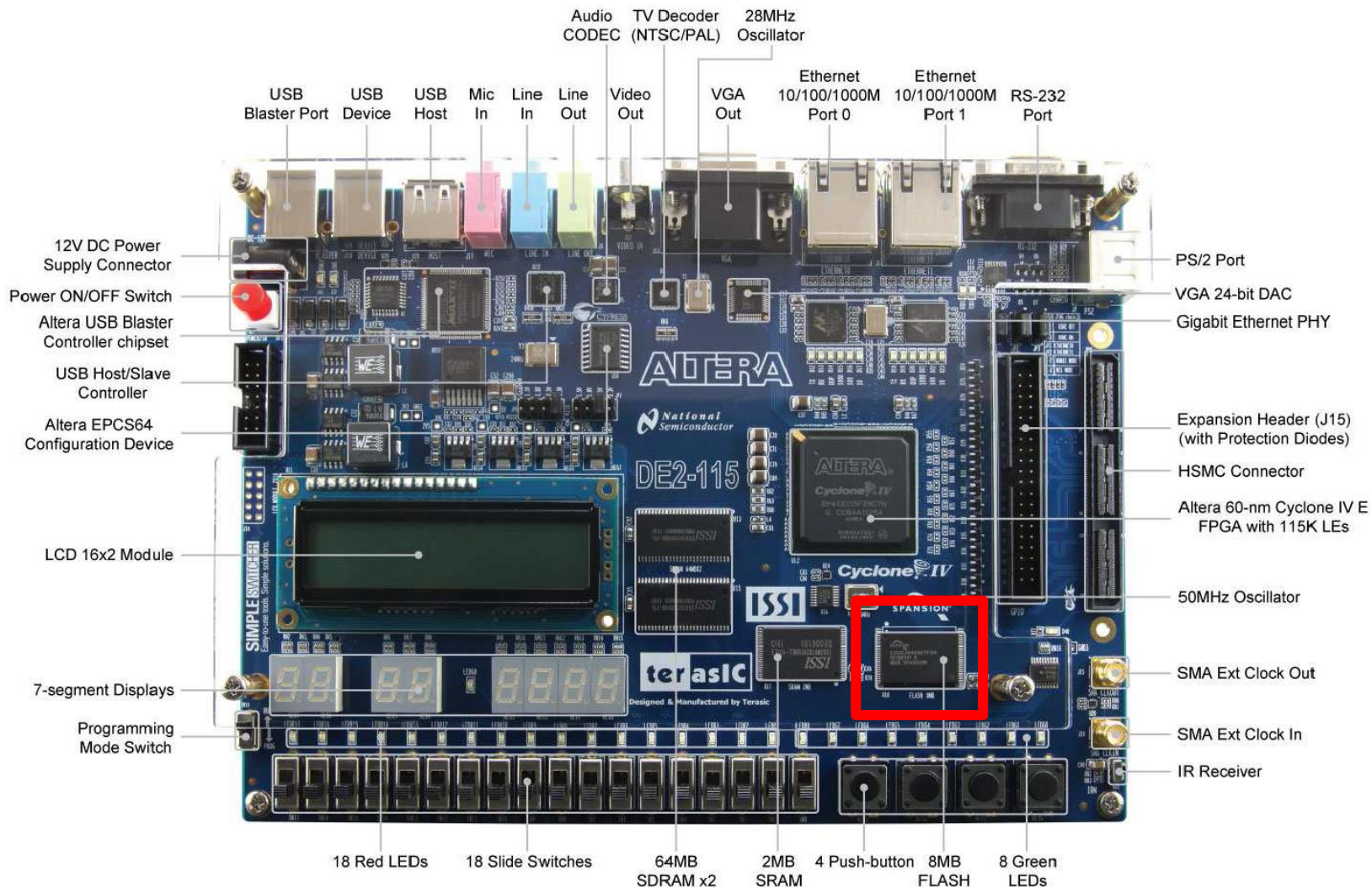
Below the table, a descriptive paragraph states: 'This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other clock reports for sign'.

The bottom console shows the following Tcl commands:

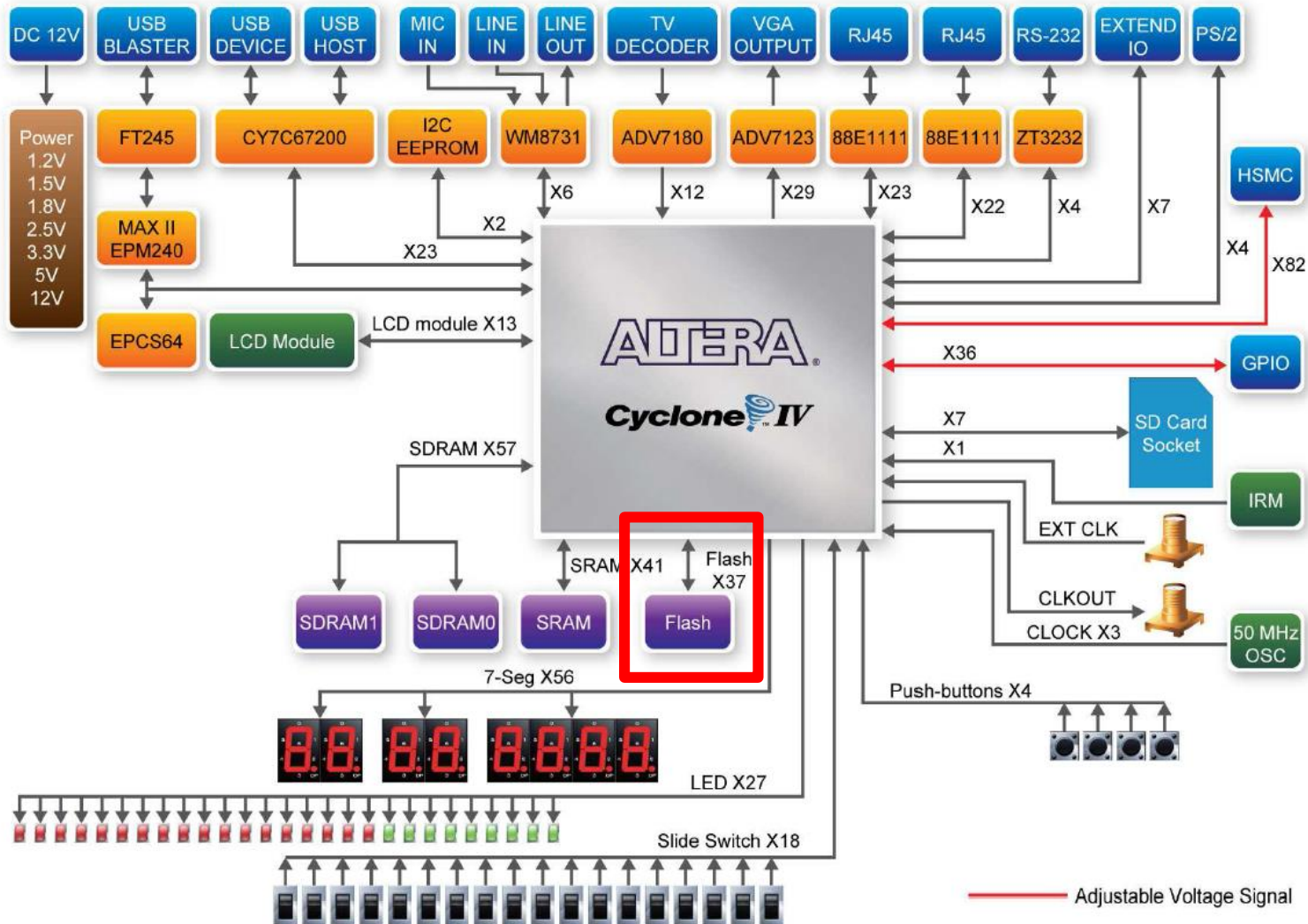
```
tcl> create_timing_summary -setup -panel_name "Summary (Setup)" -multi_corner
tcl> report_clock_fmax_summary -panel_name "Fmax Summary" -multi_corner
tcl>
```

The status bar at the bottom right shows '0%' completion, '00:00:00' time, and 'Ready' status.

# Como Armazenar a Configuração da FPGA de Forma Não Volátil no *Kit*?



# Memória FLASH (usada para armazenar a configuração de fábrica)



# Cadeia (*Chain*) JTAG do Kit DE2-115

- Interface JTAG (*Joint Test Action Group*)
  - Interface série para programação e teste (TDI, TDO – dados; TCK – clock; TMS - controlo)
  - Permite ligar dispositivos em cascata
- Usada no kit DE2-115 com “Quartus Prime” para
  - Programação da FPGA (com “Programmer”) e depuração (com “SignalTap II Logic Analyser”)
  - Programação da memória FLASH do kit (com “Programmer”)

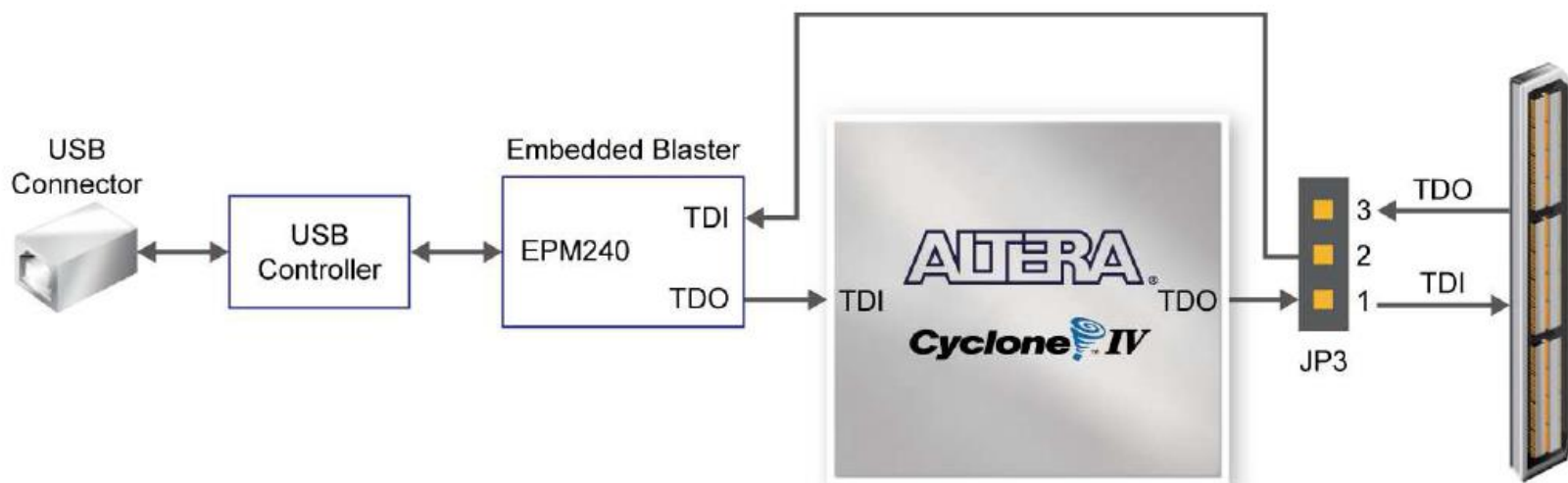


Figure 4-1 The JTAG chain on DE2-115 board



# Programação da FPGA / Depuração

- “USB Blaster Circuit” comporta-se como uma *gateway* entre USB e a interface JTAG da FPGA
- Interruptor deve estar em modo “RUN”
  - Arranque normal do sistema
- “Quartus Programmer” deve usar o modo “JTAG”

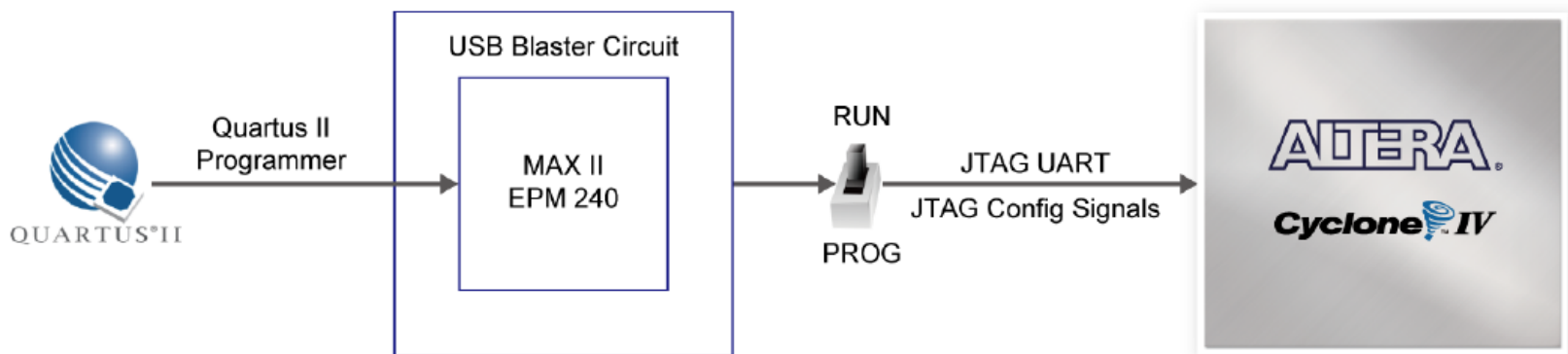


Figure 4-3 The JTAG configuration scheme

# Programação da Memória FLASH do *Kit*

- “USB Blaster Circuit” comporta-se como uma *gateway* entre USB e a interface de programação da FLASH
- Interruptor deve estar em modo “PROG”
- “Quartus Programmer” deve usar o modo “Active Serial Programming”

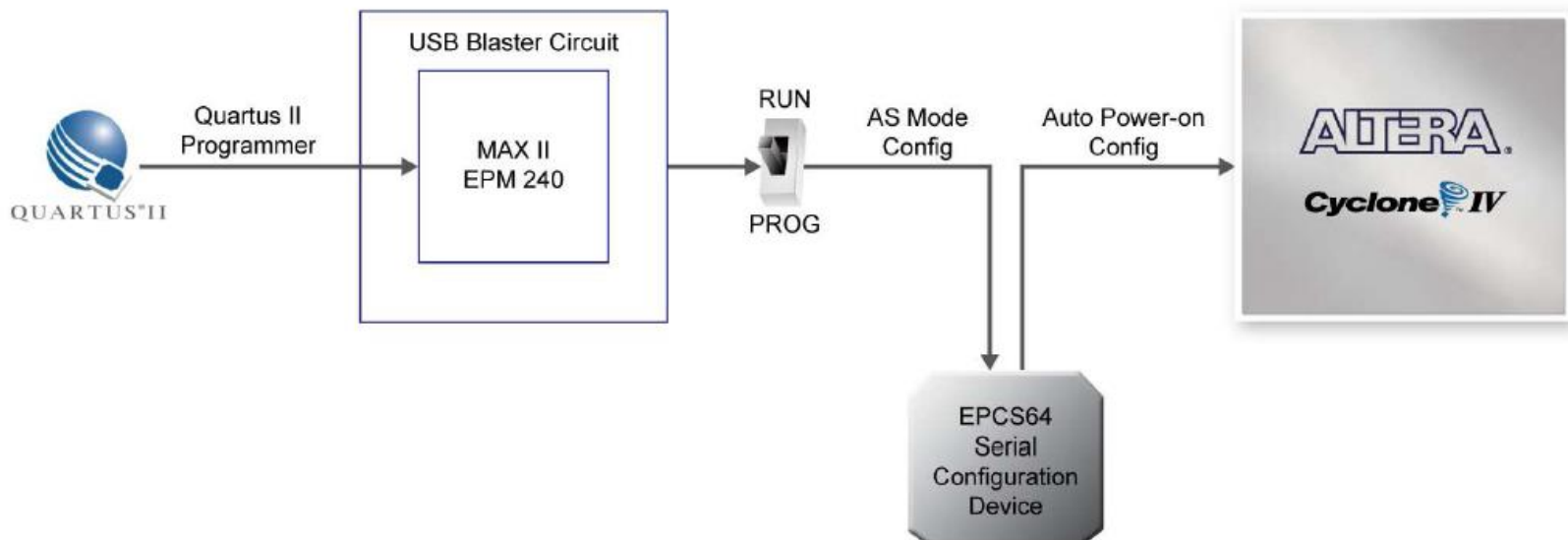


Figure 4-5 The AS configuration scheme

Quartus II 64-Bit - D:/Desktop/LSDig/DebugDemo/DebugDemo - DebugDemo

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

gDemo

CntUp.vhd x DebugDemo.vhd x Compilation Report - DebugDemo x

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- TimeQuest Timing Analyzer
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

Flow Status Successful - Sat May 10 00:25:10 2014

Quartus II 64-Bit Version 13.1.2 Build 173 01/15/2014 SJ Full Version

Revision Name DebugDemo

Top-level Entity Name DebugDemo

Family Cyclone IV E

Device EP4CE115F29C7

Timing Models Final

Total logic elements 1,034 / 114,480 (< 1 %)

Total combinational functions 610 / 114,480 (< 1 %)

Dedicated logic registers 870 / 114,480 (< 1 %)

Total registers 890

Total pins 21 / 529 (4 %)

Total virtual pins 0

Total memory bits 131,072 / 3,981,312 (3 %)

Embedded Multiplier 9-bit elements 0 / 532 (0 %)

Total PLLs 0 / 4 (0 %)

Messages

Type ID Message

- Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
- 293000 Quartus II Full Compilation was successful. 0 errors, 533 warnings

System (153) Processing (143)

Combines and/or converts programming files into other programming file formats 100% 00:00:54

Criação do ficheiro para  
programação da memória FLASH  
(.POF) a partir do ficheiro .SOF



# Criação do ficheiro para programação da memória FLASH (.POF) a partir do ficheiro .SOF

Convert Programming File - D:/Desktop/LSDig/DebugDemo/Debu

File Tools Window

Specify the input files to convert and the type of programming file to generate.  
You can also import input file information from other files and save the conversion setup inform future use.

Conversion setup files

Open Conversion Setup Data... Save Conversion Setup...

Output programming file

Programming file type: Programmer Object File (.pof)

Options... Configuration device: EPCS64 Mode: Active Serial

File name: output\_files/DebugDemo.pof

Advanced... Remote/Local update difference file: NONE

☒ Create Memory Map File (Generate DebugDemo.map)

☐ Create CvP files (Generate DebugDemo.periph.pof and DebugDemo.core.rbf)

☐ Create config data RPD (Generate DebugDemo\_auto.rpd)

Input files to convert

File/Data area	Properties	Start Address
SOE Data	Page_0	<auto>
DebugDemo.sof	EP4CE115F29	

Add Hex Data

Add Sof Page

Add File...

Remove

Up

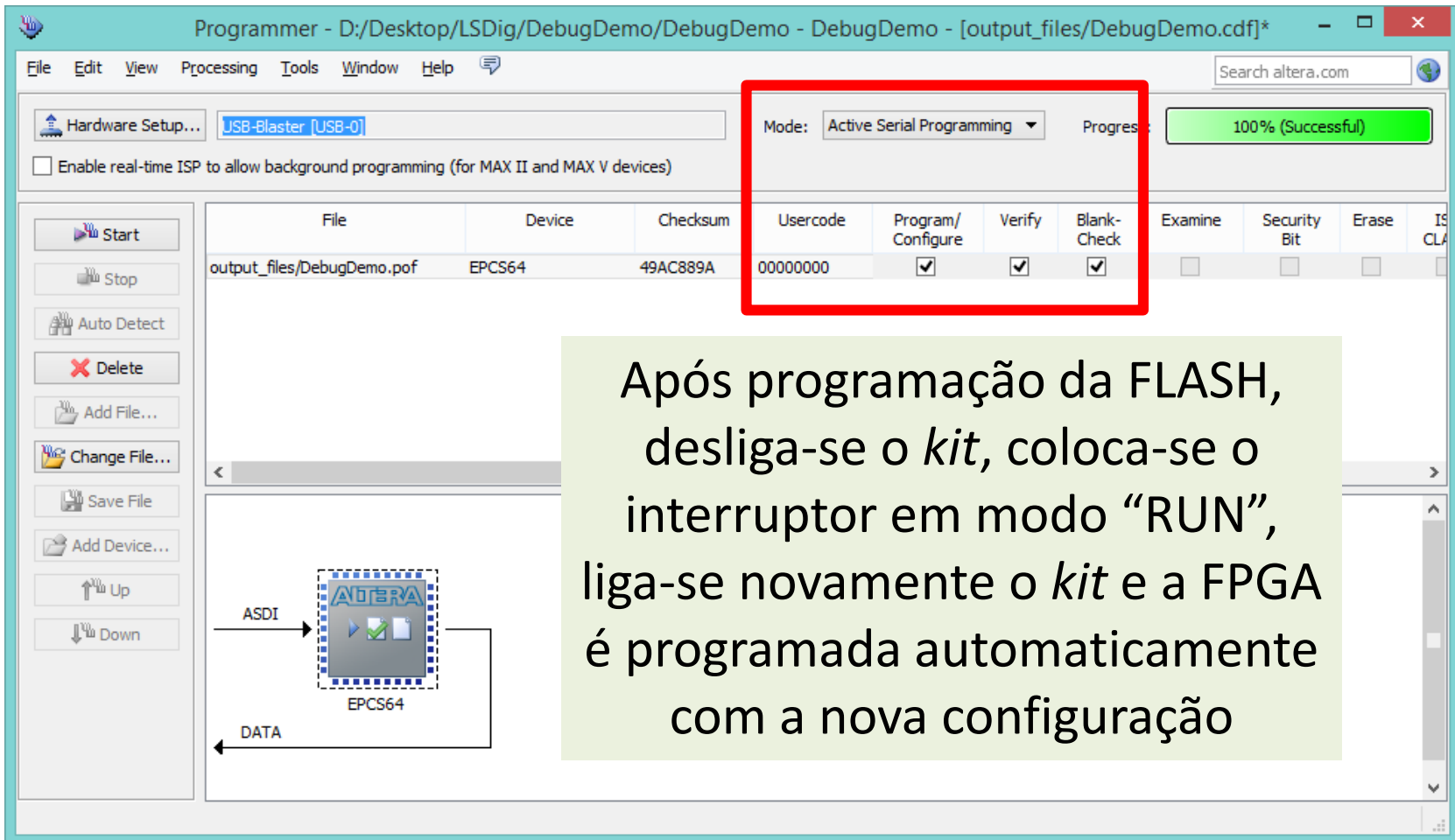
Down

Properties

Generate Close Help



# Programação da Memória FLASH com o Ficheiro .POF



The screenshot shows the Altera Programmer application window. The title bar indicates the path: D:/Desktop/LSDig/DebugDemo/DebugDemo - DebugDemo - [output\_files/DebugDemo.cdf]\*. The menu bar includes File, Edit, View, Processing, Tools, Window, and Help. The Hardware Setup dropdown is set to USB-Blaster [USB-0]. A checkbox for 'Enable real-time ISP to allow background programming (for MAX II and MAX V devices)' is unchecked. The Mode is set to 'Active Serial Programming'. The Progress bar shows '100% (Successful)'. A table lists the programming details:

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	IS
output_files/DebugDemo.pof	EPCS64	49AC889A	00000000	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	CL

Below the table, a diagram shows the ASDI connection to the EPCS64 device, with DATA lines indicated.

Após programação da FLASH, desliga-se o *kit*, coloca-se o interruptor em modo “RUN”, liga-se novamente o *kit* e a FPGA é programada automaticamente com a nova configuração

# Comentários Finais

- No final desta aula deverá ser capaz de:
  - Analisar os relatórios de implementação com os tipos e quantidades dos recursos da FPGA utilizados num dado projeto
  - Especificar restrições temporais para circuitos simples
  - Realizar análises temporais simples com a ferramenta “TimeQuest Timing Analyser”
  - Conhecer as funcionalidades da interface JTAG e saber usá-la para efeitos de programação de dispositivos (FPGA e memória FLASH) e depuração dos circuitos implementados na FPGA