

# MARC NEU

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## PROFESSIONAL SUMMARY

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Digital Systems Engineer with experience in real-time data processing on FPGA and SoC platforms. Skilled in implementing machine learning models using efficient pipelined architectures and familiar with CGRA concepts, state-of-the-art FPGAs, and hardware software co-design. Published researcher with practical experience in System Verilog, Python, digital signal processing, high-speed interfaces, verification, prototyping, and laboratory measurements.

## PROFESSIONAL EXPERIENCE

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### PhD Candidate 2022 – 2026

*Institute for Information Processing Technologies, Karlsruhe Institute of Technology (KIT), Karlsruhe*

- Designed, implemented, and commissioned an FPGA-based Graph Neural Network (GNN) module for the Belle II electromagnetic calorimeter, achieving a sustained throughput of 8 million frames per second with sub-microsecond latency.
- Developed deployment strategies for hardware-accelerated Graph Neural Networks (GNNs) and Point Cloud Networks (PCNs) tailored to large-scale scientific experiments.

### Research Assistant 2020 – 2021

*Institute for Information Processing Technologies & Institute of Radio Frequency Engineering, Karlsruhe*

- Designed and verified digital memory module with PCI-E for the Tandem-L satellite project
- Simulated broadband bondwire transitions at 240 GHz
- PCB layouts and simulations for high-frequency applications

### Working Student in Application Engineering 2019 – 2020

*Infineon Technologies AG, Munich*

- Performed circuit simulations in PSpice for power electronics applications
- Compared concepts for interfacing IGBT gate drivers and with Infineon power management ICs

### Intern in Hardware and Logic Engineering 2019

*Airbus Defence and Space, Ottobrunn*

- Contributed to a proof-of-concept development for a novel atomic clock
- Completed Bachelor thesis in cooperation with Karlsruhe Institute of Technology

## EDUCATION

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### M.Sc. Electrical Engineering and Information Technology 2019 – 2022

*Grade 1.1, Karlsruhe Institute of Technology (KIT), Karlsruhe*

*Thesis: Design and evaluation of a Track Segment Finder for the Belle II particle accelerator based on machine learning methodology*

### B.Sc. Electrical Engineering and Information Technology 2016 – 2019

*Grade 1.7, Karlsruhe Institute of Technology (KIT), Karlsruhe*

*Thesis: Design of a digital controller for a novel atomic clock*

### General Abitur 2015

*Grade 1.6, Bildungszentrum Markdorf Gymnasium, Markdorf*

## SELECTED PUBLICATIONS

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- M. Neu**, I. Haide, T. Justinger, T. Rädler, V. Dajaku, T. Ferber, J. Becker, "Real-Time Graph-based Point Cloud Networks on FPGAs via Stall-Free Deep Pipelining", in *Proc. IEEE SBCCI*, Manaus, Brazil, 2025.
- M. Neu**, C. Karle, P. Schmidt, J. Höfer, T. Harbaum, J. Becker, "A Dynamically Pipelined Dataflow Architecture for Graph Convolutions in Real-Time Event Interpretation," in *Proc. IEEE SOCC*, Dresden, Germany, 2024.
- M. Neu**, J. Becker, P. Dorwarth et al., "Real-Time Graph Building on FPGAs for Machine Learning Trigger Applications in Particle Physics," *Computing and Software for Big Science*, vol. 8, no. 8, 2024.
- M. Neu**, C. Karle, B. Nuss, P. Groeschl, J. Becker, "A Scalable and Cost-efficient Antenna Testbed using FPGA-Server Compound Structures for Prototyping 6G Applications," in *Proc. IEEE DCOSS-IoT*, Coral Bay, Cyprus, 2023.

## TECHNICAL SKILLS

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### Programming

System Verilog, Python, C++, Scala, Tcl

### Tools & Software

AMD Vivado, AMD Vitis, Cadence Virtuoso, Make, Git, Linux

### Digital System Design

Strong focus on FPGA firmware development with Hard IP Cores such as GT transreceivers, AD converters, or CMACs, Digital Signal Processing (DSP), measurements with oscilloscopes or network analyzers, soldering

## AWARDS & HONORS

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<b>Leadership Talent Academy Scholarship</b> <i>Karl Schlecht Foundation</i>	2021
<b>Germany Scholarship</b> <i>Federal Ministry of Research, Technology and Space</i>	2021
<b>Abitur Prize</b> <i>German Physical Society</i>	2015

## VOLUNTEERING & ADDITIONAL EXPERIENCE

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<b>Student Model Advisor</b> <i>Supported students in their course selection for their study programme</i>	2022 – 2025
<b>Mu-Zero Hyperloop e.V. Member</b> <i>Developed control system concept for a linear motor</i>	2020 – 2021
<b>Academic Tutor</b> <i>Optimization of Dynamic Systems, Linear Electrical Networks, Higher Mathematics II</i>	2017 – 2022
<b>Erasmus Exchange</b> <i>University of Southampton, United Kingdom</i>	2018