COEN 210 Computer Architecture

SAMPLE FINAL EXAM
Closed Books and Notes. Calculator Allowed.

1. True or false: Identify the following statements as either true or false:

( ) MIPS (million instructions per second) performance metric depends on the clock time.

( ) A CISC architecture has a fixed instruction length.

( ) Clock cycles is the only valid and unimpeachable measure of performance.

( ) Control hazards are caused by hardware conflict.

( ) When a cache miss occurs, we move the whole block containing the requested data to cache to take advantage of spatial locality.

2. Fill in the blank with the correct answer:

(1) The CPU time for executing a program is a product of _____, _____, and _____.

(2) The addressing mode of *lw $t0, 1200($t1)* is _____.

(3) Consider a cache with 64 blocks and a block size of 16 bytes. Byte address 1200 maps to _____ block number.

3. For the following multiple-choice questions, circle the correct answers:

(a) In IEEE 754 floating point standard, the number 10000000000110000000000000000000 in single prevision represents:
A. –Infinite
B. A negative denormalized number
C. A negative normalized number
D. NaN (Not a number)
E. None of the above

(b) What is the control logic for the multi-cycle processor implementation?
A. Finite state machine
B. Combinational piece of logic
C. Both A and B
D. None of the above

(c) Which of the following states is the first state of memory reference instructions.
A. Memory address computation.
B. Memory access (read).
C. Memory read completion step.
D. Memory access (write).

(d) The change that replaces the processor in a computer with a faster version to a computer system
A. Increases throughput
B. Decreases response time
C. Both A and B
D. None of the above

4. Here is a series of address references given as word addresses: 1, 14, 5, 8, 5, 11, 5, 76. Assuming a 16 word direct cache with block size =4 that is initially empty, label each reference in the list as a hit or miss and show the final contents of the cache:

Reference:	Binary	Cache index	Miss or hit
1			
14			
5			
8			
5			
11			
5			
76			

Reference List

Index	V	Tag	D0	D1	D2	D3
00						
01						
10						
11						

Cache Structure

5. Consider the attached pipelined datapath and control. Suppose in the gcc program, 45% load word instructions have data dependence with their following R-type instructions, 95% branch instructions take the branch. Also we assume that memories in the attached pipeline are caches, instruction cache miss ratio is 3%, data cache miss ratio is 5%, miss penalty is 40 cycles, and TLB/virtual memory miss ratios are zero.

a) What is the average number of penalty cycles per instruction due to cache miss using the instruction mix below?

	loads	store	R-type	branch	jumps
gcc	20%	12%	48%	18%	2%