EXERCISES ON PERFORMANCE EVALUATION

Exercise 1

A program is executed for 1 sec, on a processor with a clock cycle of 50 nsec and **Throughput$_1$** = 15 MIPS.

1. How much is the **CPI$_1$**, for the program?

Solution:

T_{CLOCK}= 50 nsec ⇒ $f_{CLOCK} = 1/T_{CLOCK}$ = 20 MHz

$CPI_1 = f_{CLOCK} / MIPS_1 \, 10^6 = 20 \, 10^6 / 15 \, 10^6 = 1{,}33$

2. Let us assume that, given some optimization techniques, the throughput of the program is optimized. In the new case, the 40% of the program instructions is executed with CPI = 1, while the fraction of remaining instructions (60%) is executed with the same CPI.
   How much is the **SpeedUp** from the case (1) to the case (2)?
   How much is the **Throughput2** expressed in MIPS?

Solution:

$F_E = 0{,}40$

$SpeedUp_E = CPI_1/CPI_E = 1{,}33 / 1 = 1{,}33$

$SpeedUp = 1 / [(1-F_E) + F_E / SpeedUp_E] = 1 / (0{,}6 + 0{,}4 / 1{,}33) = 1{,}11$

$SpeedUp = MIPS_2 / MIPS_1$

$⇒ MIPS_2 = SpeedUp \; MIPS_1 = 1{,}11 * 15 = 16{,}65$

Exercise 2

A program is executed for 1 sec, on a processor with a clock cycle of 100 nsec and $\mathbf{CPI_1}$ = 1,5.

1. How much is the $\mathbf{Throughput_1}$ expressed in MIPS?

Solution:

$\mathbf{T_{CLOCK} = 100\ nsec \Rightarrow f_{CLOCK} = 1/T_{CLOCK} = 10\ MHz}$

$\mathbf{MIPS_1 = f_{CLOCK} / CPI_1\ 10^6 = 10\ 10^6\ /1{,}5\ 10^6 = 6{,}66}$

2. Let us assume that, given some optimization techniques, the 30% of the program instructions is executed with CPI = 1, while the fraction of remaining instructions (70%) is executed with the same CPI.
   How much is the **Throughput** expressed in MIPS?
   How much is the **SpeedUp** from the case (1) to the case (2)?

Solution:

$\mathbf{F_E = 0{,}30}$

$\mathbf{SpeedUp_E = CPI_1/CPI_E = 1{,}5\ /\ 1 = 1{,}5}$

$\mathbf{SpeedUp = 1\ /\ [(1\text{-}F_E) + F_E\ /SpeedUp_E] = 1\ /\ (0{,}7 + 0{,}3\ /\ 1{,}5) = 1{,}11}$

$\mathbf{SpeedUp = MIPS_2\ /MIPS_1}$

$\mathbf{\Rightarrow MIPS_2 = SpeedUp\ MIPS_1 = 1{,}11 * 6{,}66 = 7{,}4}$

Exercise 3

A program is executed for 1 sec, on a processor with a clock cycle of 50 nsec and **Throughput$_1$** = 10 MIPS.

1. How much is the **CPI$_1$**, for the program?

Solution:

T_{CLOCK}= 50 nsec ⇒ $f_{CLOCK} = 1/T_{CLOCK}$ = 20 MHz

$CPI_1 = f_{CLOCK} / MIPS_1\ 10^6 = 20\ 10^6 /10\ 10^6 = 2$

2. Let us assume that, thanks to the introduction of a superscalar processor, the throughput of the program is optimized. In the new case, the 50% of the program instructions is executed with 3 parallel issues, while the fraction of remaining instructions (50%) is executed with one issue.
   How much is the **SpeedUp** from the case (1) to the case (2)?
   How much is the **Throughput$_2$** expressed in MIPS?

Solution:

$F_E = 0{,}50$

$SpeedUp_E = Th_E/Th_1 = 3\ Th_1 / Th_1 = 3$

$SpeedUp = 1 / [(1-F_E) + F_E /SpeedUp_E] = 1 / (0{,}5 + 0{,}5 / 3) = 1{,}5$

$SpeedUp = MIPS_2 /MIPS_1$

⇒ $MIPS_2$ = SpeedUp $MIPS_1$ = 1,5 * 10 = 15

Exercise 4

Let us consider a computer executing the following mix of instructions:

Istruction	Frequency	Clock Cycles
ALU	50	1
LOAD	20	5
STORE	10	3
BRANCH	20	2

1. How much is the ***CPI average (1)*** assuming a clock period of ***5 ns*** ?

   $CPI_1 = CPI_{1\ ave} = 0.5 * 1 + 0.2 * 5 + 0.1 * 3 + 0.2* 2 = 2.2$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(1)***?

   $MIPS_1 = f_{CLOCK} / (CPI_1 * 10^6) = (200 * 10^6) / (2.2 * 10^6) = 90.90$

2. How much is the **SpeedUp** assuming that, introducing an optimized data cache, load instructions require 2 clock cycles?

   $CPI_2 = CPI_{2\ average} = 0.5 * 1 + 0.2 * 2 + 0.1 * 3 + 0.2* 2 = 1.6$

   $Speedup = CPI_1 / CPI_2 = 2{,}2 / 1{,}6 = 1{,}375$

3. How much is the **SpeedUp** assuming that, introducing an optimized branch unit, branch instructions require 1 clock cycles?

   $CPI_3 = CPI_{3\ average} = 0.5 * 1 + 0.2 * 5 + 0.1 * 3 + 0.2* 1 = 2$

   $Speedup = CPI_1 / CPI_3 = 2{,}2 / 2 = 1{,}1$

4. How much is the **SpeedUp** assuming to introduce 2 ALUs working in parallel?

   $CPI_4 = CPI_{4\ average} = 0.5 * 0{,}5 + 0.2 * 5 + 0.1 * 3 + 0.2* 2 = 1{,}95$

   $Speedup = CPI_1 / CPI_4 = 2{,}2 / 1{,}95 = 1{,}13$

5. How much is the **SpeedUp** assuming to introduce all together the above optimizations?

   $CPI_4 = CPI_{4\ average} = 0.5 * 0{,}5 + 0.2 * 2 + 0.1 * 3 + 0.2* 1 = 1{,}15$

   $Speedup = CPI_1 / CPI_4 = 2{,}2 / 1{,}15 = 1{,}91$

Exercise 5

Let us consider a computer executing the following mix of instructions:

Instrcution	Frequency	Clock cycles
ALU	50	1
LOAD	20	4
STORE	10	4
BRANCH	10	2
JUMP	10	2

1. How much is the ***CPI average (1)*** assuming a clock period of ***5 ns*** ?
   $CPI_1 = CPI_{average} = 0.5 * 1 + 0.2 * 4 + 0.1 * 4 + 0.1* 2 + 0.1 * 2 = 2.1$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(1)?***
   $MIPS_1 = f_{CLOCK} / (CPI_1 * 10^6) = (200 * 10^6) / (2.1 * 10^6) = 95.24$

2. Let us assume that, given some opimisation techniques, the clock frequency has been incremented by **25%** and this implies a CPI increment of ALU instructions of **50%** and LOAD instructions of **25%** while the remaining instructions are executed with the same CPI.
   How much is ***CPI average (2)?***
   $CPI_2 = CPI_{average} = 0.5 * 1.5 + 0.2 * 5 + 0.1 * 4 + 0.1* 2 + 0.1 * 2 = 2.55$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(2)?***

   $f_{clock2} = 1{,}25\ f_{clock1} = 250$ MHz
   $MIPS_2 = f_{CLOCK} / (CPI_2 * 10^6) = (250 * 10^6) / (2.55 * 10^6) = 98.04$

3. How much is the ***Speedup from (1) to (2)?***
   Speedup = $MIPS_2$ / $MIPS_1$ = 98,04 / 95,24 = 1,03

   Is it better the case (1) or the case (2)?
   It is better the case (2)

   Notice that the Speedup can also be calculated by comparing the execution times taking into account that: **$T_{clock2} = 0{,}8\ T_{clock1} = 4$ ns:**

   $T_{CPU1} = IC_1\ CPI_1\ T_{clock1} = 100 * 2{,}1 * 5$ ns = 1050 ns
   $T_{CPU2} = IC_2\ CPI_2\ T_{clock2} = 100 * 2{,}55 * 4$ ns = 1020 ns
   Speedup = T_{CPU1} / T_{CPU2} = 1050 / 1020 = 1,03

   Note: It was not possible to calculate the speedup by comparing the CPIs because the clock frequencies were different.

Exercise 6

Let us consider a computer executing the following mix of instructions:

Instruction	Frequency	Clock cycles
ALU	50	1
LOAD	20	4
STORE	10	4
BRANCH	10	2
JUMP	10	2

1. How much is the ***CPI average (1)*** assuming a clock frequency of ***500 MHz?***

   $CPI_1 = CPI_{average} = 0.5 * 1 + 0.2 * 4 + 0.1 * 4 + 0.1* 2 + 0.1 * 2 = 2.1$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(1)?***

   $MIPS_1 = f_{CLOCK} / (CPI_1 * 10^6) = (500 * 10^6) / (2.1 * 10^6) = 238$

2. Let us assume that, given some opimisation techniques, the **30%** of program instructions is executed with **$CPI_E = 1.05$** and the remaining fraction of instructions (70%) is executed with the same CPI calculated in the case (1).
   How much is the **Speedup** from (1) to (2)?

   $F_E = 0.3$; $Speedup_E = CPI_1 / CPI_E = 2$; for the Amdahl's Law:

   $Speedup = 1 / [(1-F_E) + (F_E/Speedup_E)] = 1 / [0.7 + (0.3 / 2)] = 1,176$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(2)?***

   $MIPS_2 = Speedup * MIPS_1 = 1.176 * 238 = 279,88$

Exercise 7

Let us consider a computer executing the following mix of instructions::

Instruction	Frequency	Clock cycles
ALU	50	1
LOAD	20	4
STORE	10	4
BRANCH	10	2
JUMP	10	2

1. How much is the ***CPI average (1)*** assuming a clock frequency of ***500 MHz?***

   $CPI_1 = CPI_{average} = 0.5 * 1 + 0.2 * 4 + 0.1 * 4 + 0.1* 2 + 0.1 * 2 = 2.1$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(1)?***

   $MIPS_1 = f_{CLOCK} / (CPI_1 * 10^6) = (500 * 10^6) / (2.1 * 10^6) = 238$

2. Let us assume that, given a HW opimisation technique, the **40%** of instructions of the program is executed with **$CPI_E = 1.05$** and the remaining fraction of instructions (60%) is executed with the same CPI calculated in the case (1).
   How much is the **Speedup** from (1) to (2)?

   $F_E = 0.4$; $Speedup_E = CPI_1 / CPI_E = 2,1/1,05 = 2$;
   For the Amdahl's Law:
   $Speedup = 1 / [(1-F_E) + (F_E/Speedup_E)] = 1 / [0.6 + (0.4 / 2)] = 1, 25$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(2)?***

   $MIPS_2 = Speedup * MIPS_1 = 1.25 * 238 = 297,5$

3. Let us assume that, given a HW opimisation technique, `branch` and `jump` instructions require only a single clock cycle.
   How much is the **Speedup** from (1) to (3)?

   $CPI_3 = CPI_{average} = 0.5 * 1 + 0.2 * 4 + 0.1 * 4 + 0.1* 1 + 0.1 * 1 = 1,9$
   $Speedup = CPI_1 / CPI_3 = 2,1/1,9 = 1,1$;

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(3)?***
   $MIPS_3 = Speedup * MIPS_1 = 1,1 * 238 = 261,8$

4. Is it better the optimisation introduced in (2) or in (3) ?

   The optimisation (2) is better.

Exercise 8

Let us consider a computer A executing an application containing 30% of load/store instructions requiring 1 clock cycle (thanks to an instruction cache with 100% hit rate). Let us consider an optimized computer B with a clock frequency 5% faster than A and executing 30% less load/store instructions.
How much is the **Speedup**?

$$T_{CPU} = IC * CPI * T_{clock}$$

$$f_{clockB} = 1.05\ f_{clockA}$$

$$T_{clockB} = 0.95\ T_{clockA}$$

$$IC_B = 1 - (0.3 * 0.3)\ IC_A = 0{,}91\ IC_A$$

$$SpeedUp = T_{CPUA} / T_{CPUB} = (IC_A * CPI_A * T_{clockA}) / (IC_B * CPI_B * T_{clock\,B}) =$$
$$= (IC_A * CPI_A * T_{clockA}) / (0.91\ IC_A * CPI_A * 0{,}95\ T_{clock\,A}) = 1 / (0.91 * 0{,}95) = 1.16$$

Exercise 9

Let us consider a computer executing the following mix of instructions:

Instrcution	Frequency	Clock cycles
ALU	50	2
LOAD	20	6
STORE	10	6
BRANCH	10	4
JUMP	10	4

1. How much is the ***CPI average (1)*** assuming a clock frequency of ***1 GHz*** ?

   $\mathbf{CPI_1 = CPI_{average} = 0.5 * 2 + 0.2 * 6 + 0.1 * 6 + 0.1* 4 + 0.1 * 4 = 3.6}$

   How much is the ***Throughput*** expressed in ***MIPS,*** in the case ***(1)?***

   $\mathbf{MIPS_1 = f_{CLOCK} / (CPI_1 * 10^6) = (10^9) / (3.6 * 10^6) = 10^3 / 3.6 = 277.77}$

   How much is the ***execution time*** of a program composed of 100 instructions?

   $\mathbf{T_{CPU1} = IC_1\ CPI_1\ T_{clock1} = 100 * 3.6 * 1\ ns = 360\ ns}$

Let us assume that ***(case 2) ,*** the clock frequency has been incremented by **20%** and the following architecture optimisations have been introduced: 2 ALUs working in parallel, an optimized data cache implying a CPI reduction for LOAD/STORE instructions by **50%** and an optimised branch unit implying a CPI reduction for BRANCH/JUMP instructions by 25%.
Please complete the following table:

Instrcution	Frequency	Clock cycles
ALU	50	1
LOAD	20	3
STORE	10	3
BRANCH	10	3
JUMP	10	3

2. How much is the ***CPI average (2)?***

   $\mathbf{CPI_2 = CPI_{average} = 0.5 * 1 + 0.2 * 3 + 0.1 * 3 + 0.1* 3 + 0.1 * 3 = 2}$

   How much is the ***Throughput, expressed in MIPS, in the case (2)?***

   $\mathbf{MIPS_2 = f_{CLOCK} / (CPI_1 * 10^6) = (1.2 * 10^9) / (2 * 10^6) = 600}$

3. How much is the ***Speedup from (1) to (2)?***

   $\mathbf{Speedup = MIPS_2 / MIPS_1 = 600 / 277{,}77 = 2{,}16}$

   Is it better (1) or (2)?

It is better the case (2)

4. Assuming that ***(caso 3),*** with respect to 2, the clock frequency be further incremented by **10%** without any further modification on the CPI of the instructions.

   How much is the ***Speedup from 2 to 3?***

   Speedup = 1.1