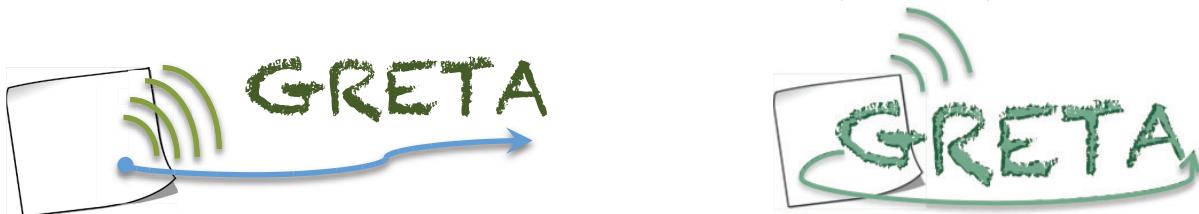


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ETICHETTE E SENSORI ECO-COMPATIBILI LOCALIZZABILI ED
IDENTIFICABILI CON TECNICHE WIRELESS A BANDA ULTRA LARGA

**GREEN TAGS AND SENSORS WITH UTRAWIDEBAND IDENTIFICATION
AND LOCALIZATION CAPABILITIES (GRETA)**



GRETA
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Report on the Third Year of Activity

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Abstract:

The present deliverable describes new results and experimental demonstrations obtained over the third year of the GRETA project. In particular, final implementation and test are described for both tag components and project demonstrator. In addition, overall main achievements of the project are described.

Keyword list: RFID, UWB, green tag, energy harvesting, range likelihood

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LIST OF ACRONYMS

| | |
|---------------|---|
| ACK | acknowledge |
| ADC | analog-to-digital converter |
| AFL | anchor-free localization |
| AGNSS | assisted-GNSS |
| AGPS | assisted GPS |
| AltBOC | alternate binary offset carrier |
| AOA | angle-of-arrival |
| AOD | angle of departure |
| AP | access point |
| API | application programming interface |
| ARNS | aeronautical radio navigation services |
| A-S | anti-spoofing |
| AS | azimuth spread |
| ASK | amplitude shift keying |
| ASIC | application specific integrated circuit |
| AWGN | additive white Gaussian noise |
| AWG | arbitrary waveform generator |
| BCH | Bose-Chaudhuri-Hocquenghem |
| BEP | bit error probability |
| BLAS | basic linear algebra subprograms |
| BOC | binary offset carrier |
| bps | bits per second |
| BPSK | binary phase shift keying |
| BPZF | band-pass zonal filter |
| BS | base station |
| BSC | binary symmetric channel |
| C/A | coarse/acquisition |
| C/NAV | commercial/navigation |
| CAD | Computer Aided Design |
| CAP | contention access period |

| | |
|------------------|--|
| CAWGN | complex additive white Gaussian noise |
| CBOC | composite binary offset carrier |
| CC | central cluster |
| CDF | cumulative distribution function |
| CDMA | code division multiple access |
| CF | characteristic function |
| CFP | contention free period |
| CH | cluster head |
| CIR | channel impulse response |
| CKF | cubature Kalman filter |
| CL | civil-long |
| CM | civil-moderate |
| CMOS | complementary metal oxide semiconductor |
| Coop-POCS | cooperative projection onto convex sets (POCS) |
| Coop-OA | cooperative outer-approximation (OA) |
| COTS | commercial off-the-shelf |
| CNLS | constrained non-linear least squares (NLS) |
| CNSS | compass navigation satellite system |
| CPR | channel pulse response |
| cps | chips per second |
| CRB | Cramér-Rao bound |
| CRLB | Cramér-Rao lower bound |
| CRC | cyclic redundancy check |
| CRPF | cost reference particle filter |
| CS | control segment/commercial service |
| CSI | channel state information |
| CSS | chirp spread spectrum |
| CTS | clear-to-send |
| CW | continuos wave |
| DAA | detect and avoid |
| DC | direct current |

| | |
|--------------|--|
| DGPS | differential GPS |
| DIFS | DCF inter-frame spacing |
| DM | data mining |
| DMLL | distributed maximum log-likelihood |
| DLL | delay-locked loop |
| DoA | direction of arrival |
| DoD | Department of Defense |
| DP | direct path |
| DPE | direct position estimation |
| DS | delay spread |
| DSSS | direct sequence spread spectrum |
| dwMDS | distributed weighted multidimensional scaling |
| DUT | Device Under Test |
| EB | energy-based |
| EBG | electromagnetic band gap |
| ECEF | Earth-centered, Earth-fixed |
| ED | energy detector |
| EGNOS | European geostationary navigation overlay system |
| EH | Energy Harvesting |
| EIRP | effective isotropic radiated power |
| EKF | extended Kalman filter |
| EKFBT | extended Kalman filter with bias tracking |
| e.m. | electro-magnetic |
| EPC | Electronic Product Code |
| EPE | Ekahau positioning engine |
| ERP | effective radiated power |
| ERQ | enhanced robust quad |
| ESA | European Space Agency |
| ESD | energy-based soft-decision |
| EU | European Union |
| F/NAV | freely accessible navigation |

| | |
|----------------|--|
| FCC | federal communications commission |
| FDMA | frequency division multiple access |
| FEC | forward error correction |
| FFD | full function device |
| FFT | fast Fourier transform |
| FIM | Fisher information matrix |
| FLL | frequency-locked loop |
| FOC | full operational capability |
| FOM | figure of merit |
| FPGA | field programmable gate array |
| FPK | Flächen-Korrektur-Parameter (area correction parameters) |
| GAGAN | GPS aided GEO augmented navigation |
| GANSS | Galileo/Additional navigation satellite systems |
| GDOP | geometric dilution of precision |
| GEO | geostationary |
| GIOVE | Galileo In-Orbit Validation Element |
| GIS | geographical information system |
| GLONASS | global orbiting navigation satellite system |
| GML | generalized maximum likelihood |
| GNSS | global navigation satellite system |
| GPRS | general packet radio service |
| GPS | global positioning system |
| GS | geodetic system |
| GSM | Global System for Mobile communications |
| HB | Harmonic Balance |
| hdwMDS | hybrid dwMDS |
| HEO | highly-inclined elliptical orbits |
| HMM | hidden Markov model |
| HOW | handover word |
| HPOCS | hybrid POCS |
| HW | hardware |

| | |
|---------------|--|
| i.i.d. | independent,identically distributed |
| I/NAV | integrity/navigation |
| IC | integrated circuit |
| ICD | interface control document |
| ICT | information and communication technologies |
| ID | IDentification |
| IE | informative element |
| IF | intermediated frequency |
| IGSO | inclined geosynchronous orbit |
| ILS | instrument landing system |
| IMN | Input Matching Network |
| IMU | inertial measurement unit |
| INS | inertial navigation system |
| IoT | Internet of Things |
| IRNSS | regional navigation satellite system |
| IR-UWB | impulse radio UWB |
| ISM | industrial scientific medical |
| ISRO | Indian space research organization |
| IST | information society technologies |
| IVP | inertial virtual platform |
| JBSF | jump back and search forward |
| JSD | Jensen-Shannon divergence |
| KDD | Knowledge Discovery |
| KF | Kalman filter |
| KNN | k-nearest-neighbor |
| LAAS | local area augmentation system |
| LAN | local area network |
| LAPACK | linear algebra package |
| LBS | location-based services |
| LCS | location services |
| LDC | low duty-cycle |

| | |
|---------------|-----------------------------------|
| LDPC | low density parity check |
| LDR | low data rate |
| LEO | localization error outage |
| LLC | logical link control |
| LLR | log-likelihood ratio |
| LLS | linear least squares |
| LNA | low-noise amplifier |
| LOB | line-of-bearing |
| LOS | line-of-sight |
| LR | likelihood ratio |
| LRT | likelihood ratio test |
| LS | least-squares |
| LSE | least squares estimator |
| LVT | Low-Voltage-Threshold |
| MAC | medium access control |
| MAP | maximum a posteriori |
| MBOC | multiplexed binary offset carrier |
| MBS | maximum bin search |
| MB-UWB | multi-band UWB |
| MCRB | modified Cramér–Rao bound |
| MDS | multi-dimensional scaling |
| MEMS | micro-electro-mechanical systems |
| MESS | maximum energy sum selection |
| MEO | medium earth orbit |
| MF | matched filter |
| MGF | moment generating function |
| MHT | multiple hypotheses testing |
| MIM | Metal-Insulator-Metal |
| MIMO | multiple-input multiple-output |
| MISO | multiple-input single-output |
| ML | maximum likelihood |

| | |
|----------------|---|
| MLE | maximum likelihood estimator |
| MMSE | minimum mean squared error |
| MN | Matching Network |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| MOSCAP | MOSFET Capacitor |
| MQKF | multiple quadrature Kalman filtering |
| MRC | maximal ratio combining |
| MS | mobile station |
| MSAS | multi-functional satellite augmentation system |
| MSB | most significant bit |
| MSE | mean squared error |
| MSK | Minimum-shift Keying |
| MST | minimum spanning tree |
| MtM | “More than Moore” |
| MTSAT | multi-functional transport satellite |
| MUI | multi-user interference |
| N/A | not available |
| NAV | navigation |
| NAVSTAR | navigation system for timing and ranging |
| NB | narrowband |
| NBI | narrowband interference |
| NDIS | network driver interface specification |
| NG | network green |
| NLOS | non-line-of-sight |
| NLS | non-linear least squares |
| NN | neural network |
| NPE | Navizon positioning engine |
| NQRT | new quad robustness test |
| NRZ | non-return to zero |
| NSI5 | non-standard I5 |
| NSQ5 | non-standard Q5 |

| | |
|---------------|--|
| NTP | network time protocol |
| OA | outer-approximation |
| OC | open circuit |
| OCS | operational control segment |
| OFDM | orthogonal frequency division multiplexing |
| OMA | open mobile alliance |
| OOA | order-of-arrival |
| OOK | on-off keying |
| O-QPSK | offset quadrature shift keying |
| OQRT | original quad robustness test |
| ORQ | original robust quad |
| OS | open service |
| OTDOA | observed TDOA |
| P2P | peer-to-peer |
| P2PP | P2P-positioning |
| PAM | pulse amplitude modulation |
| PAN | personal area network |
| PCB | Printed Circuit Board |
| PDA | personal digital assistant |
| PDF | probability density function |
| PDP | power delay profile |
| PF | particle filter |
| PHY | physical layer |
| PLL | phase-locked loop |
| PMF | probability mass function |
| PMU | Power Management Unit |
| PN | pseudo-noise |
| POC | payload operation center |
| POCS | projection onto convex sets |
| PN | pseudo-noise |
| PPM | pulse position modulation |

| | |
|--------------|---|
| PPS | precise position service |
| PR | Pseudo-random |
| PRF | pulse repetition frequency |
| PRN | pseudo-random noise |
| PRP | pulse repetition period |
| PRS | public regulated service |
| PRT | partial robustness test |
| PSD | power spectral density |
| PSDP | power spatial delay profile |
| PSK | phase shift keying |
| pTOA | pseudo time of arrival |
| PV | position-velocity |
| PVT | position, velocity, and time |
| QKF | quadrature Kalman filter |
| QZSS | quasi-zenith satellite system |
| RCS | radar cross section |
| RDSS | radio determination satellite service |
| RF | radio frequency |
| RFD | reduced function device |
| RFID | Radio frequency identification |
| R-GML | reduced complexity generalized maximum likelihood |
| RIMS | ranging and integrity monitoring stations |
| RLE | robust location estimation |
| RMS | root-mean square |
| RMSE | root mean square error |
| RMU | remote measurement unit |
| RNSS | regional navigation satellite system |
| RQ | robust quadrilateral |
| RRC | root raised cosine |
| RRLP | radius resource location protocol |
| RSMB | root square of mean biased value |

| | |
|--------------|--|
| RSS | received signal strength |
| RT | robust trilateration |
| RTCM | radio technical commission for maritime services |
| RTLS | real-time locating systems |
| RTK | real-time kinematic |
| RTS | ready-to-send |
| RTT | round-trip time |
| r.v. | random variable |
| RV | random variable |
| SA | selective availability |
| SAR | search and rescue |
| SAW | surface acoustic wave |
| SBAS | satellite-based augmentation system |
| SBS | serial backward search |
| SBSMC | serial backward search for multiple clusters |
| SC | short circuit |
| SCKF | square-root cubature Kalman filter |
| SCR | signal-to-clutter ratio |
| SDR | software defined radio |
| SDS | symmetric double sided |
| SET | SUPL enabled terminal |
| S-GML | soft generalized maximum likelihood |
| SIR | sequential importance resampling |
| SLP | SUPL location platform |
| SIFS | short inter frame spacing |
| SIMO | single-input multiple-output |
| SIS | signal-in-space |
| SISO | single-input single-output |
| SMD | Surface Mounting Device |
| SoA | state-of-the-art |
| SoL | safety-of-life |

| | |
|---------------|---|
| SMC | sequential Monte Carlo |
| SNR | signal-to-noise ratio |
| SNIR | signal-to-noise-plus-interference ratio |
| SPAWN | sum and product algorithm over a wireless network |
| SPKF | sigma-point Kalman filter |
| sps | symbols per second |
| SPS | standard position service |
| SQKF | square-root quadrature Kalman filter |
| SQNR | signal-to-quantization-noise ratio |
| SRN | secondary reference nodes |
| SS | spread spectrum/space segment |
| ST | simple thresholding |
| SUPL | secure user-plane location |
| SV | satellite vehicle |
| SW | software |
| TDMA | time division multiple access |
| TCS | threshold crossing search |
| TDOA | time difference-of-arrival |
| TDR | Time-domain reflectometry |
| TI | trilateration intersection |
| TFTC | Thin Film Transistor Circuit |
| TLM | telemetry |
| TMBOC | time-multiplexed binary offset carrier |
| TOA | time-of-arrival |
| TOF | time-of-flight |
| TOW | time of week |
| TH | time-hopping |
| TNR | normalized threshold |
| TSD | threshold-based soft-decision |
| TTFF | time-to-first-fix |
| TW-TOA | two-way-TOA |

| | |
|---------------|---|
| U.S. | United States |
| UE | user equipment |
| UERE | user equivalent range error |
| UHF | ultra high frequency |
| UKF | unscented Kalman filter |
| ULP | user location protocol |
| UMTS | universal mobile telecommunications system |
| URE | user range error |
| US | user segment |
| UT | user terminal |
| UTC | coordinated universal time |
| UTM | universal transverse Mercator |
| UTRA | UMTS terrestrial radio access |
| UWB | ultra-wide band |
| UWB-IR | ultra-wide band impulse radio |
| VANET | vehicular ad-hoc network |
| VNA | vector network analyzer |
| VRS | virtual reference station |
| WAAS | wide area augmentation system |
| WADGPS | wide area differential GPS |
| WARN | wide area reference network |
| WB | wideband |
| WE | wireless extensions |
| WGS84 | world geodetic system |
| WiMAX | worldwide interoperability for microwave access |
| WLAN | wireless local area network |
| WLS | weighted least squares |
| WMAN | wireless metropolitan area network |
| WPAN | wireless personal area network |
| WRAPI | wireless research application programming interface |
| WSN | wireless sensor network |

| | |
|-------------|---------------------------|
| WT | wireless tools |
| WWB | Weiss-Weinstein bound |
| ZZB | Ziv-Zakai lower bound |
| ZZBT | Ziv-Zakai Bellini-Tartara |

1 INTRODUCTION

1.1 Notation

Hereafter, the main notation used throughout the deliverable is listed for the reader convenience. Meanings and formats will be maintained along the text, unless otherwise stated.

| | |
|---|---|
| x, y, z, \dots | scalar variables, either deterministic or stochastic (depending on the context), either real or complex (depending on the context). |
| $\mathbf{a}, \mathbf{b}, \mathbf{c}, \dots$ | vector variables, column-wise defined, either deterministic or stochastic, either real or complex. |
| $\mathbf{A}, \mathbf{B}, \mathbf{C}, \dots$ | matrix variables, either deterministic or stochastic, either real or complex. |
| \mathbb{R}^M | Field of the real numbers, M -dimensional. |
| \mathbb{C}^M | Field of the complex numbers, M -dimensional. |
| $\mathbf{a} \in \mathbb{R}^M$ | M -element real vector. |
| $\mathbf{b} \in \mathbb{C}^N$ | N -element complex vector. |
| $\mathbf{A} \in \mathbb{R}^{M,N}$ | Real matrix, with M rows and N columns. |
| $\Re\{\cdot\}$ | Real part. |
| $\Im\{\cdot\}$ | Imaginary part. |
| $(\cdot)^T$ | Transpose operator. |
| $(\cdot)^*$ | Complex conjugate operator. |
| $(\cdot)^H$ | Hermitian operator (transpose, complex conjugate). |
| $(\cdot)^\dagger$ | Moore-Penrose pseudo-inverse. |
| $\mathbf{A} \succeq \mathbf{B}$ | The matrix $(\mathbf{A} - \mathbf{B})$ is nonnegative definite. |
| $\mathbf{A} \succ \mathbf{B}$ | The matrix $(\mathbf{A} - \mathbf{B})$ is positive definite. |
| $\mathbb{E}\{\cdot\}$ | Expected value (stochastic) operator. |
| \triangleq | Equal by definition. |
| $\nabla_{\mathbf{x}}(\mathbf{d}(\mathbf{x}))$ | Jacobian matrix (partial derivatives of $\mathbf{d}(\mathbf{x})$ w.r.t. \mathbf{x}). |
| $g(t)$ | Function of a continuous variable. E.g., signal or process as a function of the continuous time. |
| $g[n]$ | Function of a discrete variable. E.g., signal or process in the discrete time domain. |
| f_c | Carrier or central frequency. |
| B_W | Bandwidth |
| f_s | Sampling frequency. |
| T_c | Chip interval. |
| T_s | Symbol/Pulse interval. |
| c | Speed of light. |
| τ_{mean} | Mean excess delay. |
| σ_τ | Delay spread (RMS). |
| $P(\cdot)$ | Power or Probability (depending on the context). |
| $p(\cdot)$ | Probability density function. |
| d | Distance (in meters). |
| (x, y, z) | Cartesian coordinates of a point. |

1.2 Organization of the document

This deliverable describes the third year's achievements of the GRETA project (GREen TAGs and sensors with ultra-wide-band identification and localization capabilities) firstly devoted to the implementation and test of the tag's component as well as to the implementation and test of the final demonstrator.

The tag architecture has been defined according to the following three different configuration modes: stand-alone UWB tag, which provides both localization and communication by means of UWB signaling, and an additional UHF section is used for just energy harvesting and synchronization; Integrated UHF-UWB tag, where a standard off-the-shelf Gen.2 chip is exploited for the communication capability, while the UWB section is used for localization and ranging; enhanced UHF-UWB architecture, where the standard Gen.2 communication protocol interacts with the UWB subsystem in order to obtain a performance improvement.

This report is organized as follows. *Section 2* summarizes the activities pursued over the third year. *Section 3* describes the implementation and test of tag's components. *Section 4* illustrates implementation and test of the final demonstrator. *Section 5* shows the main project achievements. Finally, in *Section 6* the dissemination plan of each unit is reported.

2 SUMMARY OF 3RD YEAR OF ACTIVITY

The third year of GRETA project has been mainly devoted to the implementation and test of tag components, as well as the preparation of the final demonstrator test-bed.

An ASIC prototype of the tag was designed and implemented in a $0.18 \mu\text{m}$ CMOS process. The design targeted ultra-low power consumptions and included several interacting sub-systems: a RF part including both UHF and UWB components (UHF rectifier, UHF synchronization extractor, UWB switch), a power conversion/management section, an analog front-end for embedded sensing purposes, and a digital control circuit. The prototypes are available both as unpackaged and packaged devices.

For what concerns the tag implementation, a novel UWB-UHF antenna that integrates in the same structure two radiating elements working in two frequency bands has been designed. The antenna has been fabricated on a paper substrate and tested also in the final demonstrator. The backscatter modulator has been designed in order to operate in the UWB European lower band. The performance have been evaluated in terms of reflection coefficients and power consumption. The UHF front-end has also been implemented and is composed of a power rectifier for Energy Harvesting (EH) and a signal demodulator. The complete front-end is presented and the performance are evaluated with a harmonic balance simulation, by using an input voltage source, and through a transient simulation for the demodulator behavior with a time varying modulated input signal. For what concerns the tag test, the subsystems have been separately tested. In particular, the UWB backscatter modulator performance have been analyzed by measuring the reflection coefficients by means of a vector network analyzer, the power rectifier performance have been analyzed by measuring its output power as a function of the RF input power, and the demodulator has been tested by measuring the comparator output as a function of the RF input power.

For what concerns the final demonstrator, the GRETA test-bed has been developed at University of Bologna for assessing the performance of UWB tags based on backscatter modulation. An extensive characterization of the adopted instrumentation, configurations, processing schemes and setup is presented in this Deliverable, followed by measurement results. For the test-bed, a probe interrogation signal is built in Matlab according to the IEEE 802.15.4a specifications and at the receiver side, a Vivaldi antenna collects the signal reflected by the environment and the tag. The UWB tag has been emulated with discrete components and the sample measurements have been conducted by acquiring the samples available from an oscilloscope. Such a sample are then processed to extract the tag antenna mode component from the raw collected data and then estimate the distance between the tag and the reader after de-spreading and code synchronization. The range estimates have been also used to provide preliminary results for a case study where a stream of objects equipped with the GRETA tag have to be ordered while moving on a conveyor belt. To this aim, localization and tracking of tag positions is performed to determine the order-of-arrival (OOA) of the stream.

Besides the aforementioned two activities of the third year, the main achievements reached from each research unit are reported in this Deliverable. In order to prove the performance of the paper tag, several measurements of the prototype parts (i.d. antenna, diplexer, and tag) were conducted and the results are presented. Starting from the issues and constraints underlined in the previous Deliverables, the main guidelines for the receiver design are derived, based also on so-far unexplored readers? configurations for RFID applications. The received dynamic range and the analog-to-digital conversion is described. The signalling scheme for the UWB communication is presented together with the signal processing for communication and sensing. The latter consists in techniques for tags synchronization, tag detection, and clutter removal. The signal processing for localization and tracking is also presented. In particular, a method for the blind selection of representative observations is introduced to enhance the accuracy of the location information. Furthermore, a range information model for wideband ranging is proposed and some example of applications for soft-decision ranging are presented.

The system integration also in case of multiple reader coexistence and their synchronization is also discussed. For what concerns the network management protocols, two solutions based on Framed-Slotted ALOHA (FSA) collision arbitration with dynamic frame adaptation and compressive sensing (CS) are introduced. An alternative approach to the Mode 2 and Mode 3 for the UHF-UWB Tags are presented

based on the integration of the previously described UWB tag with a standard UHF EPC Gen.2 tag.

3 IMPLEMENTATION AND TEST OF TAG COMPONENTS

3.1 Introduction

This section describes the GRETA tag architectures, including the viable technologies that can be adopted. In particular, a general modular tag architecture with 3 different configuration modes has been conceived for the project. The idea is to design a modular tag with different configuration modes:

- (Mode 1) Stand-alone UWB tag, which provides both localization and communication by exploiting the UWB signaling, with an additional UHF section for energy harvesting and synchronization. This mode is innovative and extremely low-power consuming, but non compatible with Gen.2 UHF standard.
- (Mode 2) Integrated UHF-UWB tag, where a standard off-the-shelf Gen.2 chip is exploited. In this case the UHF section provides the communication capability and the UWB section is exploited for localization only. This mode is appealing for the compatibility with the Gen.2 standard; it fulfils all the GRETA requirements with a reasonable complexity and implementation effort. It is not optimized for energy efficiency.
- (Mode 3) Enhanced UHF-UWB version, in which the standard Gen.2 communication protocol is modified to enable a tighter interaction with the UWB part for performance maximization. The possibility to implement the 3rd mode is strictly conditioned on the actual effort available. It is appealing for the compatibility with the Gen.2 standard, and optimized for communication and energy efficiency. It requires the design of additional circuits and the implementation of the overall Gen.2 stack (and the additional protocol features).

The advancements in energy harvesting techniques and tag implementation are then described. As a main result of the project, this section also describes the implementation of CMOS integrated circuit implementing the tag in all the above mentioned architectures. The IC is designed in a UMC RF/mixed-mode $0.18\mu\text{m}$ CMOS process.

3.2 Configuration Modes

The GRETA project focuses on innovative solutions and technologies aimed at the realization of a distributed system for identification, localization, tracking and monitoring in indoor and outdoor scenarios, based on environmentally friendly materials. In this context, tags are required to be:

- localizable with sub-meter precision even in indoor scenarios or in presence of obstacles;
- small-sized (with an area in the order of a few square centimeters) and lightweight (i.e., without cumbersome batteries);
- eco-compatible (i.e., made with recyclable materials as paper);
- energy-autonomous;
- easy integrable in goods, clothes and packages;
- low-cost to permit the employment of several tags in the environment;
- capable of sensing physical quantities of the environment.

To improve the ranging accuracy, the UWB backscatter scheme proposed in [1] and investigated in [2] has been considered. In fact, thanks to the high temporal resolution of impulse-based UWB signals, ranging accuracies in the order of a few centimeters are achievable together with the capability to mitigate interference, manage multiple access (multi-tag/multi-reader), and tolerate multipath propagation.

Despite the localization accuracy enabled by the recently-introduced concept of ultra-wide band (UWB)-Radio frequency identification (RFID), several drawbacks arise when such systems have to be deployed, as investigated in [3]. In particular the main limitations are:

- *The poor link budget:* due to the two-hop communication scheme and the standard carrier frequency of 4GHz usually adopted for UWB schemes in Europe, the received signal backscattered by the tag is weak. In order to counteract this effect and ensure proper tag detection, communication and ranging capabilities, the usual approach consists in adopting packets of several pulses per bit in order to enhance the effective signal-to-noise ratio (SNR). For typical indoor distances of some meters, as investigated in [2], around 10,000 pulses per bit are necessary for a robust tag detection, resulting in a quite long symbol time (e.g., 1 ms symbol time when a 100 ns pulse repetition period (PRP) is considered).

Particular solutions to overcome the link-budget limitations can be considered. An example is the exploitation of multitastic RFID configurations, where several low complexity transmitters, called *energy sprinklers* or *energy showers*, spread UHF/UWB signals to power up and interrogate tags around them [4]. Then, according to this paradigm, transmitters and receivers usually constituting the reader can be not co-located.

- *The multi-tags management:* when adopting UWB backscatter communication, no anti-collision protocol can be implemented due to the extremely simple tag front-end and the absence of any receiver and processing unit at tag side. For this reason, all the complexity must be moved to the reader side by exploiting a code division multiple access (CDMA)-based scheme for the simultaneous communication with multiple tags [2]. Unfortunately such a scheme poses several challenges in terms of tag code design and interference mitigation [2]; moreover, the simultaneous detection, communication and localization of several tags require a dedicated processing unit for each tag tuned on the specific tag code.
- *The energy-related aspects:* although UWB backscattering is an extremely-low power consumption technique since only a UWB switch is required to perform signal modulation, the circuitry at tag side (UWB switch, control logic and sensors) must be properly powered so energy-harvesting techniques have to be considered. Due to the impossibility of extracting significant energy from the UWB link because of regulatory issues, a possibility is to exploit the UHF band to transfer the required energy to the tag as done in Gen.2 RFID. Obviously this requires a proper antenna design. An additional source of energy, for example exploiting the ultra high frequency (UHF) band, must be accounted for.

Considering these issues and following the project requirements, a general modular tag architecture with 3 different modes has been conceived in GRETA (see also [5]). All the modes are based on the simultaneous exploitation of both UWB and UHF signals and foresee a hybrid tag able to operate as follows:

1. *UWB Stand-Alone:* Stand-alone UWB tag providing both localization and communication by exploiting the UWB signaling, with an additional UHF section for energy-harvesting and synchronization.
2. *Gen.2-UWB:* Integrated UHF-UWB tag, where a standard off-the-shelf Gen.2 chip is included. The UHF section provides the communication capability while the UWB section is exploited for localization only.
3. *Gen.2 - UWB Enhanced:* An enhanced UHF-UWB version where the standard Gen.2 communication protocol is modified to enable a tighter interaction with the UWB part. This is similar to mode 2 with an optimization of communication and energy efficiency.

In all the 3 architectures a common control logic block ensures the tag operation driving the UWB/UHF backscatters modulators, managing the sensor units and accomplishing the time-critical tasks. In the following the 3 architectures for the UWB tag will be described.

3.2.1 Mode 1: UWB Stand-Alone

According to this mode, the UWB tag works as a stand-alone entity without the integration of the standard Gen.2 protocol. The corresponding architecture is shown in Fig. 1. The UWB communication provides the tag identifier (e.g., the 96 bits of the EPC code), as well as the sensor data, to the reader. For this

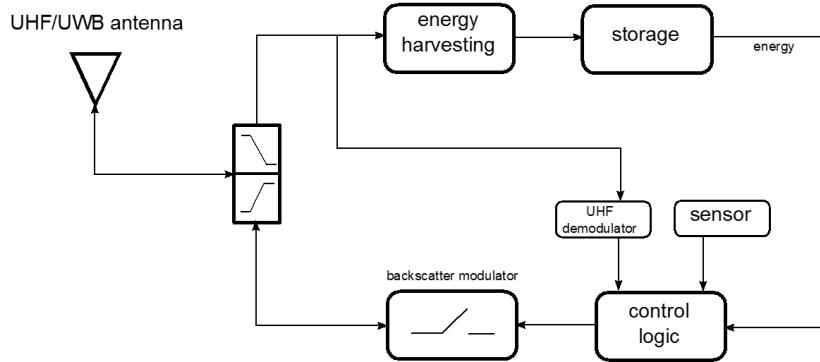


Figure 1: UWB Stand-Alone tag (mode 1).

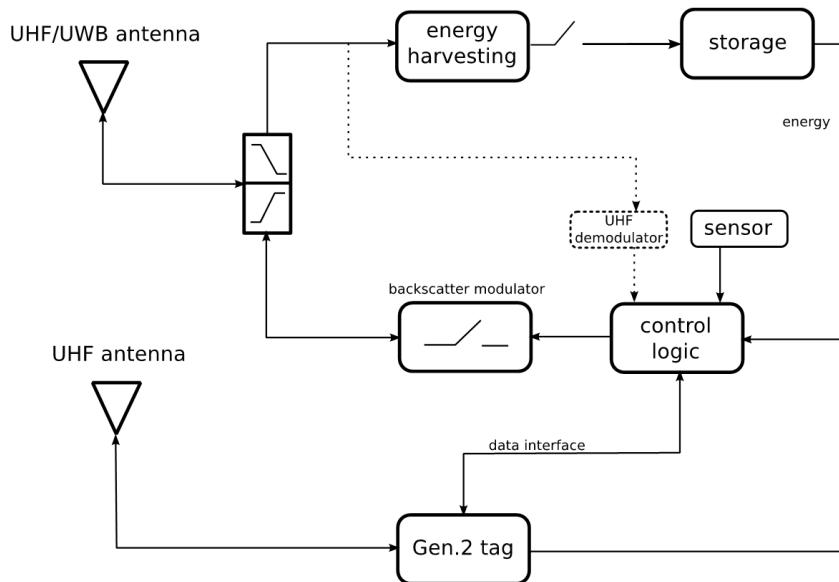


Figure 2: Gen.2 - UWB tag (mode 2).

reason the time necessary to transmit the entire packet is long (e.g., 128 ms per packet), and multiple tags have to coexist and communicate with the reader at the same time in order to obtain a suitable refresh rate (i.e., number of tags readings per second) considering the aforementioned CDMA scheme. This requires the adoption of proper quasi-orthogonal spreading codes for encoding the communication [2].

Energy-harvesting and synchronization are ensured through the UHF link. In fact, the energy is provided by an UHF energy-harvesting block, and a proper diplexer is included to separate the UHF channel, used for harvesting and synchronization, and the UWB channel, used for backscattering communication.

Since it is fundamental to provide good reader-tags synchronization, and to avoid clock drift problems due to the long transmitted packet (and to the simple electronic considered), synchronization can be performed by adopting a proper amplitude shift keying (ASK) or on-off keying (OOK) modulation of the UHF carrier used for powering-up the tag. In this case, the modulation works at a frequency which is about 1/10 of the spreading code chip rate (in the order of 1 MHz) as trade off between the effects of clock drift at tag side and hardware consumption. Specifically, a command to reset the spreading code generator and start the UWB backscatter modulation is derived from the beginning of the ASK/OOK modulation on the continuous wave UHF carrier. Differently, also a simple circuit detecting the absence of the carrier wave can be adopted [6]. Such a modulation could be also exploited to trigger periodically the local tag clock generator in order to prevent drift during the transmission of the (long) packet.

Once reader and tags are synchronized, the UWB communication starts. In particular, the control logic provides the bits to be transmitted to the backscatter modulator by giving the proper switching timing for the modulation of the UWB backscatter signal. In fact, the tags send back to the reader their own information by varying their antenna's load between open and short circuit, and thus modifying accordingly the properties of the reflected signal.

Note that this solution ensures the minimum energy consumption, since all the blocks of Fig.1 can be integrated in a dedicated autonomous chip, but it is not backward compatible with the Gen.2 UHF standard.

3.2.2 Mode 2: Gen.2 - UWB

This mode foresees the UWB tag subsystem as an add-on of a standard Gen.2 UHF passive tag. The Gen.2 protocol is adopted to identify the tag and to read and write data from/to it. The UWB link is used only for high-accuracy ranging (see Fig. 2).

The interrogation cycle starts following a standard Gen.2 UHF signaling scheme between the reader and the tag. During this phase, the tag is powered up and all contentions to address only a specific tag are solved. With the considered architecture, since only one tag per time is active, a unique spreading code is sufficient for ranging thus leading to a considerably simplified reader. In this case, the synchronization can be conceived in two different manners:

1. Once the UHF tag is addressed, an enable/sync command is sent to the tag control logic via the UHF chip data interface in order to activate the UWB backscatter modulator;
2. Once the UHF tag is addressed, an enable command is sent to the tag via the UHF chip data interface. Then, the UHF carrier exploited for energy-harvesting is modulated with ASK/OOK modulation, and this is recognized as a starting command for UWB backscattering.

In both cases the collision-free tag multiple access is guaranteed since only one tag is addressed by the standard UHF protocol. At the same time a more precise synchronization can be ensured by the ASK/OOK modulation. Once the tag is activated and addressed, the UWB interrogation cycle follows. Upon availability of a different channel for the tag synchronization, the UWB operation can be conducted either in parallel or in serial with the following UHF interrogation.

Among the possible benefits of such a solution, it is important to underline that channel multiple access is handled by the standard Gen.2 UHF protocol: since only one tag per time is allowed to communicate with the reader, the multi-user interference problem in the UWB link is avoided. Moreover, very simple and robust spreading codes can be exploited to drastically simplify synchronization and acquisition at reader side. The communication is faster than that of mode 1 (Sec. 3.2.1) as no data are transmitted in the slow UWB communication link, and only 1-2 UWB symbols and one unique spreading code are sufficient for ranging (obtaining a 1-2 ms UWB interrogation duration). As a consequence, the receiver complexity is drastically reduced: in fact, in order to perform tag detection and localization, there is no need to replicate the receiver structure for each tag spreading code, then guaranteeing a high refresh rate (up to 200 reads/s).

This solution ensures a reasonable low complexity and is simple to implement, but is not optimized from the energy consumption point of view due to the presence of an off-the-shelves additional UHF chip.

3.2.3 Mode 3: Gen.2 - UWB Enhanced

With the mode 3 the goal is to maximize the performance of the UHF-UWB tag by optimizing the standard Gen.2 protocol for the needs of the joint UWB-UHF RFID system [7]. The tag architecture is reported in Fig. 3. In this mode, the UWB and the UHF subsystems coexist and support each other. In particular, the ranging/localization capabilities of tags are ensured by the UWB backscatter modulation which enhances the Gen.2 protocol, and its communication capability, and makes it operate with wireless coverage awareness. The integration of the sensing capabilities makes such tags extremely appealing and capable of fulfilling the requirements described at the beginning of Sec. ???. The development of such

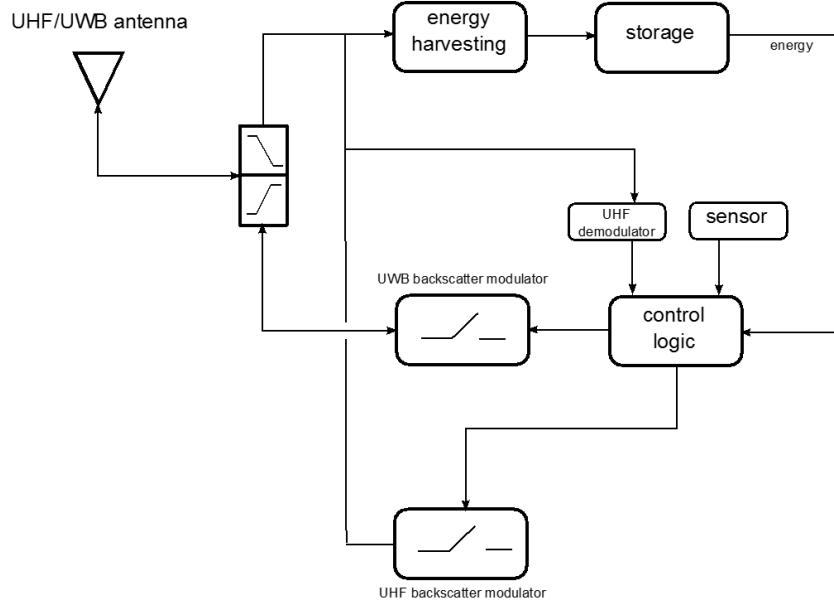


Figure 3: Gen.2 - UWB Enhanced (mode 3).

a solution encompasses the design of a novel integrated Gen.2-compatible and UWB chip to be connected on a multi-band UHF-UWB antenna, providing then the maximum efficiency in terms of energy consumption, synchronization precision, refresh rate and communication timeliness.

Since the UHF backscatter modulator must be realized on chip, without exploiting a standard Gen.2 compatible chip, a single UHF/UWB antenna or two separated UHF and UWB antennas can be adopted. In any case, the UHF antenna has to provide at the same time the possibility of being loaded with the backscatter modulator and the energy-harvesting block, as happens in the standard UHF chips. Note that a single control logic handles both UWB and UHF channel operations ensuring an optimized behavior from both the communication and the energy efficiency point of view. As an example, the UWB ranging information can be exploited in the UHF domain to select optimal parameters for multiple access control.

This solution represents an optimal design and can be considered as the most appealing for a practical implementation of the GRETA architecture. However, its realization requires the design of what usually included in a standard UHF chip (e.g., the UHF backscatter modulator) and of a more complex ad-hoc control logic which has to manage both the standard-compatible UHF protocol stack and the UWB communication protocol.

3.3 Energy Harvesting

The Energy Harvesting operation is implemented by means of an RF-to-DC rectifier, designed on the miniaturized diplexer, which is directly connected to the tag antenna. The diplexer is composed by a circuitry enabling the simultaneous dual-band functionalities of the tag, that is UHF Energy Harvesting and UWB backscatter communication. The diplexer is responsible for the correct operation and management of the signal received by the tag radiating element. Since the tag is designed for the simultaneous operation in both the UHF and UWB bands, the first functionality of the diplexer is that of separating the two signals, by filtering the UHF and the UWB bands, as well as providing high decoupling between the two, so that no mutual interference affects the tag operations. The integrated UWB-UHF antenna impedance needs a proper matching network towards the RF-to-DC rectifier in order to be able to deliver the maximum amount of incident RF power in the UHF band. This matching operation is obtained, together with the UHF band filtering and decoupling, by means of a lumped-elements network composed by a series inductor and a shunt capacitor. These operations are obtained with a single-stage lumped-element network, which provides a direct match from the UHF antenna impedance to the RF-to-DC rectifier input

impedance without an intermediate matching step towards the conventional 50Ω , typical of measurement instruments. This solution has the main drawback of preventing an intermediate test of the single UHF filter/matching network or of the RF-to-DC rectifier, but it guarantees the substantial advantage of avoiding losses due to the introduction of additional components in the UHF network. For the rectifying section a voltage-doubler topology is adopted, which provides the best trade-off between rectified voltage and RF-to-DC conversion efficiency. The rectifier topology is shown in Fig. 4, in which the UHF filter, as well as the UWB path, is also present. Two Schottky diodes from Skyworks have been adopted, together with two capacitances from ATC. The table in Fig. 4 summarizes the commercially-available components used, where the value of the optimum load connected after the rectifier is also indicated.

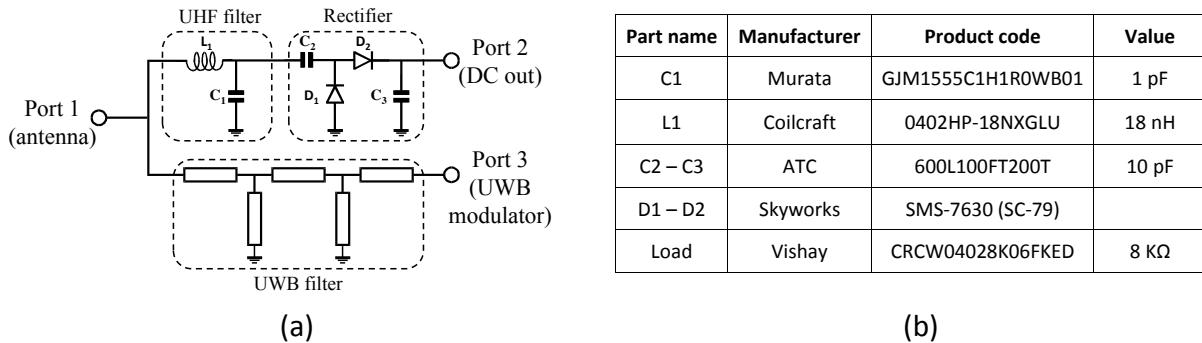


Figure 4: (a) Diplexer schematic and (b) table of the corresponding components.

In order to provide simultaneous recovery of RF energy while communicating in the UWB band, a non-linear/electromagnetic co-simulation of the whole circuit has been carried out, including real component models, and taking into account the dispersive behavior of the antenna, with the goal of maximizing the RF-to-DC conversion efficiency. Since RF Energy Harvesting has to deal with typically low-levels of incoming signals, the optimization has been mainly focused on incoming available RF power ranging from -15 to -5 dBm. The resulted conversion efficiency, in optimum loading conditions, is shown in Fig. 5 for this range of available RF input power: values from 40 to 50 % are clearly observed.

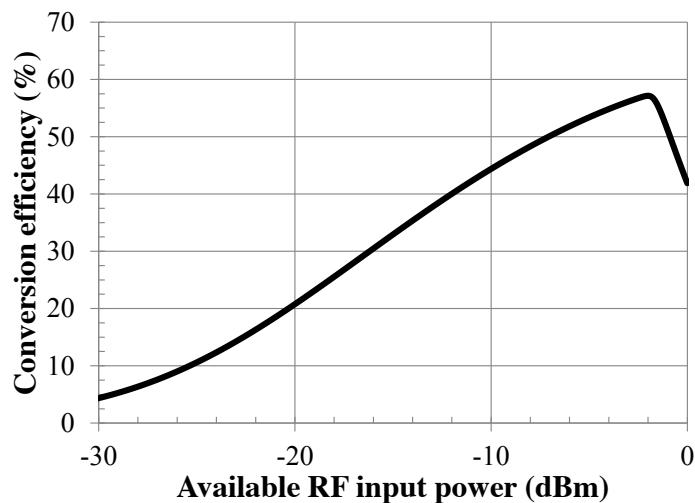


Figure 5: RF-to-DC conversion efficiency for low-levels of incoming RF available power.

3.4 Tag Implementation

3.4.1 Antenna and external front-end

As tag radiating element, the UNIBO unit has designed the novel UWB-UHF antenna reported in Fig. 6. This particular antenna integrates in the same structure two radiating elements working in two frequency bands: the UWB 3.1 to 4.8 GHz band, which is covered by means of an Archimedean spiral antenna, and the UHF 868 MHz band, guaranteed by means of a meandered dipole obtained from the extension of the spiral outer arms. The two elements share the same port, for compactness purposes.

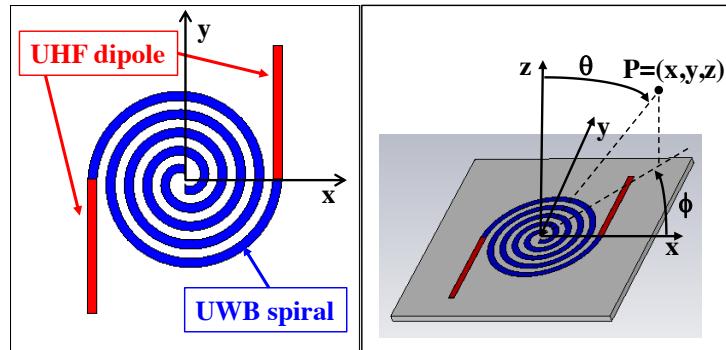


Figure 6: UWB-UHF antenna architecture.

After different prototype realizations on FR-4 and Taconic RF60A substrates, the antenna has been designed and fabricated on a paper substrate, having thickness equal to $370 \mu\text{m}$, permittivity $\epsilon_r=2.55$ and loss tangent $\tan(\delta)=0.05$. Both the antenna and the diplexer, designed by the UNIBO group, have been realized by the UNIPG group with a fabrication process consisting in laying on the paper substrate a copper adhesive tape etched by means of a photo-lithographic process. The 1.5λ -long dipole provides a resonance behavior at the 868 MHz frequency, while at the same time preserving little antenna dimensions, since the spiral length contributes to the dipole antenna. The radiation efficiency of the dipole is 88%, while the realized gain equals the 0 dBi value. The auto-complementarity and auto-similarity principles of the spiral antenna guarantee an almost constant behavior over the whole 3.1 to 4.8 GHz band, with an efficiency of more than 80% and a realized gain of about 3 dBi. A picture of the prototype is reported in Fig. 7.

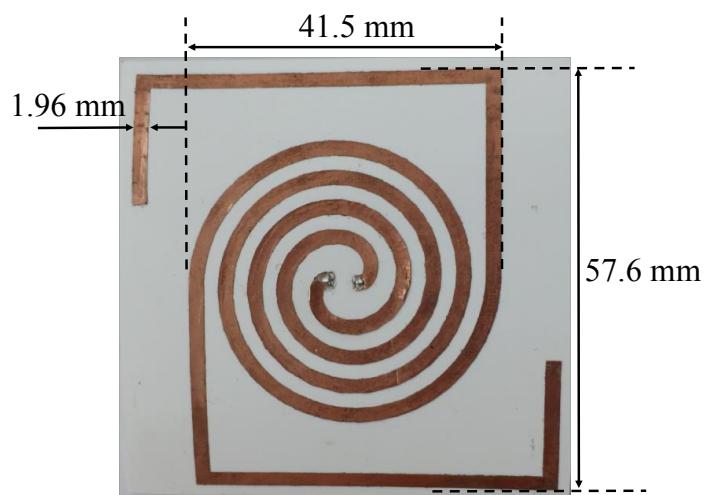


Figure 7: UWB-UHF integrated antenna on paper substrate.

Due to the absence of a ground plane, the radiation pattern of the dual-band antenna is bi-directional

and for such reason, the presence of circuitry metallization close to the antenna can deteriorate its performance. For this reason the diplexer, which is responsible for the correct operation of both the UWB backscattering and the UHF Energy Harvesting, has been designed on the paper substrate, leading to a dimension of only 1.3-cm². This dimension is the chosen as the maximum allowed in order not to degrade the radiation pattern significantly. A comparison between the simulated radiation patterns of the sole antenna and of the complete tag comprising both the antenna and the diplexer is reported in Fig. 8 for the UWB band central frequency.

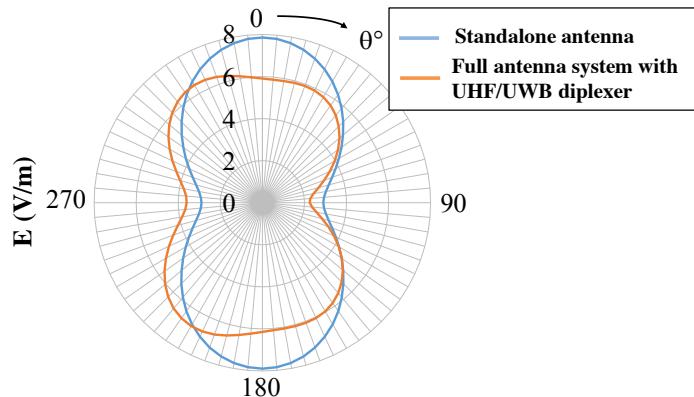


Figure 8: Comparison between the radiation patterns of the standalone antenna and in the presence of the diplexer, for the UWB central frequency of 4 GHz.

In order to guarantee an extremely low profile, the designed diplexer is directly connected on the center part of the backside antenna substrate. The connection is realized by means of two thin wires in a balun-free transition; one wire connects one antenna arm to the diplexer ground plane, while the second wire connects the other antenna arm to the diplexer microstrip line. The overall tag structure results in a less than 1 mm thickness. A schematic representation of the tag structure is provided in Fig. 9; while pictures of the backside of the tag are reported in Fig. 10, which clearly show the relative position and dimensions of the diplexer with respect to the antenna.

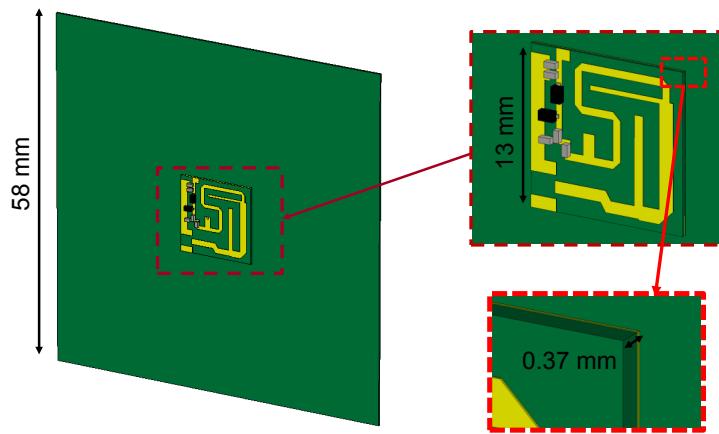


Figure 9: Schematic representation of the tag backside, with zoomed view.

The 1.3 mm-wide diplexer is mainly composed of three sections: the UHF matching and filtering circuit, the rectifying section and the microstrip UWB matching and filtering circuit. The communication in the UWB band is provided by passive backscattering, therefore the UWB port of the diplexer will be connected to a backscatter modulator, which will be responsible for the modulation of the incoming signal by switching its impedance between the two mismatched conditions of open and short circuit terminations. The expected diplexer performance are provided in Fig. 11 in terms of scattering parameters; in order

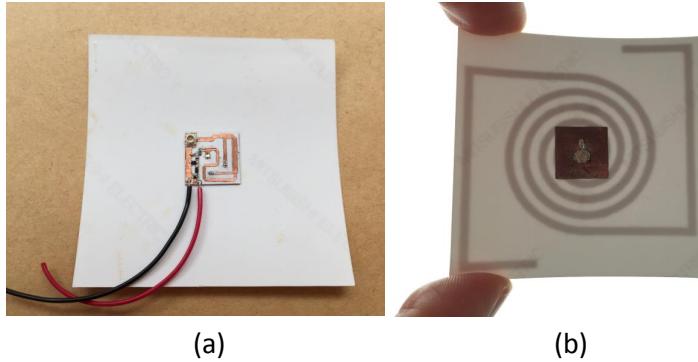


Figure 10: (a) Tag implementation, backside view. (b) Diplexer ground plane and the antenna in backlight, which clearly illustrates their relative positions.

to evaluate the UHF filter performance a fictitious port 2 is added after the UHF lumped components network, by loading it with the rectifying section mean value for low levels of incoming RF signal (i.d. $20-j*250 \Omega$). The UWB port (port 3) is loaded by 50Ω for design purpose, while port 1 is loaded by antenna impedance at the respective frequencies.

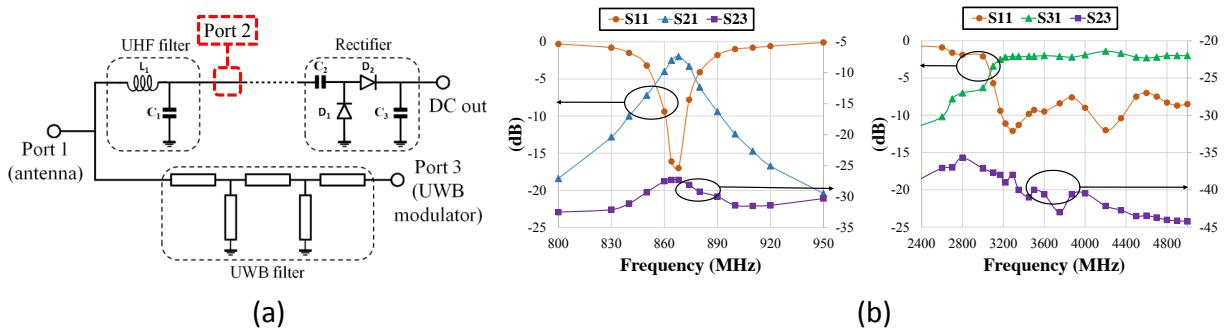


Figure 11: (a) Diplexer schematic with added test port 2. (b) Diplexer performance in terms of scattering parameters. The UHF filter is loaded by the rectifying section mean value, while the UWB port is loaded by 50Ω .

As can be seen from the graphs, the UHF filter provides matching conditions in the 868 MHz, while its insertion loss is of about 2.5 dB. The insertion loss in the whole UWB band is of only 2 dB. Moreover it is clearly shown how high decoupling is provided between the two bands; this guarantees the simultaneous correct operation in both bands, with no mutual interference.

3.4.2 Block diagram of the ASIC

The block diagram of the integrated circuit designed in the UMC 0.18 μm CMOS process is shown in Fig. 12. The ASIC is a mixed-signal custom integrated circuits including: a power management sub-circuit, a digital control sub-circuit, a RF sub-circuit, and an analog front-end sub-circuit. The RF sub-circuits integrates a rectifier, a synchronization extractor, and an UWB switch. The power management sub-circuit implements an inductor-less DC/DC converter based on a reconfigurable charge-pump and an ultra-low voltage low drop-out regulator, with the purpose of generating a stable and sufficient supply voltage for all the circuits blocks from the output of the UHF rectifier part. The digital sub-circuit integrates the core logic required to drive the back-scattering switch based on the possible configurations of the ASIC. The analog front-end includes a micro-power temperature sensor and a generic impedance sensing interface for external sensors, along with a micropower ADC. The floorplan of the ASIC is shown

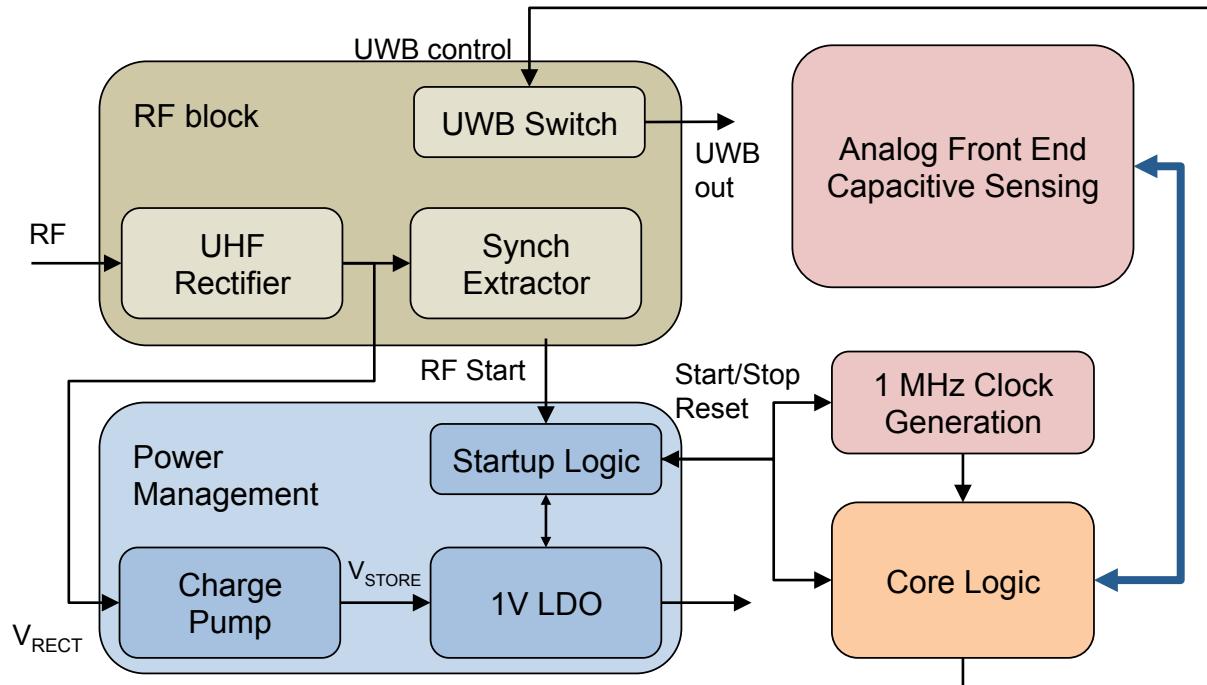


Figure 12: Block diagram of the designed ASIC.

in Fig. 13.

Among the main features of the ASIC it is worth to mention:

- a minimum required rectified voltage $V_{RECT} = 400\text{mV}$ in order to properly drive the charge pump up to the required output voltage
- on-chip local energy storage capacitors (5.4 nF, 2V maximum voltage)
- on-chip low drop-out regulator for generating a 1 V supply voltage for the analog and digital cores
- ultra-low quiescent currents: 300 nA for the LDO and the start-up logic at 1.5V input voltage, 220 nA for the charge pumps with a 400 mV input voltage, 550 nA for the local oscillator generating and distributing the clock, < 1 μA for the sensing circuitry supplied at 1 V, and 1 μA for the digital core supplied at 1 V

Clock generation and analog circuits consume power only when enabled.

3.4.3 IC Subsystems: Start-up and power management

The main part of this section is a configurable charge pump, where the number of active stages automatically switches from 6 to 4 based on the state of charge of the storage capacitor in order to reduce the distance from the maximum power point. The circuit is highlighted in Fig. 14. The decision is triggered when the value of the voltage at the fourth stage exceeds 1.67V. The pump capacitors are integrated and have a 4.87 pF capacitance each. The charge pump is driven by a local oscillator generating two non-overlapping clock signals running at a 556 kHz frequency when the input voltage is 400 mV.

The LDO circuit is shown in Fig. 15. It is stable for loads (i.e. the internal analog and digital cores) ranging from 20 $\text{k}\Omega$ to open. Its quiescent current consumption is 225 nA, mainly due to the operational amplifier.

3.4.4 IC Subsystems: Analog front-end

The analog sub-section integrates a clock generator for the whole system, and a sensing interface for temperature and impedance.

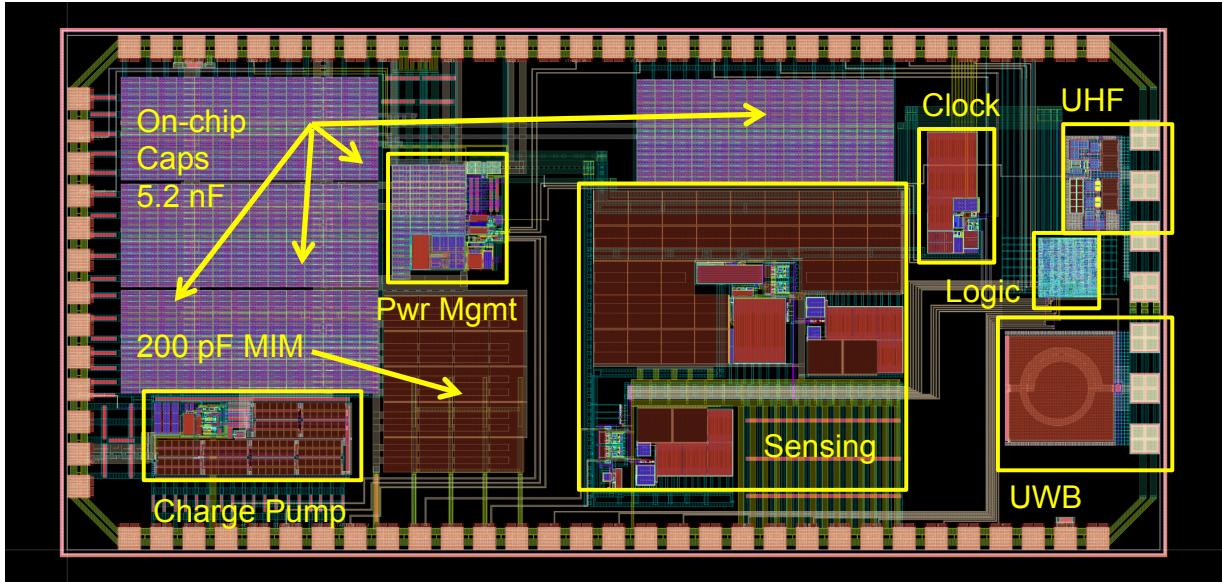


Figure 13: Floorplan of the designed ASIC.

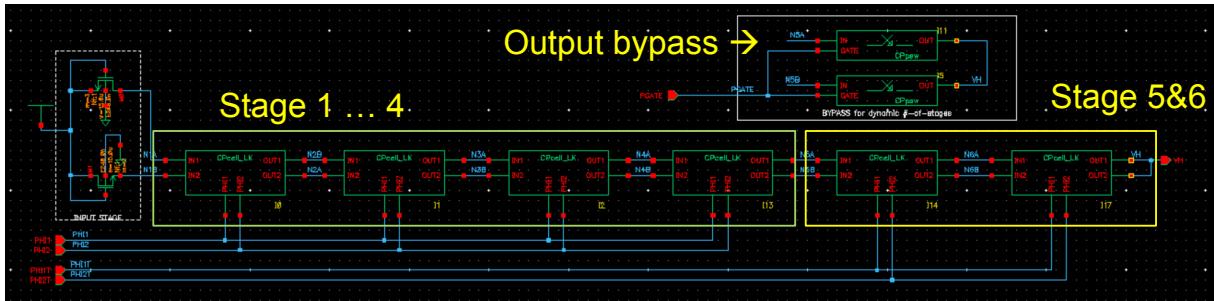


Figure 14: Schematic of the charge pump.

The clock can generated either internally or externally. Internal clock generation is based on a relaxation oscillator, as depicted in Fig. 16. The estimated performance of this sub-circuits includes:

- a nominak frequency of 1 MHz
- a power consumption of 560 nW
- a line sensitivity of 4%/V
- very fast rise and fall times in the order of 1 ns

The sensing interface manages either an internal temperature sensor or an external impedance sensor (Fig. 17). Temperature sensing is performed by generating internally two currents: the first current is proportional to absolute temperature (PTAT), whereas the second is contant with temperature (CWT). The PTAT and CWT currents are integrated on matched capacitances until they reach a reference voltage V_{REF} . The delay between the two is estimated by means of a differential counter. The expected resolution is 8 bit, with a power consumption lower than 1 μ W, where the temperature sensitivity is 0.3 nA/ $^{\circ}$ C, the sensing time is lower than 2 ms, the line sensitivity is lower than 6%/V.

3.4.5 IC Subsystems: Digital control logic

The digital section of the ASIC has been implemented with fully synthesizable logic in advanced CAD EDA environments. The digital control includes:

- a UWB switch gate drive
- logic for data transmission

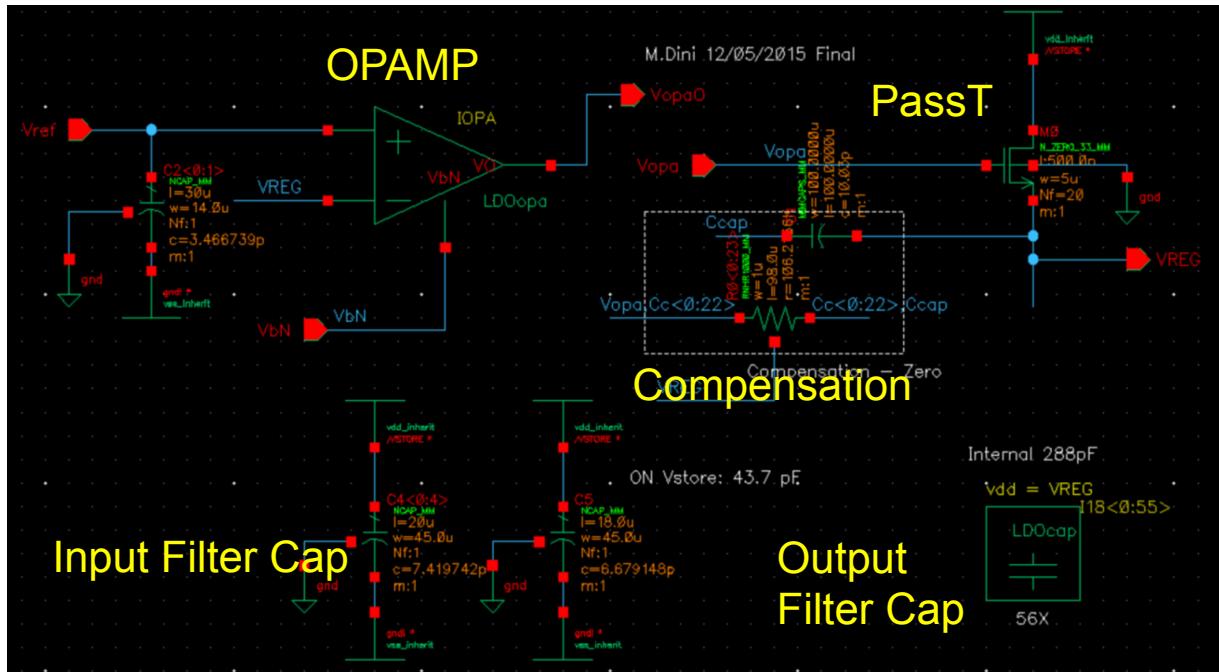


Figure 15: Schematic of the low drop-out regulator (LDO).

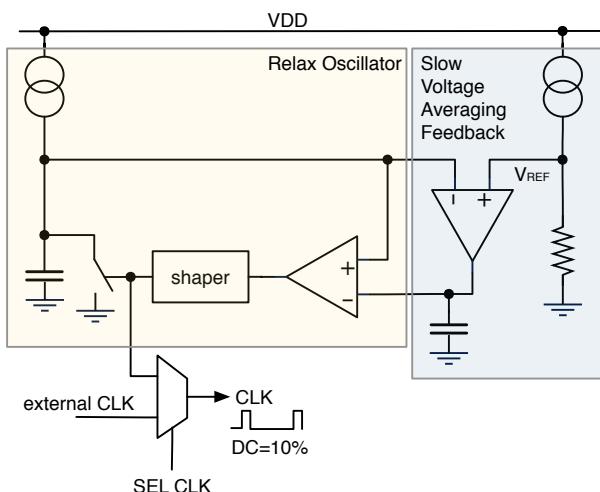


Figure 16: Schematic of the clock generation circuit.

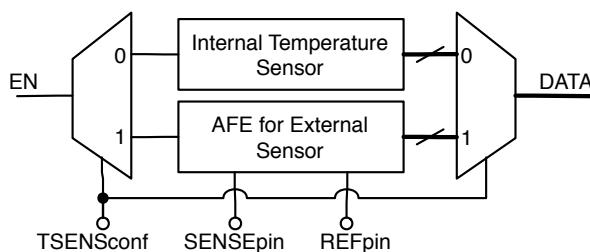


Figure 17: Structure of the sensing interface.

- 8 selectable pseudo-random 1024-bit sequences
- SPI interface for communication with external components such as a GEN2 RFID tag.

- debug outputs

. A sketch of the interface of the digital part is shown in Fig. 18. Besides controlling the UWB switch, the digital part is in charge of controlling all the interactions between the sub-systems of the ASIC and of providing synchronization and hand-shake sequences, as well as managing communication of sensor data either with the UWB or the wired SPI protocols. A simplified flow chart is reported in Fig. 19.

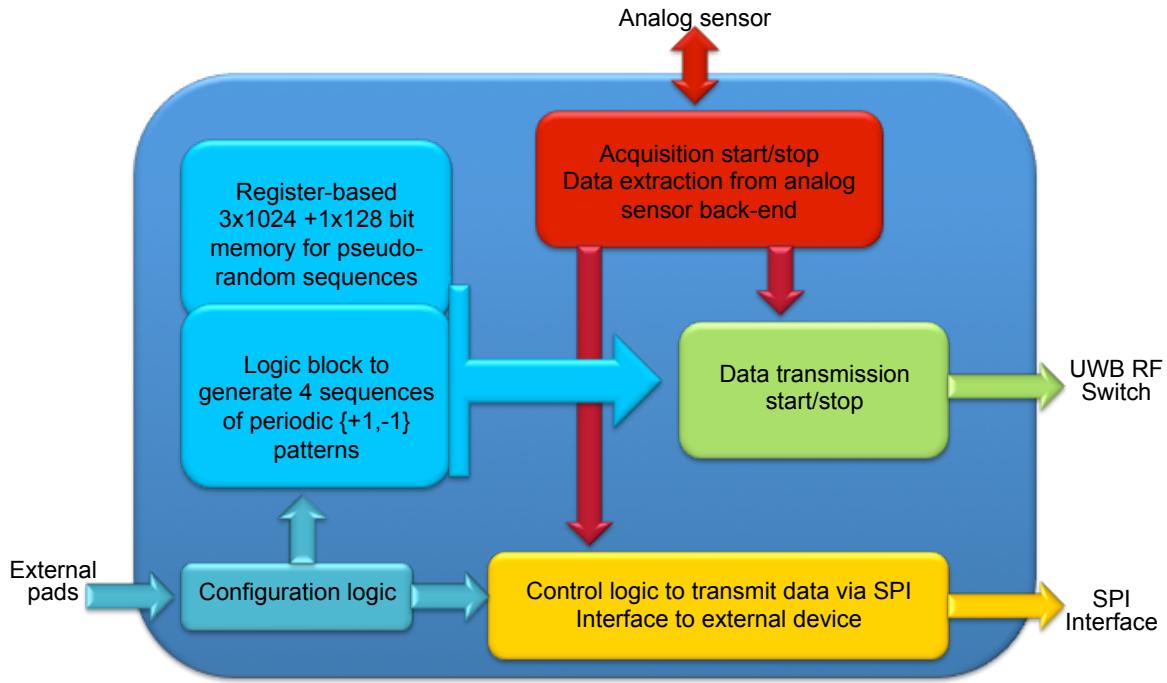


Figure 18: A sketch of the interface of the digital section of the ASIC.

The silicon area is approximately $180 \times 180 \mu\text{m}^2$, with 3.5k logic gates.

The operating frequency is 1 MHz. The lowest power consumption is achieved with the simplest +1,-1 sequence applied to the UWB switch. In this case the internal power consumption is roughly $2 \mu\text{W}$, the switching power is $0.5 \mu\text{W}$, the leakage power is $1.1 \mu\text{W}$. With the embedded 1024-bit pseudo-random sequences the required power increases up to $13 \mu\text{W}$.

Preliminary tests showed that the digital section is operating successfully. A first set of tests was performed with the aim of assessing the functionality of the back-scatter modulator with one of the 1024-bit pseudo-random sequences. The acquired waveforms are reported in Fig. 20. More specifically, it was observed that the produced bit stream corresponds to the considered pseudo-random sequence, which is managed with proper timings and inverted where required.

3.4.6 IC RF Subsystems: UWB Backscatter Modulator

The backscatter modulator [8–16] has been designed in order to operate in the UWB frequency band 3.1–4.8 GHz. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistor acts as a switch and an inductor is used to optimize the phase difference of the two states of the modulator. The switch is designed considering an antenna impedance equal to 50Ω . Ideally, the magnitude of the reflection coefficients must be equal to 1 (0 dB), and the phase difference of the two switch conditions, short circuit (SC) and open circuit (OC), equal to 180° .

The schematic of the backscatter modulator is shown in Fig. 21: A identifies the control inverter, it is useful to compute the power consumption and the switching time of the modulator; B is the modulator core, an RF transistor in series with an inductor; C, is an radio frequency (RF) port and represents the antenna; V_b is the bias source and V_c is the control signal. The modulator is not directly biased but

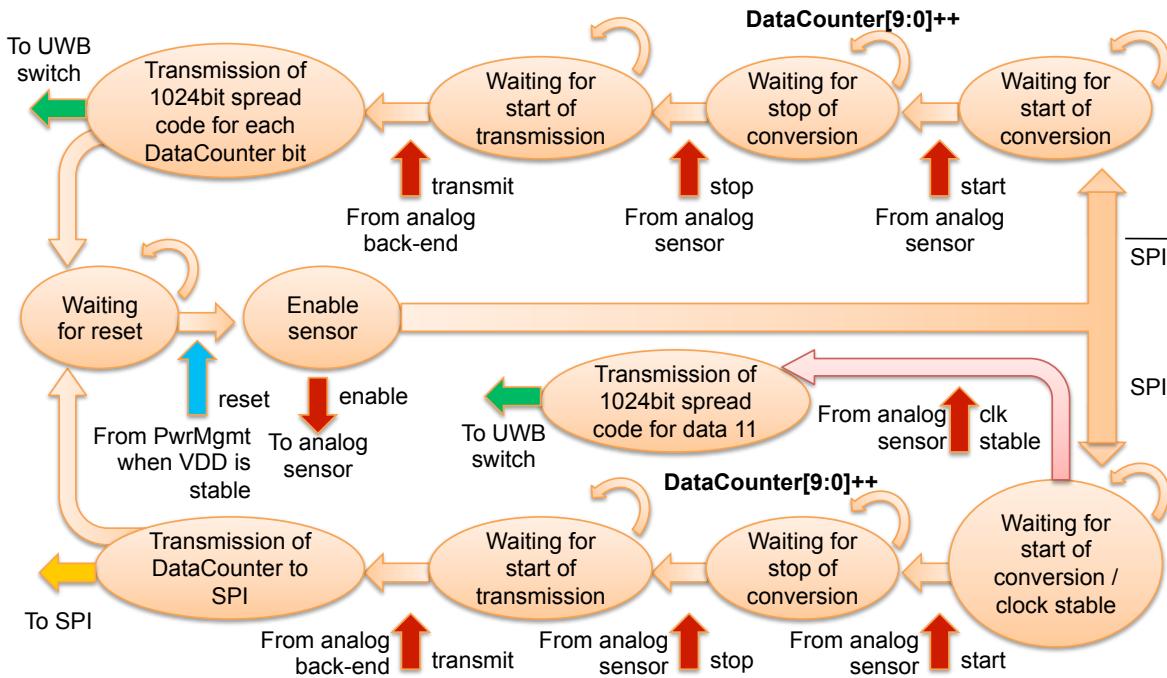


Figure 19: A simplified flow chart of the digital control of the system.

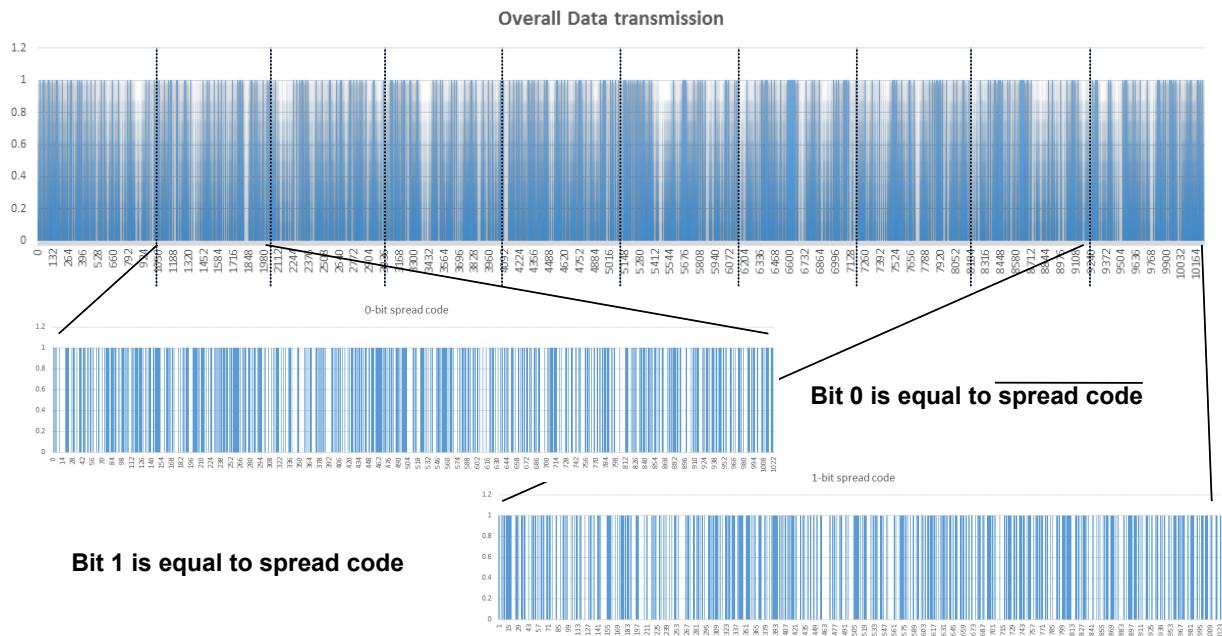


Figure 20: Preliminary results of tests of the digital section

controlled by an inverter connected to the switch gate. The RF transistor and inductor dimensions have been optimized in order to obtain the best performance in terms of best trade-off between reflection magnitude and phase difference of the two switch states.

The performance of the backscatter modulator in terms of reflection coefficients are shown in Fig. 22. The plots are obtained in two different conditions: for a bias voltage of 1 V and 1.8 V. In the two cases the phase difference in the SC and OC condition is about 180° thanks to the inductor. However, the bias voltage and the parasitics affect the reflection coefficient magnitude, particularly, in the SC state: for

a bias voltage of 1.8 V and 1 V the magnitude is -3.5 dB and -5.5 dB, respectively. In the OC state the magnitude is about -0.5 dB. Moreover, time domain simulations have been performed to evaluate the time response of the modulator switch by controlling it with a square signal. In all the analyzed cases (bias voltage 1 V and 1.8 V and high-to-low and low-to-high transitions) the worst transition time is lower than 1 ns.

The dynamic power consumption of the only switch transistor can be computed with the following equation:

$$P_D = V_{HIGH}^2 * C_{MOS} * f_S \quad (1)$$

where P_D is the dynamic power, V_{HIGH} the high level gate voltage, C_{MOS} the MOSFET gate capacitance and f_S the average switching frequency. Must be noticed that the capacitance C_{MOS} varies for the OC (voltage applied to gate-source V_{GS} is 0 V) and SC (V_{GS} is equal to V_{HIGH}) conditions. In Table 1 are resumed the power consumption values considering the two different capacitance values and an average switching $f_S = 0.1$ MHz. In both cases, bias voltage equal to 1 V and 1.8 V, the C_{MOS} is the same. In any case, conservatively talking, the power consumption is lower than 0.1 μ W and in the best case it is equal to about 10 nW.

Table 1: Backscatter modulator dynamic power consumption.

| State | OC | SC | OC | SC |
|---------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| V_{HIGH} | 1.8 V | 1.8 V | 1 V | 1 V |
| C_{MOS} | 0.11 pF | 0.21 pF | 0.11 pF | 0.21 pF |
| $P_D/f_S =$ $V_{HIGH}^2 * C_{MOS}$ | 0.36 pJ | 0.69 pJ | 0.11 pJ | 0.21 pJ |
| P_D ($f_S=0.1$ MHz) | 0.036 μW | 0.068 μW | 0.011 μW | 0.021 μW |

The power consumption can also be computed with transient simulations by measuring the instantaneous power, integrating it over a switching period, and multiplying if for the frequency as follow:

$$e = \int_0^T p(t) dt \quad (2)$$

$$P_{avg} = \frac{e}{T} = e * f_S \quad (3)$$

where $p(t)$ is the instantaneous power, e the energy, $T = 1/f_S$ the average switching period and f_S the average switching frequency, P_{avg} the average power consumption.

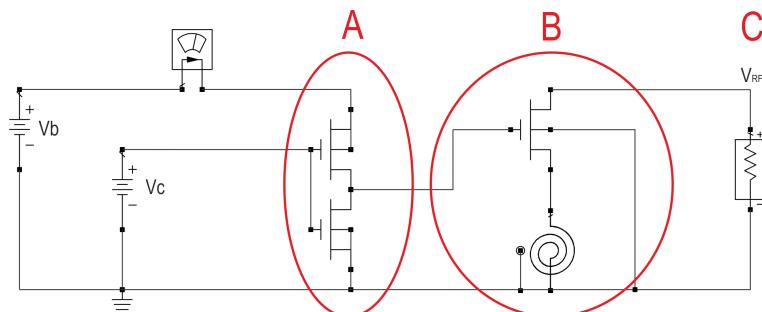
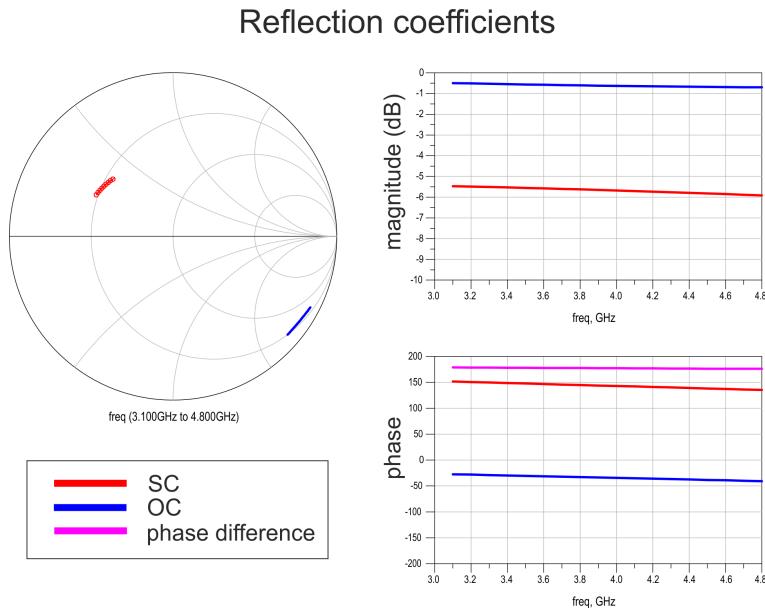
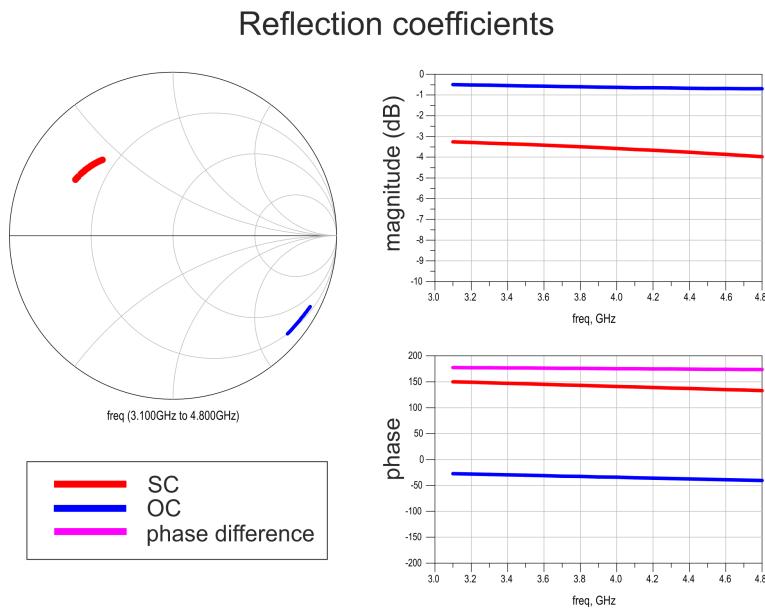


Figure 21: Schematic of the backscatter modulator with the control circuit: A, control circuit (CMOS inverter); B, switch; C, RF load (antenna).



(a)



(b)

Figure 22: Simulated reflection coefficients of the backscatter modulator controlled by using a voltage equal to: 0 V for the OC and 1 V for the SC (a); 0 V for the OC and 1.8 V for the SC (b).

The power meter in cascade to the bias generator in the schematic measures the instantaneous power consumption of the UWB switch transistor with the inverter used to control the switch (see Fig. 21). The values obtained by processing the instantaneous power measured from the two power meters are listed in the Tables 2. In the worst cases the power consumption is lower than $0.1 \mu\text{W}$ and $0.03 \mu\text{W}$ for a bias voltage equal to 1.8 V and 1 V, respectively.

The layout of the switch, designed with Cadence Virtuoso, is shown in Fig. 23. Its dimensions are strictly related to the inductor that is greater than the RF transistor.

Table 2: Backscatter modulator power consumption for both low-to-high and high-to-low transitions.

| | Power (with inverter) | Power (with inverter) |
|---|----------------------------------|----------------------------------|
| V_{HIGH} | 1.8 V | 1 V |
| e | 0.96 pJ | 0.27 pJ |
| $P_{avg} = e * f_S$ ($f_S=0.1$ MHz) | 0.096 μW | 0.027 μW |

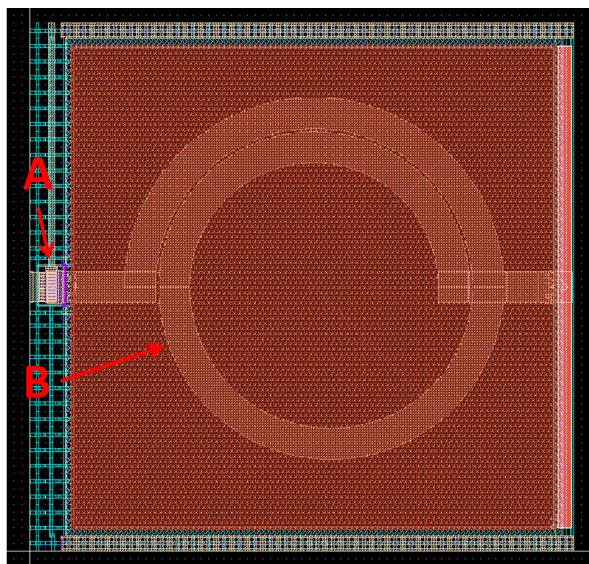


Figure 23: Layout of the backscatter modulator: A, RF transistor; B, inductor.

3.4.7 IC RF Subsystems: UHF Front-end

The UHF front-end of the RFID tag, operating in the frequency bands around 900 MHz, is made of:

- a power rectifier for EH [16–19];
- a signal demodulator made of different subsystems (signal rectifier, comparator, and current generator) [16–26].

3.4.8 IC RF Subsystems: UHF Power Rectifier for EH

The rectifier, used to harvest energy from the UHF signal and convert it in direct current (DC) useful to bias the integrated circuit (IC) system, is a 2-cells voltage multiplier based on Low-Voltage-Threshold (LVT) transistors in diode configuration. Metal-Insulator-Metal (MIM) capacitors and MOSFET Capacitor (MOSCAP) are used as DC blocks and for the storage of DC current. The schematic of the power rectifier is shown in Fig. 24: A is the unit cell with 2 transistor in diode configuration, a MIM in series with the RF input and a MOSCAP in shunt configuration as DC blocks; B is the low-pass filter with a transistor in diode configuration, in order to block the DC current that flows backward, a MOSCAP to storage the energy, and a load resistor to simulate the power management unit of the chip.

The plots in figures 25 show the results obtained from the Harmonic Balance (HB) simulations of the schematic of the power rectifier in parallel with the signal rectifier for demodulation. The results with and without the signal rectifier in parallel are very close (error of about 1 % in terms of impedance) because of the high input impedance of the signal rectifier. An output DC voltage of 130 mV, an output DC power of -28 dBm and a conversion efficiency (ratio of the output DC power and the RF input power) of 16 % for

an RF input power of -20 dBm; for an input power of -10 dBm the output voltage is 620 mV, the output power is -14 dBm and the efficiency is about 37 %. The efficiency increases up to 55 % for an input of 0 dBm. These values are obtained for a load of $10 \text{ k}\Omega$ and they are affected by it and by the number of rectifier stages (unit cells): by increasing the stages number, in order to obtain an higher output voltages, the efficiency decreases for the losses introduced by the transistor series resistance. The input impedance of the UHF front-end (see figure 26) varies as a function of the input power being a non-linear system and it is about $50 - j325 \Omega$ for an input power of -20 dBm.

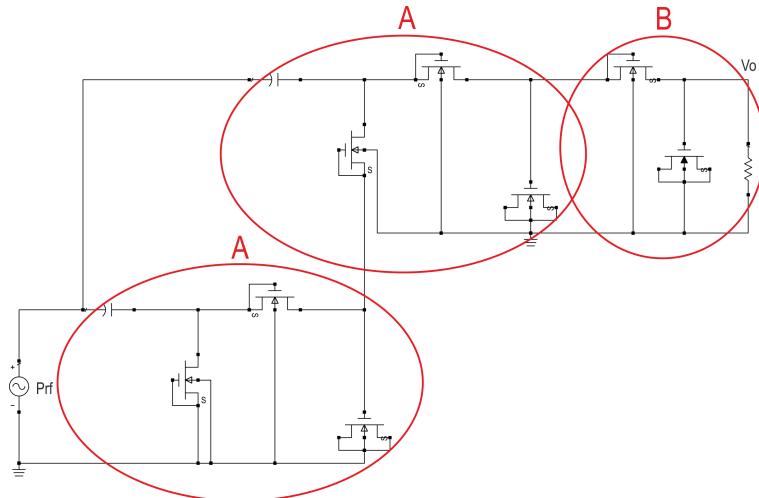


Figure 24: Schematic of the power rectifier for EH. A, unit cell of the rectifier; B, output low-pass with a load impedance corresponding to the power management circuit input impedance (only on the schematic for the simulations).

The layout of the unit cell of the power rectifier and the layout of the two stage power rectifiers are shown in Fig. 27.

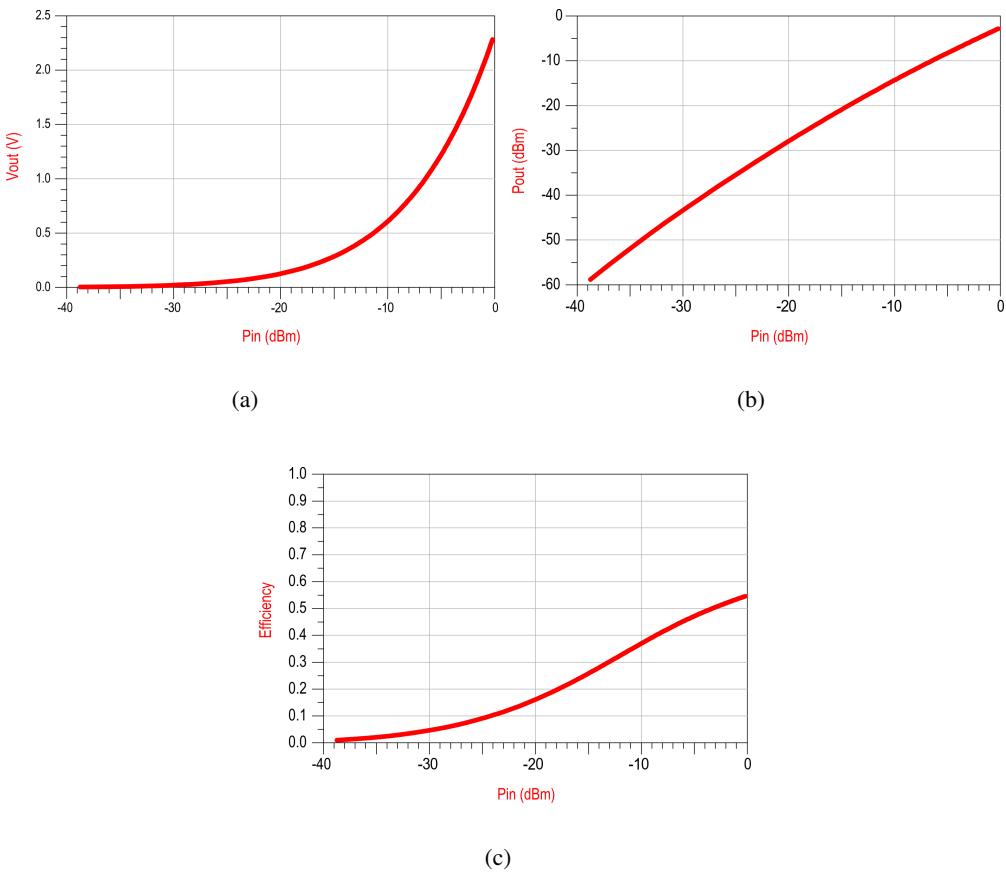


Figure 25: Simulation of the power rectifier for EH: output power (a), output voltage (b), and conversion efficiency (c) vs. RF input power.

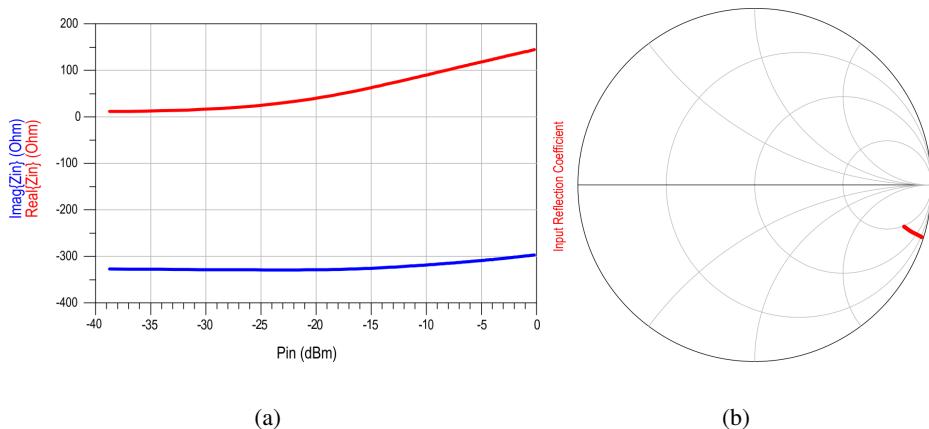


Figure 26: Simulation of the power rectifier for EH: (a) input impedance and (b) reflection coefficient vs. RF input power.

3.4.9 IC RF Subsystems: UHF Signal Rectifier for Demodulation

The signal rectifier is the first stage of the demodulator, in particular it acts like an envelope detector and its output signals, the envelop signal and the reference one, are sent to a comparator. Its schematic is shown in Fig. 28. Such as the previous rectifier, a 2-cells voltage multiplier based on LVT transistors

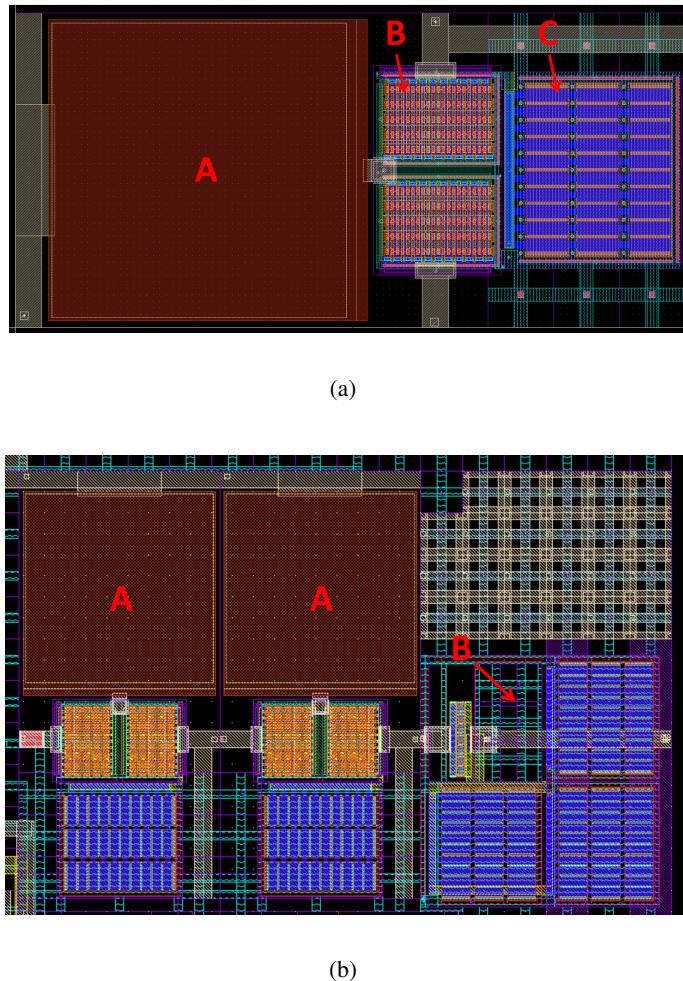


Figure 27: Layout of the unit cell of the power rectifier (a): A, MIM capacitor; B, low-voltage threshold MOSFETs; C, MOS capacitor. Complete layout of the power rectifier for EH (b): A, unit cell of the power rectifier; B, low-pass filter.

in diode configuration is adopted but it differs from the previous one for the presence of two low-pass filter, one per each stage, with different time constant. In particular, the low-pass filter with low time constant is connected to the second stage and generate the envelope signal; the low-pass filter with high time constant is connected to the first stage and generate the reference signal. Two series transistors in diode configuration are used as voltage limiters to protect the circuitry from high voltage levels.

The simulation results obtained with a harmonic balance simulation are plotted in Fig. 29. The output signal V_p and the reference output signal V_n are computed as a function of the RF input power for the signal rectifier in parallel with the power rectifier described in the previous section. The output signal is higher than the reference one and the effects of the voltage limiters can be noticed for input powers greater than -10 dBm.

In Fig. 30 are plotted the envelope simulations results. The two stage rectifier generates the output signals V_p and V_n as a function of an input modulated square pulse. In particular, the signals are analyzed for a modulated input signal with magnitude 0.2 V (only the envelope of the input signal is shown in plots). The output signal, V_p , is higher than the reference one, V_n , when the RF input is available (logic level is one) and it decreases more rapidly than the reference one when the RF input is not available (logic level is zero) thank to the different time constants of the output low-pass filters. The comparison of the two output signals is possible by means of a comparator with a threshold voltage introduced to avoid errors

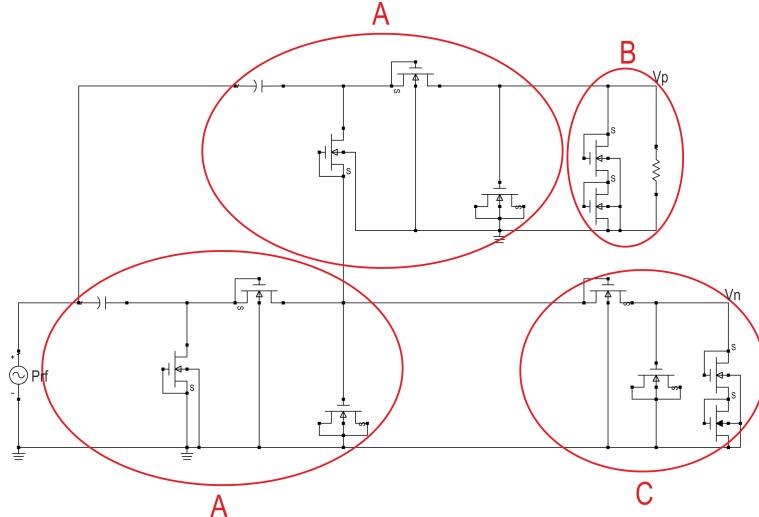


Figure 28: Schematic of the rectifier for demodulation. A, unit cell of the signal rectifier; B, output low-pass filter with low time constant; C, output low-pass filter with high time constant.

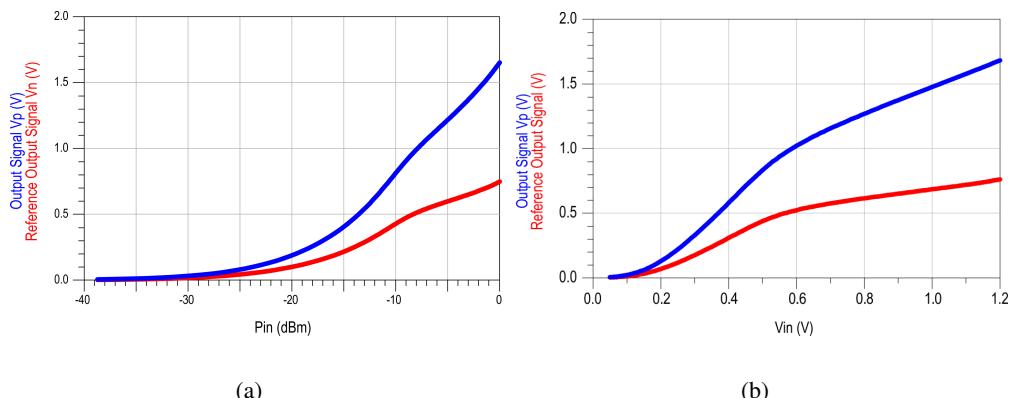


Figure 29: Simulation of the demodulator rectifier: output signal V_p and reference output signal V_n vs. RF input power (a) and vs. the RF input voltage magnitude (b).

when the output level are similar after a long time that the RF input is not available.

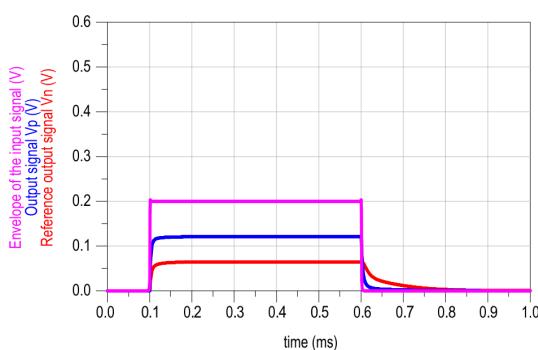
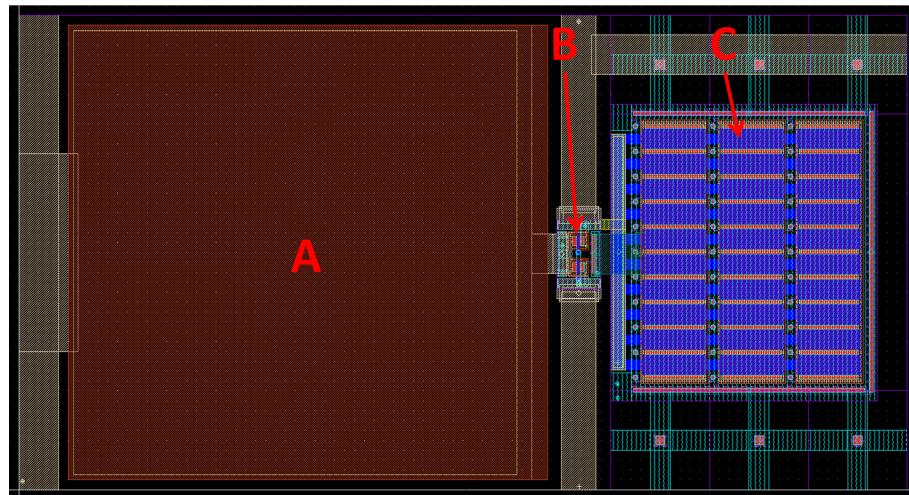


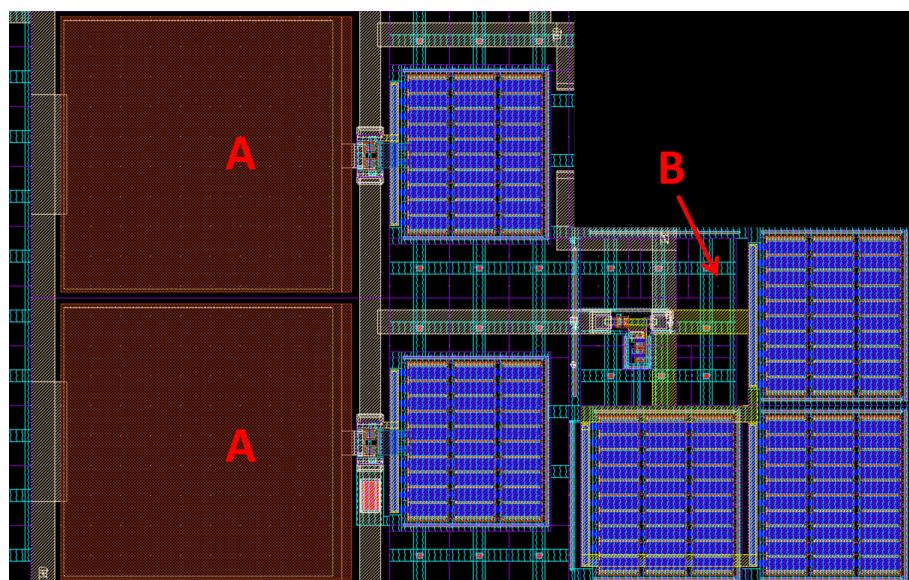
Figure 30: Simulation of the demodulator rectifier: output signal V_p and reference output signal V_n for a modulated input pulse of magnitude 0.2V.

The layout of the unit cell of the power rectifier and the layout of the two stage power rectifier are shown in Fig. 31. Unlike the power rectifier (see Fig. 27), optimized to obtain the best power efficiency,

in this case the transistor size has been reduced.



(a)



(b)

Figure 31: Layout of the unit cell of the signal rectifier for demodulation (a): A, MIM capacitor; B, low-voltage threshold MOSFETS; C, MOS capacitor. Layout of the signal rectifier for demodulation without the low-pass filter of the second stage (b): A, unit cell of the signal rectifier; B, first-stage low-pass filter.

3.4.10 IC RF Subsystems: Comparator for Demodulation

The comparator, used to compare the output signals generated by rectifier, is made of:

- a current generator;
- the comparator core.

3.4.10.1 Current generator

The current generator is used to bias the comparator core and it is based on a current mirror based on pMOS transistors. The current mirror (see Fig. 32) is able to provide on the load resistor (used only for the design) a current three times the current on the nMOS based reference load. The resistance of the nMOS channel is opportunely tuned with a voltage divider made of a cascade of five nMOS transistors in diode configuration.

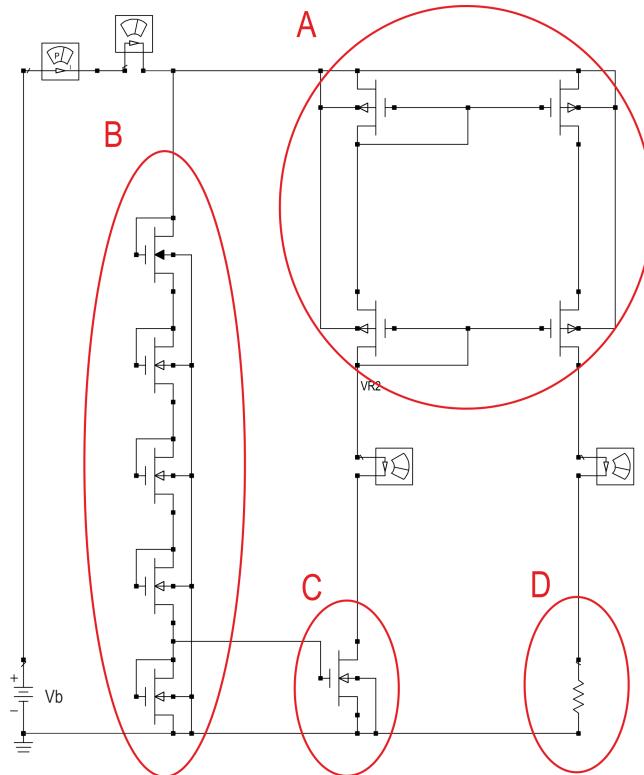


Figure 32: Schematic of the current generator. A, current mirror based on pMOS; B, voltage divider used to control C, the nMOS based reference load; D, load for simulations.

The performance of the current generator are shown in Fig. 33. The current provided to the load results constant by varying the load resistance in the range 1Ω - $10 \text{ k}\Omega$. In particular, for a bias voltage of 1 V, the current on the reference load transistor and on the load resistance is 30 nA and 150 nA, respectively, verifying the multiplication factor equal to 5. The current is a function of the bias voltage: at 0.8 V the provided current is about 50 nA and at 1.2 V it is about 400 nA.

The layout of the current generator is shown in Fig. 34.

3.4.10.2 Comparator core

The comparator core allows to compare the signals V_p and V_n (see Fig. 30) provided by the signal rectifier. Its schematic is shown in Fig. 35: the circuit is biased by the system bias voltage and by the current provided by the current generator. The use of a current generator allows the circuitry power consumption to be reduced, by providing the desired current that in this case is equal to 150 nA, and the branches connected to the bias voltage act as level converters. The output voltage is a logic one if V_p is greater than V_n and it is a logic zero if V_p is smaller than V_n , without considering a tolerance voltage. The comparator presents also a tolerance voltage, V_t , that is a function of the transistors dimensions N_1 and N_2 (in the present case the tolerance voltage is positive being N_1 size greater than N_2 size, in other words the logic one is obtained for $V_p > V_n + V_t$ and the logic zero for $V_p < V_n + V_t$) and also of other parameters such as the bias current.

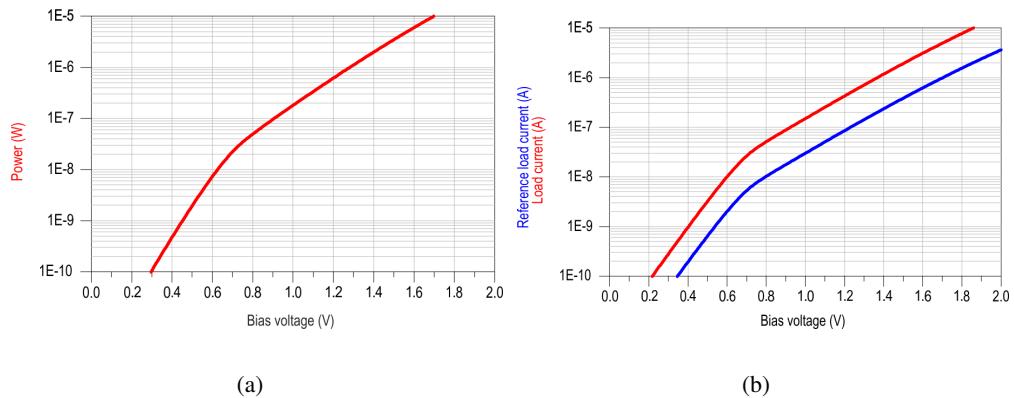


Figure 33: Simulation of the current generator (a): power consumption vs bias voltage. Simulation of the current generator (b): load current and reference load current vs bias voltage. The curves obtained by varying the load resistance in the range $1\ \Omega$ - $10\ k\Omega$ are overlapped in both cases.

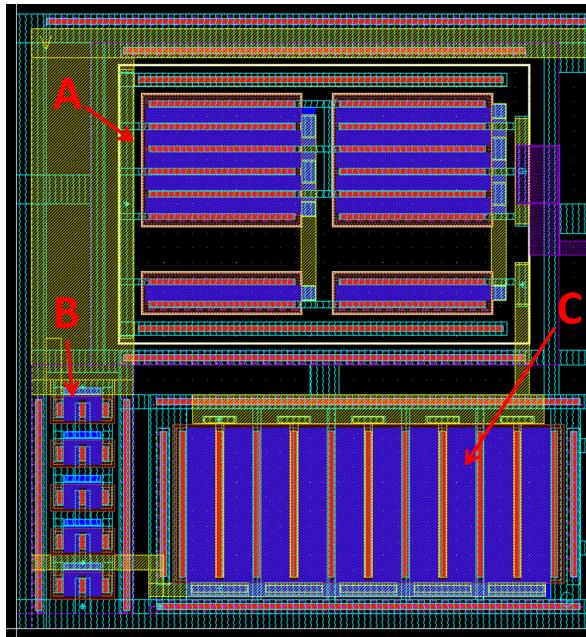


Figure 34: Layout of the current generator. A, current mirror based on pMOS; B, voltage divider used to control C, the nMOS based reference load.

Two analysis have been performed: static and transient. The static analysis results allowed to evaluate the static power consumption that is strictly related to the bias current provided by the current generator and in the simulated worst case it is about 160 nW. The results of the transient simulation, obtained by applying a square input signal V_p for different constant reference signal V_n (from 0 to 100 mV with a step of 25 mV), are shown in Fig. 36. The tolerance voltage allows to obtain an output equal to zero for V_p equal to V_n and it is equal to about 25 mV, evaluated by applying an input square signal with long transitions time (100 μ s). The delay of the output signal (see Fig. 36(a)) is due to the comparator circuitry and the threshold voltage; however, the contribution of the only circuitry can be evaluated by applying an input square signal with negligible transitions time (1 ns) and it is equal to 340 ns in the worst case and to 120 ns in the best case for evaluating both the high-to-low and the low-to-high transitions. The use of output inverters allows to reduce the “smoothness” of the comparator output introducing a negligible delay as shown in Fig. 36(b).

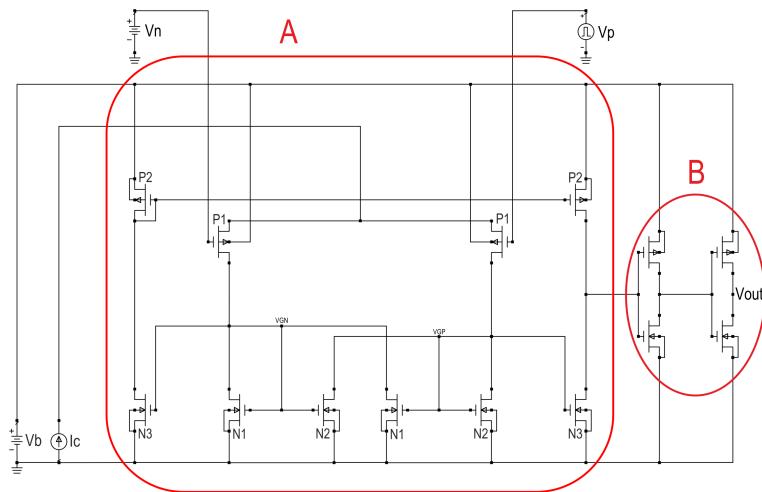


Figure 35: Schematic of the comparator core. A, comparator circuitry; B, inverters for output levels conditioning.

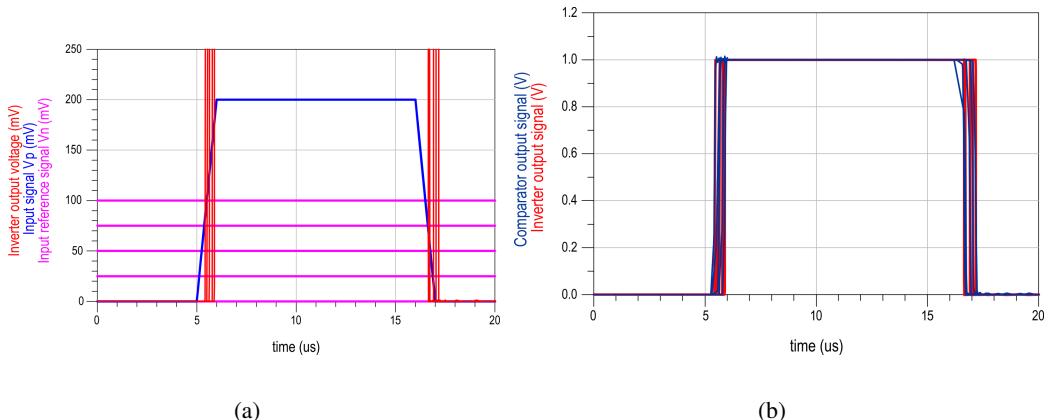


Figure 36: Transient simulation results of the comparator core obtained by applying a square input signal V_p for different constant reference signals V_n (from 0 to 100 mV): (a) input signal and output inverter signal; (b) comparator vs inverter output signal.

The layout of the comparator core is shown in Fig. 37.

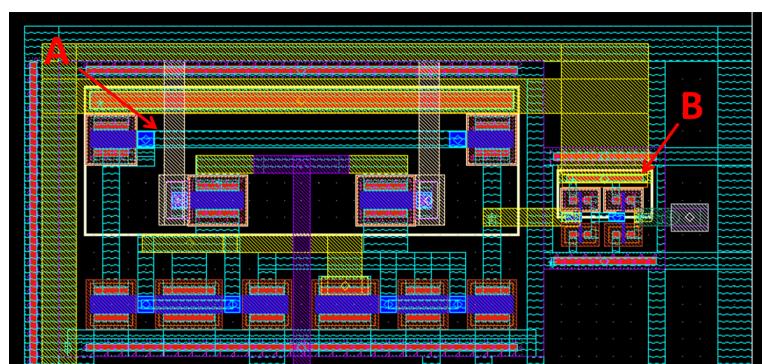


Figure 37: Layout of the comparator core. A, comparator circuitry; B, inverters for output levels conditioning.