A Low Latency Library in FPGA Hardware for High Frequency Trading (HFT)

Analysis and implementation

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HFT involves

- Using computers to place orders based on pre-defined algorithms

Traders

Definition

A trader is an individual who engages in the buying and selling of financial assets in any financial market, either for himself or on behalf of another person or institution.

[1] Overnight positions refer to open trades that have not been liquidated by the end of the normal trading day, which are quite common in foreign exchange and futures markets.

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What's the difference between a trader and an investor?

- A trader holds an asset for a shorter period of time to capitalize on short-term trends; investors use also overnight positions.[1]

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Trading venues make current pricing information available as continuous streams of electronic data then:

- Traders monitor these streams of data, asking for relevant stocks and assets to determine when and what to trade
- Exploiting fleeting variations in stocks price they accumulate profit by making tiny gains on large numbers of transactions.

Traders

In practice:

[2]The term order book refers to an electronic list of buy and sell orders for a specific security or financial instrument organized by price level.

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- The final step is to enter these orders into the exchange via a broker

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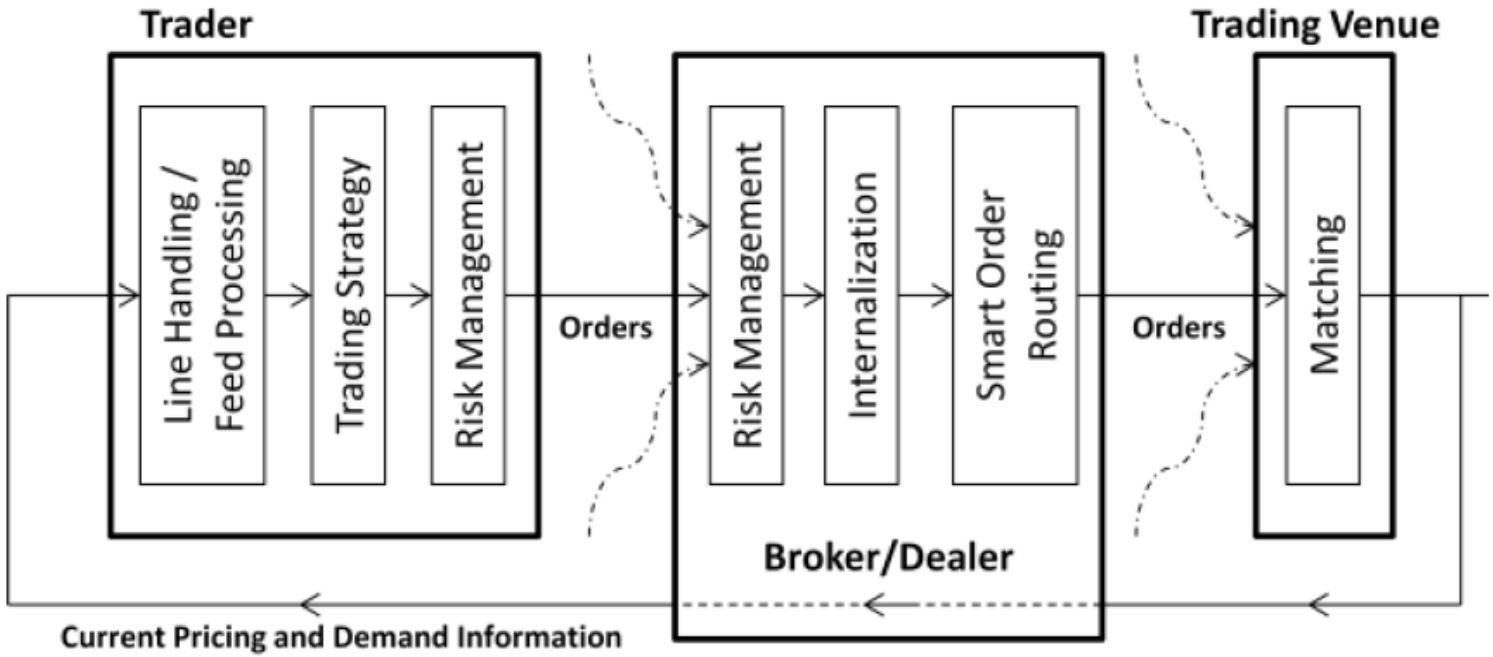
- They match orders from different clients with each other internally, without sending them to the exchange

From traders to exchange path

Block diagram of traders, brokers and venues



Challenges in Financial Markets

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- Throughput: it implies handling large volume of data

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Secondary challenges

- Throughput: it implies handling large volume of data
- Flexibility: due to the sudden and persistent change of the market it allows to adapt to changing risks and trading strategies

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To reduce this source of latency, providers are implementing network interface cards that allow to bypass the operating system kernel.

Hands on latency data, current approaches

Software

1. Linux 10GE NICs
   - $15 - 20$ μs for Half-Round Trip Time through un-optimized kernel
   - TCP Offload: 2.9 μs Transmit $+6$ μs Receive for half round trip
2. Datagram Bypass Layer (DBL)
   - $3.5\mu s$ for UDP and $4.0\mu s$ for TCP
3. Infiniband MPI
   - $1\mu s$ (excluding application layer)

Hardware

1. Graphics Processor (GPU)
   - Optimized for throughput, but not optimized for low latency
   - Incurs additional overhead of passing data through PCIe bus
2. ASIC
   - Achieves sub-μs latency
   - But lacks flexibility to handle new protocols and features
3. FPGA
   - Provides $0.2\mu s$ latency w/TCP
   - Has the flexibility to support new protocols and features

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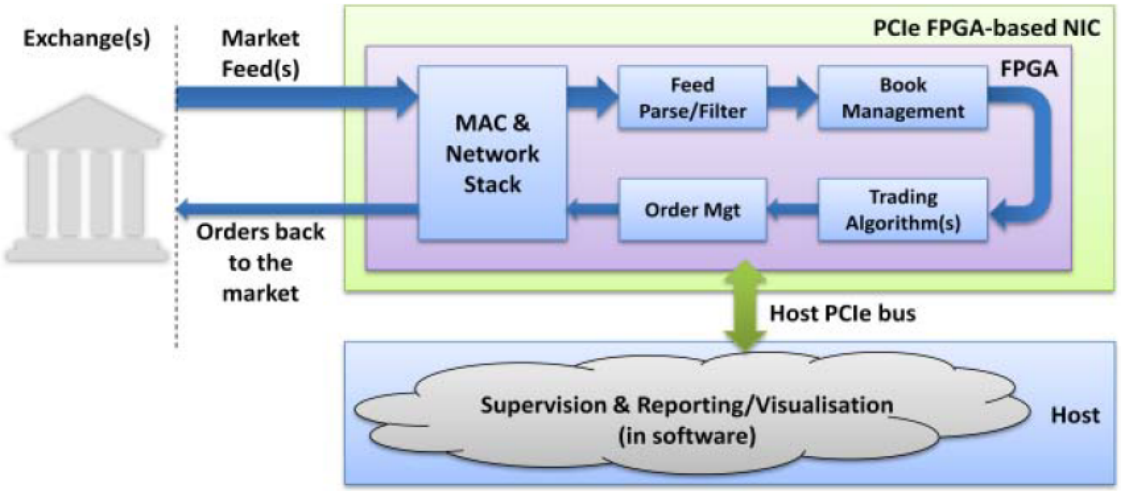
Advantages

- CPUs introduce power processing cores, large multi level caches and are best suited to control-intensive parts of an application
- FPGAs perform best at non-floating-point tasks such as integer, binary, character or fixed-point data processing

Smart-NICs based hybrid computing

- CPU is connected to one or more FPGA modules via PCIe bus



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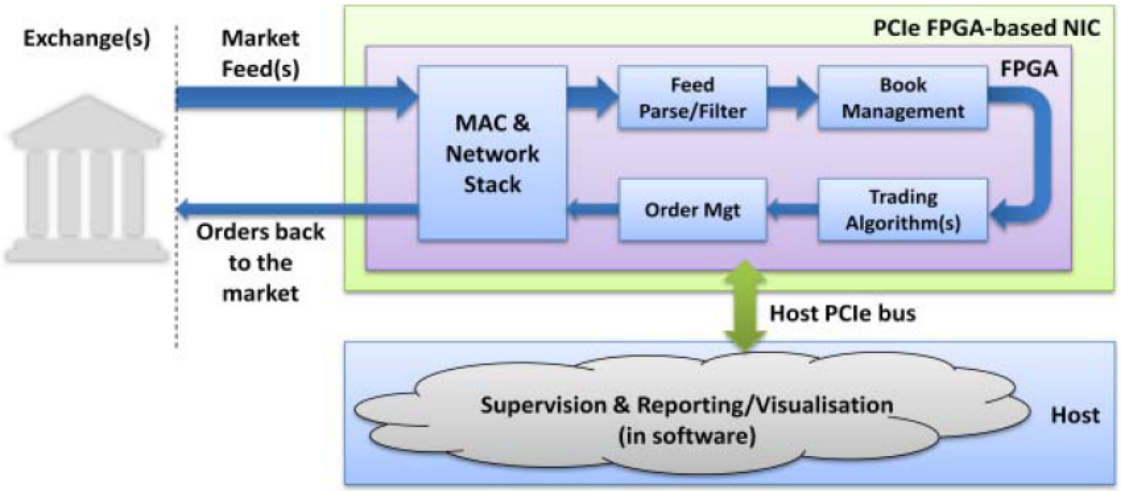
- CPU is connected to one or more FPGA modules via PCIe bus
- FPGA-based NICs can turn around financial trades with a predictable latency of 2.7μs (considering the NASDAQ protocol)



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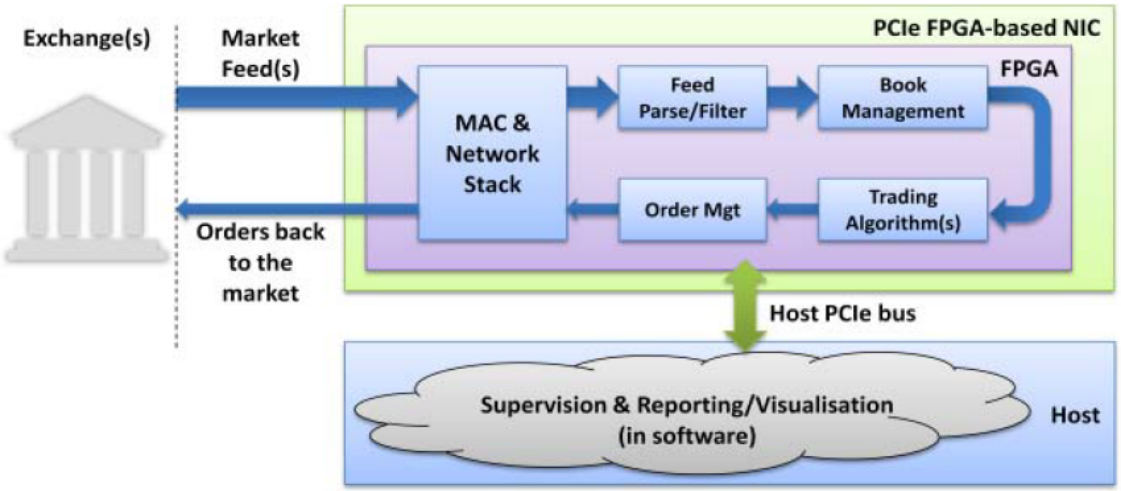
- The software counterpart without kernel bypass displays a value of $38 \pm 20\mu s$



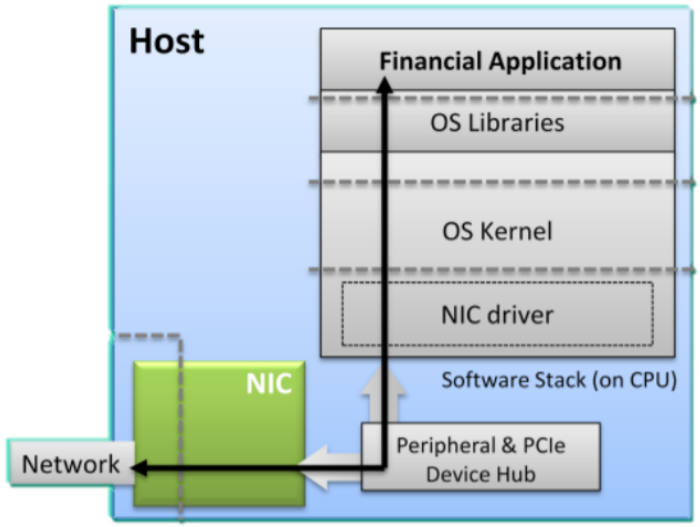
Smart-NICs based hybrid computing

Disadvantages

Requiring network traffic to be received on a network adapter implies:

- Unpredictable PCIe bus transfer: processes could be piled up before executed even if FPGA work in parallel pipelines, increasing execution time
- Memory copy
- Potential cache misses
- Amdahl's law

CPU + NIC + FPGA Offload



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Packet reading: In contrast with software-based approach there are:

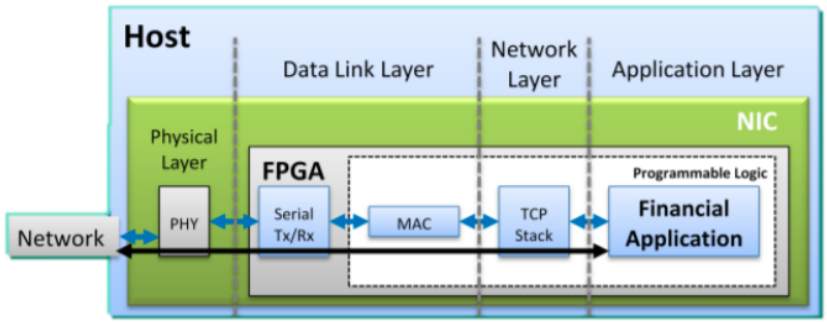
- No bus copy
- No memory copy
- No cache misses
- No parallel execution limitations
- No interrupt-driven software stacks

Pure FPGA computing

Advantages

- The incoming network data is fed directly into an application-specific processing pipeline via hardware PHY and MAC blocks.

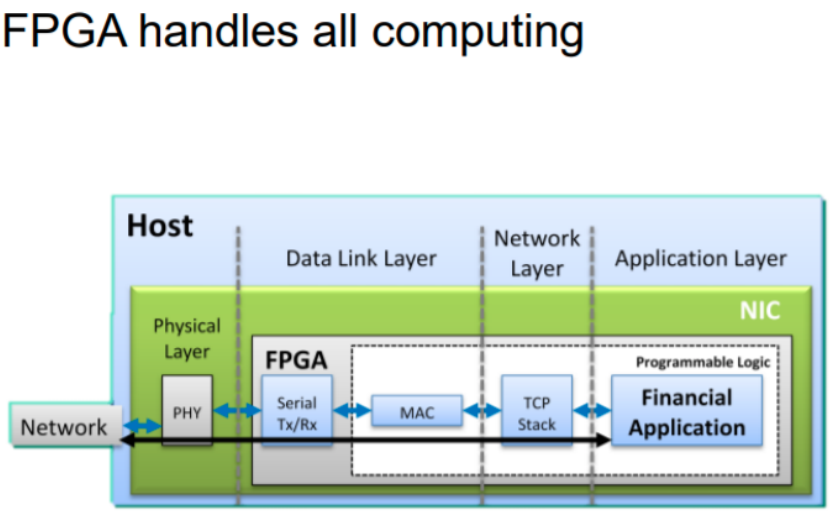
FPGA handles all computing



Pure FPGA computing

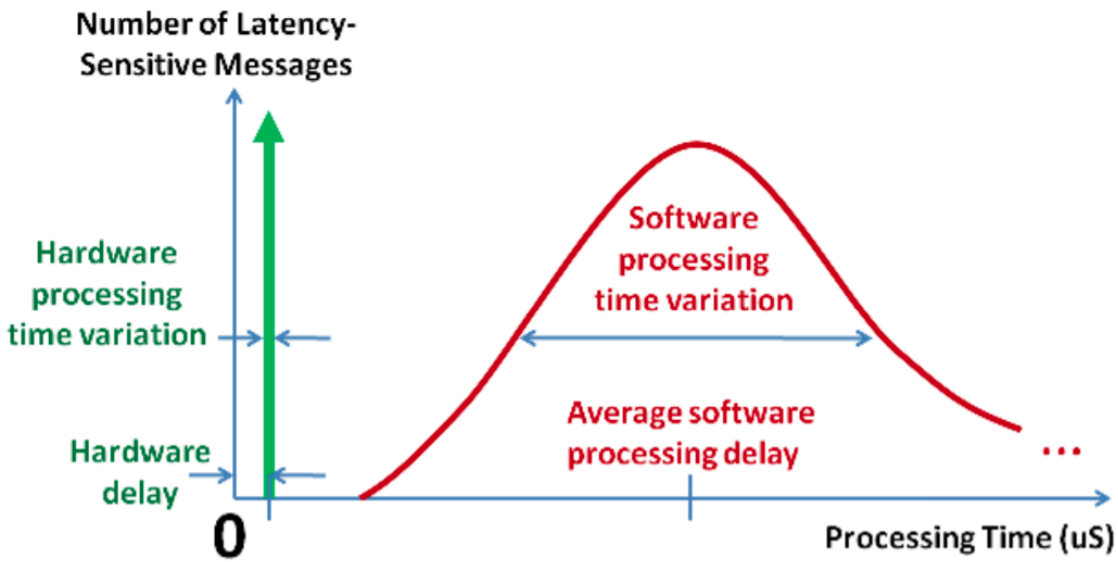
Advantages

- The incoming network data is fed directly into an application-specific processing pipeline via hardware PHY and MAC blocks.
- Relevant information within a packet can in fact be extracted before the complete packet is received, and the available bit-level access to incoming data greatly simplifies protocol parsing (a task tedious to describe using a standard programming language).



Pure FPGA computing

- The availability and the processing time for any piece of information is completely predictable down to a clock cycle



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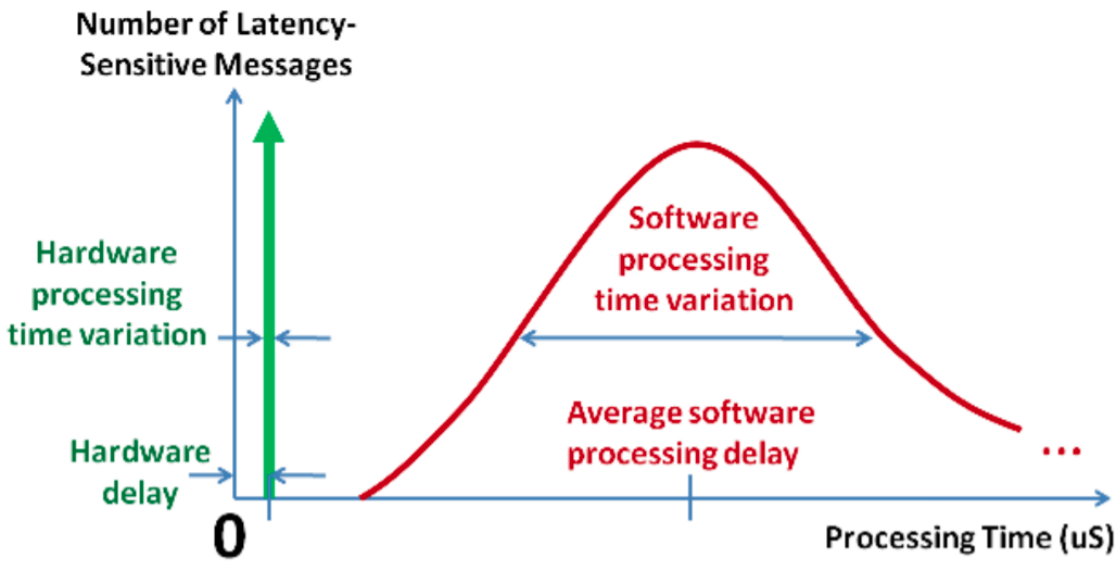

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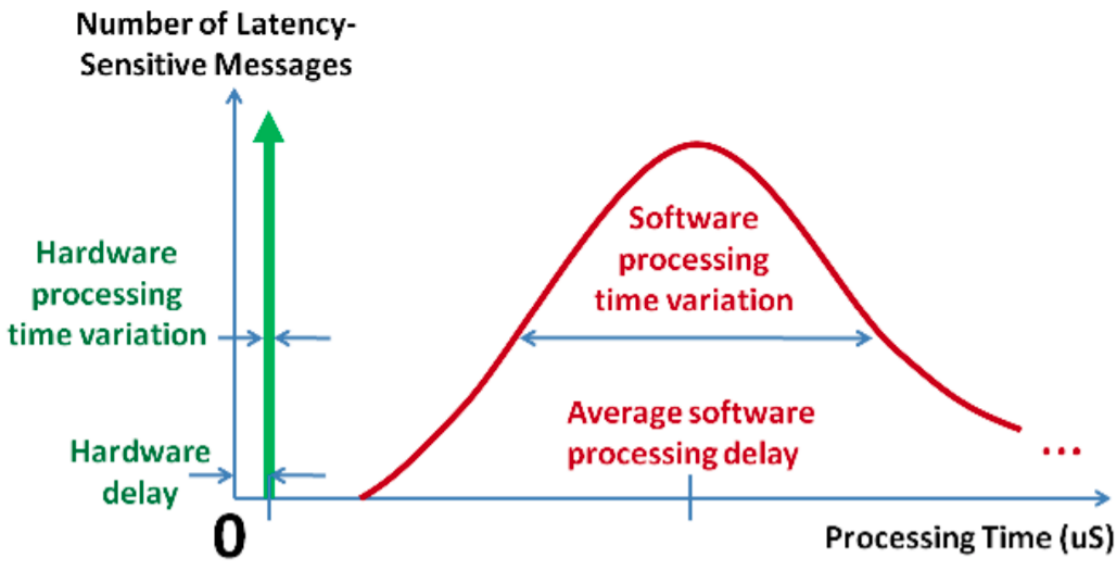
- Flexibility: long-lived trading strategies



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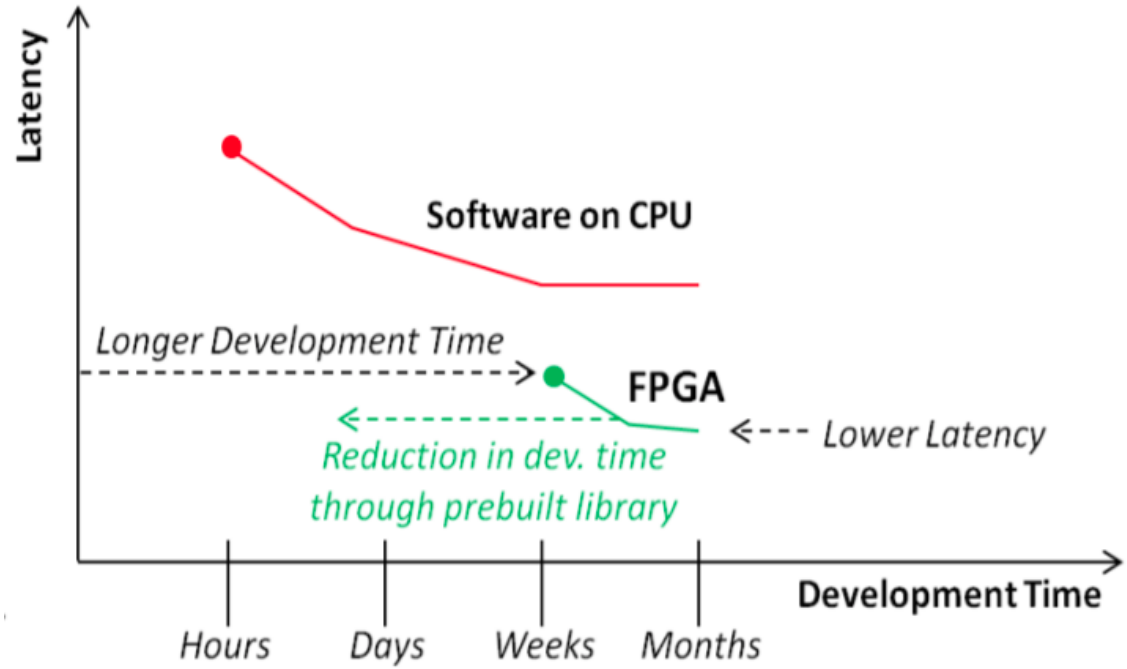

Pure FPGA computing

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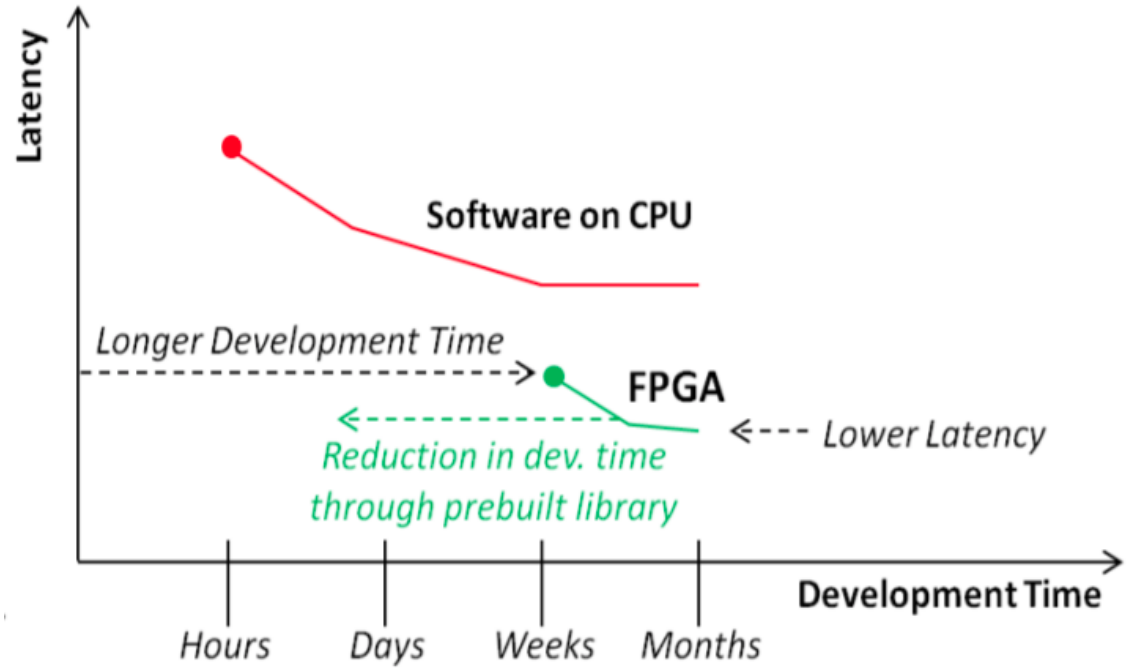
- Greater complexity of the development flow: building and verifying new hardware is more time consuming
- Many developers of financial applications are unfamiliar with FPGA technology and HDL



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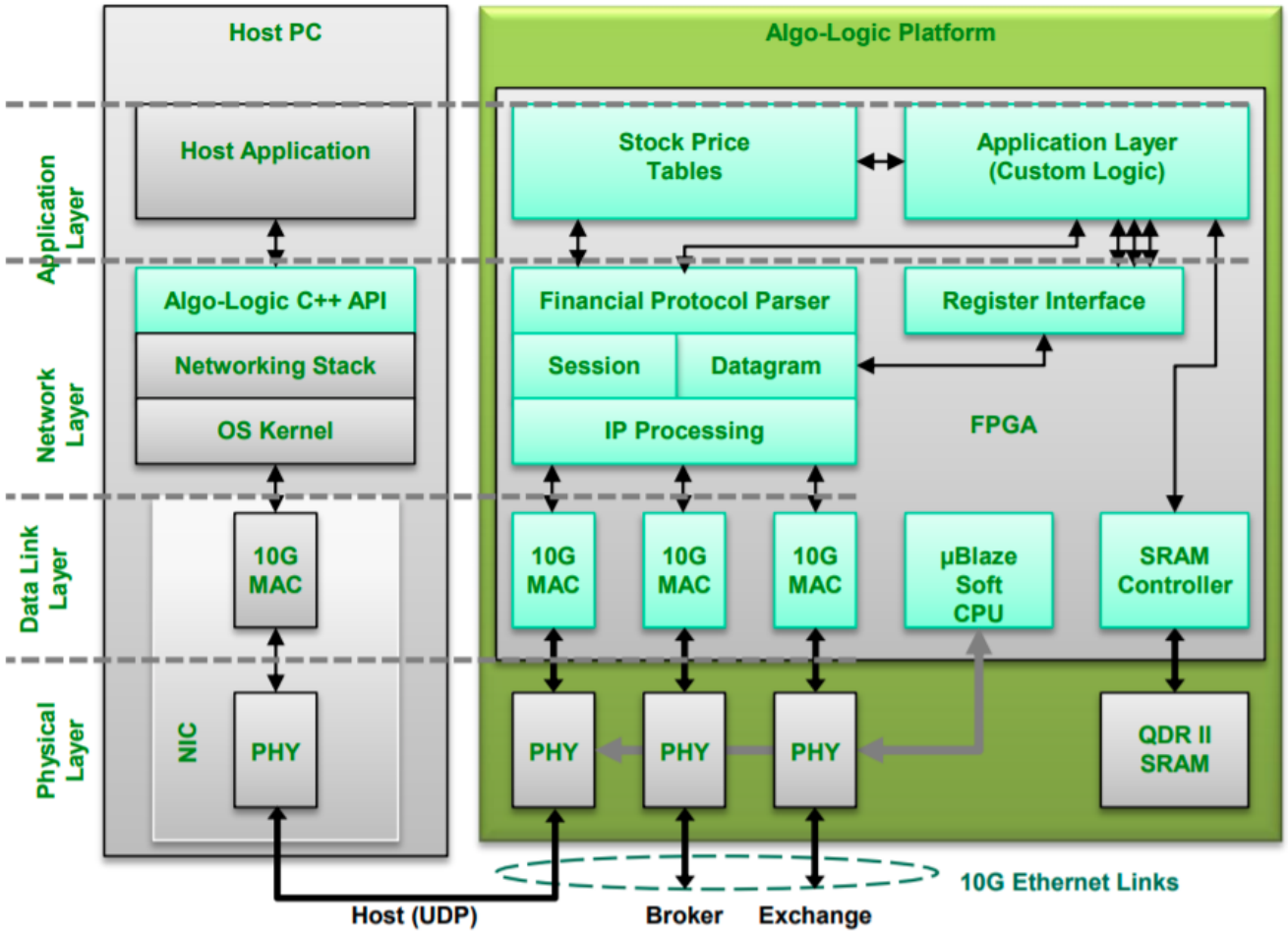
- The library components are used to construct custom trading applications, reducing time-to-market

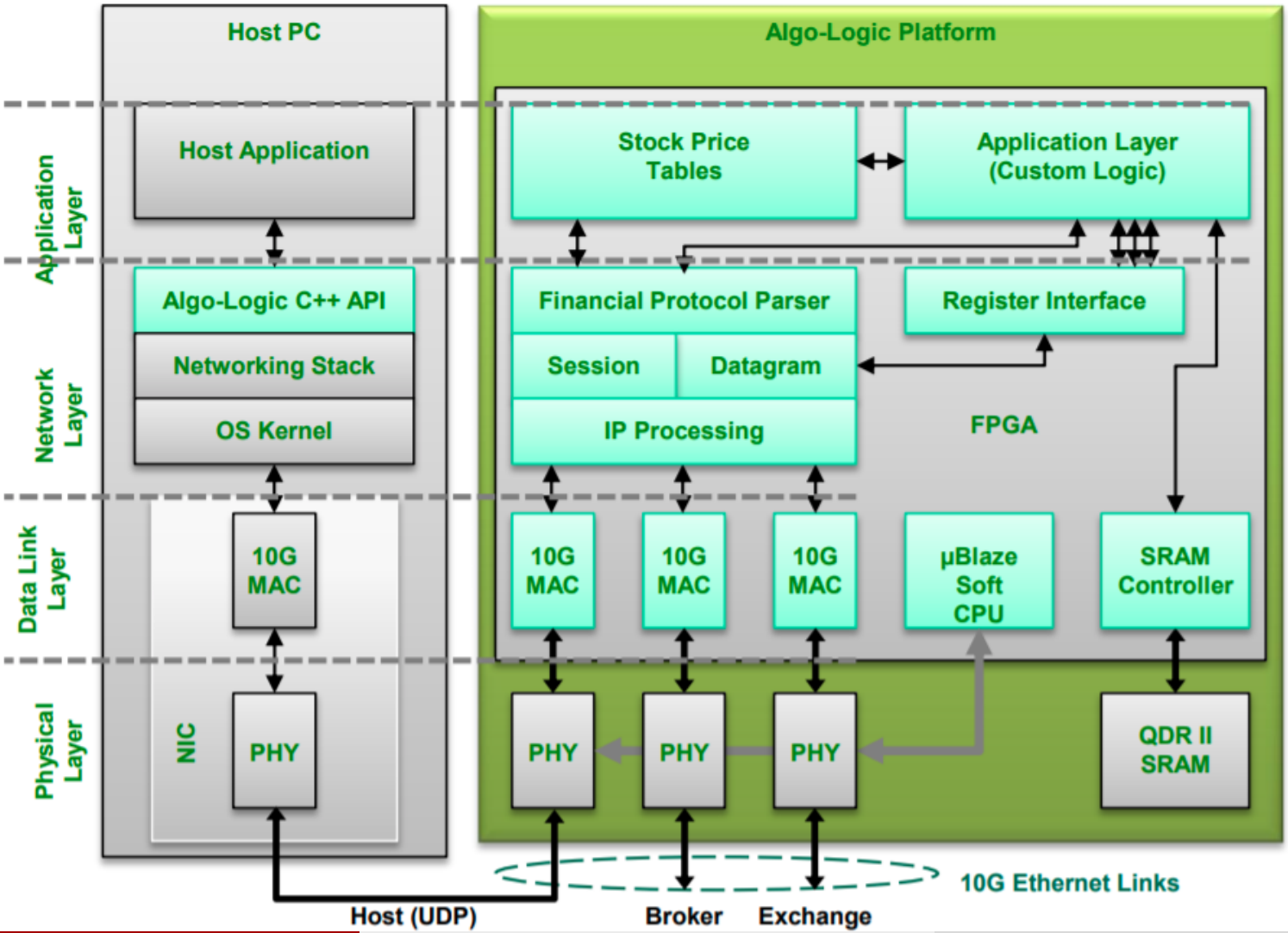
IP blocks categories

1. Infrastructure Components
2. Financial Processing Components



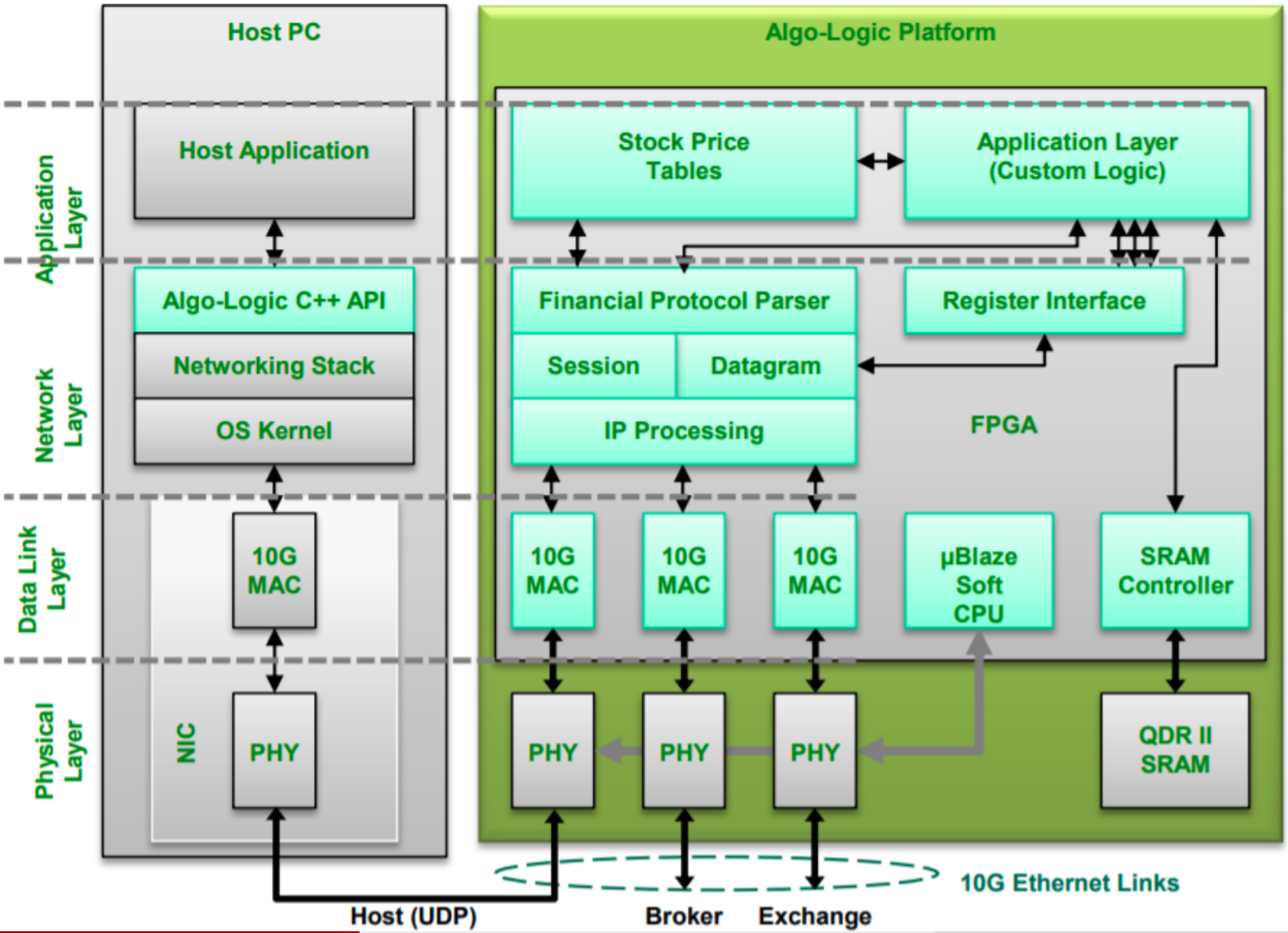
1-Infrastructure components

- All components share a common 64bit data word and AXI4 stream protocol



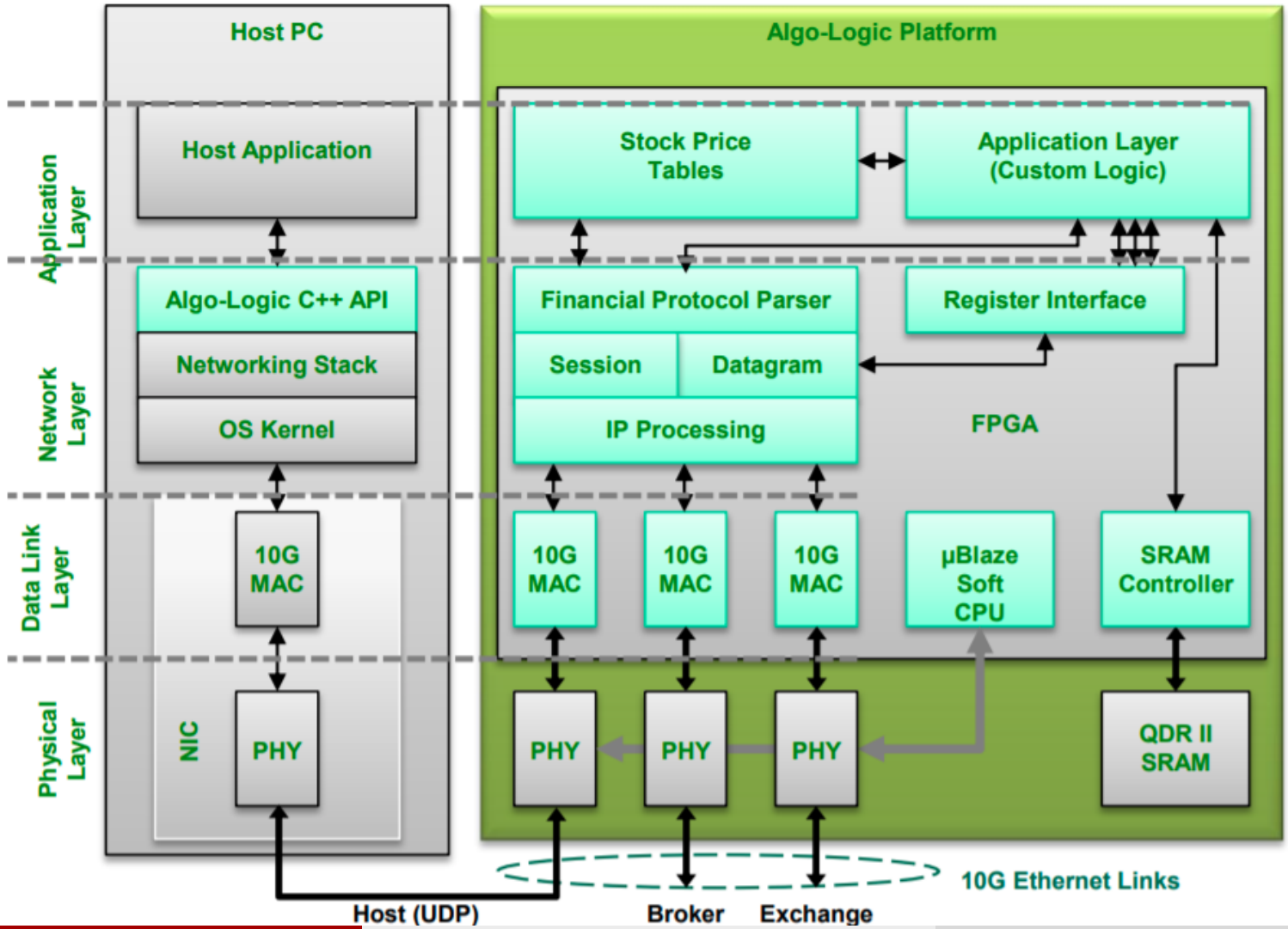
1-Infrastructure components

- A Register Interface module controls and monitors the status of registers written and read by host software



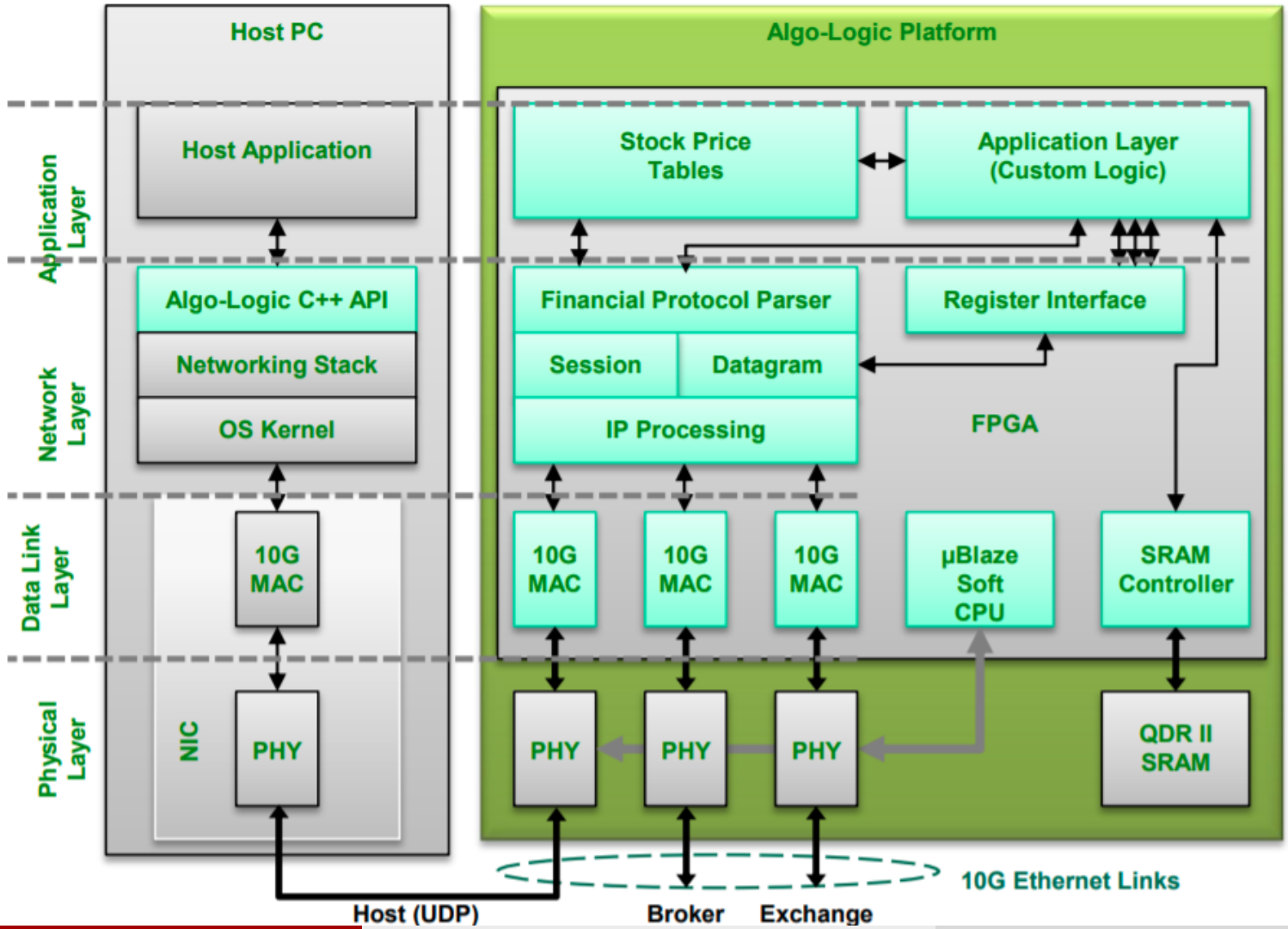
1-Infrastructure components

- TCP/IP separates headers from payloads(according to the financial protocol) and sends the payloads to the application layer



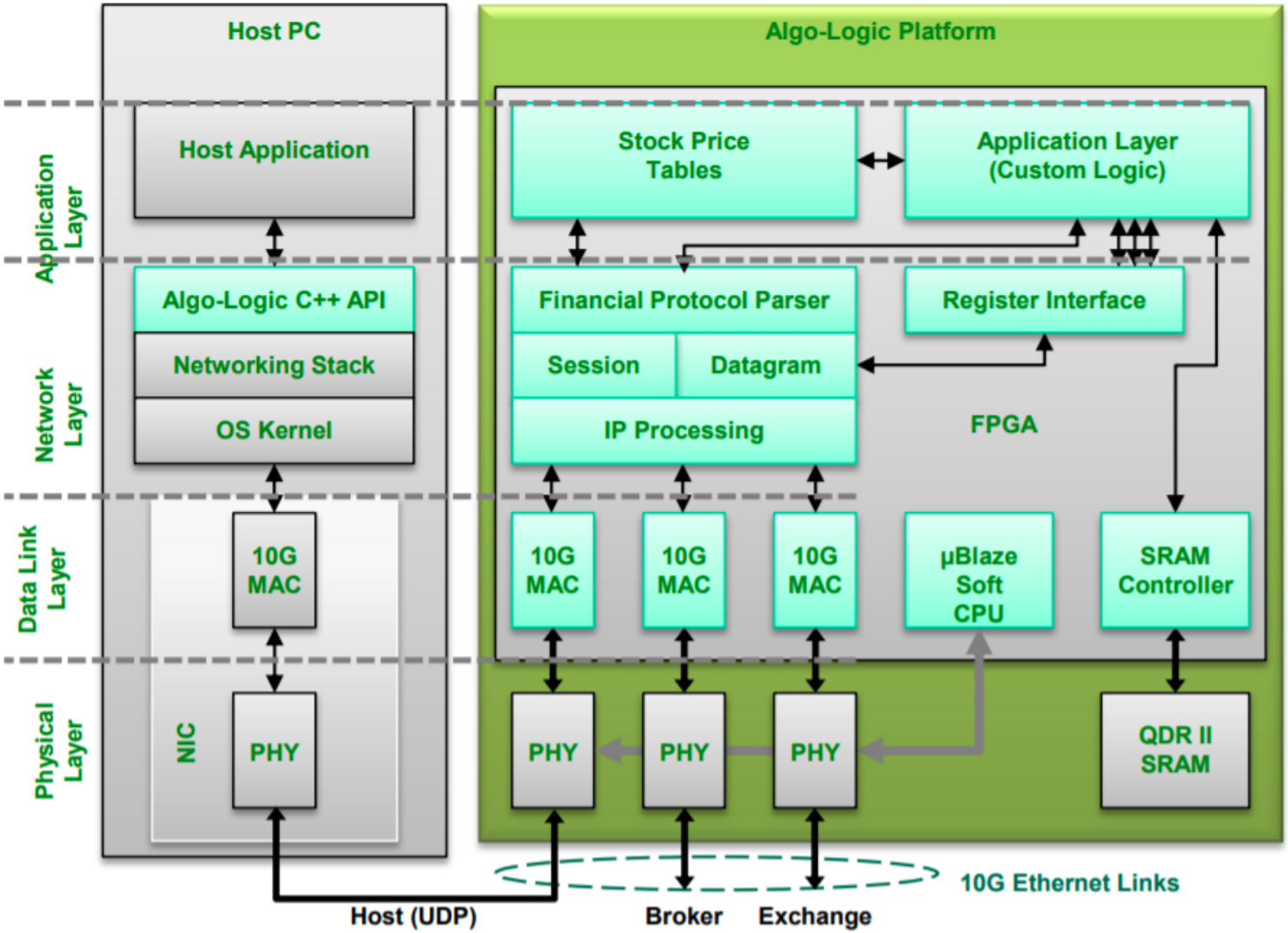
1-Infrastructure components

- Application layer processes packet payloads and sends them back to the TCP/IP layer



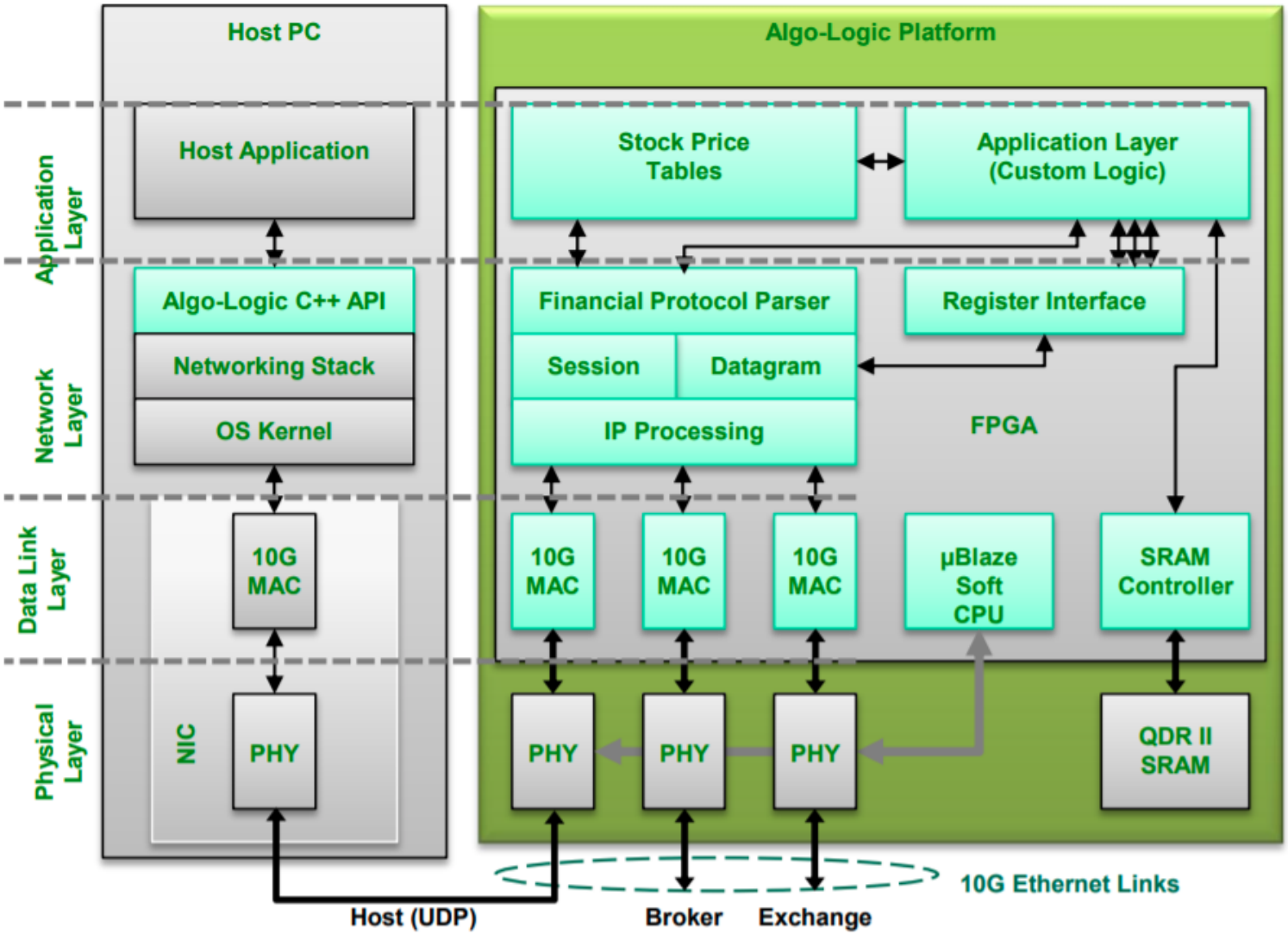
1-Infrastructure components

- TCP/IP reassembles headers and payloads and performs a checksum



1-Infrastructure components

- QDR (quad data rate) II SRAM is used in order to store prices of other stocks or historic data



2-Financial processing components

- Algo-Logics library includes IP blocks designed to process application layer messages for HFT.
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There may be distinguished the following components:

1. Financial protocol parser
2. Market data parsing and on-chip storage for price data

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Protocols

- **FIX** Financial Information eXchange
- **OUCH** NASDAQ
- **XPRS** DirectEdge
- **BOE** BATS BZX
- **ArcaDirect** NYSE Arca
- **Native Trading Gateway** LSE

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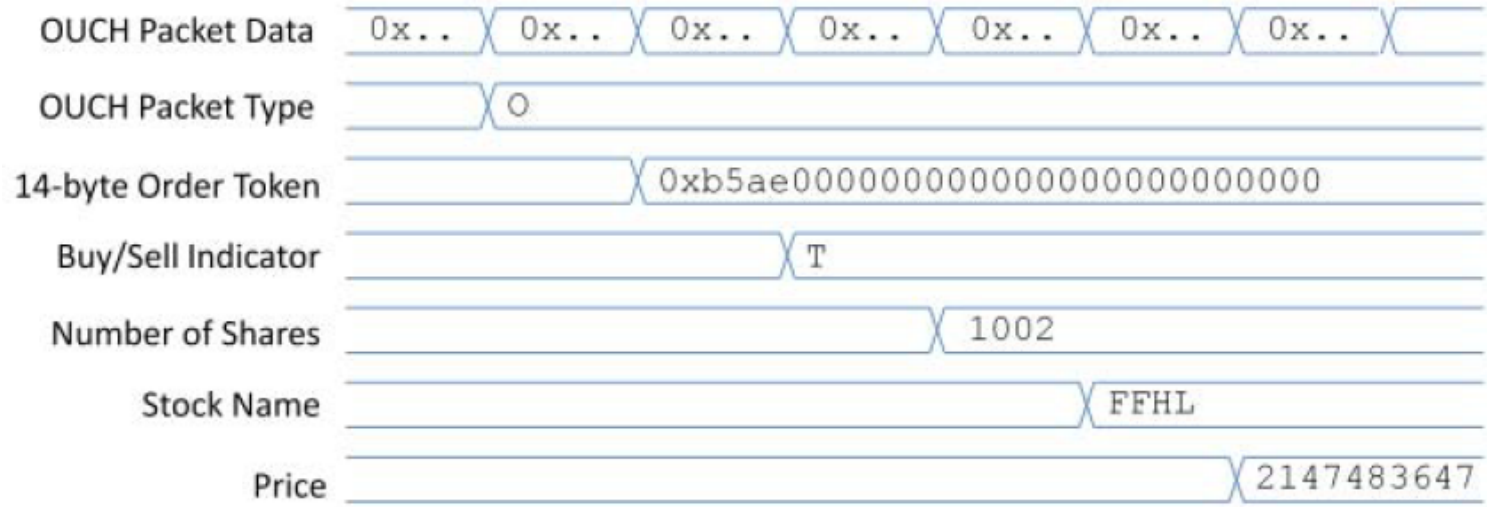
- the circuit extracts all OUCH packet fields within exactly 6.4 nanoseconds of the packets arrival with no jitter



Market data parsing and on-chip storage for price data

Observation

In financial processing applications need to know in real time the price of securities that appear in the orders.

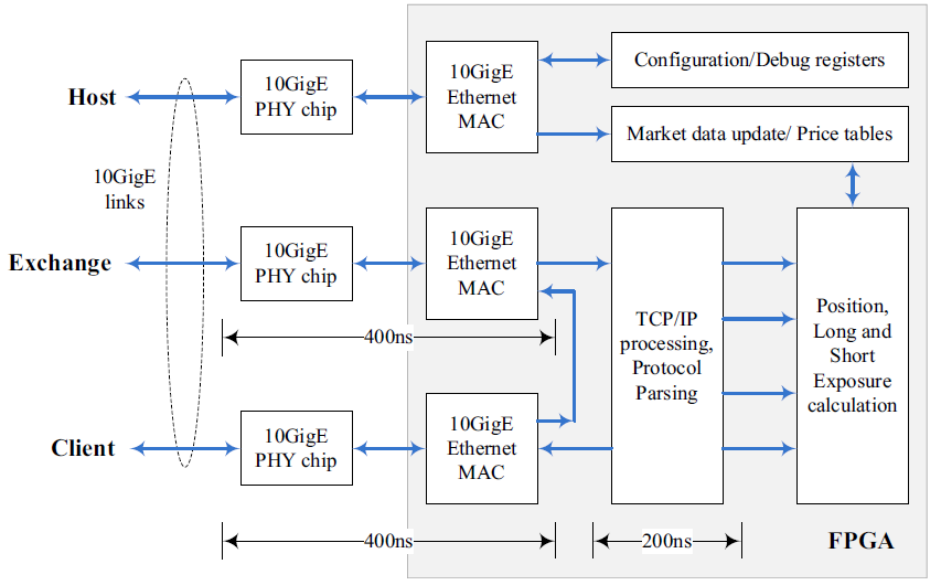
To track them:

- Market data is fed into the card via UDP/IP datagrams
- When they are exctracted they are stored on chip-in memory (8000 securities traded on U.S. Exchanges fit within the FPGAs on-chip memory)

FPGA implementation on NetFPGA-10G

Observation

AlgoLogics system acts as a bump in the wire between broker and exchange, processing the FIX execution reports coming from the exchange while passing on orders coming from the involved brokers. A third 10GE interface connects the appliance with the control and logging host.



Total wire-to-wire delay = 1µsec.
(400ns (PHY+MAC) + 200ns (Logic processing) + 400ns (PHY+MAC))

FPGA implementation on NetFPGA-10G

1. The design includes three instances of the 10GE MAC to interface to the host, the broker and the exchange

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4. Traffic from brokers and FIX execution reports from the exchange are passed from the MACs to the TCP/IP processing module

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2. The host interacts via the configuration/debug register module and can access the market data update/price table module
3. Current market prices for each security are received via UDP from the exchange and stored within on-chip memory
4. Traffic from brokers and FIX execution reports from the exchange are passed from the MACs to the TCP/IP processing module
5. The Exposure and Position calculation module receives the traffic from the TCP/IP module and updates the market data/price tables

FPGA implementation on NetFPGA-10G

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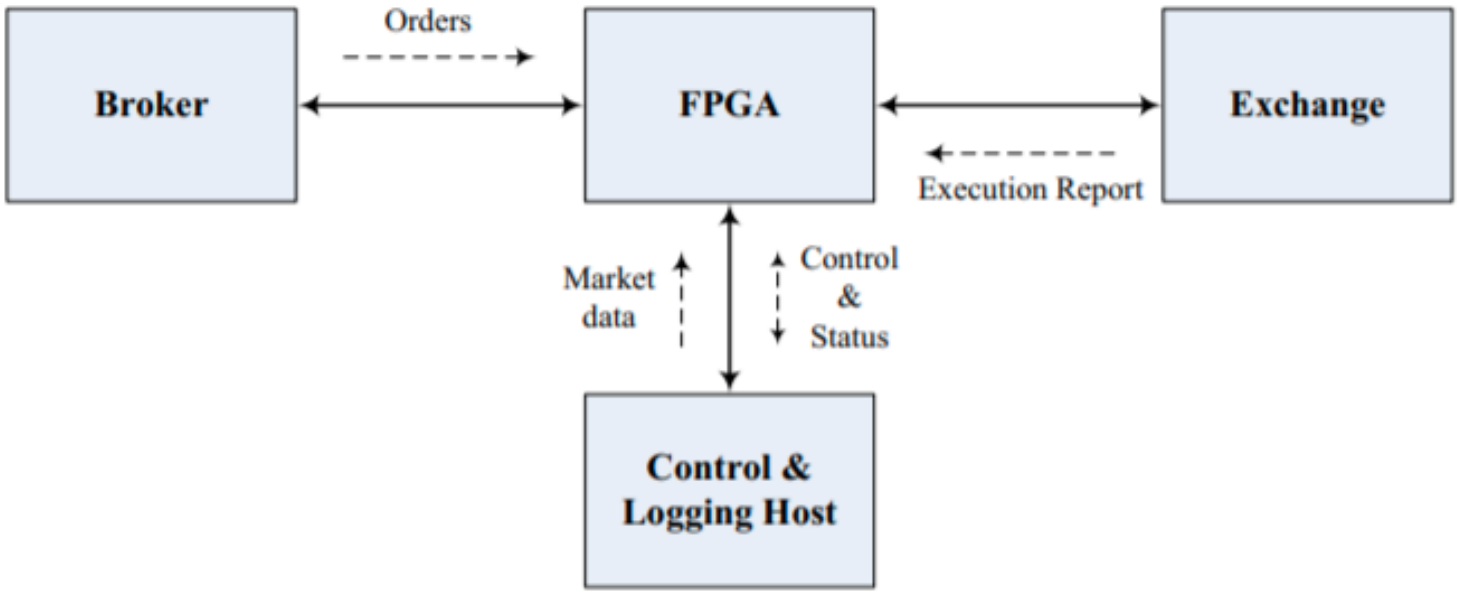
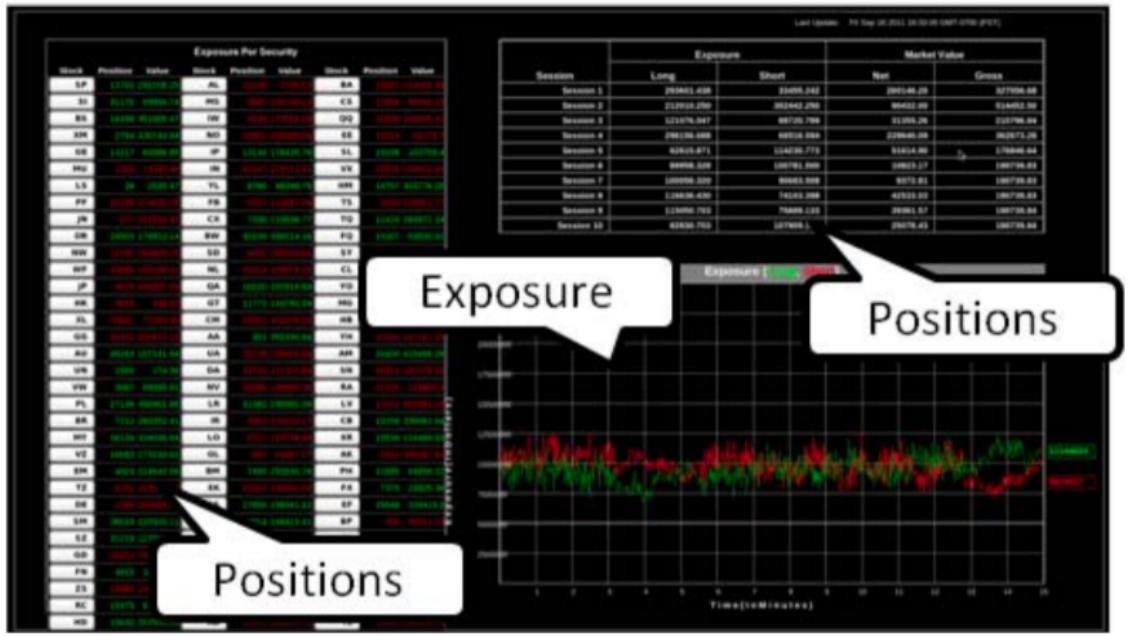
4. Traffic from brokers and FIX execution reports from the exchange are passed from the MACs to the TCP/IP processing module
5. The Exposure and Position calculation module receives the traffic from the TCP/IP module and updates the market data/price tables
6. Finally, the FIX execution reports are forwarded to the clients providing details of order execution

Implementation block diagram



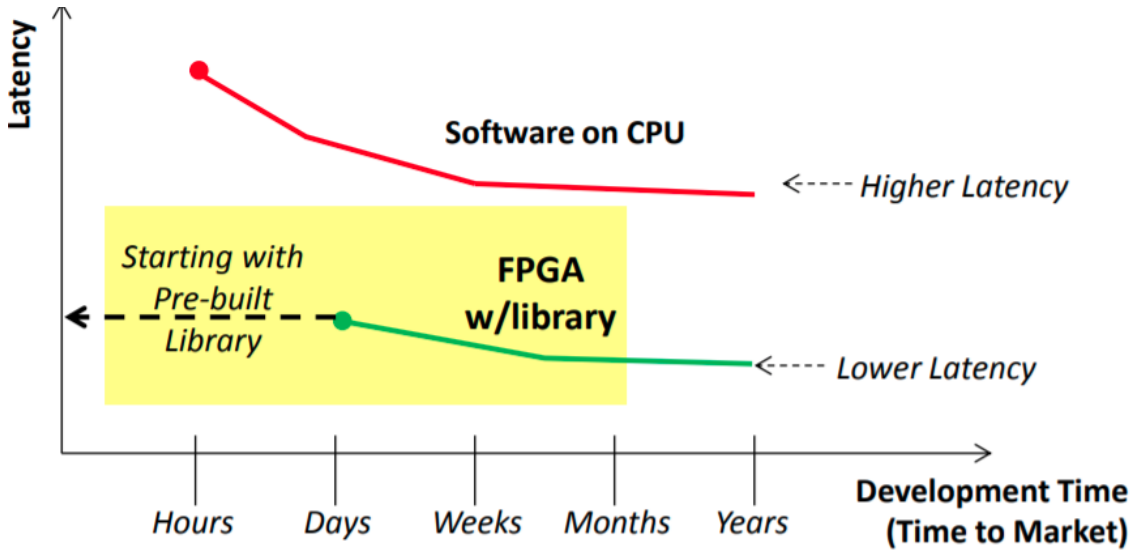
GUI

Web-based GUI showing Exposure and Position



Contents

Results



- The total wire-to-wire latency in this application is $1\mu s$ with liertally no jitter
- It is worth noting that the $1\mu s$ round-trip latency through this design is between one and two orders of magnitude lower than a recent software implementation
- The throughput is roughly $6.1M$ FIX messages/second

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