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Specification and simulation of digital systyems

The “Fm receiver” project is a digital frequency modulated receiver, projected using the hardware description language vhdl for the Zybo board, where we will use its integrated fpga and analog to digital converter.

The main component is the demodulator, who takes in input 12 bit samples from the XADC, eventually connected to an antenna, and outputs demodulated 12 bit samples.  
After that, the low pass filter removes the output noise generated by the digital elaboration (sampling and demodulation).

Finally, the 12 bit samples could be sent to a digital to analog converter and played with an attuator.  
Like described later, we propose two different internal designs for the demodulator: the first, classic pll, acts like a digital phase locked loop, based on a quadrature of the input signal, while the second, dpll, use a mechanism based on exor and an integrator to demodulate at a fixed frequence.

In both cases the demodulator was designed to obtain signals at 125 Khz, so will not work for classic italian radio frequencies (87 Mhz – 106 Mhz). This is due to the limited maximum clock frequency of the Zybo board, that is 1 Mhz.

1. 1-bit preamplifier with hysteresis

This component receives 12 bit samples from the external xadc, and every clock tik simply outputs a bit, representing the sign of the sample. Internally, the component use a hysteresis mechanism to partially eliminate the high frequency noise. The hysteresis threshold is fixed and the best value was chosen after digital simulations.

The behavior is simple: for each interval where the next input will be and for every value of the last input, the output will be 0 or 1. So there arefour possible cases, and four “if” conditions.

Obliviously, if the “rst” signal is 1, the output will be 0 for every input value.

1. Entity demodulator

This entity, internally described using structural description, represents the phase locked loop (pll) used to demodulate the signal.

Because of the two different approaches we found to obtain the result, there are two different possible architectures: the first (classic pll) uses feedback mechanism, while the other (the Dpll) doesn’t need it and produces better results in simulations.

1. Entity FM receiver

This entity, internally described using structural description, represents the top level desin of the circuit, that get input samples and produces output demodulated samples

The architecture is simple, because is just the combination of a demodulator, described above, and the final low pass filter.

4) Low pass filter

This component is a 12 bits third order low pass filter and is the last stage of the fm receiver. The filter takes in input the signal coming from the demodulator. The filter is designed using a butter filter model whose coefficients were calculated with Matlab, and cuts frequencies higher than 15 KHz.

The filter is a "Direct Form II Transposed" implementation of the standard difference equation:

a(1)\*y(n) = b(1)\*x(n) + b(2)\*x(n-1) + ... + b(nb+1)\*x(n-nb) - a(2)\*y(n-1) - ... - a(na+1)\*y(n-na)

b = 0.0005 0.0011 0.0005

a = 1.0000 -1.9334 0.9355

a(1) is 1 because the filter was normalized and his gain is unit.