ECS615U Digital Systems Design Lab 1

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October 26, 2016

Contents

1 Introduction

The aim of this lab was to introduce us with the basics of the VHDL language, ISim and programming to the FPGA board. We tackled the task of creating different gates at the lowest level so we can use these building blocks for later labs at a higher level. We witnessed how to use simple gates in a half and full adder to get a taste of what's to come.

2 Method

1. VHDL source code written for each gate
2. Test bench file written for each gate
3. Simulation of the test benches using iSIm
4. Screenshot result
5. Recording and verifying that the simulation matches the expected results
6. Constraint files created with PlanAhead for each VHDL source code
7. Constraint files and source code files programmed to the FPGA board with IMPACT to physically run the code.

3 Theoretical and experimental results

For all the presented Truth Tables, the desired output is bolded.

3.1 NOT Gate

3.1.1 Truth Table

a	$\neg$	a
1	**0**	1
0	**1**	0

3.1.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

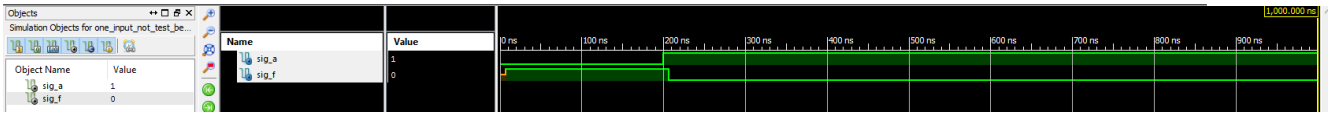

Figure 1: NOT gate timing diagram tested on iSim

3.2 NAND Gate

3.2.1 Truth Table

a	b	$\neg$	$(a$	$\wedge$	$b)$
1	1	**0**	1	1	1
1	0	**1**	1	0	0
0	1	**1**	0	0	1
0	0	**1**	0	0	0

3.2.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

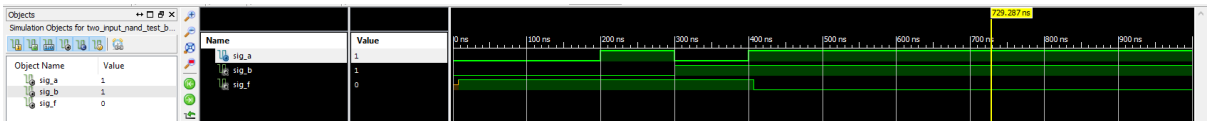

Figure 2: NAND gate timing diagram tested on iSim

3.3 AND Gate

3.3.1 Truth Table

a	b	a	$\wedge$	b
1	1	1	**1**	1
1	0	1	**0**	0
0	1	0	**0**	1
0	0	0	**0**	0

3.3.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

Figure 3: AND gate timing diagram tested on iSim

3.4 OR Gate

3.4.1 Truth Table

a	b	a	$\vee$	b
1	1	1	**1**	1
1	0	1	**1**	0
0	1	0	**1**	1
0	0	0	**0**	0

3.4.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

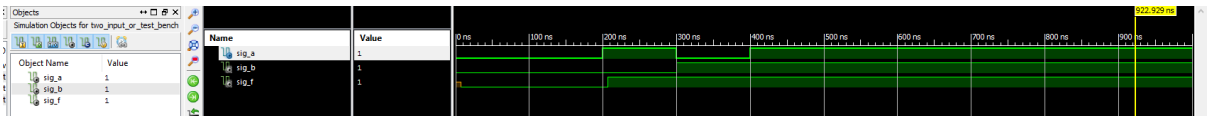

Figure 4: OR gate timing diagram tested on iSim

3.5 XOR Gate

3.5.1 Truth Table

a	b	$(a$	$\wedge$	$(\neg$	$b))$	$\vee$	$((\neg$	$a)$	$\wedge$	$b)$
1	1	1	0	0	1	**0**	0	1	0	1
1	0	1	1	1	0	**1**	0	1	0	0
0	1	0	0	0	1	**1**	1	0	1	1
0	0	0	0	1	0	**0**	1	0	0	0

3.5.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

Figure 5: XOR gate timing diagram tested on iSim

3.6 NOR Gate

3.6.1 Truth Table

a	b	$\neg$	$(a$	$\vee$	$b)$
1	1	**0**	1	1	1
1	0	**0**	1	1	0
0	1	**0**	0	1	1
0	0	**1**	0	0	0

3.6.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

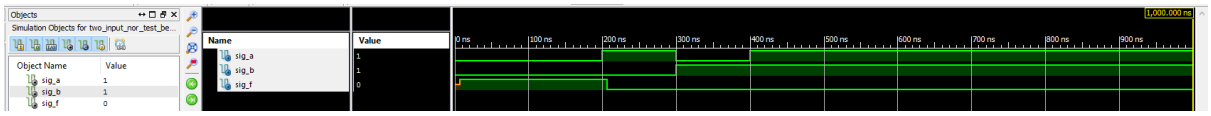

Figure 6: NOR gate timing diagram tested on iSim

3.7 Half Adder

3.7.1 Truth Table

Below the Truth Table for the Sum.

a	b	$(a$	$\wedge$	$(\neg$	$b))$	$\vee$	$((\neg$	$a)$	$\wedge$	$b)$
1	1	1	0	0	1	**0**	0	1	0	1
1	0	1	1	1	0	**1**	0	1	0	0
0	1	0	0	0	1	**1**	1	0	1	1
0	0	0	0	1	0	**0**	1	0	0	0

Below the Truth Table for the Carry out

a	b	a	$\wedge$	b
1	1	1	**1**	1
1	0	1	**0**	0
0	1	0	**0**	1
0	0	0	**0**	0

3.7.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the individual gates at the low-level is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

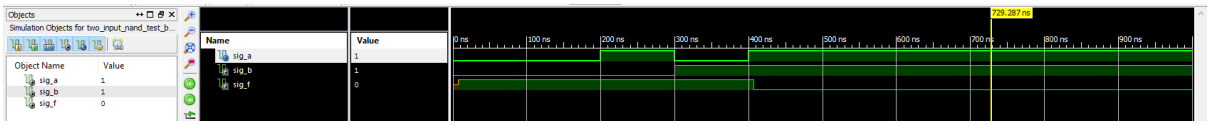

Figure 7: Half Adder timing diagram tested on iSim

3.8 3-Input OR Gate

3.8.1 Truth Table

a	b	c	$(a$	$\vee$	b	$\vee$	$c)$
1	1	1	1	1	1	**1**	1
1	1	0	1	1	1	**1**	0
1	0	1	1	1	0	**1**	1
1	0	0	1	1	0	**1**	0
0	1	1	0	1	1	**1**	1
0	1	0	0	1	1	**1**	0
0	0	1	0	0	0	**1**	1
0	0	0	0	0	0	**0**	0

3.8.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

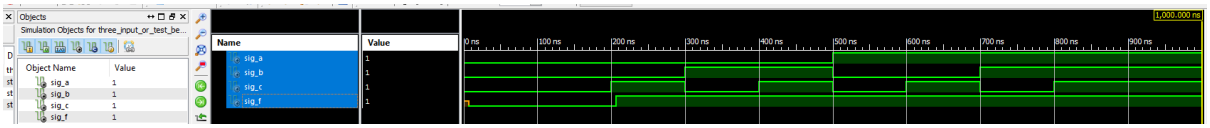

Figure 8: 3-Input OR gate timing diagram tested on iSim

3.9 4-input NOR Gate

3.9.1 Truth Table

a	b	c	d	$\neg$	$(a$	$\vee$	b	$\vee$	c	$\vee$	$d)$
1	1	1	1	**0**	1	1	1	1	1	1	1
1	1	1	0	**0**	1	1	1	1	1	1	0
1	1	0	1	**0**	1	1	1	1	0	1	1
1	1	0	0	**0**	1	1	1	1	0	1	0
1	0	1	1	**0**	1	1	0	1	1	1	1
1	0	1	0	**0**	1	1	0	1	1	1	0
1	0	0	1	**0**	1	1	0	1	0	1	1
1	0	0	0	**0**	1	1	0	1	0	1	0
0	1	1	1	**0**	0	1	1	1	1	1	1
0	1	1	0	**0**	0	1	1	1	1	1	0
0	1	0	1	**0**	0	1	1	1	0	1	1
0	1	0	0	**0**	0	1	1	1	0	1	0
0	0	1	1	**0**	0	0	0	1	1	1	1
0	0	1	0	**0**	0	0	0	1	1	1	0
0	0	0	1	**0**	0	0	0	0	0	1	1
0	0	0	0	**1**	0	0	0	0	0	0	0

3.9.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

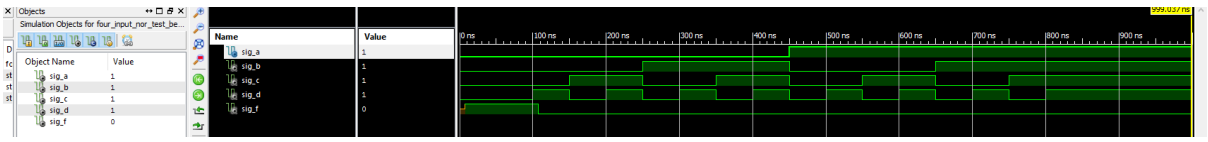

Figure 9: NAND gate timing diagram tested on iSim

3.10 2-input Multiplexer

3.10.1 Truth Table

a	b	z	$((\neg$	$z)$	$\wedge$	$a)$	$\vee$	$(z$	$\wedge$	$b)$
1	1	1	0	1	0	1	**1**	1	1	1
1	1	0	1	0	1	1	**1**	0	0	1
1	0	1	0	1	0	1	**0**	1	0	0
1	0	0	1	0	1	1	**1**	0	0	0
0	1	1	0	1	0	0	**1**	1	1	1
0	1	0	1	0	0	0	**0**	0	0	1
0	0	1	0	1	0	0	**0**	1	0	0
0	0	0	1	0	0	0	**0**	0	0	0

3.10.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

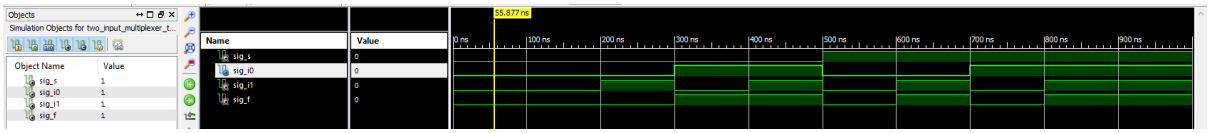

Figure 10: Multiplexer timing diagram tested on iSim

3.11 Full Adder

3.11.1 Truth Table

Below the Truth Table for the Sum

a	b	c	$((\neg$	$a)$	$\wedge$	$(\neg$	$b)$	$\wedge$	$c)$	$\vee$	$((\neg$	$a)$	$\wedge$	(b)	$\wedge$	$(\neg$	$c))$	$\vee$	$((a)$	$\wedge$	$(\neg$	$b)$	$\wedge$	$(\neg$	$c))$	$\vee$	$((a)$	$\wedge$	(b)	$\wedge$	$(c))$
1	1	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	0	0	1	**1**	1	1	1	1	1
1	1	0	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0	0	1	0	0	1	0	1	0	**0**	1	1	1	0	0
1	0	1	0	1	0	1	0	0	1	0	0	1	0	0	0	0	1	0	1	1	1	0	0	0	1	**0**	1	0	0	0	1
1	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	1	1	1	1	0	1	1	0	**1**	1	0	0	0	0
0	1	1	1	0	0	0	1	0	1	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	1	**0**	0	0	1	0	1
0	1	0	1	0	0	0	1	0	0	1	1	0	1	1	1	1	0	1	0	0	0	1	0	1	0	**1**	0	0	1	0	0
0	0	1	1	0	1	1	0	1	1	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	1	**1**	0	0	0	0	1
0	0	0	1	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	**0**	0	0	0	0	0

Below the Truth Table for the Carry Out

a	b	c	$(a$	$\wedge$	$b)$	$\vee$	$(a$	$\wedge$	$c)$	$\vee$	$(b$	$\wedge$	$c)$
1	1	1	1	1	1	1	1	1	1	**1**	1	1	1
1	1	0	1	1	1	1	1	0	0	**1**	1	0	0
1	0	1	1	0	0	1	1	1	1	**1**	0	0	1
1	0	0	1	0	0	0	1	0	0	**0**	0	0	0
0	1	1	0	0	1	0	0	0	1	**1**	1	1	1
0	1	0	0	0	1	0	0	0	0	**0**	1	0	0
0	0	1	0	0	0	0	0	0	1	**0**	0	0	1
0	0	0	0	0	0	0	0	0	0	**0**	0	0	0

3.11.2 Timing Diagram analysis

The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gates present at low level is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

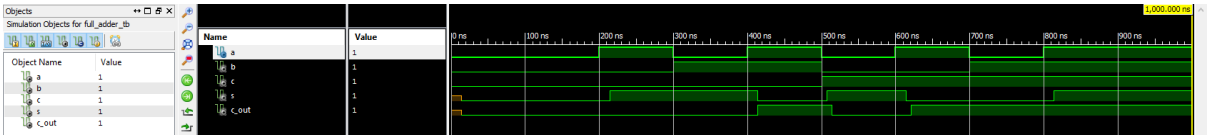

Figure 11: Full Adder timing diagram tested on iSim

3.12 Discussion

As tested in lab, the results observed on the FPGA are in agreement both with the Timing Diagram and with the Truth table of this tested gate. We assume there's going to be a different time delay in the FPGA due to non-idealised conditions. As mentioned in the Timing Diagram analysis for every component, this non-idealised conditions are modelled by generating a small delay at the beginning of the output signal.

3.13 Conclusion

In this lab we were able to successfully write, simulate and test all eleven required devices. At the same time we also became familiar with a number of new programs and skills such as; the ISE software, VHDL language, iSim simulation, PlanAhead and FPGA programming which is invaluable in creating a solid foundation for future labs. All the simulation results matched the theoretical expectations which confirms we are able to use these devices in higher level designs in the coming weeks.