# ECS615U Digital Systems Design Lab 2

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## Contents



## 1 Introduction

The aim of this lab was to develop, test and implement both a Algorithmic Logic Unit (ALU) and a Shifter/Rotator. The development tools involved in the task were VHDL language, ISim and a FPGA board on which to load our design.

# 2 Method

1. VHDL source code written for each gate
2. Test bench file written for each gate
3. Simulation of the test benches using iSIm
4. Screenshot result
5. Recording and verifying that the simulation matches the expected results
6. Constraint files created with PlanAhead for each VHDL source code
7. Constraint files and source code files programmed to the FPGA board with IMPACT to physically run the code.

# 3 Theoretical and experimental results

## 3.1 4-Bit ALU

The below figure displays the RTL schematic for the 4-Bit ALU.

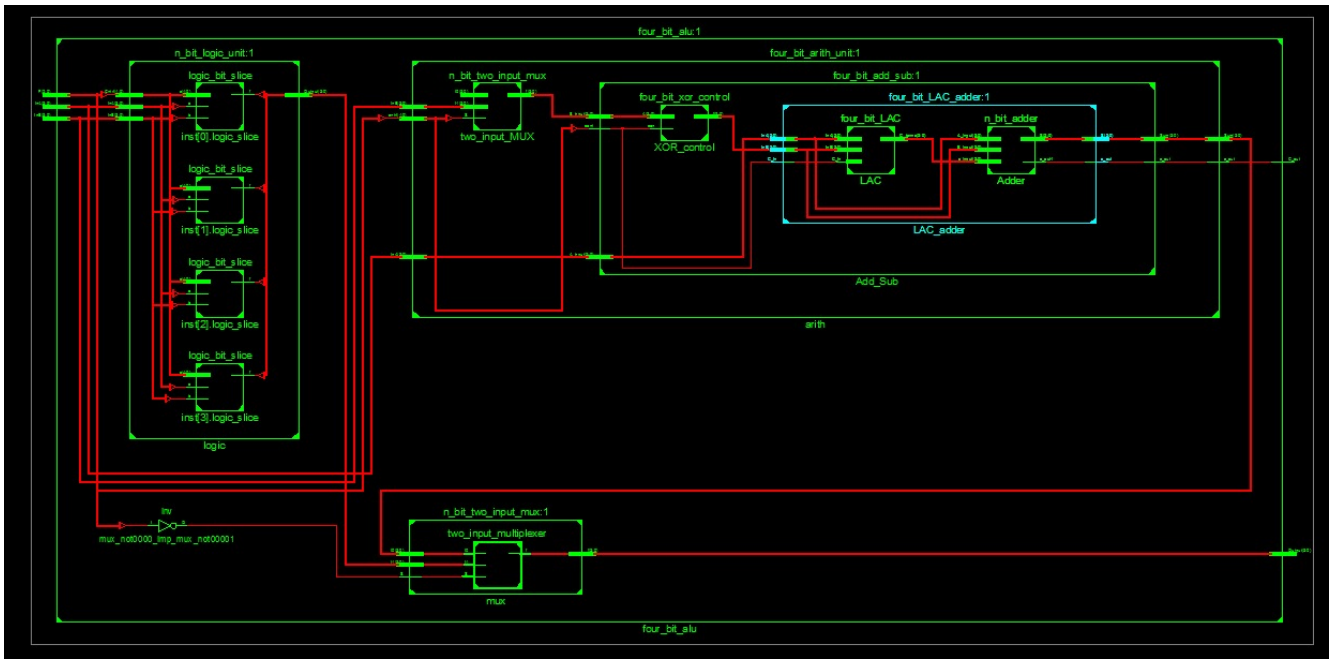


**Figure 1:** RTL schematic of a 4-Bit ALU

In the following sections Truth tables and timing diagrams for all the devices involved in the design are presented below. We follow a top-down approach and will exclude from the report those lower-level devices analysed in Lab 1.

### 3.1.1 Top level

Truth Table

| Function | F | InA | InB | Output | C_out |
|---|---|---|---|---|---|
| NOT A | 000 | 0101 | XXXX | 1010 | X |
| A AND B | 001 | 0011 | 0101 | 0001 | X |
| A XOR B | 010 | 0011 | 0101 | 0110 | X |
| A OR B | 011 | 0011 | 0101 | 0111 | X |
| Inc A | 100 | 0000 | XXXX | 0001 | 0 |
| A+B | 101 | 0001 | 1111 | 0000 | 1 |
| Dec A | 110 | 0000 | XXXX | 1111 | 0 |
| A-B | 111 | 1111 | 0001 | 1110 | 1 |

Timing Diagram analysis The timing diagram visible below confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

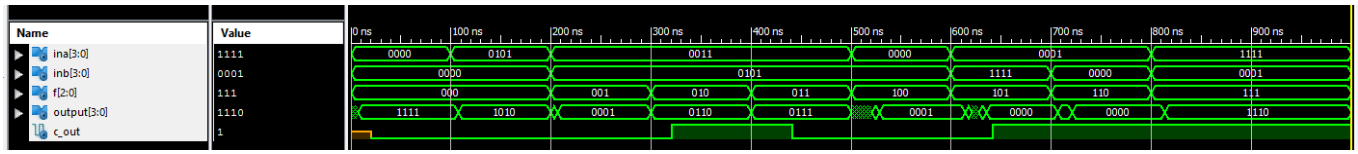


**Figure 2:** 4-Bit ALU timing diagram tested on iSim

### 3.1.2 4-Bit Arithmetic Unit

Truth Table

| Function | Control | InA | InB | Sum | C_out |
|---|---|---|---|---|---|
| A+1 | 00 | 0000 | 0000 | 0001 | 0 |
| A+B | 01 | 0001 | 0001 | 0010 | 0 |
| A-1 | 10 | 0010 | 0010 | 0001 | 0 |
| A-B | 11 | 0011 | 0011 | 0000 | 0 |
| A+1 | 00 | 0100 | 0100 | 0101 | 0 |
| A+B | 01 | 0101 | 0101 | 1010 | 0 |
| A-1 | 10 | 0110 | 0110 | 0101 | 0 |
| A-B | 11 | 0111 | 0111 | 0000 | 0 |
| A+1 | 00 | 1000 | 1000 | 1001 | 0 |
| A+B | 01 | 1001 | 1001 | 0010 | 1 |
| A-1 | 10 | 1010 | 1010 | 1001 | 0 |
| A-B | 11 | 1011 | 1011 | 0000 | 0 |
| A+1 | 00 | 1100 | 1100 | 1101 | 0 |
| A+B | 01 | 1101 | 1101 | 1010 | 1 |
| A-1 | 10 | 1110 | 1110 | 1101 | 0 |
| A-B | 11 | 1111 | 1111 | 0000 | 0 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with.

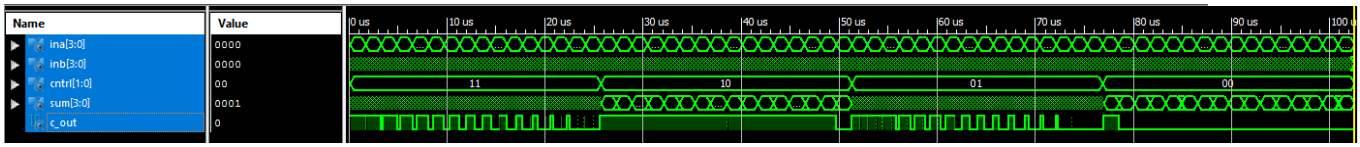


**Figure 3:** 4-Bit Algorithmic Unit timing diagram tested on iSim

Below, instead, a portion of the above timing diagram which confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

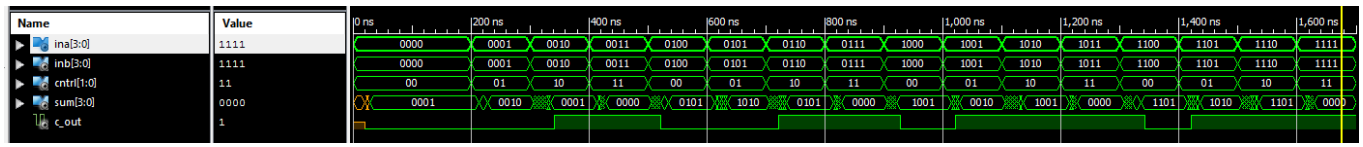


**Figure 4:** Portion of the 4-Bit ALU timing diagram tested on iSim

### 3.1.3 n-Bit 2-input MUX

Truth Table

| Control (N_i=2, N_d = 4) | InA (N_i=2, N_d = 4) | InB (N_i=2, N_d = 4) | Output (N_i=2, N_d = 4) |
|---|---|---|---|
| 0 | 0000 | 1111 | 0000 |
| 1 | 0001 | 1110 | 1110 |
| 0 | 0010 | 1101 | 0010 |
| 1 | 0011 | 1100 | 1100 |
| 0 | 0100 | 1011 | 0100 |
| 1 | 0101 | 1010 | 1010 |
| 0 | 0110 | 1001 | 0110 |
| 1 | 0111 | 1000 | 1000 |
| 0 | 1000 | 0111 | 1000 |
| 1 | 1001 | 0110 | 0110 |
| 0 | 1010 | 0101 | 1010 |
| 1 | 1011 | 0100 | 0100 |
| 0 | 1100 | 0011 | 1100 |
| 1 | 1101 | 0010 | 0010 |
| 0 | 1110 | 0001 | 1110 |
| 1 | 1111 | 0000 | 0000 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with.

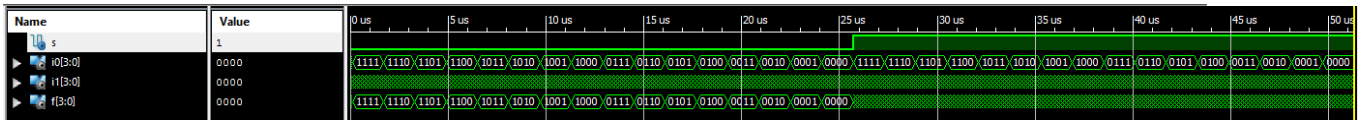


**Figure 5:** n-Bit 2-Input MUX timing diagram tested on iSim

Below, instead, a portion of the above timing diagram which confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

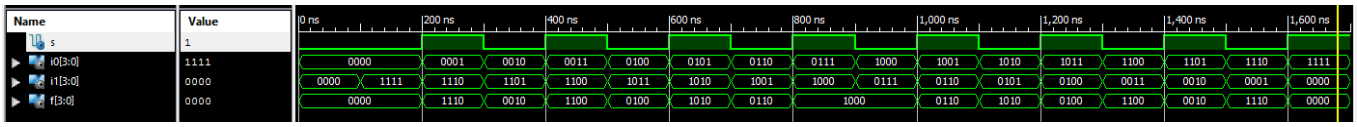


**Figure 6:** Portion of the n-Bit 2-Input MUX timing diagram tested on iSim

### 3.1.4 4-Bit Adder/Subtractor

Truth Table

| Control | InA | InB | Sum | C_out |
|---|---|---|---|---|
| 0 | 0000 | 1111 | 1111 | 0 |
| 1 | 0001 | 1110 | 0011 | 0 |
| 0 | 0010 | 1101 | 1111 | 0 |
| 1 | 0011 | 1100 | 0111 | 0 |
| 0 | 0100 | 1011 | 1111 | 0 |
| 1 | 0101 | 1010 | 1011 | 0 |
| 0 | 0110 | 1001 | 1111 | 0 |
| 1 | 0111 | 1000 | 1111 | 0 |
| 0 | 1000 | 0111 | 1111 | 0 |
| 1 | 1001 | 0110 | 0011 | 0 |
| 0 | 1010 | 0101 | 1111 | 0 |
| 1 | 1011 | 0100 | 0111 | 0 |
| 0 | 1100 | 0011 | 1111 | 0 |
| 1 | 1101 | 0010 | 1011 | 0 |
| 0 | 1110 | 0001 | 1111 | 0 |
| 1 | 1111 | 0000 | 1111 | 0 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with.

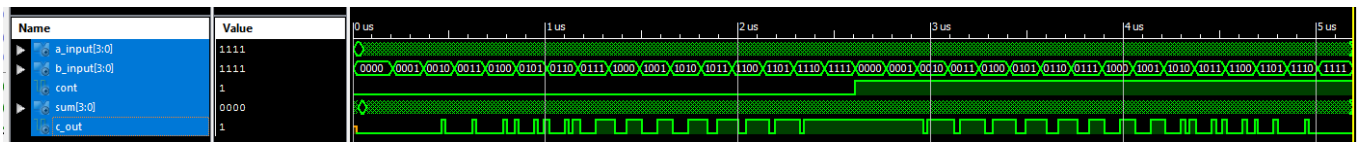


**Figure 7:** 4-Bit Adder/Subtractor timing diagram tested on iSim

Below, instead, a portion of the above timing diagram which confirms what expected from

the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

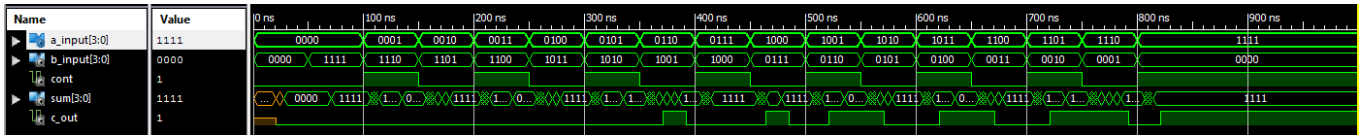


**Figure 8:** Portion of the 4-Bit Adder/Subtractor timing diagram tested on iSim

### 3.1.5 n-Bit XOR Control

Truth Table

| Control (N_i=4) | InA (N_i = 4) | Output |
|---|---|---|
| 0 | 0101 | 0101 |
| 1 | 0101 | 1010 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with. It confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

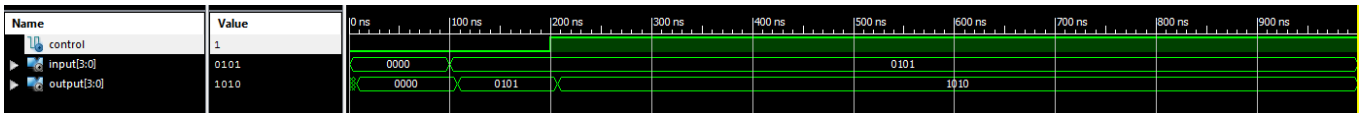


**Figure 9:** n-Bit XOR Control timing diagram tested on iSim

### 3.1.6 4-Bit LAC Adder

Truth Table

| C_In | InA | InB | Sum | C_out |
|---|---|---|---|---|
| 0 | 0000 | 1000 | 1000 | 0 |
| 0 | 0001 | 1001 | 1010 | 0 |
| 0 | 0010 | 1010 | 1100 | 0 |
| 0 | 0011 | 1011 | 1110 | 0 |
| 0 | 0100 | 1100 | 0000 | 1 |
| 0 | 0101 | 1101 | 0010 | 1 |
| 0 | 0110 | 1110 | 0100 | 1 |
| 0 | 0111 | 1111 | 0110 | 1 |
| 0 | 1000 | 0000 | 1000 | 0 |
| 1 | 1001 | 0001 | 1011 | 0 |
| 1 | 1010 | 0010 | 1101 | 0 |
| 1 | 1011 | 0011 | 1111 | 0 |
| 1 | 1100 | 0100 | 0001 | 1 |
| 1 | 1101 | 0101 | 0011 | 1 |
| 1 | 1110 | 0110 | 0101 | 1 |
| 1 | 1111 | 0111 | 0111 | 1 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with.

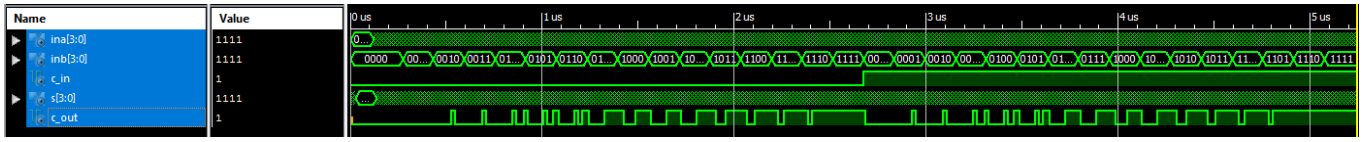


**Figure 10:** 4-Bit LAC Adder timing diagram tested on iSim

Below, instead, a portion of the above timing diagram which confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

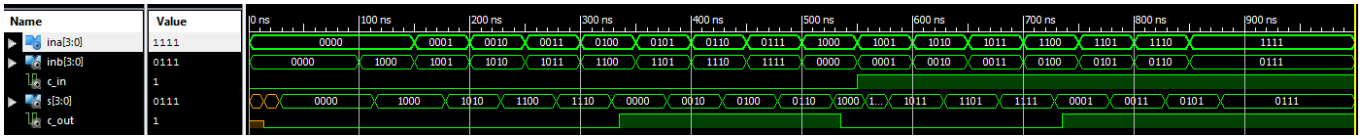


**Figure 11:** Portion of the 4-Bit LAC Adder timing diagram tested on iSim

### 3.1.7 4-Bit LAC Adder Unit

Truth Table

| InA | InB | Output |
|---|---|---|
| 0000 | 0000 | 0000 |
| 0001 | 0001 | 0010 |
| 0010 | 0010 | 0100 |
| 0100 | 0100 | 1000 |
| 0001 | 1111 | 1110 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with. This confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

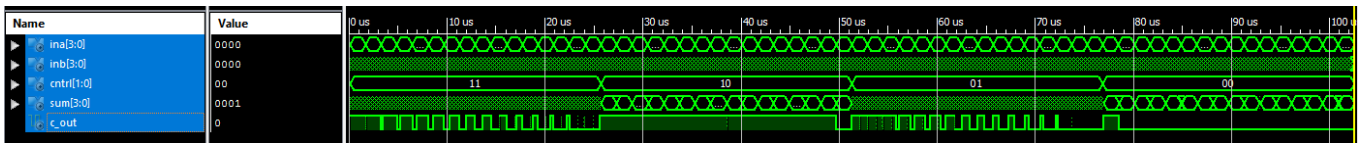


**Figure 12:** 4-Bit LAC Adder Unit timing diagram tested on iSim

### 3.1.8 n-Bit Adder

Truth Table

| InA | InB | Carry In | S | Carry out |
|---|---|---|---|---|
| 0000 | 0000 | 0000 | 0000 | 0 |
| 0001 | 0001 | 0000 | 0000 | 0 |
| 0011 | 0010 | 0000 | 0001 | 0 |
| 1100 | 1000 | 0000 | 0100 | 1 |
| 1001 | 1101 | 0100 | 0000 | 1 |
| 1010 | 1001 | 0100 | 0111 | 1 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with. This confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

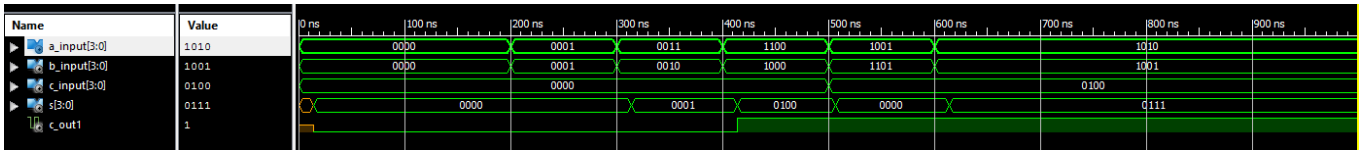


**Figure 13:** n-Bit Adder timing diagram tested on iSim

### 3.1.9 n-Bit Logic Unit

Truth Table

| Function | Cntrl | InA | InB | Output |
|---|---|---|---|---|
| Complement A | 00 | 0000 | 1000 | 1111 |
| | 00 | 0001 | 1001 | 1110 |
| | 00 | 0010 | 1010 | 1101 |
| | 00 | 0011 | 1011 | 1100 |
| | 00 | 0100 | 1100 | 1011 |
| A and B | 01 | 0101 | 1101 | 0101 |
| | 01 | 0110 | 1110 | 0110 |
| | 01 | 0111 | 1111 | 0111 |
| | 01 | 1000 | 0000 | 0000 |
| A xor B | 10 | 1001 | 0001 | 1000 |
| | 10 | 1010 | 0010 | 1000 |
| | 10 | 1011 | 0011 | 1000 |
| | 10 | 1100 | 0100 | 1000 |
| A or B | 11 | 1101 | 0101 | 1101 |
| | 11 | 1110 | 0110 | 1110 |
| | 11 | 1111 | 0111 | 1111 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with.

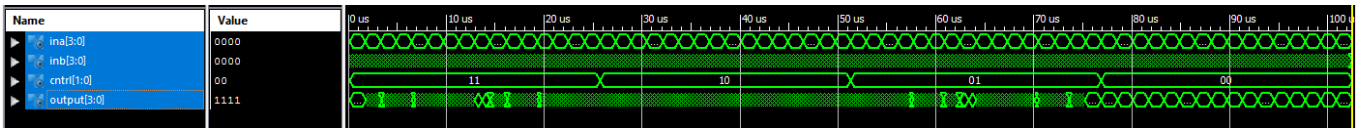


**Figure 14:** n-Bit Logic Unit timing diagram tested on iSim

Below, instead, a portion of the above timing diagram which confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

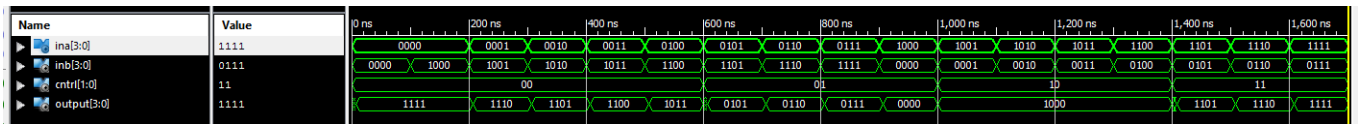


**Figure 15:** Portion of the n-Bit Logic Unit timing diagram tested on iSim

### 3.1.10 1-Bit Slicer

Truth Table

| Function | c | a | b | Output |
|---|---|---|---|---|
| Complement A | 00 | 1 | 1 | 0 |
| A and B | 01 | 1 | 1 | 1 |
| A xor B | 10 | 1 | 1 | 0 |
| A or B | 11 | 1 | 1 | 1 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with. This confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

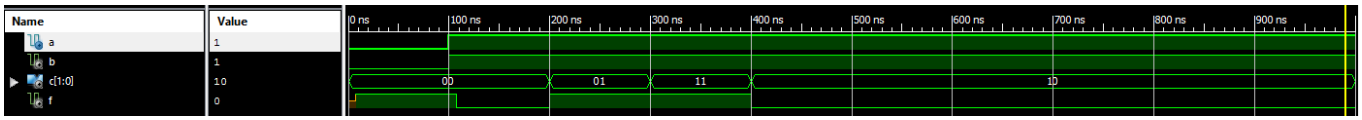


**Figure 16:** 1-Bit Slicer timing diagram tested on iSim

## 3.2 4-Bit Shifter

The below figure displays the RTL schematic for the 4-Bit Shifter.

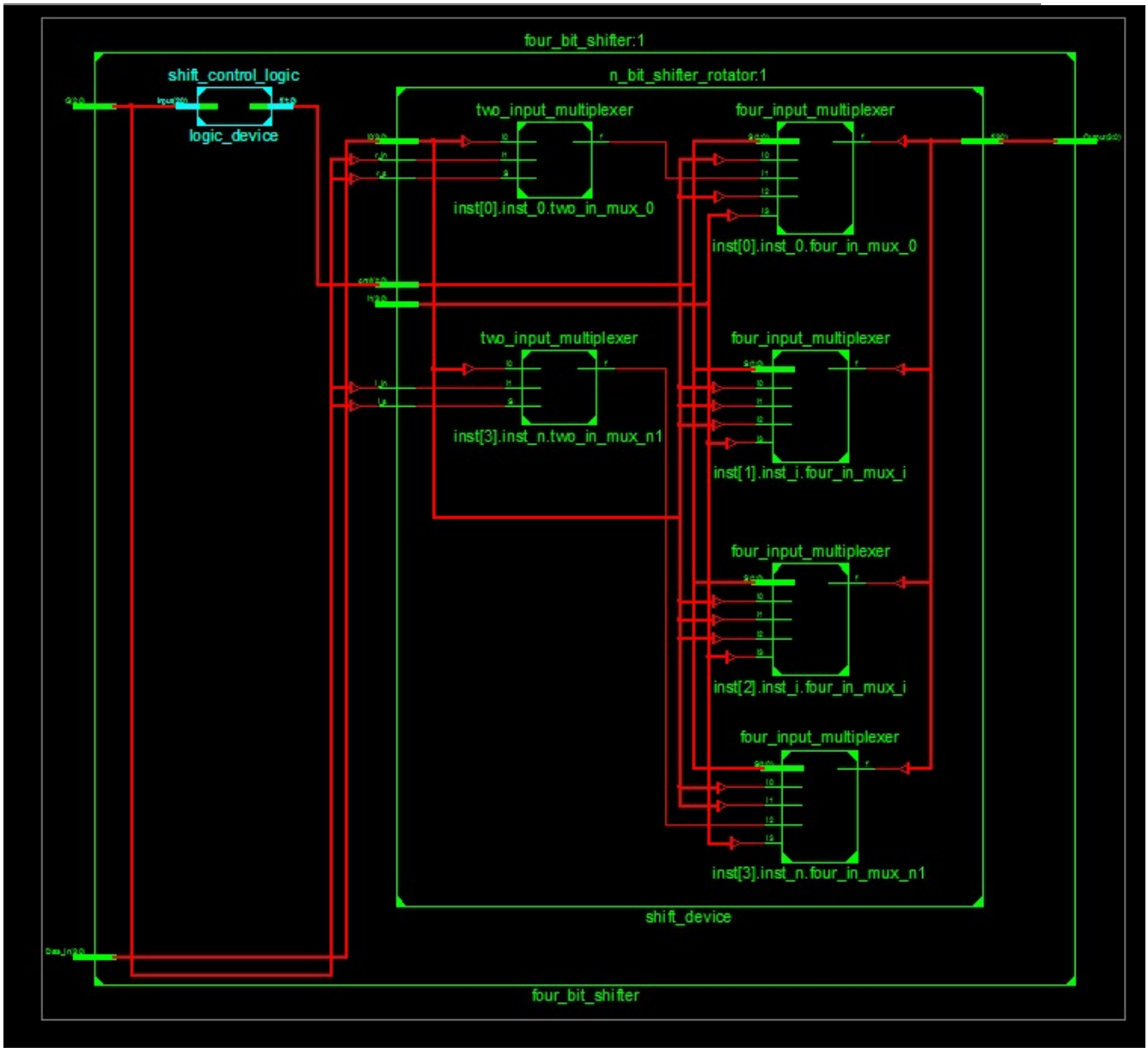


**Figure 17:** RTL schematic of a 4-Bit Shifter

In the following sections Truth tables and timing diagrams for all the devices involved in the design are presented below. We follow a top-down approach and will exclude from the report those lower-level devices analysed in Lab 1.

### 3.2.1 Top Level

Truth Table

| Function | G | Data_in | Output |
|---|---|---|---|
| Pass | 000 | 0101 | 0101 |
| Rotate Left | 001 | 0101 | 1010 |
| Shift Left (0) | 010 | 1111 | 1110 |
| Shift Left (1) | 011 | 0000 | 0001 |
| Pass | 100 | 1010 | 1010 |
| Rotate right | 101 | 1010 | 0101 |
| Shift right (0) | 110 | 1111 | 0111 |
| Shift right (1) | 111 | 0000 | 1000 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with. This confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

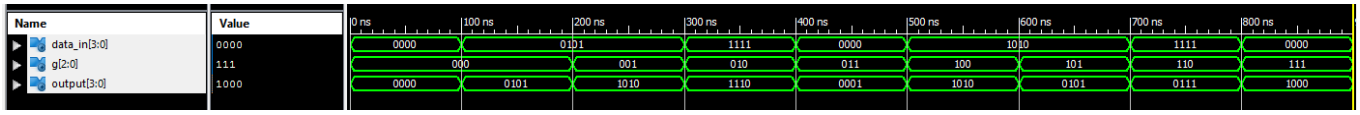


**Figure 18:** 4-Bit Shifter timing diagram tested on iSim

### 3.2.2 n-Bit Shifter/Rotator Unit

Truth Table

| I0 | I1 | R_in | R_s | L_in | L_s | Cntrl | Output |
|---|---|---|---|---|---|---|---|
| 0000 | 0000 | 0 | 0 | 0 | 0 | 00 | 0000 |
| 0010 | 0100 | 0 | 1 | 0 | 1 | 01 | 0100 |
| 0100 | 0010 | 1 | 1 | 0 | 1 | 10 | 0010 |
| 0001 | 0001 | 0 | 1 | 0 | 1 | 00 | 0001 |
| 1000 | 1000 | 0 | 1 | 0 | 1 | 00 | 1000 |

rotator.PNG

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with.

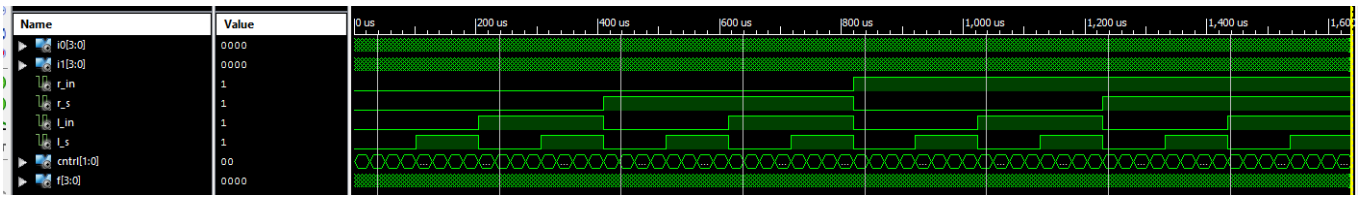


**Figure 19:** n-Bit Logic Unit timing diagram tested on iSim

Below, instead, a portion of the above timing diagram which confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

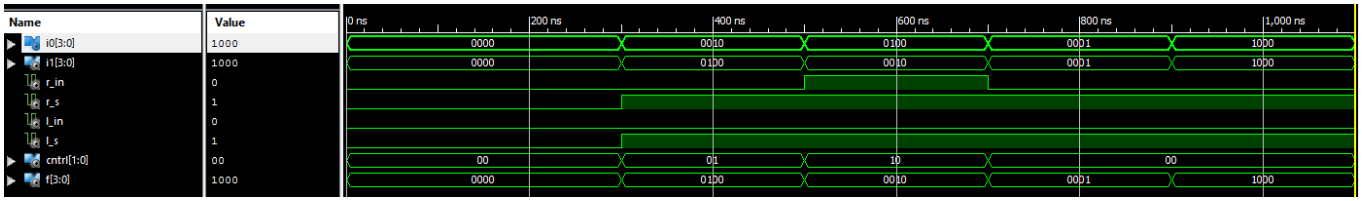


**Figure 20:** Portion of the n-Bit Logic Unit timing diagram tested on iSim

### 3.2.3 Shift Control Logic

Truth Table

| Input | Output |
|---|---|
| 000 | 00 |
| 111 | 10 |
| 110 | 10 |
| 101 | 10 |
| 100 | 00 |
| 011 | 01 |
| 010 | 01 |
| 001 | 01 |
| 000 | 00 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with. This confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

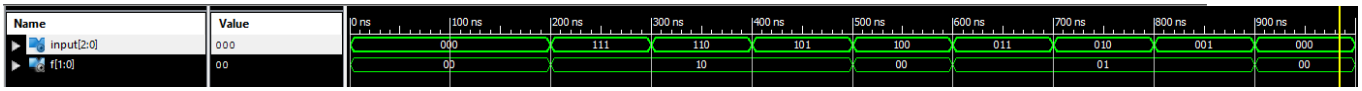


**Figure 21:** Shift Control Logic timing diagram tested on iSim

### 3.2.4 4-Input Multiplexer

Truth Table

| s | I3 | I2 | I1 | I0 | Output |
|---|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 0 | 0 |
| 01 | 1 | 0 | 1 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 | 0 |
| 11 | 1 | 0 | 1 | 0 | 1 |

Timing Diagram analysis The timing diagram visible below includes all the possibilities the device can be tested with. This confirms what expected from the truth table. A time delay, equivalent to the delay generated by the gate is visible at the beginning of the diagram. This delay then propagates throughout the duration of the Test Bench.

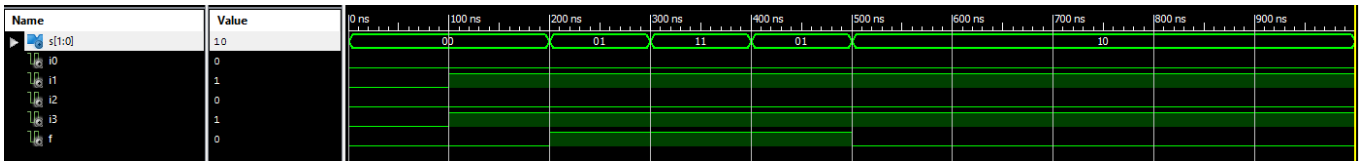


**Figure 22:** 4-Input Multiplexer timing diagram tested on iSim

# 4 Discussion

As tested in the lab, the results observed on the FPGA are in agreement both with the Timing Diagram and with the Truth table of the tested device. We assume there's going to be a different time delay in the FPGA due to non-idealised conditions. As mentioned in the Timing Diagram analysis for every component, this non-idealised conditions are modelled by generating a small delay at the beginning of the output signal.

# 5 Conclusion

In this lab we were able to successfully write, simulate and test all fourteen required devices. All the simulation results matched the theoretical expectations which confirms we are able to use these devices in higher level designs in the coming weeks.