Nano MOSFETs in Modern Electronics

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Abstract

Transistors are semiconductor devices that regulate or control current flow or voltage, amplifying electrical signals and acting as a switch or gate for them. Modern nanotransistors, 14nm in size, operate much differently than regular transistors and require new understanding of electron transport in nanoscale systems. This paper explores the physics required to understand electron transport at the nanoscale level and how this information is used in the context of nanotransistor design and fabrication. We will also explore the ongoing effort of making even smaller transistors and the challenges faced doing so.

1 Introduction

Transistors are semiconductor devices that regulate or control current or voltage flow, amplifying electrical signals and acting as a switch or gate for them . They are the foundation of all modern electronics and are arguably the most important invention in the modern age [1]. Modern apple iPhone chips contain 16 billion transistors! The first working transistor built by scientists at Bell Laboratories in 1947, was about 1cm in size [2]. Modern transistors today are around 14nm in size, around 6 orders of magnitude smaller! Modern MetalOxide-Semiconductor Field-Effect Transistor (MOSFET) nanotransistors operate much differently than regular transistors and require new understanding of electron transport in nanoscale systems. More specifically, the flow of electrons through a nano MOSFET is very different than regular MOSFETS. In this paper, We will explore MOSFET theory formulated in the 1960s. We will then explore how our theory was forced to evolve as the scales our our systems were driven down. The theory explored will be based on new understanding of electron transport that has emerged from research on molecular and nanoscale electronics [3]. We will

then explore how these nano-transistors are fabricated and the difficulties faced in trying to go even smaller.

2 MOSFET Fundamentals

The left side of figure 1 shows the configuration of a MOSFET transistor. Electrons enter the device through the source. The gate controls the electron flow from the source across the channel. These electrons then exit the transistor through the drain. The right side of figure 1 shows a silicon MOSFET Circa 2000 imaged by a scanning electron micrograph [3]. The source and drain are doped silicon as is the substrate the transistor is built on. The gate electrode is siting on to of the device and is separated from the silicon substrate by a thin, insulating layer. In n-channel MOSFETs, the drain and source are n-type Si and the substrate is p-type. The opposite is true for p-channel MOSFETs. The particular example shown is an enhancement mode MOSFET, meaning a you need to reach a certain threshold voltage to activate the transistor and let current pass. These are often used as switching devices.

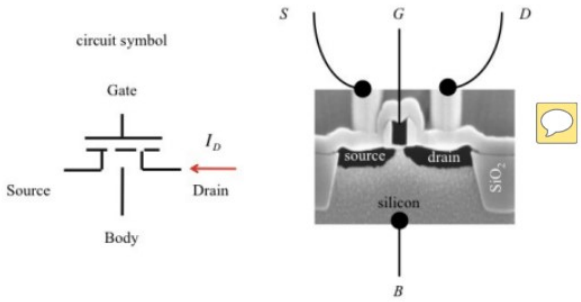

Figure 1: Left: The circuit schematic of an enhancement mode MOSFET. The dashed line indicates that this is an enhancement mode MOSFET, meaning the MOSFET will conduct current when the gate voltage is above a threshold voltage. Right: A cross-section of a silicon MOSFET circa 2000. The channel is the gap between the source and the drain. [3].

In both cases, the MOSFET operates by controlling current through the manipulation of an energy barrier with a gate voltage. classical transistor states that the conventional current through the drain to the source, I_{DS}, is proportional to the width of the MOSFET

,W, amount of charge in the channel, Q_n, and the average of it's speed, $\langle v \rangle$.

$$I_{ds} = W|Q_n(V_{GS}, V_{DS})| \langle v \rangle \tag{1}$$

The charge is controlled by MOS electrostatics, meaning it is altered by manipulating the energy barrier between the source and the channel. This means the charge is a function of the voltage difference between the gate and the source, V_{GS}, and the voltage difference between the drain and the source, V_{DS}. This theory works well for larger transistors but moving to lower length scales requires new formalism [3].

3 The virtual source model

The virtual source model (VSM) is a model for nano-transistors developed by a team at the Massachusetts Institute of Technology (MIT). This model describes, similar to classical theory, the drain current as proportional to the width, the amount of charge and it's velocity.

$$I_{DS} = W|Q_n(x = 0, V_{Gi}, V_{Di})|F_{SAT}(V_{Di})v_{inj} \tag{2}$$

V_{Di} and V_{Gi} are the intrinsic voltages at the drain and gate. $F_{SAT}(V_{Di})v_{inj}$ in this equation is what they call the velocity of the *"virtual source"*. The charge at this virtual source is obtained semi-empirically:

$$|Q_n(V_{Gi}, V_{Di})| = mC_G(inv)(\frac{k_BT}{q}) \ln 1 + e^{q(V_{Gi}-V_T-\alpha(k_BT/q)F_f)/mk_BT}, \tag{3}$$

where α is chosen to fit data. The inversion transition function, F_f expressed by

$$F_f = \frac{1}{1 + exp(\frac{V_{Gi}-(V_T-\alpha(k_BT/q)/2)}{\alpha k_BT/q})} \tag{4}$$

produces an increase in threshold voltage by k_BT/q when the MOSFET gets activated, a factor not seen in classical theory. The MVS model uses a second empirical function for $F_SAT(V_{Di}$. This model can be fit to measured data to deduce very important parameters [4]. The drain current remains proportional to the charge and it's velocity even when going to

nanoscales, but the equations governing the charge and the velocity do change, and some statistical mechanics effects come in to play, making classical theories obsolete at these scales. Figure 2 shows a fit of the drain current as a function of the drain source current for a 30nm transistor using the MVS model, showing it's accuracy even with it's simplicity [3].

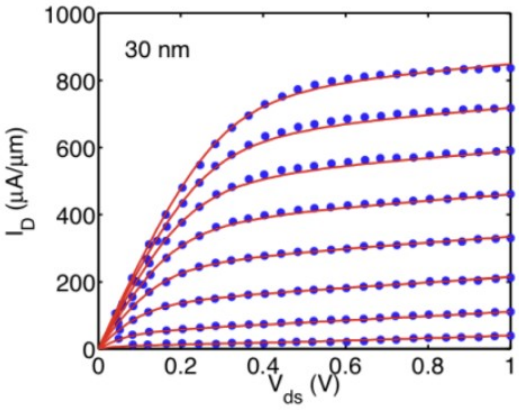

Figure 2: Measured drain-source voltage vs drain current for a 30nm MOSFET. The measured data is shown in blue and the MVS fits in red. The different paths indicate different gate-source voltages, from 0.2V to 0.9V, increasing by steps of 0.1V [4].

4 Nano Transistor Fabrication

We first start with a uniformly doped silicon wafer. We then move to the first major step, lithography. This is used to transfer the pattern of the gate area of a MOSFET from a photomask to the surface of the wafer. We then proceed to etching, a process made to remove material selectively in order to create patterns defined by the etching mask. The unmasked material can be removed by wet or dry etching. The next step is deposition, where multiple material layers are deposited on the wafer. This is done either by physical or chemical vapor deposition. Chemical mechanical planarization is then used to plane the wafer surface with the help of a chemical slurry. We then oxidize the wafer to convert the wanted silicon to silicon dioxide. Ions are then implanted to indroduce dopant impurities in the silicon. This is done with an electric field, accelerating the ionized atoms to allow them to penetrate into the target material and bond with the silicon atoms. The final step is

difussion, which moves the impurities in the device at high temperature and is used to form the source, drain, and channel regions in a MOSFET [5]. The basic fabrication steps for a semiconductor device is shown in figure 3.

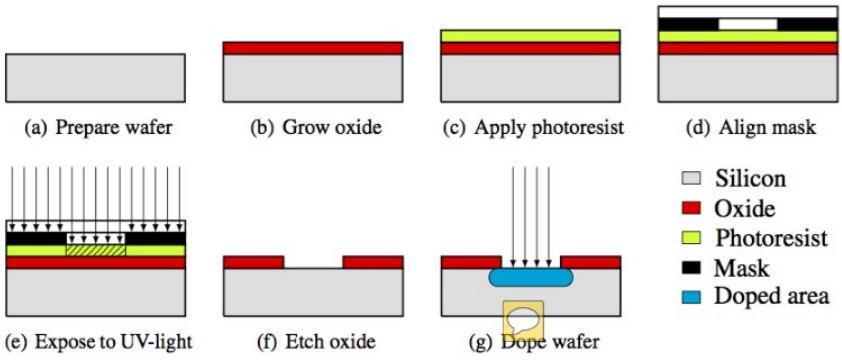

Figure 3: Basic steps of a semiconductor device fabrication process [6].

5 Discussion

Since the invention of the transistor, the MOSFET in particular, there has been a big driving force to produce these devices as small as possible for increased computing power. Scaling down comes with it's challenges. Other than the new physics arising from this, there is also many practical and engineering challenges that are introduced. The ultimate challenge, and even limit, to scaling a MOSFET is direct source-to-drain tunneling. If the channel length is small enough for electrons to tunnel through the barrier without gate bias, MOSFETs no longer can be used as a switch. This turns out to be a length of about 5 nm in modern computers [7]. There is also the challenge that nano MOSFETs made from the same wafer will have threshold voltage variations, increasing as the size of your device decreases. Variations in V_{th} directly effect device speed, so minimizing this variation is crucial. A final challenge to list would be the increase in leakage current when the gate voltage is below threashold, which can cause issues as current is flowing at undesired times. These points are simply to state that although nano transistors are very useful and have changed the world, they still have their limitations. To scale even further down, we will have to develop new solutions to trnasistors, such as Single Electron Transistors (SETs) or Nanowire (NW) transistors [7].

References

[1] J. H. V. V. Zhirnov, R.K. Cavin III and G. Bourianoff, *Limits to Binary Logic Switch Scaling – A Gedanken Model.* Proc. IEEE, 2003. 1

[2] M. Riordan, *transistor.* Encyclopedia Britannica, 2022. [Online]. Available: https://www.britannica.com/technology/transistor 1

[3] M. Lundstrom, *Fundamentals of Nanotransistors.* WORLD SCIENTIFIC, 2017. [Online]. Available: https://www.worldscientific.com/doi/abs/10.1142/9018 1, 2, 3, 4

[4] A. Khakifirooz, O. Nayfeh, and D. Antoniadis, "A simple semiempirical short-channel mosfet current–voltage model continuous across all regions of operation and employing only physical parameters," *Electron Devices, IEEE Transactions on*, vol. 56, pp. 1674 – 1680, 09 2009. 3, 4

[5] C. Hollauer, "Semiconductor fabrication processes." [Online]. Available: https://www.iue.tuwien.ac.at/phd/hollauer/node6.html 5

[6] M. Rovitto, "Semiconductor fabrication." [Online]. Available: https://www.iue.tuwien.ac.at/phd/rovitto/node10.html 5

[7] Y.-B. K. Kim, "Challenges for nanoscale mosfets and emerging nanoelectronics," *TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS*, vol. 11, pp. 93 – 105, 06 2010. 5