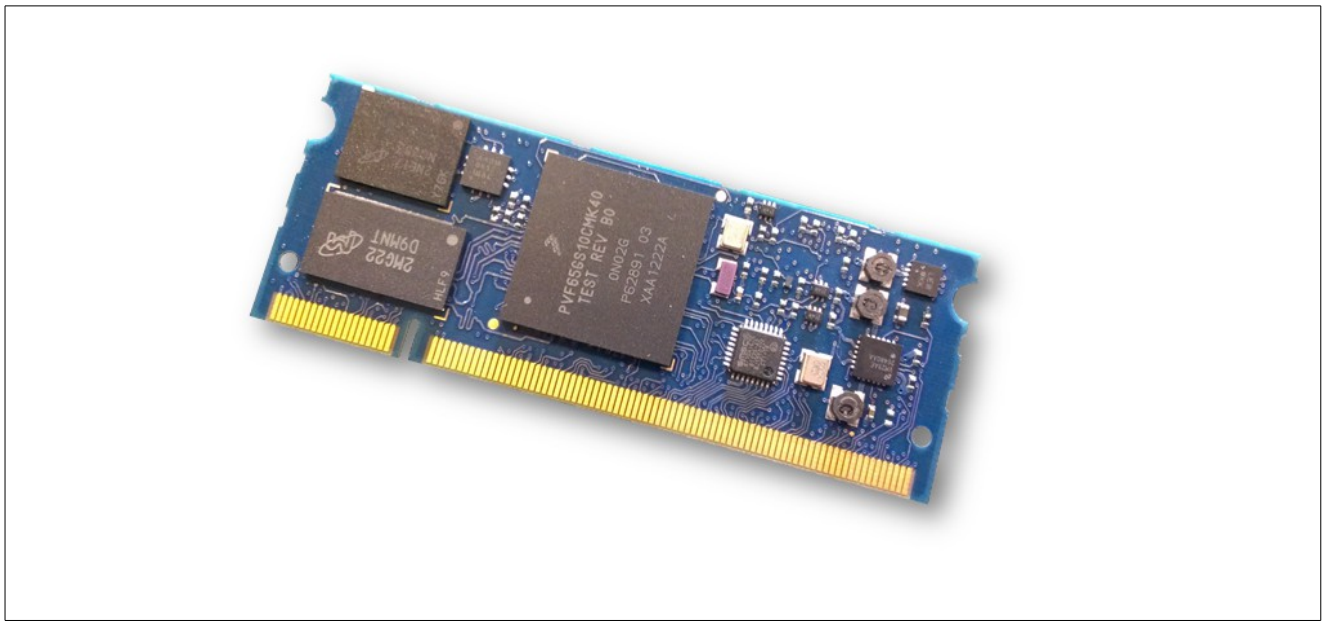
CHIMERA
Getting started manual



***** REV 1.0.0 *****

DATE	REVISION	CHANGE DESCRIPTION
13/05/2014	1.0.0	Release

Summary

1. Mechanical data

The Chimera module has a standard SO DIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector. The PCB dimensions is L 67.60 x W 32 x H 1 mm. The distances available on PCB under the module are from tbd mm

1.1 Assembly Top View

The Chimera Module has a Standard SODIMM footprint where odd pins are on top (component) side and even pins are on bottom side. In Figure 2 and 3 is shown assembly and pin1 and pin 2 positions.

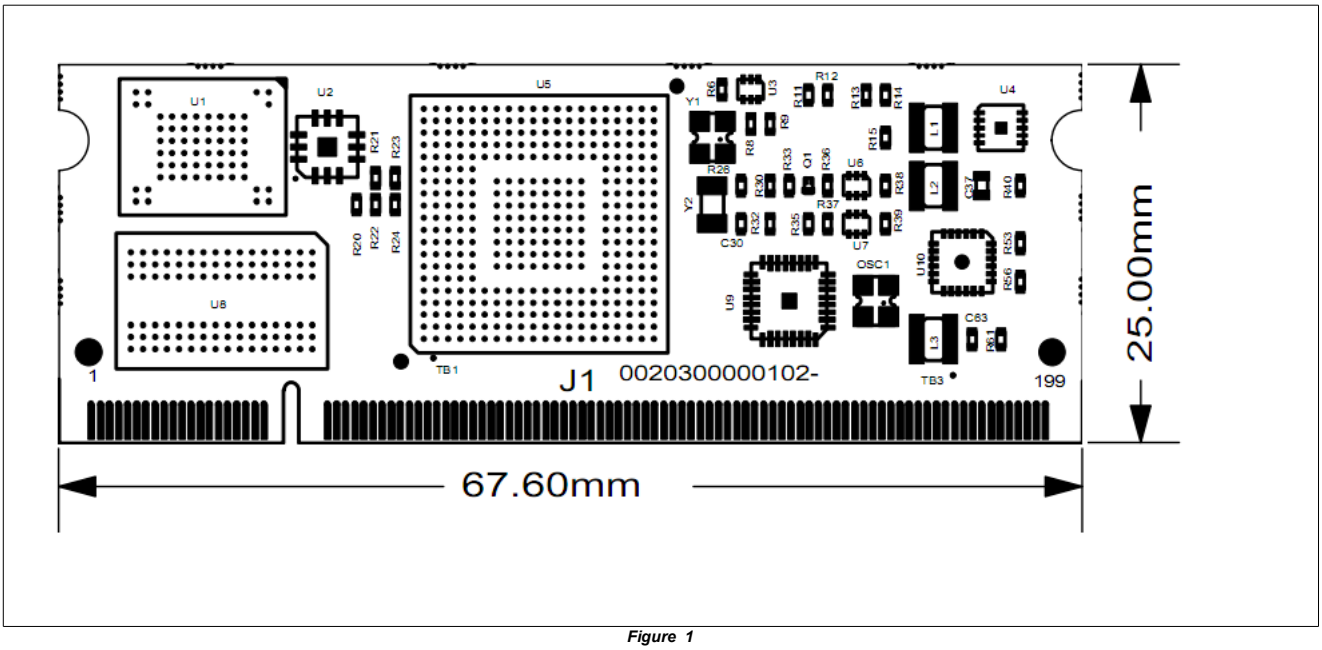


Figure 1

1.2 Assembly Bottom View

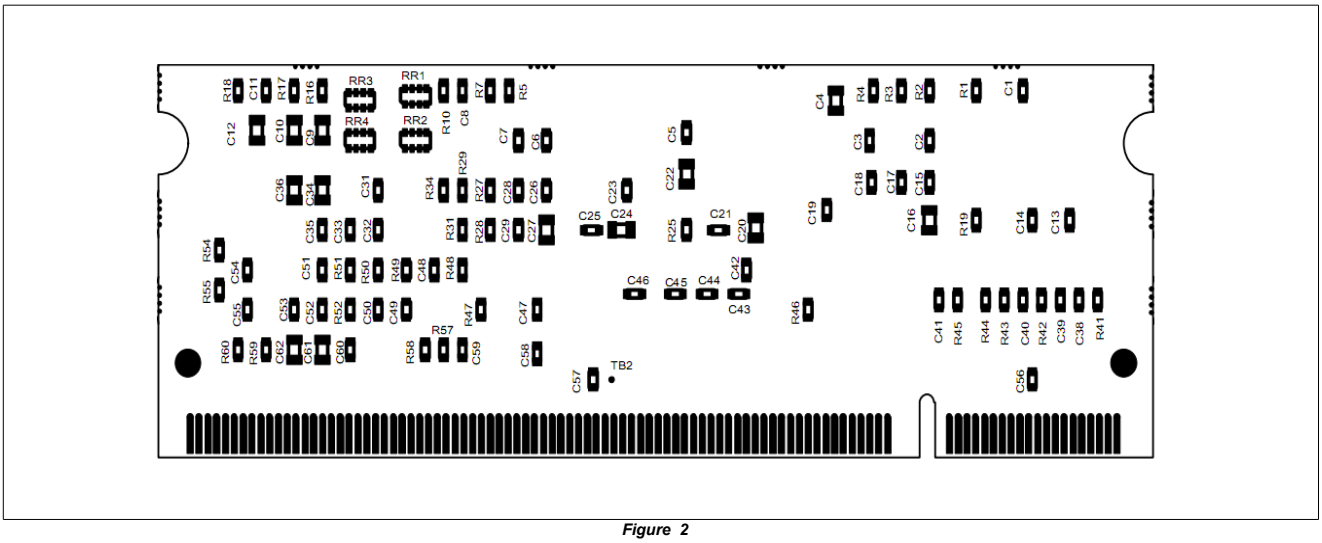


Figure 2

2. Ordering Information

Following we provide the ordering informations and the description for the Basic technical specifications modules:

Marking Code	Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C
CHIMERA F600	00258000003091	1	Modulo Chimera F600 Dual	Vybrid A5+M4 Core **-40 to 105 °C ***	-40 to +85 °C
CHIMERA F600	00257000003091	58	Modulo Chimera F600 Dual	128MB DDR3, 256MB NAND Industrial Temperature	-40 to +85 °C

Table 1

**** Note: internal junction temperature***

3. Module Pin OUT

The module's interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible

Pin	Name	Pin Name on Vybrid	Primary Function Description	GPIO Capable	Voltage
1	+1,8V	-	Power PIN	N	-
2	+1,8V	-	Power PIN	N	-
3	GND	-	Power PIN	N	-
4	GND	-	Power PIN	N	-
5	GND	-	Power PIN	N	-
6	FTM3CH0	PTD24	Motor control/general purpose timer	Y	+3,3V
7	FTM3CH1	PTD25	Motor control/general purpose timer	Y	+3,3V
8	FTM3CH2	PTD26	Motor control/general purpose timer	Y	+3,3V
9	FTM3CH3	PTD27	Motor control/general purpose timer	Y	+3,3V
10	FTM3CH4	PTD28	Motor control/general purpose timer	Y	+3,3V
11	FTM3CH5	PTD29	Motor control/general purpose timer	Y	+3,3V
12	FTM3CH6	PTD30	Motor control/general purpose timer	Y	+3,3V
13	FTM3CH7	PTD31	Motor control/general purpose timer	Y	+3,3V
14	FTM1_QD_PHA	PTA18	Motor control/general purpose timer	Y	+3,3V
15	FTM1_QD_PHB	PTA19	Motor control/general purpose timer	Y	+3,3V
16	PTB12	PTB12	Generic GPIO	Y	+3,3V
17	NC	-	-	-	-
18	+Vcoin	-	Power PIN	N	-
19	NC	-	-	-	-
20	NC	-	-	-	-
21	NC	-	-	-	-
22	GND	-	Power PIN	N	-
23	I2C2_SCL ***	PTA22	I2C SCL Signal	Y	+3,3V
24	I2C2_SDA ***	PTA23	I2C SDA Signal	Y	+3,3V
25	TS_XP	-	-	N	+3,3V
26	TS_XN	-	-	N	+3,3V
27	TS_YP	-	-	N	+3,3V
28	TS_YN	-	-	N	+3,3V
29	ADC0SE8 **	ADC0SE8	ADC 0 channel 8 input	N	+3,3V
30	ADC0SE9 **	ADC0SE9	ADC 0 channel 9 input	N	+3,3V
31	GND	-	Power PIN	N	-
32	ADC1SE9 **	ADC1SE9	ADC 1 channel 8 input	N	+3,3V
33	ADC1SE8 **	ADC1SE8	ADC 1 channel 9 input	N	+3,3V
34	EXT_AUDIO_MCLK *	PTB18	Clock Controller Module	Y	+3,3V
35	FTM0CH0	PTB0	Motor control/general purpose timer	Y	+3,3V
36	FTM0CH1	PTB1	Motor control/general purpose timer	Y	+3,3V
37	FTM0CH2	PTB2	Motor control/general purpose timer	Y	+3,3V
38	FTM0CH3	PTB3	Motor control/general purpose timer	Y	+3,3V
39	GND	-	Power PIN	N	-
40	FTM0CH6	PTB6	Motor control/general purpose timer	Y	+3,3V
41	DACO0 **	DACO0	12 bit DAC 0 Interface		+3,3V
42	NC	-	-	-	-
43	DACO1 **	DACO1	12 bit DAC 1 Interface		+3,3V
44	NC	-	-	-	-
45	NC	-	-	-	-

Pin	Name	Pin Name on Vybrid	Primary Function Description	GPIO Capable	Voltage
46	NC	-	-	-	-
47	NC	-	-	-	-
48	NC	-	-	-	-
49	NC	-	-	-	-
50	NC	-	-	-	-
51	NC	-	-	-	-
52	NC	-	-	-	-
53	NC	-	-	-	-
54	NC	-	-	-	-
55	NC	-	-	-	-
56	NC	-	-	-	-
57	NC	-	-	-	-
58	NC	-	-	-	-
59	NC	-	-	-	-
60	NC	-	-	-	-
61	NC	-	-	-	-
62	NC	-	-	-	-
63	PTC30	PTC30	Generic GPIO	Y	+3,3V
64	GND	-	Power PIN	N	-
65	PTB23 *	PTB23	Generic GPIO	Y	+3,3V
66	PTC10	PTC10	Generic GPIO	Y	+3,3V
67	PTB8	PTB8	Generic GPIO	Y	+3,3V
68	PTC9	PTC9	Generic GPIO	Y	+3,3V
69	PTC31	PTC31	Generic GPIO	Y	+3,3V
70	PTB26	PTB26	Generic GPIO	Y	+3,3V
71	GND	-	Power PIN	N	-
72	PTC29	PTC29	Generic GPIO	Y	+3,3V
73	PTD5	PTD5	Generic GPIO	Y	+3,3V
74	PTB13	PTB13	Generic GPIO	Y	+3,3V
75	PTB9	PTB9	Generic GPIO	Y	+3,3V
76	PTD4	PTD4	Generic GPIO	Y	+3,3V
77	PTD6	PTD6	Generic GPIO	Y	+3,3V
78	PTC11	PTC11	Generic GPIO	Y	+3,3V
79	NC	-	-	-	-
80	nSD_BOOT	-	SD start configuration	-	+3,3V
81	PTD10	PTD10	Generic GPIO	Y	+3,3V
82	PTC12	PTC12	Generic GPIO	Y	+3,3V
83	PTD11	PTD11	Generic GPIO	Y	+3,3V
84	PTC13	PTC13	Generic GPIO	Y	+3,3V
85	PTD12	PTD12	Generic GPIO	Y	+3,3V
86	PTC16	PTC16	Generic GPIO	Y	+3,3V
87	PTD13	PTD13	Generic GPIO	Y	+3,3V
88	PTD9	PTD9	Generic GPIO	Y	+3,3V
89	GND	-	Power PIN	N	-
90	PTD8	PTD8	Generic GPIO	Y	+3,3V
91	PTD7	PTD7	Generic GPIO	Y	+3,3V
92	PTE5	PTE5	Generic GPIO	Y	+3,3V
93	NC	-	-	-	-
94	PTE6	PTE6	Generic GPIO	Y	+3,3V

Pin	Name	Pin Name on Vybrid	Primary Function Description	GPIO Capable	Voltage
95	PTE13	PTE13	Generic GPIO	Y	+3,3V
96	NC	-	-	-	-
97	PTE21	PTE21	Generic GPIO	Y	+3,3V
98	PTE14	PTE14	Generic GPIO	Y	+3,3V
99	PTE22	PTE22	Generic GPIO	Y	+3,3V
100	NC	-	-	-	-
101	NC	-	-	-	-
102	NC	-	-	-	-
103	NC	-	-	-	-
104	NC	-	-	-	-
105	SCI2_CTS	PTD3	UART2 CTS signal	Y	+3,3V
106	SCI2_RTS	PTD2	UART2 RTS signal	Y	+3,3V
107	GND	-	Power PIN	N	-
108	SCI2_TX	PTD0	UART2 TX signal	Y	+3,3V
109	SCI2_RX	PTD1	UART2 RX signal	Y	+3,3V
110	I2C3_SDA	PTA31	I2C SDA Signal	Y	+3,3V
111	I2C3_SCL	PTA30	I2C SCL Signal	Y	+3,3V
112	SCI3_TX	PTA20	UART3 TX signal	Y	+3,3V
113	SCI3_RX	PTA21	UART3 RX signal	Y	+3,3V
114	SAI2_RX_DATA	PTC14	Synchronous Audio Interface Rx Data	Y	+3,3V
115	SAI2_TX_SYNC	PTC17	Synchronous Audio InterfaceTx Frame Sync	Y	+3,3V
116	SCI1_TX	PTB4	UART1 TX signal	Y	+3,3V
117	SCI1_RX	PTB5	UART1 RX signal	Y	+3,3V
118	CAN0_TX	PTB15	CAN 0 transmit signal	Y	+3,3V
119	CAN0_RX	PTB14	CAN 0 receive signal	Y	+3,3V
120	CAN1_TX	PTB17	CAN 1 transmit signal	Y	+3,3V
121	CAN1_RX	PTB16	CAN 1 receive signal	Y	+3,3V
122	SAI2_TX_DATA	PTC15	Synchronous Audio Interface Tx Data	Y	+3,3V
123	GND	-	Power PIN	N	-
124	SAI2_TX_BCLK	PTA16	Synchronous Audio Interface Tx Bit Clock	Y	+3,3V
125	DISP0_CLK	PTE2	LCD interface	Y	+3,3V
126	NC	-	-	-	-
127	ETH_TXN	-	Fast Ethernet TXN signal		
128	OD_nRESET	RESET	Reset signal		
129	ETH_TXP	-	Fast Ethernet TXP signal		
130	NC	-	-	-	-
131	ETH_RXN	-	Fast Ethernet RXN signal		
132	FTM0_CH7	PTB7	Motor control/general purpose timer	Y	+3,3V
133	ETH_RXP	-	Fast Ethernet RXP signal		
134	+3,3V	-	Output Power PIN	N	-
135	+3,3V	-	Output Power PIN	N	-
136	NC	-	-	-	-
137	ETH_LED_10_100_KATHOD		Led Indicator Cathode signal		
138	NC	-	-	-	-
139	ETH_LED_ACT_ANOD	-	Led indicator Anode signal		
140	+3,7V	-	Output Power PIN	N	-
141	DISP0_D17 *	PTE10	LCD interface	Y	+3,3V
142	DISP0_D16 *	PTE9	LCD interface	Y	+3,3V
143	DISP0_D15 *	PTE8	LCD interface	Y	+3,3V

Pin	Name	Pin Name on Vybrid	Primary Function Description	GPIO Capable	Voltage
144	DISP0_D14 *	PTE7	LCD interface	Y	+3,3V
145	DISP0_D13	PTE6	LCD interface	Y	+3,3V
146	DISP0_D12	PTE5	LCD interface	Y	+3,3V
147	DISP0_D11 *	PTE18	LCD interface	Y	+3,3V
148	DISP0_D10 *	PTE17	LCD interface	Y	+3,3V
149	DISP0_D9 *	PTE16	LCD interface	Y	+3,3V
150	DISP0_D8 *	PTE15	LCD interface	Y	+3,3V
151	DISP0_D7	PTE14	LCD interface	Y	+3,3V
152	DISP0_D6	PTE13	LCD interface	Y	+3,3V
153	DISP0_D5 *	PTE26	LCD interface	Y	+3,3V
154	DISP0_D4 *	PTE25	LCD interface	Y	+3,3V
155	DISP0_D3 *	PTE24	LCD interface	Y	+3,3V
156	GND	-	Power PIN	N	-
157	DISP0_D2 *	PTE23	LCD interface	Y	+3,3V
158	DISP0_D1	PTE22	LCD interface	Y	+3,3V
159	DISP0_D0	PTE21	LCD interface	Y	+3,3V
160	DISP0_VSYNC *	PTE1	LCD interface	Y	+3,3V
161	DISP0_HSYNC *	PTE0	LCD interface	Y	+3,3V
162	DISP0_DRDY	PTE4	LCD interface	Y	+3,3V
163	NC	-	-	-	-
164	NC	-	-	-	-
165	NC	-	-	-	-
166	NC	-	-	-	-
167	DSPI0_SOUT	PTB20	SPI interface	Y	+3,3V
168	DSPI0_SIN	PTB21	SPI interface	Y	+3,3V
169	DSPI0_SCK	PTB22	SPI interface	Y	+3,3V
170	NC	-	-	-	-
171	DSPI0_PCS0 *	PTB19	SPI interface	Y	+3,3V
172	NC	-	-	-	-
173	NC	-	-	-	-
174	JTAG_TDO	PTA10	JTAG Interface	Y	+3,3V
175	JTAG_TDI	PTA9	JTAG Interface	Y	+3,3V
176	JTAG_TMS	PTA11	JTAG Interface	Y	+3,3V
177	JTAG_TCK	PTA8	JTAG Interface	Y	+3,3V
178	NC	-	-	-	-
179	NC	-	-	-	-
180	USB1_VBUS	USB1_VBUS_DETECT	USB HOST interface	N	-
181	BOOT_MODE	-	Boot from USB UART or on board Nand Flash	-	-
182	GND	-	Power PIN	N	-
183	PTA7_SD1_CD	PTA7	eSDHC CD Signal	Y	+3,3V
184	PTA12	PTA12	Generic GPIO	Y	+3,3V
185	SD1_D2	PTA28	eSDHC DAT 2 signal	Y	+3,3V
186	SD1_D3	PTA29	eSDHC DAT 3 signal	Y	+3,3V
187	SD1_D1	PTA27	eSDHC DAT 1 signal	Y	+3,3V
188	SD1_D0	PTA26	eSDHC DAT 0 signal	Y	+3,3V
189	SD1_CLK	PTA24	eSDHC CLK signal	Y	+3,3V
190	SD1_CMD	PTA25	eSDHC CMD signal	Y	+3,3V
191	PTA17	PTA17	Generic GPIO	Y	+3,3V
192	USB0_DP	USB0_DP	USB HOST interface	N	-

Pin	Name	Pin Name on Vybrid	Primary Function Description	GPIO Capable	Voltage
193	USB0_DM	USB0_DM	USB HOST interface	N	-
194	USB1_DP	USB1_DP	USB HOST interface	N	-
195	USB0_VBUS	USB0_VBUS_DETECT	USB HOST interface	N	-
196	USB1_DM	USB1_DM	USB HOST interface	N	-
197	+5Vin	-	Power PIN	N	-
198	+5Vin	-	Power PIN	N	-
199	+5Vin	-	Power PIN	N	-
200	+5Vin	-	Power PIN	N	-

Table 2

** Note: for the use of this pin please refer to boot option in "**Boot Mode Pin"** chapter*

*** For the range of of voltage and further details of ADC and DAC interfaces, please refer to Reference Manual*

**** WARNING:*
the address 1001000 (0x48) *of the 7-bit I2C bus is used by the touch controller (e.g. using the temperature sensor TI LM75 there is bus conflict)*

The yellow lines highlight the required minimum electrical connections in order to make the module working correctly.

5. Carrier Board Design

5.1 Carrier board recommended specifications

Following we'll describe the specifications required to carrier board to avoid problems of assembly process. The module is interfaced with the carrier board through a SO-DIMM with 200 positions connector type TYCO ELECTRONICS code 1473005-1 or compatible.
For proper assembly is strongly recommended to paying attention to:

Planarity in finish process

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process (we suggest and use for our carrier boards a type Chemical Gold finish).

Planarity of PCB

Also the planarity of the entire Printed Circuit Board must be kept in check especially when the your carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged

Note: for further detail please refer to your SO-DIMM connector's data-sheet

5.2 How to power the Chimera module

Please read carefully the related sections before start your power stage design. This module needs to be supply up to +5Vin power. Please refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is about 250-350 mA, but **the system must provide at least a power of 1 A at 5V to allow the start of the module.**

	Min	Typ	Max
Voltage range	-	+5V	-
Current @ 5,0V	-	tbd mA	-

Table 3

In the following table are shown the module power supply pins numbering, please connect all power supply pins in order to avoid damage.

Number	Name	Primary Function Description	GPIO Capable	Voltage
197	+5Vin	Power PIN	N	-
198	+5Vin	Power PIN	N	-
199	+5Vin	Power PIN	N	-
200	+5Vin	Power PIN	N	-
3	GND	Power PIN	N	-
4	GND	Power PIN	N	-
5	GND	Power PIN	N	-
22	GND	Power PIN	N	-
31	GND	Power PIN	N	-
39	GND	Power PIN	N	-
64	GND	Power PIN	N	-
71	GND	Power PIN	N	-
89	GND	Power PIN	N	-
107	GND	Power PIN	N	-
123	GND	Power PIN	N	-
156	GND	Power PIN	N	-
182	GND	Power PIN	N	-

Table 4

Chimera module has 5 Output power PIN usable for power source. In the table below are shown the power supply pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
1	+1V8	Output Power PIN	N	-
2	+1V8	Output Power PIN	N	-
134	+3V3_OUT	Output Power PIN	N	-
135	+3V3_OUT	Output Power PIN	N	-
140	+3V7_OUT	Output Power PIN	N	-

Table 5

In the following table are shown the nominal maximum rating of power output:

Power output	Max output current
3,3 V outputs	~ 600 mA (Total)
+3V7_OUT	~ 50 mA (Total)
+1V8	~ 80 mA (Total)

Table 6

For further details on the power supply please refer to "Vybrid" data sheet and Reference Manual.

5.3 How to connect two 3-wire RS232 serial port

In this section is shown how to use the Chimera SCI1 and SCI3 as 3-wire RS232 serial ports.
In the following table are shown the UART named SCI1 and SCI3 pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
112	SCI3_TXD	UART3 TXD signal	Y	+3,3V
113	SCI3_RXD	UART3 RXD signal	Y	+3,3V
116	SCI1_TXD	UART1 TXD signal	Y	+3,3V
117	SCI1_RXD	UART1 RXD signal	Y	+3,3V

Table 7

The signal on the module's UART pins are 3.3V logic level, this can not be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

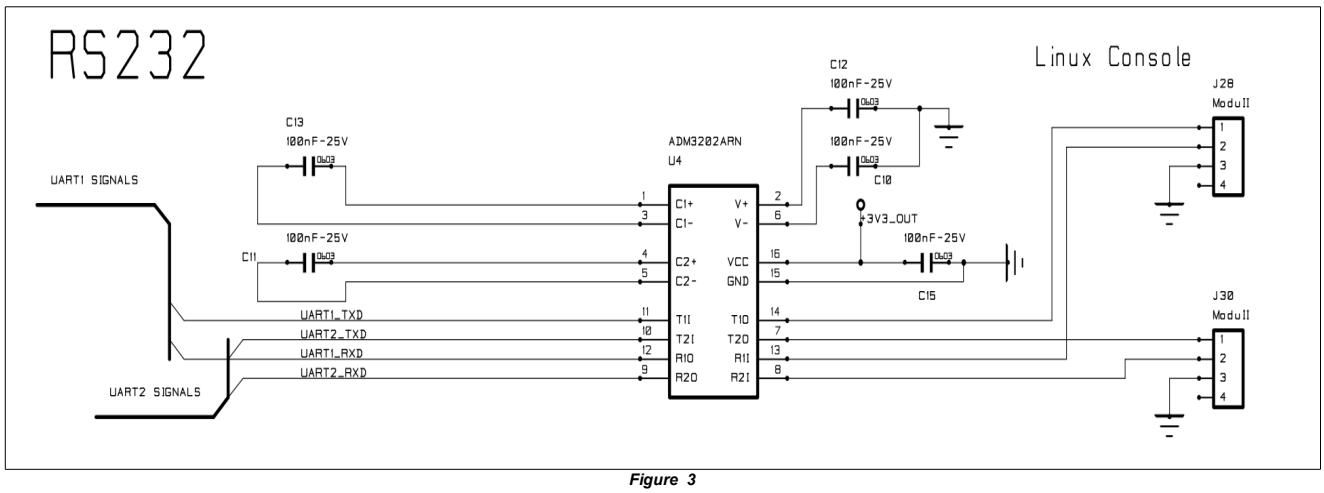


Figure 3

In the previous figure is shown the UART1 and UART3 (labelled UART2 in the picture) are connected in the Chimera evaluation board. In this example an ADM3202ARN IC from Analog Device is used like transceiver for both UART without any control signal. In case RTS and CTS are need, a transceiver must be used for this signals.

When Linux is installed on a module, UART1 is used like console. The default communications settings is shown in the table below.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 8

5.4 How to connect a RS485 serial port

In this chapter is shown how an RS485 serial port can be connected to the module. In the figure below is shown how SCI2 (labelled UART3 in the picture) is used to connect to a RS485 transceiver on the starter kit.

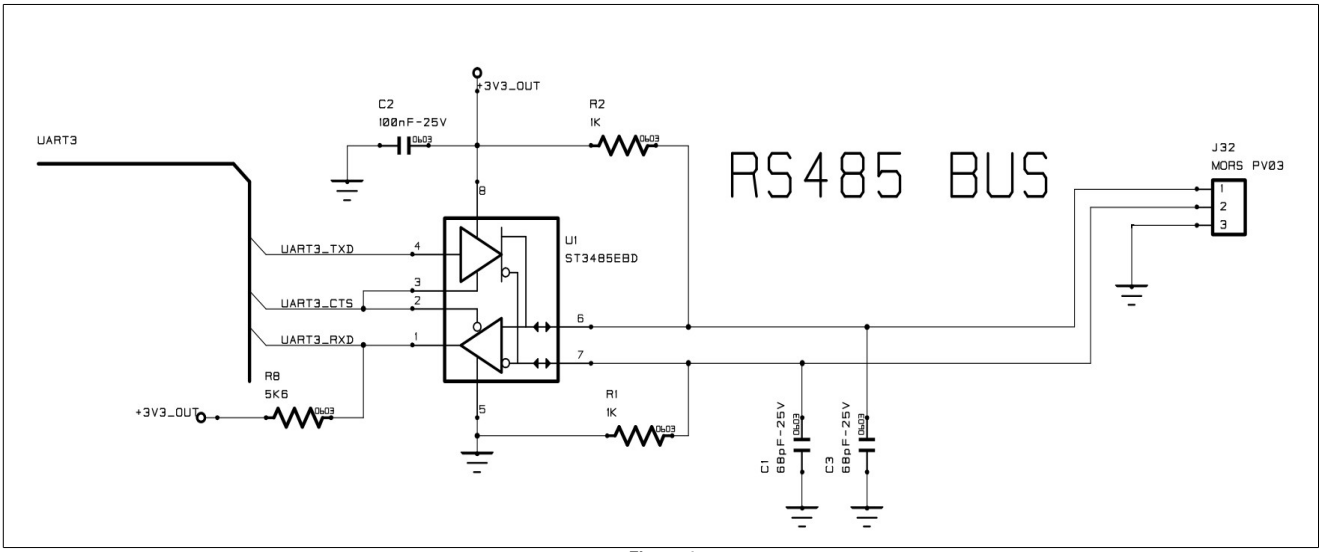


Figure 4

The pins involved in this RS485 communication example are listed in the following table.

Number	Name	Primary Function Description	GPIO Capable	Voltage
105	SCI2_CTS	UART3 CTS signal	Y	+3,3V
106	SCI2_RTS	UART3 RTS signal	Y	+3,3V
108	SCI2_TX	UART3 TXD signal	Y	+3,3V
109	SCI2_RX	UART3 RXD signal	Y	+3,3V

Table 9

5.5 How to connect CAN BUS interfaces

In this chapter is described how CAN bus transceiver can be connected to a Chimera module. In the figure is shown how CAN bus1 and 2 are connected in the evaluation board. Both CAN buses have been implemented.

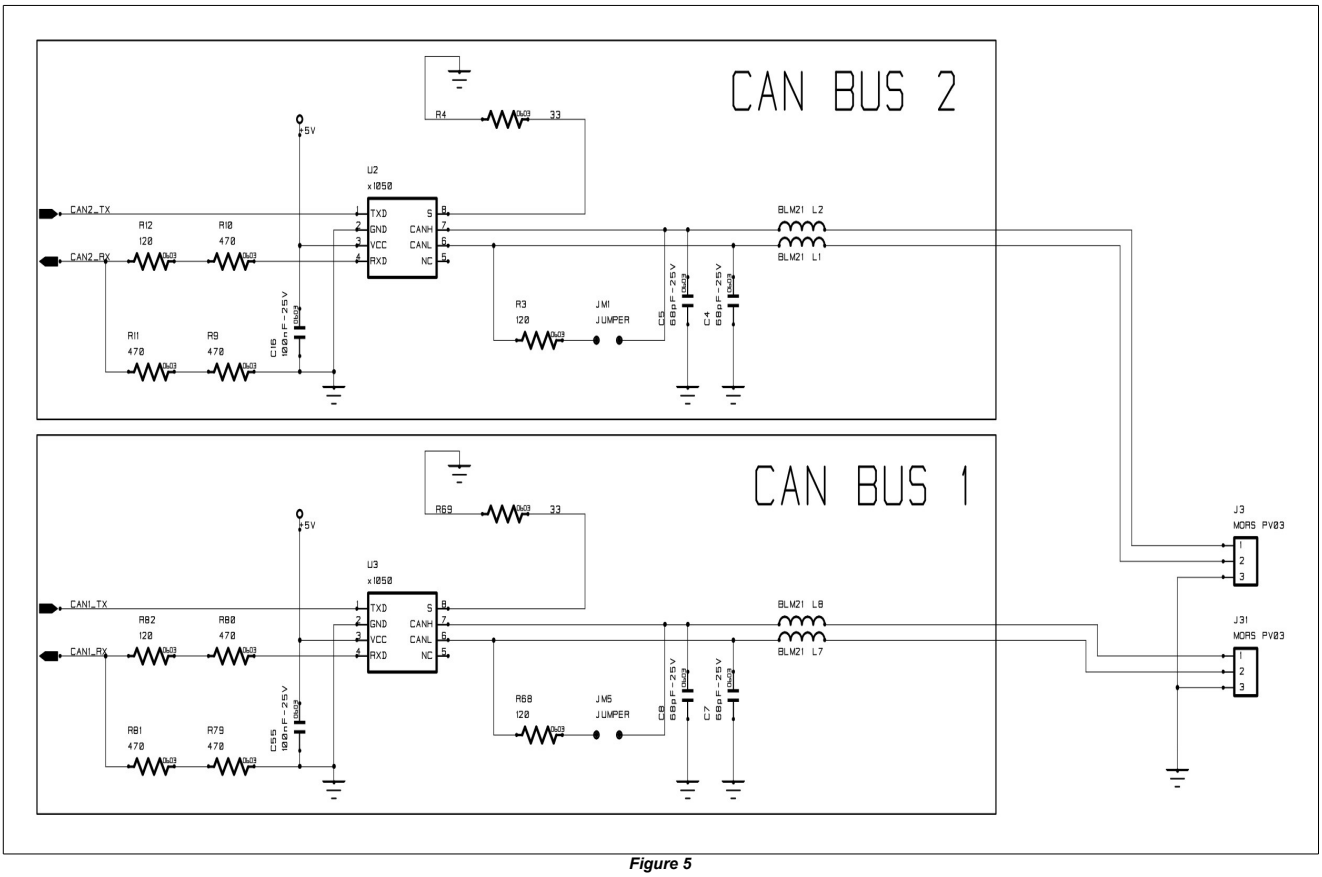


Figure 5

The following table describes the pins' numbering in the main connector involved in the CAN interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
118	CAN0_TX	CAN 0 transmit signal	Y	+3,3V
119	CAN0_RX	CAN 0 receive signal	Y	+3,3V
120	CAN1_TX	CAN 1 transmit signal	Y	+3,3V
121	CAN1_RX	CAN 1 receive signal	Y	+3,3V

Table 10

The Jumpers JM1, JM5 are used to close the load of the CAN Bus to 120 Ω

5.6 How to design the Ethernet interface

The Freescale Chimera Ethernet Media Access Controller (MAC number 0) is designed to support both 10 and 100 Mbps Ethernet/IEEE standard 802.3™ networks. The 10-Mbps and 100-Mbps RMII Ethernet physical interfaces is supported. In the figure is shown how to connect the Ethernet interface to module.

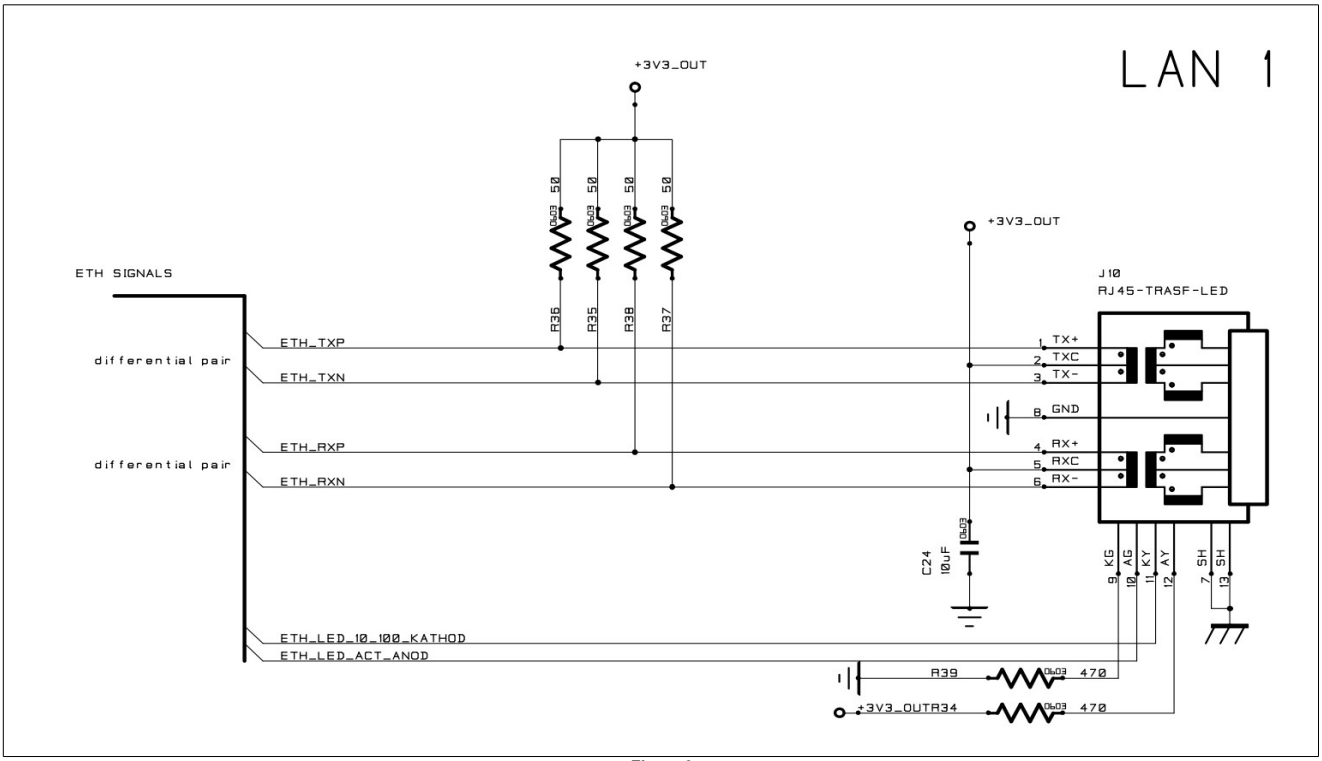


Figure 6

In the table below are listed all Ethernet signal of the module:

Number	Name	Primary Function Description	GPIO Capable	Voltage
127	ETH_TXN	Fast Ethernet TXN signal	-	+3,3V
129	ETH_TXP	Fast Ethernet TXP signal	-	+3,3V
131	ETH_RXN	Fast Ethernet RXN signal	-	+3,3V
133	ETH_RXP	Fast Ethernet RXP signal	-	+3,3V
137 *	ETH_LED_10_100_KATHOD	Led Indicator Cathode signal	-	+3,3V
139 *	ETH_LED_ACT_ANOD	Led indicator Anode signal	-	+3,3V

Table 11

* ***Note:*** If not used, this pin must be left floating.

5.6.1 Component Placement considerations

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and PHY should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between PHY and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector, away from the board of PCB.
5. The 49.9 ohm pull-up resistors on the differential lines should be placed within 10 mm of the PHY device
6. The signals RX & TX should be independently matched in length to within 6mm

See following figure

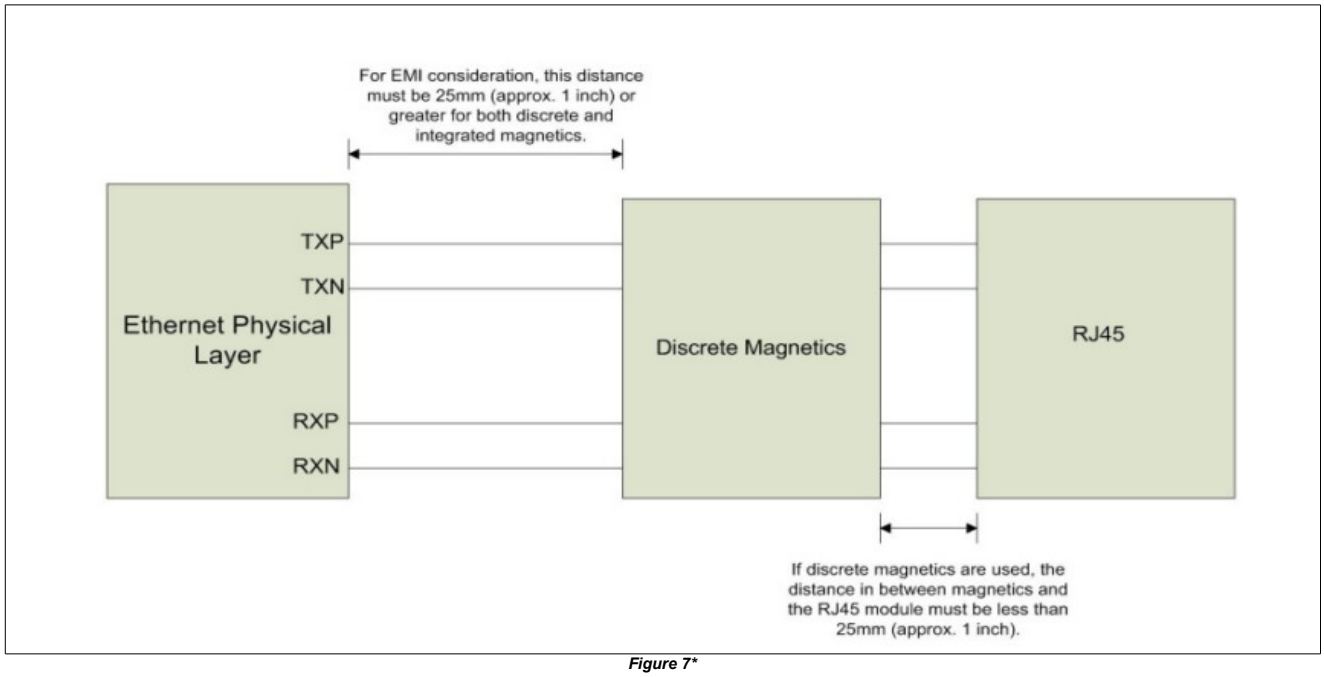


Figure 7*

The PHY used in the module is the ***SMSC LAN8710***.
Please for more information refer to the ***SMSC Ethernet Physical Layer Layout Guidelines***.

For a list of magnetics selected to operate with the SMSC LAN8710, please refer to the Application note ***AN 8-13 Suggested Magnetics.***

*** this is the figure 2.3 from SMSC Ethernet Physical Layer Layout Guidelines**

5.6.2 Cable Transient Event and PHY Protection

Cable transient events are + and - DC surges that are induced across the transformer onto the PHY side of the TX+/- and RX+/- signals as shown in figure below. The PHY side of the transformer should not contain any DC component other than the typical 3.3V pull-up on the centre tap of the transformer for analog signal biasing. In POE applications, there are two main reasons why cable transient events occur, negative rail PSE switching, and hot unplug/plug-in events.

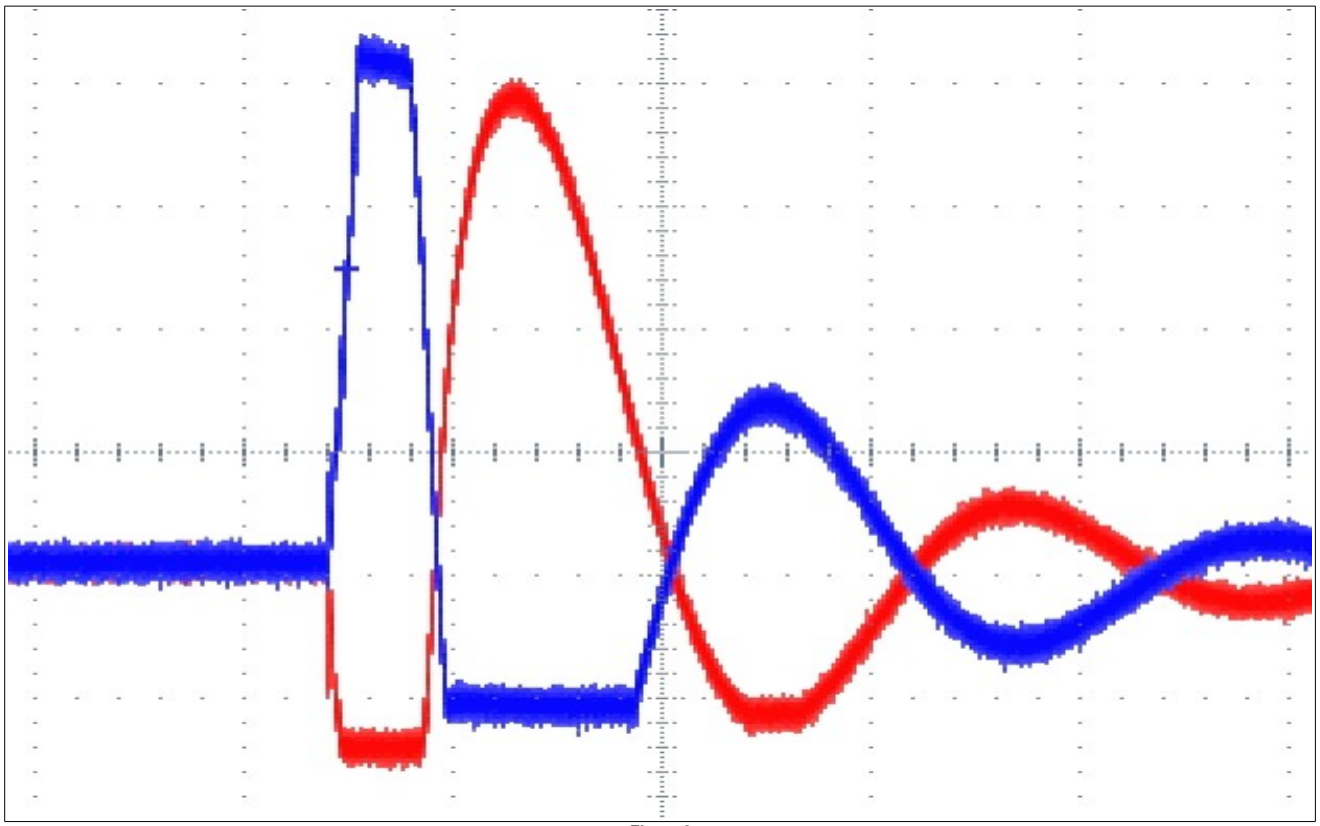


Figure 8

Transient observer on the PHY side of Eth Magnetics
Scale X = 1uS/div
Scale Y = 5V/div

Note: *for further details about Cable transient events please refers to file AN1718 of SMSC*

5.6.3 PHY Ethernet

When using an SMSC device in POE applications, external transient protection is recommended as shown in figure below. The schematic shows an example of a TVS suppression solution. This solution couples the energy differentially into the two TVS diodes on each differential pair. For cases when the transient is across the TX+/- pair in the figure below, the voltage is clamped at a value equivalent to the forward bias voltage across D1, plus the zener voltage of D2. This transient voltage must be clamped at a voltage no **greater than 5V**. D3 and D4 act the same way when the transient is across the RX+/- differential pair. The total capacitance seen by each differential pair must not exceed 50pF (25pF single ended).

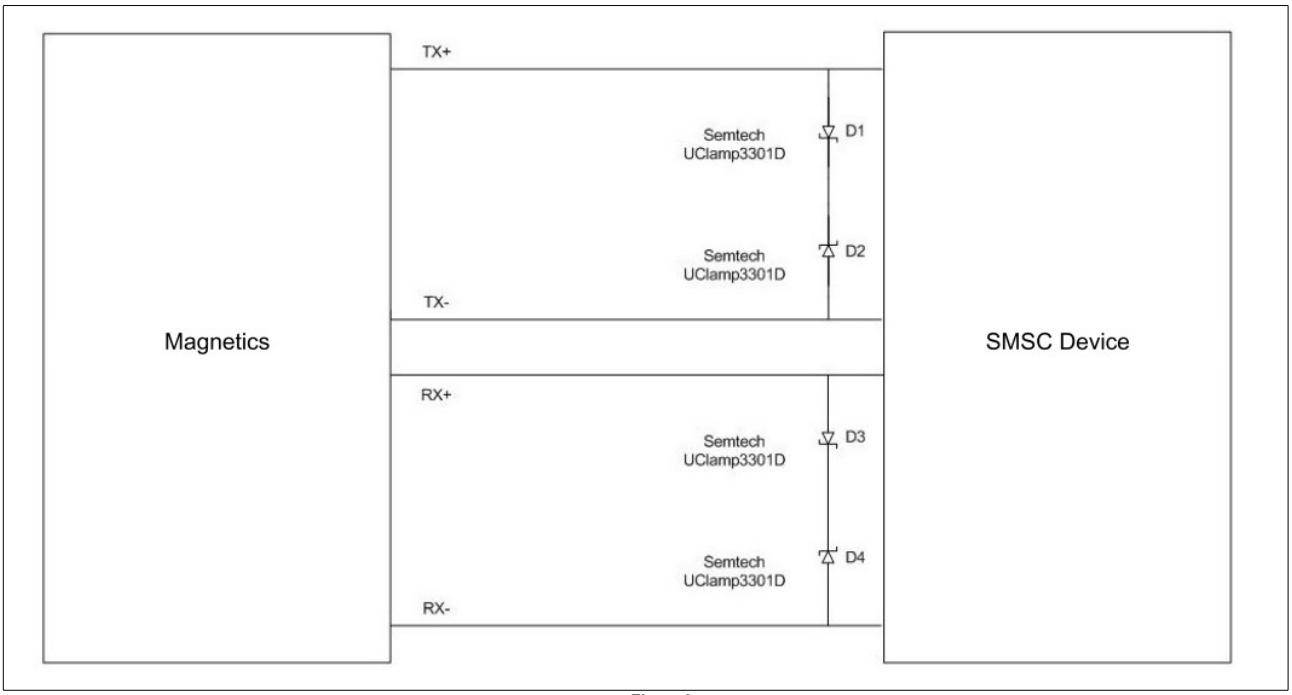


Figure 9

Recommended by SMSC:

Low Voltage µClamp™ for ESD and CDE Protection Semtech uClamp3301D

Note: *for further details about PHY Protection please reffers to file AN1718 of SMSC*

5.7 USB interface

5.7.1 How to connect the USB/OTG interface

The Freescale Chimera USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. In figure is shown how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. In the following table are listed all USB/OTG signal of mail connector.

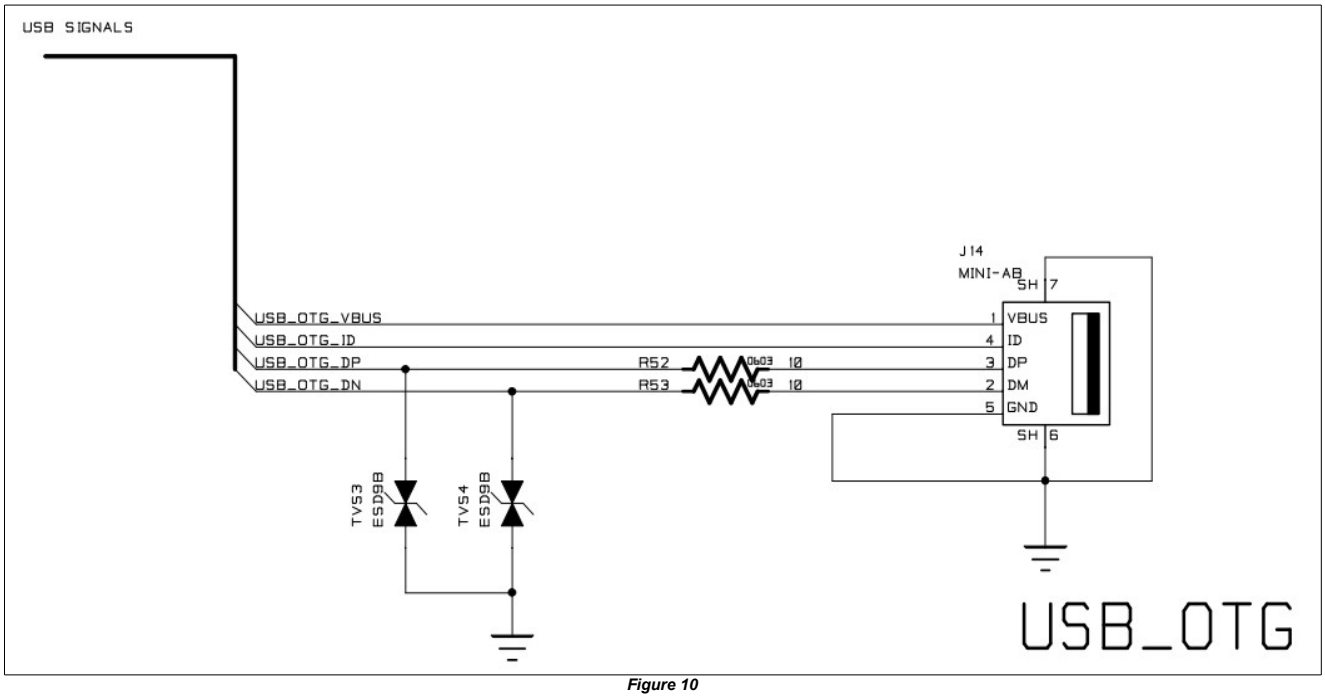


Figure 10

Number	Name	Primary Function Description	GPIO Capable	Voltage
195	USB_OTG_VBUS*	USB on the go interface	N	-
192	USB_OTG_DP	USB on the go interface	N	-
191	USB_OTG_ID	USB on the go interface	N	-
193	USB_OTG_DN	USB on the go interface	N	-

Table 12

**Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to 5V*

5.7.2 How to connect the USB host interface

The module provides one port for USB host interface. In the figure is shown how to connect this port to the Module.

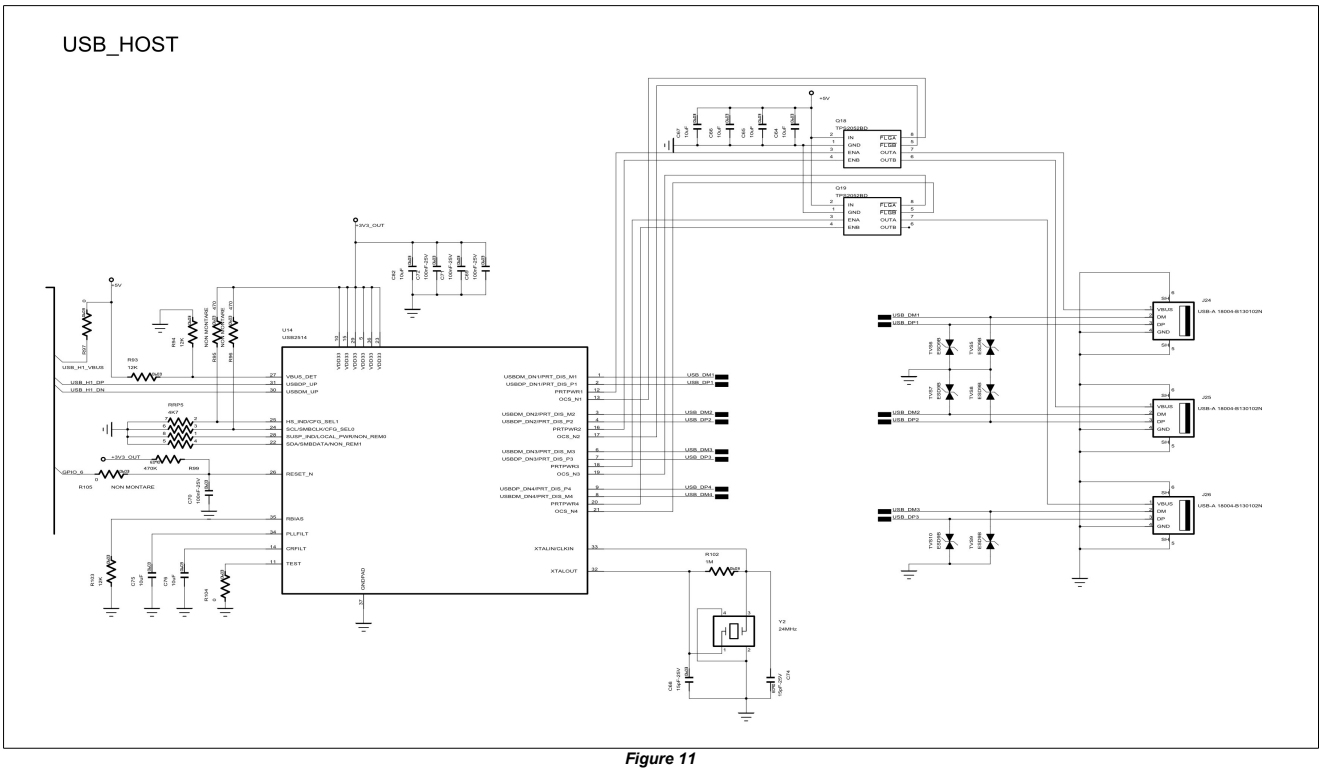


Figure 11

Engicam's evaluation board is equipped with an USB HUB to multiply the USB port available on module, if you just need one port you can connect it as one of the four output ports of the HUB

Number	Name	Primary Function Description	GPIO Capable	Voltage
180	USB1_VBUS	USB HOST interface	N	-
194	USB1_DP	USB HOST interface	N	-
196	USB1_DM	USB HOST interface	N	-

Table 13

** Note: The USB1_VBUS is an INPUT power signal. It must be connected to 5V*

5.8 How to connect the SD/CARD interface

The Freescale Chimera enhanced Secured Digital Host Controller (eSDHC) provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. The module include this features and in figure is shown how the Micro SD Card connector is connected to Chimera Module in the evaluation board. The eSDHC signal of the module's main connector are listed in table below.

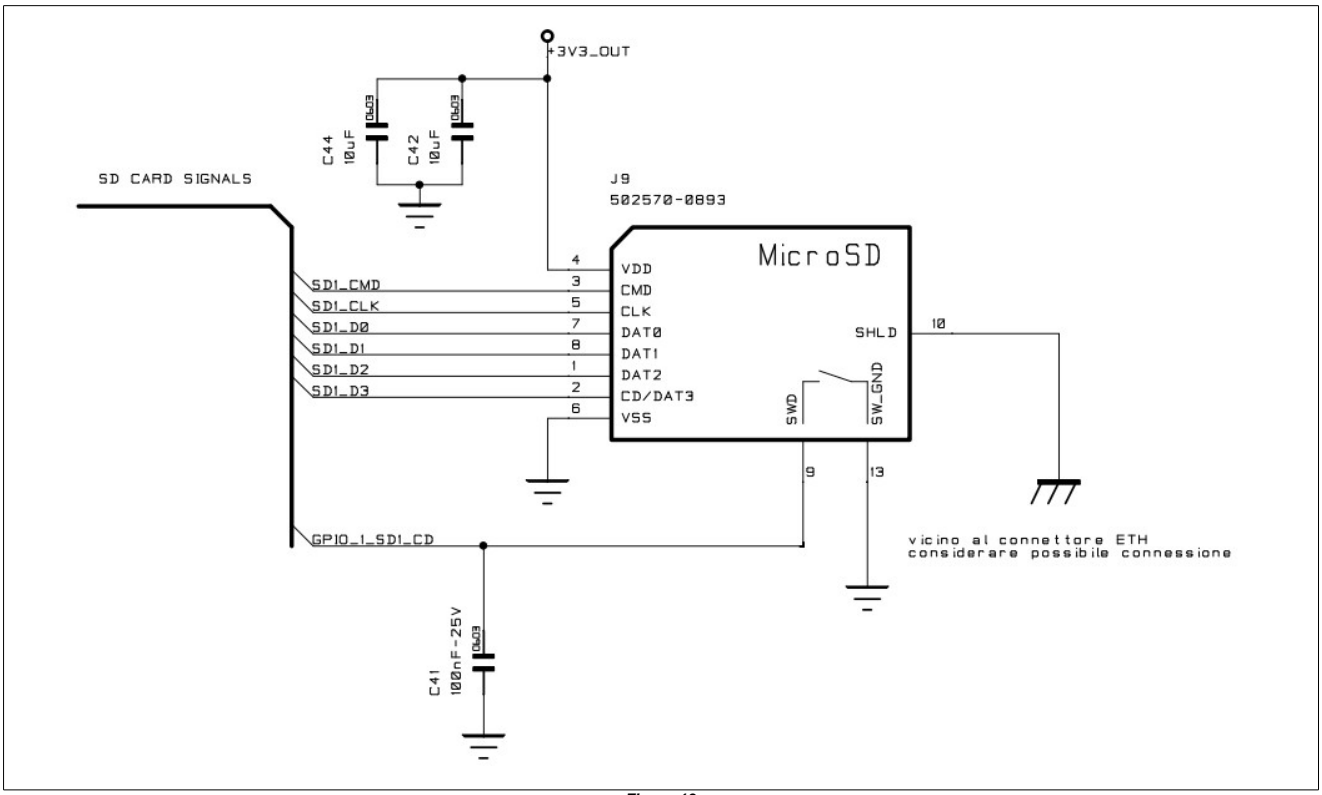


Figure 12

Number	Name	Primary Function Description	GPIO Capable	Voltage
183	PTA7_SD1_CD	eSDHC CD Signal	Y	+3,3V
185	SD1_D2	eSDHC DAT 2 signal	Y	+3,3V
186	SD1_D3	eSDHC DAT 3 signal	Y	+3,3V
187	SD1_D1	eSDHC DAT 1 signal	Y	+3,3V
188	SD1_D0	eSDHC DAT 0 signal	Y	+3,3V
189	SD1_CLK	eSDHC CLK signal	Y	+3,3V
190	SD1_CMD	eSDHC CMD signal	Y	+3,3V

Table 14

5.9 How to connect an LCD display

The evaluation board of Chimera is equipped with one RGB data port, this interface contains RGB data of 18 bit, pixel clock.
Following are reported the schematic interface with parallel URT and the map of signals.

Number	Name	Primary Function Description	GPIO Capable	Voltage
125	DISP0_CLK	LCD interface	Y	+3,3V
141	DISP0_D17	LCD interface	Y	+3,3V
142	DISP0_D16	LCD interface	Y	+3,3V
143	DISP0_D15	LCD interface	Y	+3,3V
144	DISP0_D14	LCD interface	Y	+3,3V
145	DISP0_D13	LCD interface	Y	+3,3V
146	DISP0_D12	LCD interface	Y	+3,3V
147	DISP0_D11	LCD interface	Y	+3,3V
148	DISP0_D10	LCD interface	Y	+3,3V
149	DISP0_D9	LCD interface	Y	+3,3V
150	DISP0_D8	LCD interface	Y	+3,3V
151	DISP0_D7	LCD interface	Y	+3,3V
152	DISP0_D6	LCD interface	Y	+3,3V
153	DISP0_D5	LCD interface	Y	+3,3V
154	DISP0_D4	LCD interface	Y	+3,3V
155	DISP0_D3	LCD interface	Y	+3,3V
157	DISP0_D2	LCD interface	Y	+3,3V
158	DISP0_D1	LCD interface	Y	+3,3V
159	DISP0_D0	LCD interface	Y	+3,3V
160	DISP0_VSYNC	LCD interface	Y	+3,3V
161	DISP0_HSYNC	LCD interface	Y	+3,3V
162	DISP0_DRDY	LCD interface	Y	+3,3V

Table 15

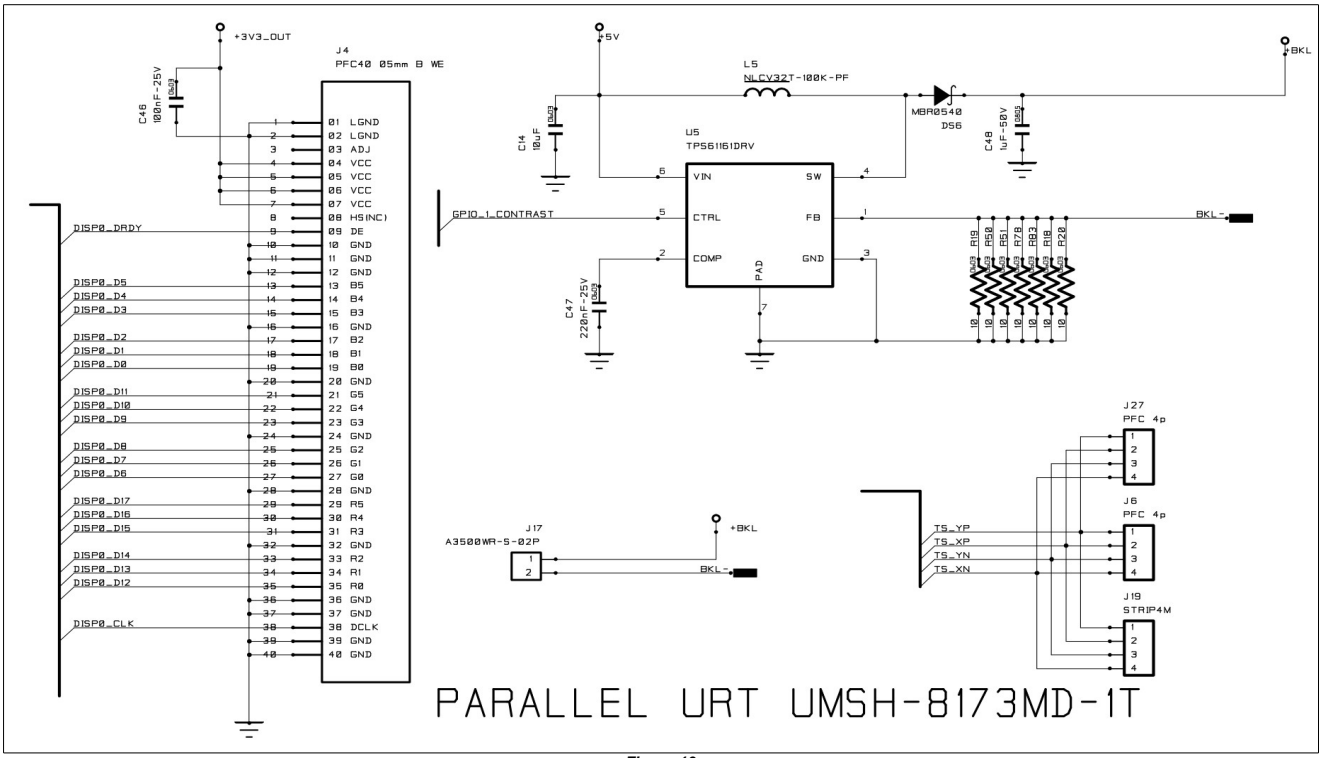


Figure 13

5.9.1 Connection map for 18 bit TFT only

The following map represent the connection mode applied to 18 bit TFT display
For every connection the colour controlled is joined

Number	Name	18 bit TFT connections
159	DISP0_D0	BLU 0
158	DISP0_D1	BLU 1
157	DISP0_D2	BLU 2
155	DISP0_D3	BLU 3
154	DISP0_D4	BLU 4
153	DISP0_D5	BLU 5
152	DISP0_D6	GREEN 0
151	DISP0_D7	GREEN 1
150	DISP0_D8	GREEN 2
149	DISP0_D9	GREEN 3
148	DISP0_D10	GREEN 4
147	DISP0_D11	GREEN 5
146	DISP0_D12	RED 0
145	DISP0_D13	RED 1
144	DISP0_D14	RED 2
143	DISP0_D15	RED 3
142	DISP0_D16	RED 4
141	DISP0_D17	RED 5

Table 16

5.10 JTAG Interface

Joint Test Action Group (**JTAG**) is the common name used for the IEEE 1149.1 standard entitled **Standard Test Access Port and Boundary-Scan Architecture** for test access ports used for testing printed circuit boards using boundary scan. JTAG is often used as an IC debug or probing port.

There are no official standards for JTAG adapter physical connectors. Development boards usually include a header to support preferred development tools; in some cases they include multiple such headers, because they need to support multiple such tools. For example, a micro-controller, FPGA, and ARM application processor will rarely share tools, so a development board using all of those components might have three or more headers. Production boards may omit the headers; or when space is tight, just provide JTAG signal access using test points.

Figure below is shown how to connect a JTAG interface to Chimera Module.

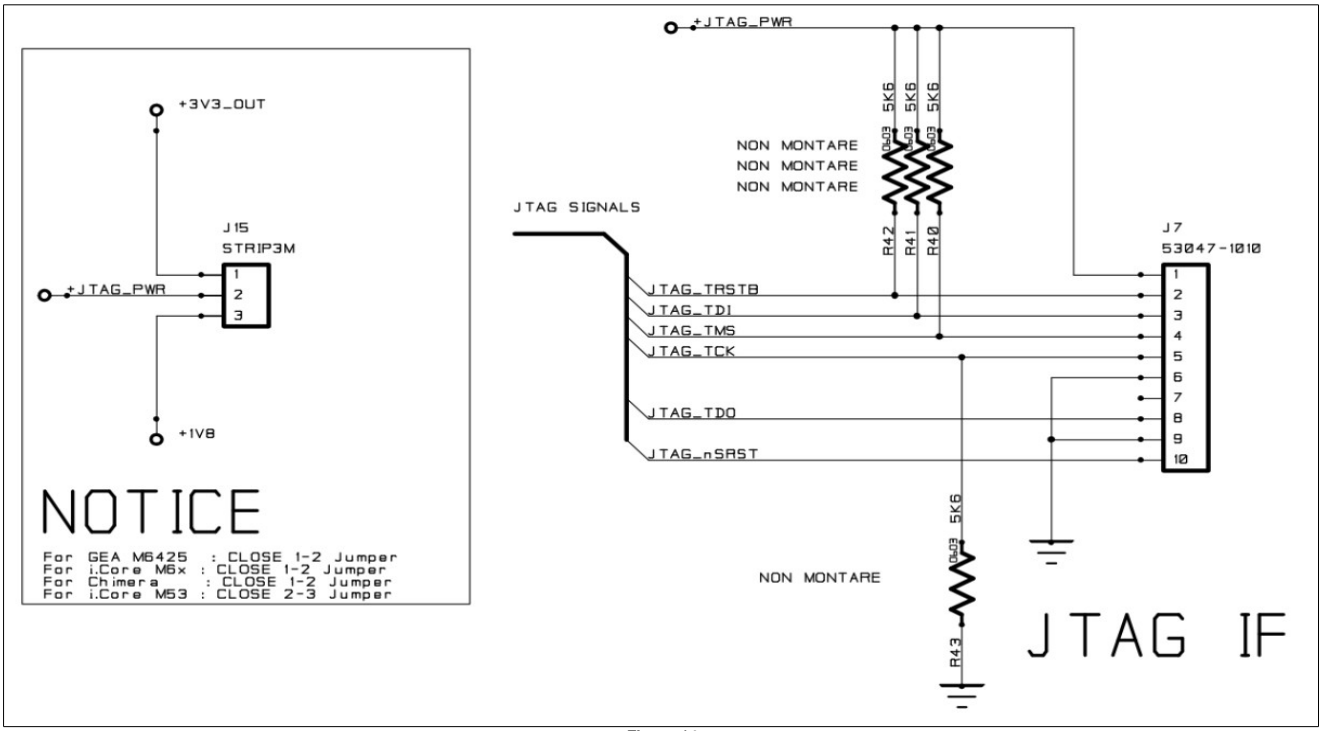


Figure 14

In the table are listed all JTAG signals as mapped in the main connector.

Number	Name	Primary Function Description	GPIO Capable	Voltage
173	JTAG_TRSTB	JTAG Interface	N	+3,3V
174	JTAG_TDO	JTAG Interface	N	+3,3V
175	JTAG_TDI	JTAG Interface	N	+3,3V
176	JTAG_TMS	JTAG Interface	N	+3,3V
177	JTAG_TCK	JTAG Interface	N	+3,3V
179	JTAG_nSRST	JTAG Interface with Pull-up on module	N	+3,3V

Table 17

To obtain the compatibility with Vybrid Module, in the evaluation board of the Chimera the JTAG signals are pulled up through +JTAG_PWR which could be put to +1,8V or +3,3V using jumper referenced J15.
If you intend to use both module on your main board and don't use a JTag external console is mandatory to remove the pull-up/down resistors.

Please for further details refer to Vybrid reference manual.

5.11 Boot Mode Pin

Boot mode pin determines how the module boot. The following table listed the possible options of the boot mode:

BOOT_MODE	Action
0	Boot from internal modules
1	Boot from USB/OTG

Table 18

The boot from USB OTG is usually used for the boot loader deploy.

In the figure is shown the boot section compatible with iCoreM53 module. The closing of JM2 corresponds to put at logical 1 the boot mode pin. Also in this case to switch from iCoreM53 module to Chimera or other modules is necessary to use the J15 jumper to set the right value of voltage.

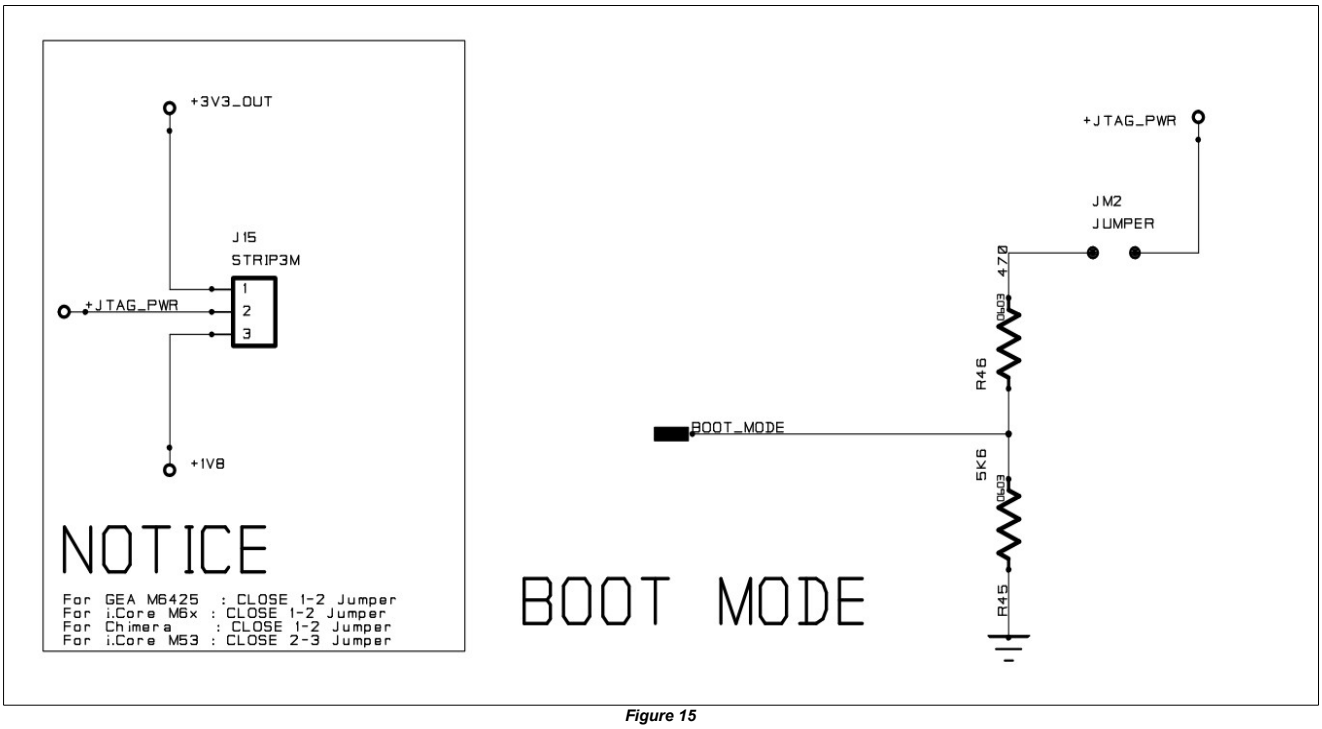


Figure 15

In Table below is listed the boot mode Pin numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
181	BOOT_MODE	Boot from USB/UART or on board Nand Flash	N	-

Table 19

In the evaluation board we set-up all the configurations for bootstrap from NAND and from SD card

In the figure below is shown the boot options for Vybrid.

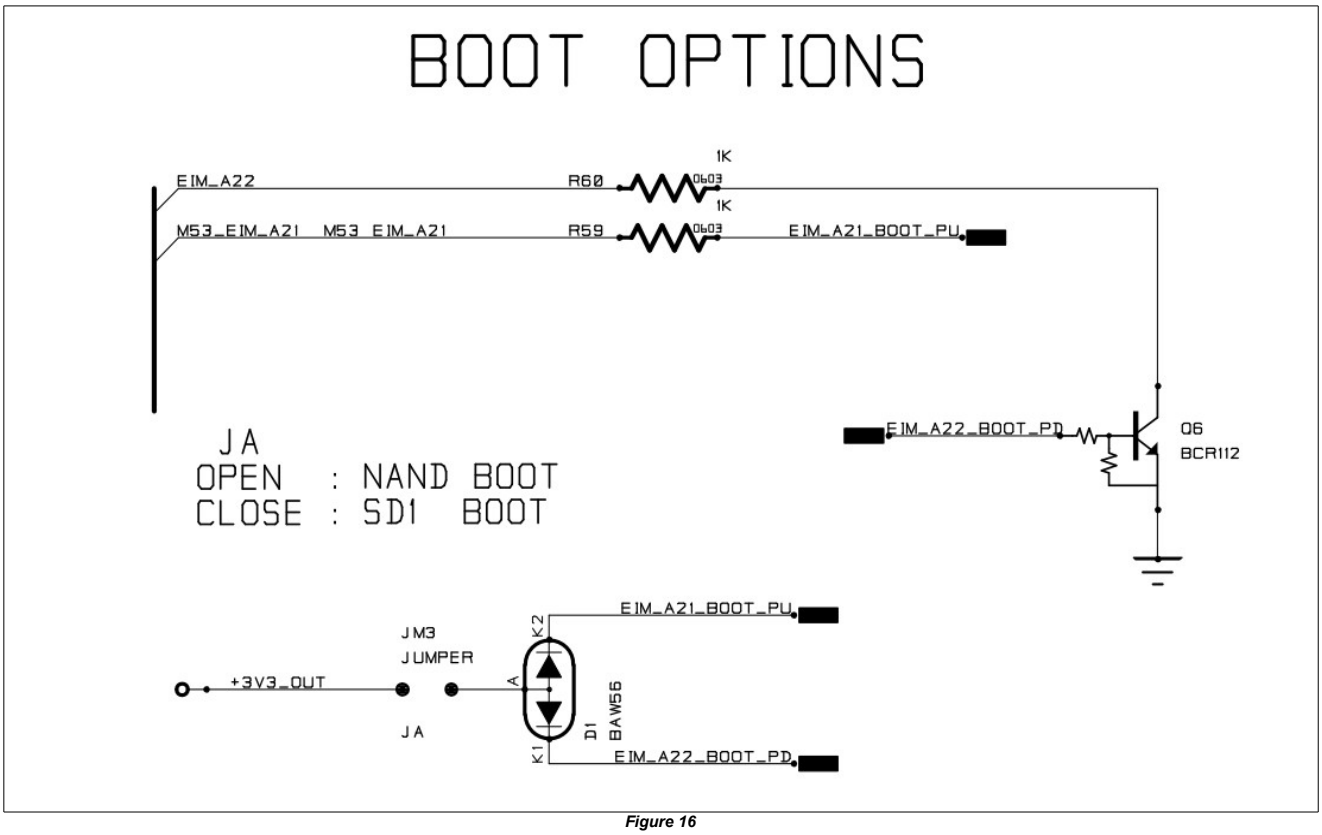


Figure 16

The signal used to configure the boot is **nSD_BOOT**. **This signal, label EIM_A22 on carrier board, is pulled up with a 55KOhm resistor in the Chimera Module (signal name nSD_BOOT)**.

In the standard condition the signals are setting to boot from NAND Flash (jumper left open), or from SD card simply closing the jumper.

Following you can see the signal logical level on modules to implement a custom starting sequence.

BOOT FROM NAND	
Signal	**LOGIC LEVEL**
nSD_BOOT	1

Table 20

The choice of boot from SD1 means short-cutting the jumper A in the evaluation board, you can have the same effect by pulling EIM_A22 down with a 1KOhm resistor.

BOOT FROM SD1	
Signal	**LOGIC LEVEL**
nSD_BOOT	0

Table 21

In the evaluation board whatever starting sequence you chose you must consider the pins 80 of main connector useful for boot configuration.

In a custom board you must also consider belonging to the boot sequence the following signals:

Signal	Connector Pin number
nSD_BOOT	80
DISP0_D17	141
DISP0_D16	142
DISP0_D15	143
DISP0_D14	144
DISP0_D11	147
DISP0_D10	148
DISP0_D9	149
DISP0_D8	150
DISP0_D5	153
DISP0_D4	154
DISP0_D3	155
DISP0_D2	157
DISP0_VSYNC	160
DISP0_HSYNC	161
DSPI0_PCS0 *	171
EXT_AUDIO_MCLK **	34

Table 22

Note: Please leave these pins floating during the processor's reset status

* DO NOT use pull up on this signal (12K pull down)

** DO NOT use pull down on this signal (1K pull up)

Note: for using of any customized boot options please refer to the Freescale reference manual of Vybrid

5.12 Touch Screen Controller

Touch screen signals are implemented on MAX11801 Touch-Screen Controllers. The devices contain a 12-bit SAR ADC and a multiplexer to interface with a resistive touch-screen panel. The MAX11801's reference voltage for Touch screen signals is +3,3V

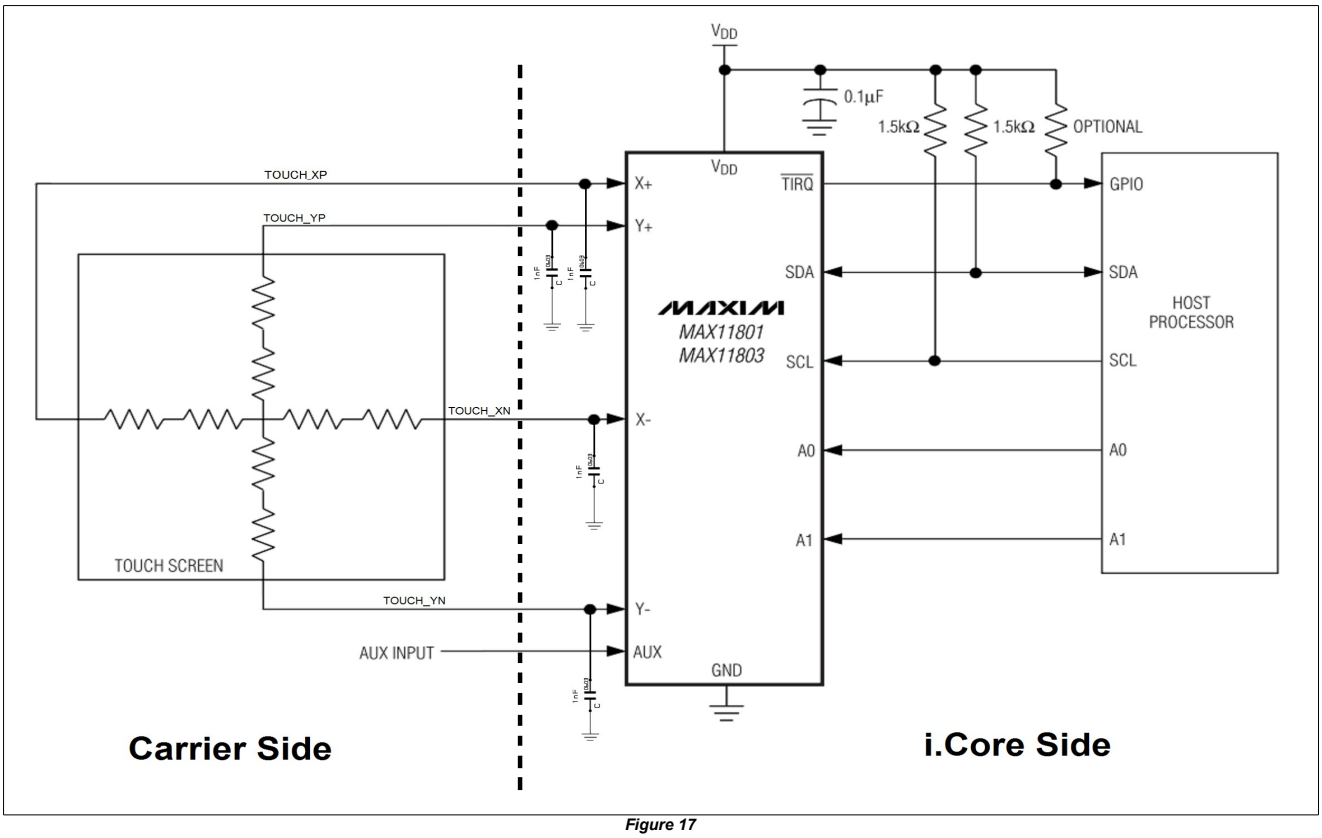


Figure 17

WARNING:
It's strongly recommended to put in the carrier board's layout a ceramic capacitor per signal line (X, Y P/N) as close as possible to SODIMM connector. Through the adjust of capacitor value it's possible to improve the disturbance due to noise on X/Y signals.

Note: A 1nF capacitor is already present on each line of the i.CoreM6x modules but it could not be enough to suppress noise.

6. Peripheral multiplexing description

Following we describe the opportunity to use alternative interfaces using the properties of multiplexing pin
Please refer to the Freescale's reference manual and documentation for further details (document name Vybrid RM).

6.1 SPI & IIS Configuration

Using pin multiplexing 's features we may have the following SPI and IIS connections. In the tables below are shown the output signals on the Connector's module.

DSPI0 signals interfaces +3,3V

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
167	PTB21	DSPI0_SOUT	+3,3V
168	PTB20	DSPI0_SIN	+3,3V
169	PTB22	DSPI0_SCK	+3,3V
171	PTB19	DSPI0_PCS0 *	+3,3V

Table 23

DSPI1 signals interfaces +3,3V

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
73	PTD5	DSPI1_PCS0	+3,3V
77	PTD6	DSPI1_SIN	+3,3V
90	PTD8	DSPI1_SCK	+3,3V
91	PTD7	DSPI1_SOUT	+3,3V

Table 24

The following tables show the pin configurations for IIS Bus on module's connector.

SAI2 (Signal Audio interface)

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
82 / 124	PTC12 / PTA16	SAI2_TX_BCLK	+3,3V
14 / 122	PTA18 / PTC15	SAI2_TX_DATA	+3,3V
15 / 115	PTA19 / PTC17	SAI2_TX_SYNC	+3,3V
23 / 114	PTA22 / PTC14	SAI2_RX_DATA	+3,3V

Table 25

SAI3 (Signal Audio interface)

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
188	PTA26	SAI3_TX_BCLK	+3,3V
186	PTA29	SAI3_TX_DATA	+3,3V
110	PTA31	SAI3_TX_SYNC	+3,3V
185	PTA28	SAI3_RX_DATA	+3,3V

Table 26

6.2 Alternative PWM pins table

It's possible to set the pins shown in the following table as PWM signals.

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
14 / 67	PTA18 / PTB8	FTM1_QD_PHA	+3,3V
15 / 75	PTA19 / PTB9	FTM1_QD_PHB	+3,3V

Table 27

6.3 Flex Timer Module (FTM)

Using pin multiplexing 's features we may have the following FTM. In the tables below are shown the output signals on the Connector's module.

FTM0

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
35	PTB0	FTM0_CH0	+3,3V
36	PTB1	FTM0_CH1	+3,3V
37	PTB2	FTM0_CH2	+3,3V
38	PTB3	FTM0_CH3	+3,3V
116	PTB4	FTM0_CH4	+3,3V
117	PTB5	FTM0_CH5	+3,3V
40	PTB6	FTM0_CH6	+3,3V
132	PTB7	FTM0_CH7	+3,3V

Table 28

FTM1

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
67	PTB8	FTM1_CH0	**+3,3V**
75	PTB9	FTM1_CH1	**+3,3V**

Table 29

FTM3

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
6	PTD31	FTM3_CH0	+3,3V
7	PTD30	FTM3_CH1	+3,3V
8	PTD29	FTM3_CH2	+3,3V
9	PTD28	FTM3_CH3	+3,3V
10	PTD27	FTM3_CH4	+3,3V
11	PTD26	FTM3_CH5	+3,3V
12	PTD25	FTM3_CH6	+3,3V
13	PTD24	FTM3_CH7	+3,3V

Table 30

6.4 I2C Configuration

It's possible to set the pins shown in the following table as I2C signals.

I2C0 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
184 / 119	PTA12 / PTB14	I2C0_SCL	+3,3V
124 / 118	PTA16 / PTB15	I2C0_SDA	+3,3V

Table 31

I2C1 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
191 / 121	PTA17 / PTB16	I2C1_SCL	+3,3V
14 / 120	PTA18 / PTB17	I2C1_SDA	+3,3V

Table 32

I2C2 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
9 / 23	PTD28 / PTA22	I2C2_SCL	+3,3V
10 / 24	PTD27 / PTA23	I2C2_SDA	+3,3V

Table 33

I2C3 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
111	PTA30	I2C3_SCL	+3,3V
110	PTA31	I2C3_SDA	+3,3V

Table 34

6.5 Alternative UART pins table

The following table shows an alternative UART configuration

UART1 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
116 / 65	PTB4 / PTB23	SCI1_TX	+3,3V
117	PTB5	SCI1_RX	+3,3V
40	PTB6	SCI1_RTS	+3,3V
132 / 70	PTB7 / PTB26	SCI1_CTS	+3,3V

Table 35

UART2 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
40 / 108	PTB6 / PTD0	SCI2_TX	+3,3V
132 / 109	PTB7 / PTD1	SCI2_RX	+3,3V
106	PTD2	SCI2_RTS	+3,3V
105	PTD3	SCI2_CTS	+3,3V

Table 36

UART3 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
112 / 111	PTA20 / PTA30	SCI3_TX	+3,3V
113 / 110	PTA21 / PTA31	SCI3_RX	+3,3V
65	PTB23	SCI3_RTS	+3,3V

Table 37

UART4 interfaces

Pin number	Pin Name on Vybrid	Signal reference	Voltage reference
185	PTA28	SCI4_TX	+3,3V
186	PTA29	SCI4_RX	+3,3V
111	PTA30	SCI4_RTS	+3,3V
110	PTA31	SCI4_CTS	+3,3V

Table 38