TB3226

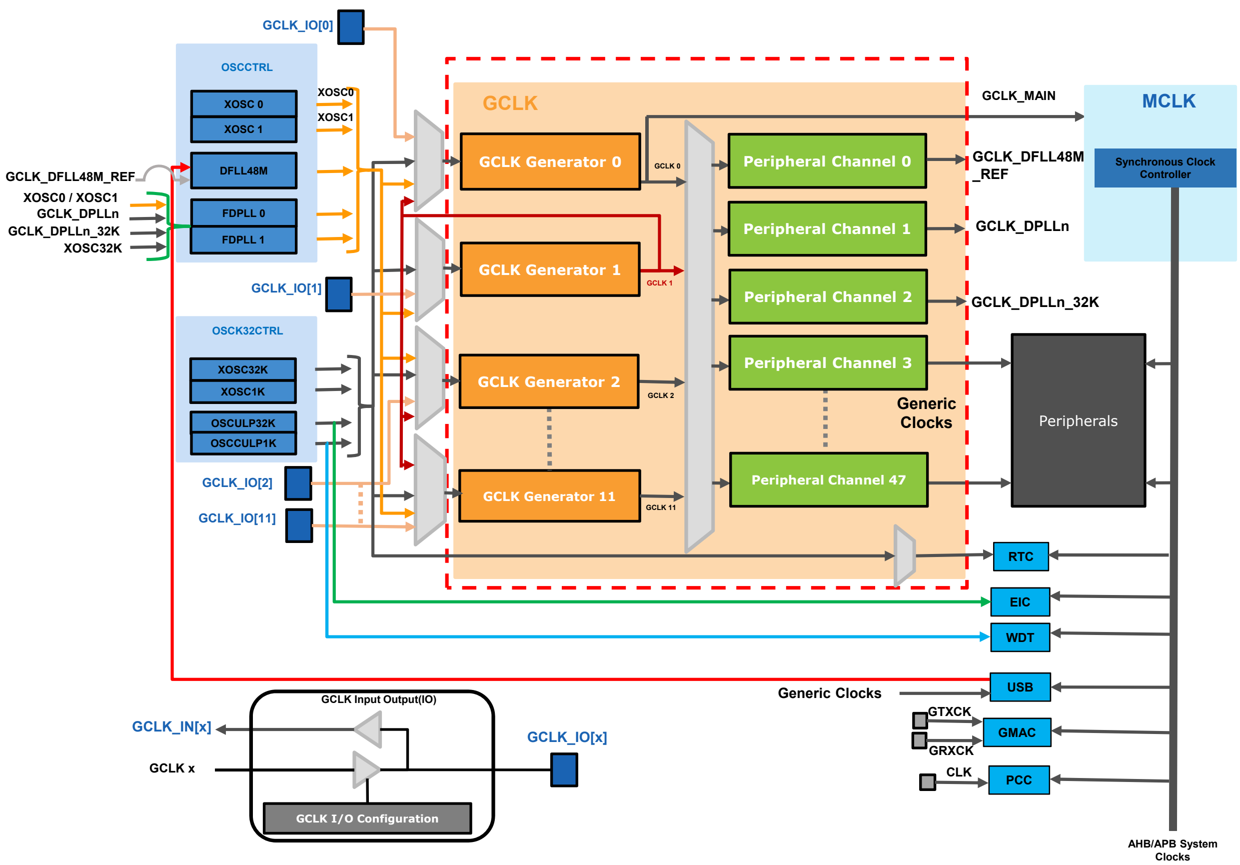
Clock System Configuration and Usage on SAM E5x (Cortex M4) Devices

Introduction

The SAM E5x family of microcontrollers (MCUs) contains a sophisticated clock distribution system designed to give maximum flexibility to the user application. The clock system allows the tuning of the performance and power consumption of the device in a dynamic manner to achieve the best trade-off between the two for an application.

The following figure illustrates the clock management diagram of the SAM E54 MCU.

Figure 1. SAM E54 Clock Distribution



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1. Description

The clock system of the SAM E54 MCU consists of the following blocks:

Clock Sources
The SAM E54 MCU has several clock source modules. The supported clock source modules are as follows:

OSCCTRL: High frequency clock sources

- XOSCn – 8 to 48 MHz External Oscillator
- DFLL48M – 48 MHz Internal Oscillator (Open Loop)
- FDPLLn – 96 to 200 MHz Fractional Digital Phase Locked Loop Oscillator

OSCK32CTRL: Low-frequency clock sources

- XOSC32K – 32 kHz External Crystal Oscillator, provides both 32 kHz and 1.024 kHz clock outputs
- OSCULP32K – 32 kHz Internal Crystal Oscillator, provides both 32 kHz and 1.024 kHz clock outputs

Generic Clock Controller (GCLK)
The GCLK provides Generic Clocks to various peripheral clock domains. The GCLK consists of 12 GCLK generators and 48 peripheral channels. The GCLK_IO (Generic Clock Controller Input/Output) blocks act as a clock source to the GCLK generators.

Note:
1. GCLK_IO[x] is Generic Input/Output External Clock Signal.
2. GCLK1 is the output of the GCLK generator 1, and is one of the clock sources for all GCLK generators except GCLK generator 1.

The GCLK Generators consists of programmable prescaler. The programmable prescaler scales down the input frequency from one of the Clock Sources (as discussed above) to a slower rate to use with a peripheral.

The peripheral channels multiplex and gate various generator outputs to one or more peripherals within the device. This setup allows a single common generator to feed one or more peripheral channels, which can then be enabled or disabled individually as required.

Main Clock Controller (MCLK)
The MCLK also known as the Synchronous Clock Controller provides the synchronous clocks (CPU, bus (AHB, APB) clocks) to the system. The main clock GCLK_MAIN to the MCLK is fed from the GCLK generator 0 through peripheral channel 0. The MCLK contains clock masks that can turn on and off the user interface of a peripheral as well as prescalers for the CPU clocks.

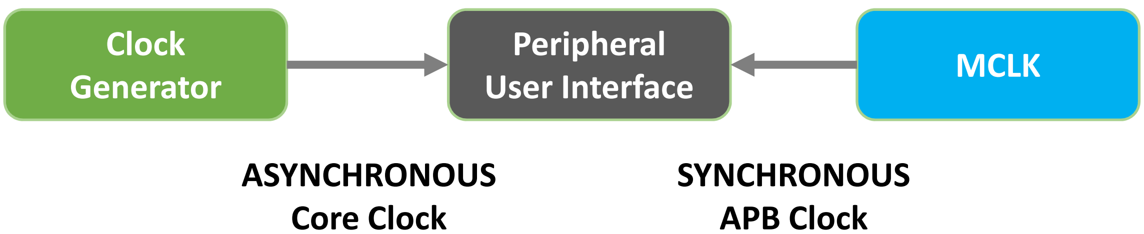
2. Clock Synchronization

The peripherals on the SAM E54 MCU composed of the following two clock domain interfaces:

- Synchronous interface: It is connected to the AHB/APB bus running from the synchronous clock in the Main clock (MCLK) domain. The CPU accesses the peripheral registers through the synchronous interface.
- Asynchronous interface: It is connected to the core peripheral running from the asynchronous peripheral Generic Clock (GCLK) domain. The core peripheral runs at the asynchronous peripheral generic clock.

Communication between these clock domains must be synchronized. This mechanism is implemented in the hardware through the SYNCBUSY peripheral status register. The synchronization process takes place even if the peripheral generic clock is running from the same clock source and on the same frequency as the bus interface.

Figure 2-1. Clock Synchronization



3. Power and Performance Considerations

In an application, the system and peripheral clock frequencies are configured based on the power and performance requirements of the application. Power consumption of a device is directly proportional to the frequency of operation. A device running at high speeds consumes more power versus a device running at low speed.

For SAM E54 MCU, refer to the chapter “Electrical Characteristics” of the device data sheet for power and performance values.

Each GCLK generator operates independently, enabling the GCLK generators to drive different clock frequencies for different peripherals, and to drive different clock frequencies for different instances of the same peripheral. This capability of the GCLK generators enable power saving, hence only the necessary clocks are generated. In Power Saving mode of the MCU, when a peripheral is not utilizing the peripheral clock, the GCLK generator will not source from the oscillator until the peripheral requests the clock.

As noted above, the peripherals on the SAM E5x devices run on the asynchronous clock domain. These asynchronous peripheral clocks are synchronized to the system clocks (CPU, AHB/APB) when the CPU accesses the peripheral registers. The synchronization time is an important factor in the overall response time of the system.

For example, running a peripheral with a very low speed has a lower active power consumption. However, at the same time, the synchronization to the synchronous clock domain is dependent on the peripheral clock speed. The slower peripheral clock leads to lower response time and needs more wait time for the synchronization to complete.

4. Configuring Clocks with MPLAB Harmony v3

MPLAB® Harmony is a modular framework that provides interoperable firmware libraries for application development on 32-bit microcontrollers and microprocessors. It includes an easy to use graphical user interface, MPLAB Harmony Configurator (MHC) for selection, configuration, generation of starter code, peripheral libraries, and middleware (USB, TCP/IP, graphics, and so on). The MHC provides an easy to use UI window, Clock easy View, to configure system and peripheral clocks.

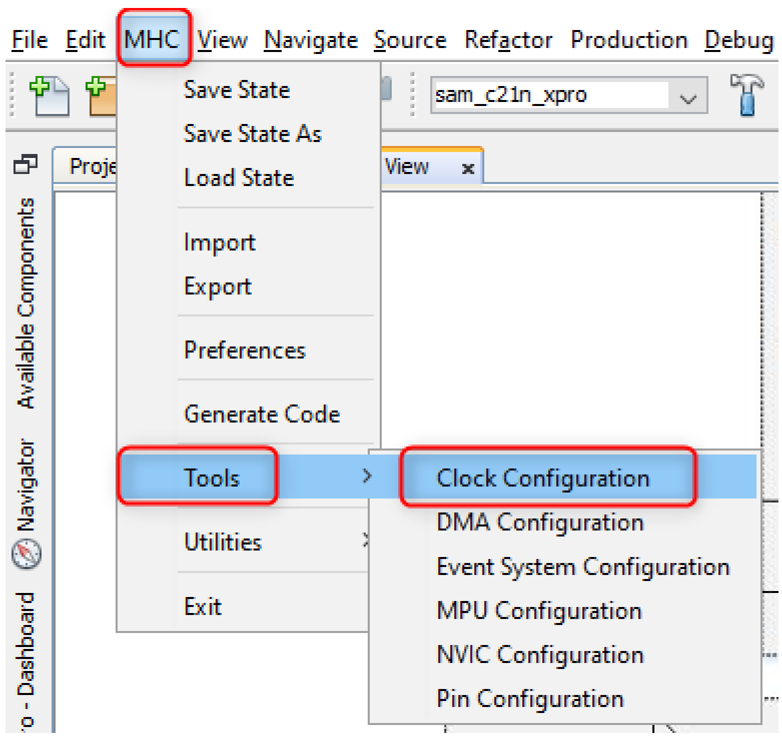
For detailed information on MPLAB Harmony v3 refer to: https://www.microchip.com/mplab/mplab-harmony/mplab-harmony-v3.

4.1 Use Case Scenarios

The following use case scenarios demonstrate how to use MHC Clock Manager, Clock Easy View window to configure the clocks.

1. To launch Clock Easy View in MPLAB X IDE, select **MHC** and then select *Tools* > *Clock Configuration*, see figure below.

Figure 4-1. Harmony 3 Clock Configuration Launcher



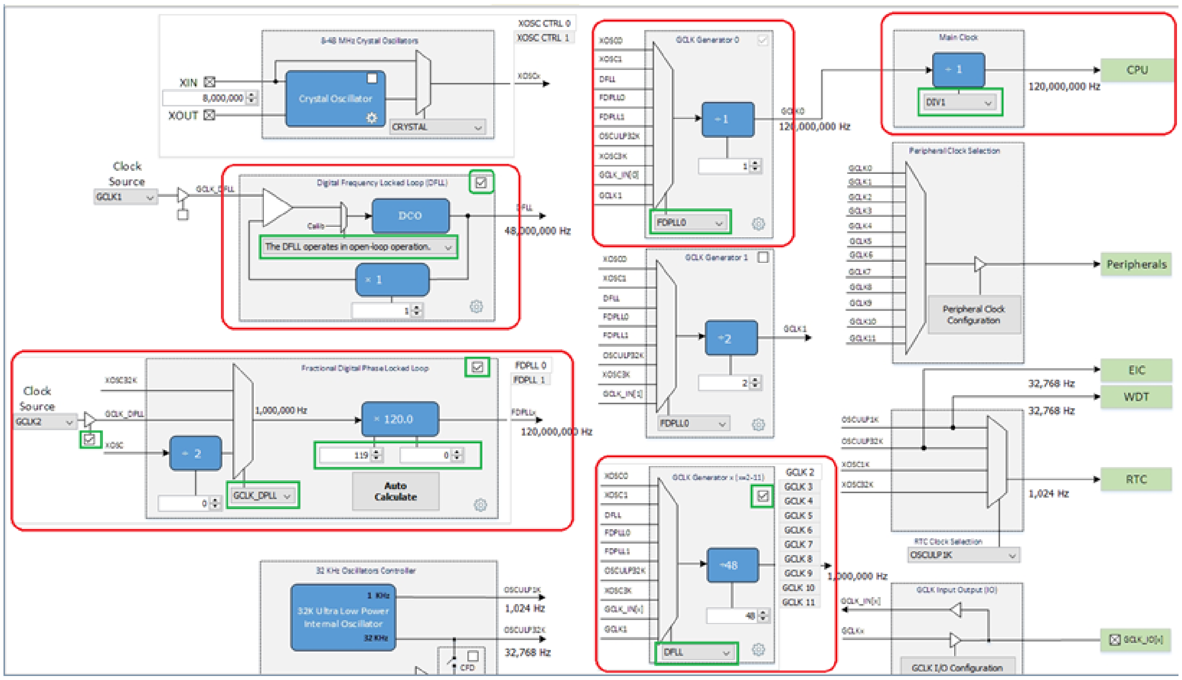
2. Click on the **Clock Easy View** tab.

Use Case Scenario 1

Configure the device to run at a maximum possible speed. Measure the frequency of the configured clock by routing a prescaled clock signal to a GPIO pin.

1. SAME54 operates at 120 MHz maximum frequency. One of the FDPLL must be configured and enabled to run the main clock at the maximum frequency. All clocks in the system are routed through the GCLK generators, therefore the configured FDPLL must be fed as input to the GCLK0 generator and a suitable clock divider and masker must be selected to achieve the maximum frequency (120 MHz). Refer to the following figure to configure the main clock.

Figure 4-2. Harmony 3 Main Clock Configuration



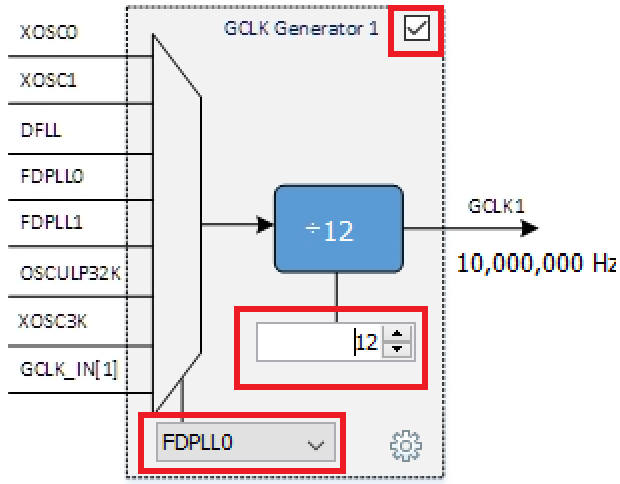
Follow these steps to configure the system to run at maximum frequency:

- Configure and enable the DFLL in Open-Loop mode to generate 48 MHz.
- Configure and enable the GCLK2 to generate 1 MHz from the DFLL.
- Configure and enable the FDPLL0 to generate 120 MHz using the GCLK2 and feed this FDPLL output to the GCLK0 by selecting the FDPLL0 as the source. The Main Clock will be derived from the GCLK0.

Tip: Double click on the Clock Easy View tab to maximize the window.

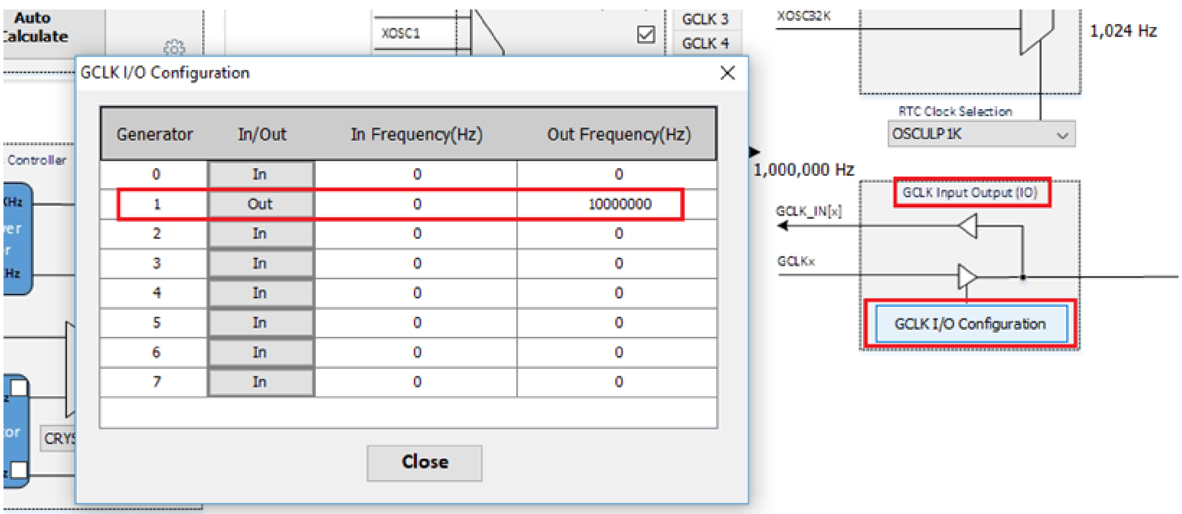
2. Enable the GCLK generator 1 and select the oscillator FDPLL0 as generator input. The divider value of a generator will be used to derive the lower frequency clocks from the GCLK generator. Configure the divider value as 12 to achieve a 10 MHz clock frequency at the GCLK generator 1. The output is shown in the figure below. Refer to the “SAM D5x/E5x Family Data Sheet” for the maximum clock frequency an I/O pin can operate at.

Figure 4-3. Clock Divider Configuration



3. This output can be used to measure the frequency and accuracy of the main clock. Click **GCLK I/O Configuration** to check the configured GCLK I/O [1] clock frequency, see figure below.

Figure 4-4. GCLK I/O Configuration



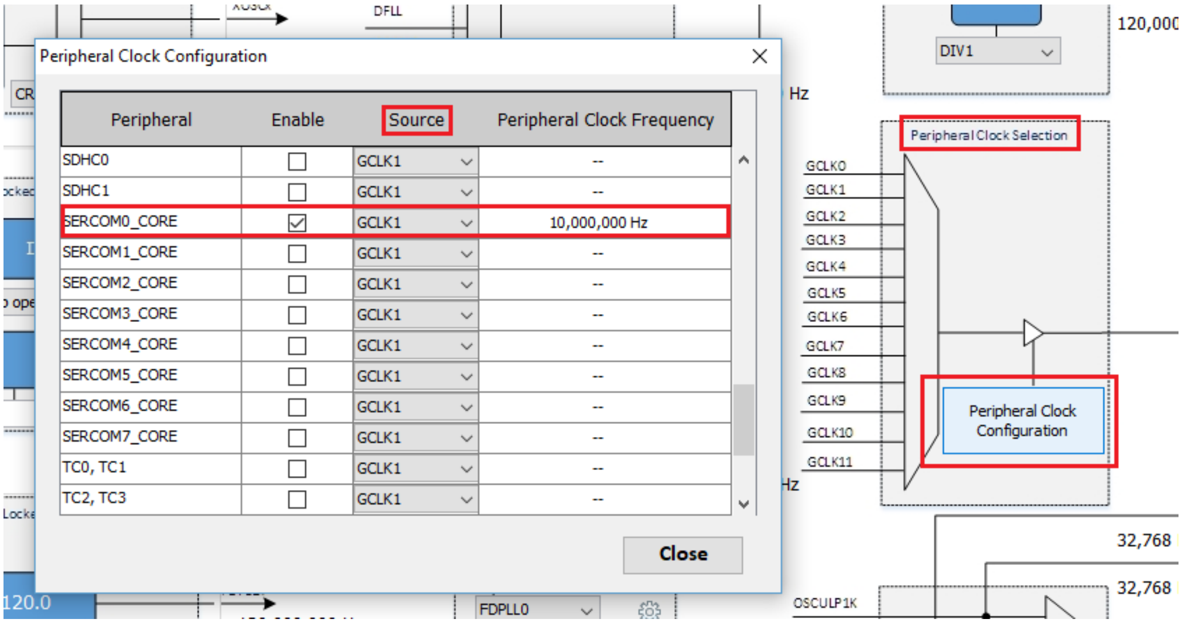
4. Configure the pin, which maps to GCLK1 on the device. To configure clock signal GCLK1 to a pin, use the Pin Configuration option in MHC. To launch Pin Configuration in MPLAB X IDE, select *MHC > Tools > Pin Configuration*.

Use Case Scenario 2

Configure the SERCOM peripheral clock to run the SERCOM (as USART) peripheral.

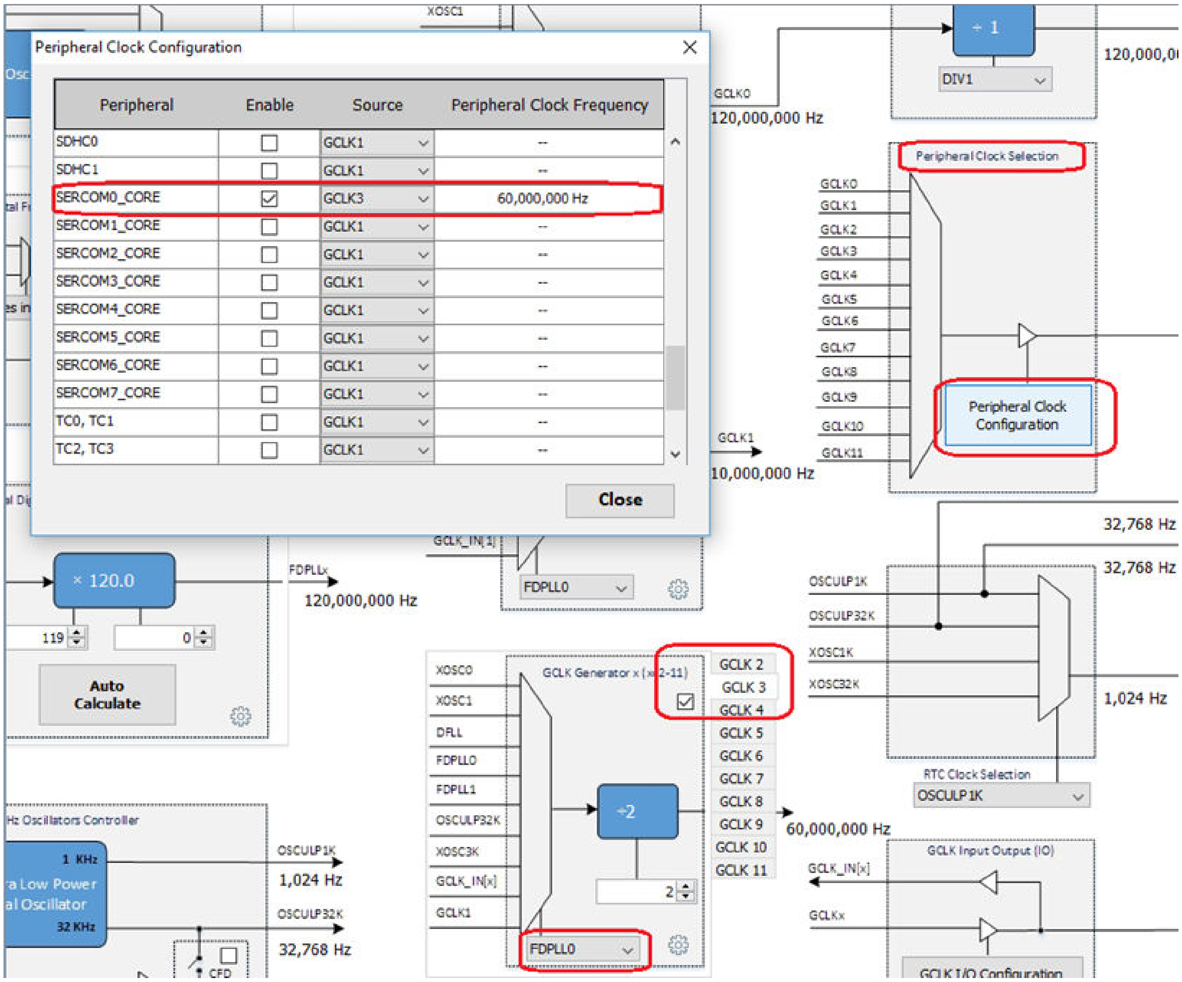
1. Configure the main clock, as shown in “Step 1” of the Use Case Scenario 1.
2. By default, MHC automatically enables the peripheral, APB and AHB clocks, when a peripheral is added to the project graph. Click **Peripheral Clock Configuration** to verify the specific peripheral (SERCOM) clock. The SERCOM0 clock source is selected as GLCK1, which is set to 10 MHz, see figure below.

Figure 4-5. SERCOM Peripheral Clock



3. The Peripheral Clock Configuration window can be used to configure the peripheral to run at a frequency different from the default frequency (10 MHz). A different clock source can be selected. Refer to the figure below to configure the SERCOM0 peripheral clock with 60 MHz frequency by using the GCLK3 as a source.

Figure 4-6. SERCOM Peripheral Clock Configuration



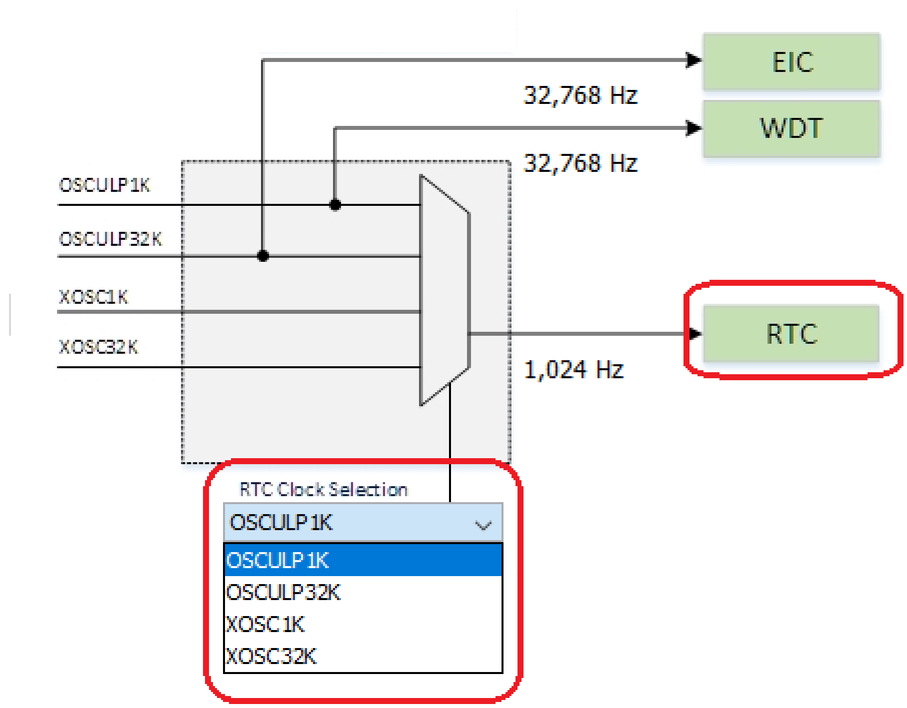
4. Configure the SERCOM (as USART) pins on the device. To configure the SERCOM (as USART) pins, use the Pin Configuration option in the MHC. Launch Pin Configuration by selecting the MHC in MPLAB X IDE V5.20.02, and then select *Tools* > *Pin Configuration*.

Use Case Scenario 3

Follow these steps to configure the RTC peripheral clock in Harmony 3 to run the RTC peripheral at low power.

1. Configure the main clock, as shown in “Step 1” of the Use Case Scenario 1.
2. On SAME54, some of the peripherals, such as the RTC, WDT, and EIC will run directly with the 32 KHz oscillator controller outputs (OSCULP32K, OSCULP1K[3], XOSC32K, XOSC1K).
3. While selecting the OSCULP1K oscillator as the RTC peripheral clock input, the RTC will run at low power. The OSCULP1K oscillator will provide a 1 KHz clock frequency as the oscillator output by running at low power. Refer to the figure below to configure the RTC peripheral clock.

Figure 4-7. RTC Peripheral Clock Configuration



4. The RTC peripheral can be used for different applications. For example, the RTC used as a calendar requires an accurate clock source. When the RTC is used as a calendar, it uses an external accurate clock source. The external clock sources (XOSC1K or XOSC32K) can be configured in the MHC.

Note:

1. Advanced clock configuration options, such as RUN in STANDBY, ONDEMAND clock, DFLL COARSE, FINE,and so on can be configured in the clock tree view. Refer to the MHC *Project graph* > *System* > *Clock*.
2. In the use case scenarios above, the MHC UI screen shots are captured using MPLAB Harmony 3 Configurator, version 2.0.5.2 and repositories Chip Support Package (CSP) version 3.4.0.
3. OSCULP1K is an Oscillator name used in MPLAB Harmony 3 configurator for 1.024 kHz output from 32 kHz internal Oscillator.

5. Resources

For additional information on clock systems and low-power features, refer to the Tech Brief " What is SleepWalking? How it Helps to Reduce Power Consumption" *(DS90003183)*, which is available for download from the Microchip web site: http://ww1.microchip.com/downloads/en/DeviceDoc/90003183A.pdf.

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