DAC INL and DNL Measurement Reference Design

Publish Date: Oct 12, 2011

Overview

This example performs Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) tests on a digital to analog converter (DAC) using the National Instruments PXI platform.

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Overview

INL and DNL measurements are performed on Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) to verify their performance characteristics. Together with gain and offset errors, INL and DNL measurements define the device's static error specifications.

For DACs, a typical approach for making INL measurements is to supply a digital ramp to the DAC inputs and to then compare the DAC's acquired response to an ideal response.

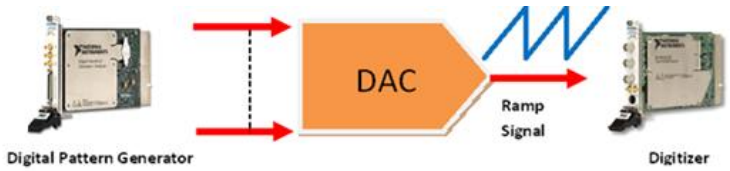


Fig 1: Conceptual Hardware Setup for Testing INL/DNL

There are two commonly accepted methods for choosing the ideal response for INL measurement analysis. The best fit method minimizes the error by choosing a reference line that best matches the DAC response measurements. The end point method uses the first and last measurements as the ends of the reference line.

In either case, the INL measurement is defined as the worst-case deviation between the measurement and the ideal response, and the DNL measurement is defined as the largest incremental error between successive output measurements.

1. Configuring the Hardware

This reference design uses a PXI-6552 or PXI-6542 high-speed DIO board to generate the ramp and a PXI-5922 flexible resolution digitizer to measure analog output voltage. Although a digitizer is used here to accelerate the measurements, a DMM could also be used to measure the DAC response.

Other system components include the DAC clock source (in this case supplied by the HSDIO board) and a low noise power supply provided with a PXI-4130 source measurement unit to power the DAC.

Hardware Connections

Figure 2 below shows how to connect the instruments to the DAC.

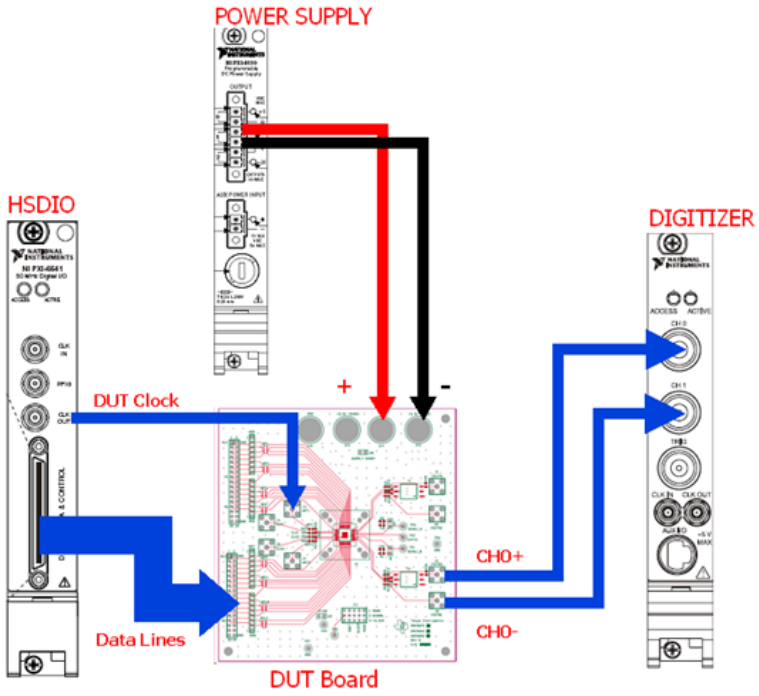


Fig 2: Hardware Diagram illustrating connections between NI hardware and DAC DUT Board

To summarize the connections between the instruments and the DUT:

• Power the DAC chip using SMU Channel 1

• Connect the HSDIO data output lines to the DUT digital inputs

• Connect the HSDIO CLK OUT to the DUT clock input

• Wire the DAC analog output to the digitizer inputs using a differential connection

2. Configuring the Software

You can configure the reference design example code using the front panel Setup tab:

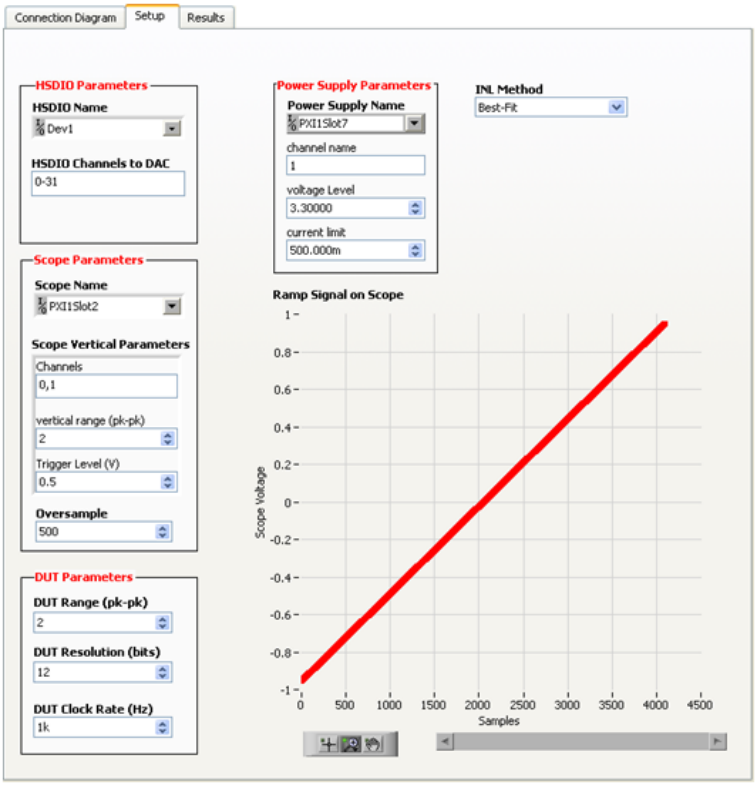


Fig 3: Front Panel of the INL/DNL Test Sample Code

Configure each of the measurement parameters as follows:

Power Supply Parameters

Choose the appropriate voltage for power rails of the chip and set the current limit to protect the chip and the test system.

DUT Parameters

Set the clock rate at around 1 kHz. Set the resolution and output voltage based on the specifications found in the DAC datasheet.

HSDIO Parameters

Configure the list of HSDIO outputs that are connected to the DAC. The DAC clock rate will be set internally to the DUT clock rate and exported to the HSDIO Clock Out pin.

Scope Parameters

Configure the digitizer as described below

a) Choose a pair of channels to perform a differential measurement on the DAC output

b) Choose a vertical range that is larger than the DAC's peak-to-peak output range. Choose the next larger measurement range to maximize the digitizer's dynamic range.

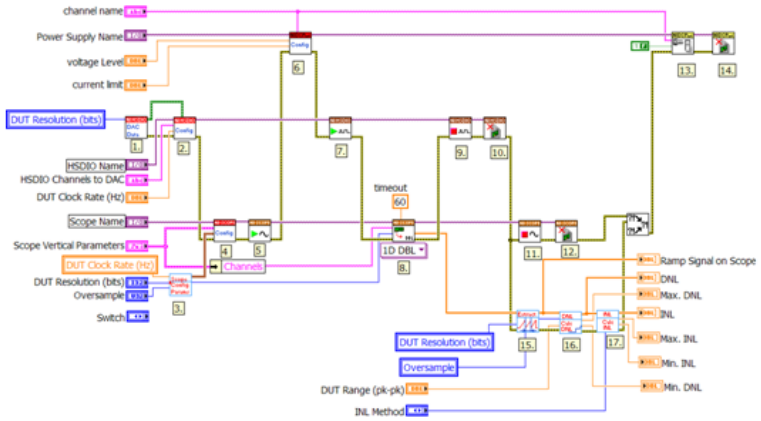
c) Configure the oversample ratio. The oversample Ratio is the number of samples acquired by the digitizer for each DAC output value. Oversampling the DAC output allows you to use averaging to improve the precision of the INL/DNL measurements.

INL Method

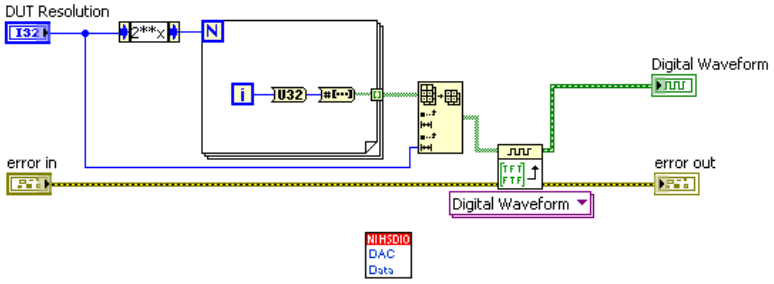
Choose the Best-Fit or End-Point analysis method for the INL measurement.

Software Overview

The reference software design uses NI LabVIEW and the NI-Scope and NI-HSDIO drivers. The following diagram shows the code behind the front panel. As you can see, it is organized using a "railroad track" layout to make it more readable. The first track controls the power supply, the second track controls the HSDIO, the third track controls the digitizer, and the last track performs the analysis.

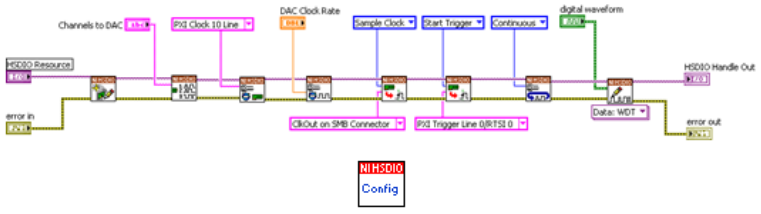


Step 1: The "Generate DAC Digital Data.vi" creates the digital ramp waveform data. The diagram is shown below.

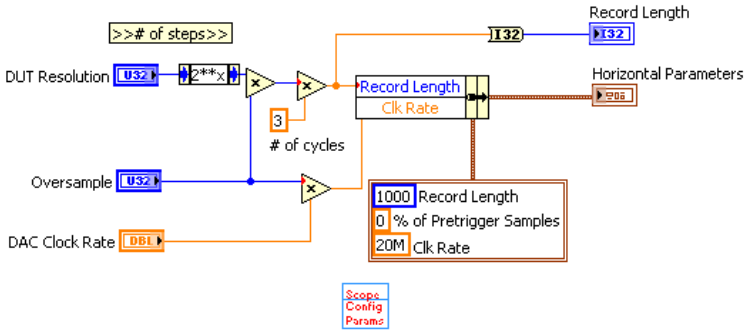


Generate DAC Digital Data.vi

Step 2: The "HSDIO Configure.vi" initializes the HSDIO board using the resource name and channels you configured on the front panel. It then sets the clock rate and sets the reference clock source to PXI clock 10 to synchronize the digitizer and the HSDIO. It also exports the Sample Clock on the front panel SMB Connector for connection to the DAC. Finally, it downloads the ramp signal to the HSDIO onboard memory.

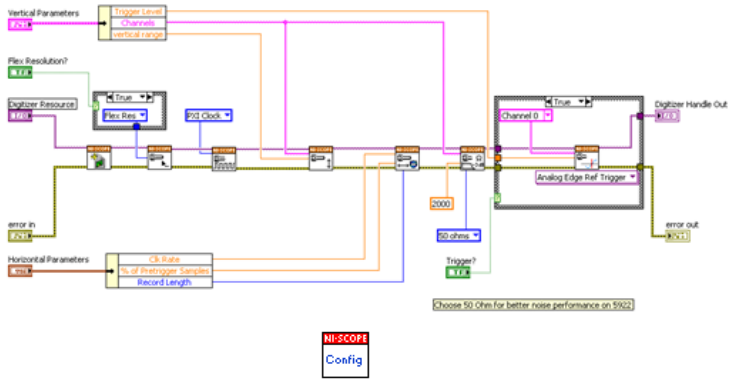


Step 3: The “Configure Horizontal Params.vi” generates digitizer configuration parameters for acquiring 3 cycles of the ramp signal response. Acquiring multiple cycles of DAC output response will allow the measurement analysis algorithm to skip the first measurement, which can contain noise and ringing associated with startup conditions. The digitizer clock rate is the oversample ratio multiplied by the DAC clock rate. The record length is the number of DAC steps multiplied by the digitizer oversample ratio multiplied by the number of DAC response curve measurement cycles (in this case 3).



Configure Horizontal Params.vi

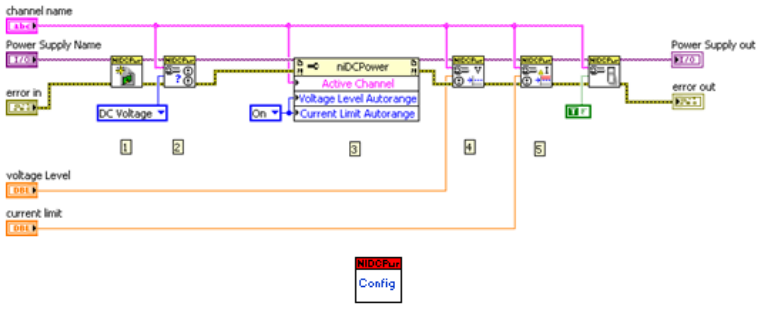
Step 4: The “Scope Configure.vi” initializes the digitizer using the resource name and vertical parameters you configured on the front panel. It sets the resolution of PXI-5922 to “flex-resolution” mode and selects the PXI clock 10 as the reference Clock to synchronize the digitizer and the HSDIO, which also synchronizes the DAC output measurements to the ramp signal updates. It then configures the vertical parameters such as input range, offset and coupling using the values you specified on the front panel. It also sets the horizontal parameters using the values generated by Configure Horizontal Params.vi. Finally, it configures the digitizer input impedance to 50 Ohms and sets the trigger type to Analog Edge. You may want to select the high-impedance input configuration if that is appropriate for your DAC device.



Scope Configure.vi

Step 5: The “niScope Initiate Acquisition.vi” arms the digitizer to acquire the DAC output response on the next trigger.

Step 6: The “Power Supply Configure.vi**”** initializes the SMU using the power supply and channel names you configured on the front panel. It also sets the output mode to “DC Voltage” and enables voltage and current limit auto-ranging. It then configures the output voltage level and sets the current limit to protect the DUT and the test fixture. When the SMU configuration is complete it enables the power supply output.

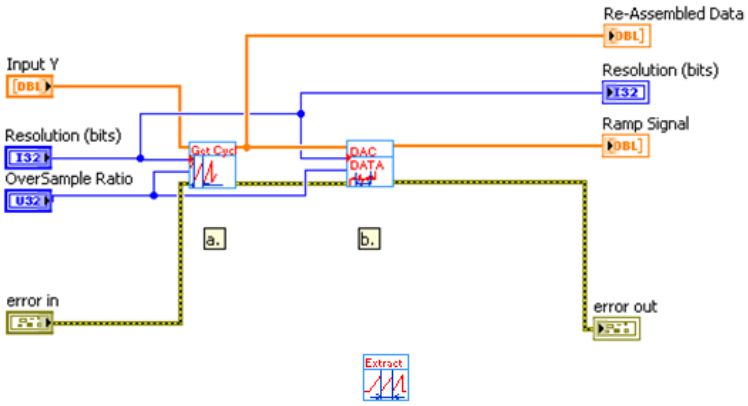


Power Supply Configure.vi

Steps 7 and 8: Start the digitizer acquisition and then HSDIO generation

Steps 9 – 13: Stop and close the HSDIO, digitizer, and power supply sessions

Step 14: Extract one measurement cycle



Extract Single Cycle.vi

a) Extract a single cycle of ramp signal for analysis

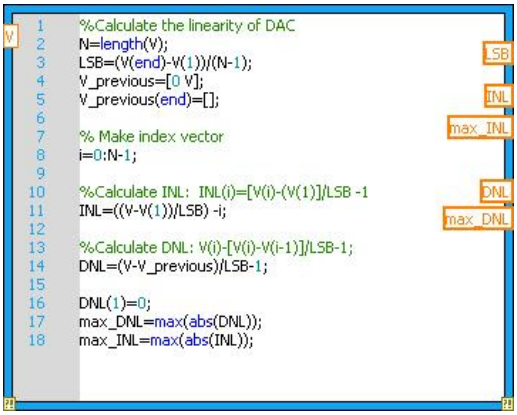
The acquisition of data on the digitizer starts with a digital trigger from the digital pattern generator. Because of this, there is a dead-time where noise is collected before the actual ramp signal is acquired by digitizer. In order to exclude this noise from proper INL/DNL analysis, three cycles of ramp signal are acquired. By locating the start of each ramp cycle (using derivative analysis on the DAC output signal), the middle of the three ramp cycles is extracted for further processing of data.

b) Average the measurements for each DAC code

The digitizer was configured to oversample the DAC output voltage, so the measured values for each DAC code can be averaged to get a single measurement that is more accurate than .

Step 15: Calculate DNL and INL

Mathscript node is used to calculate INL and DNL. The picture below shows computation of INL and DNL



Download the Reference Design Code

INL/DNL Measurement Reference Design