

# DC/DC Power Supply Module 3

Surge-Stopper

Application Report

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# Contents

Abstract.....	3
What is a Surge-Stopper?.....	4
Module Characteristics .....	5
Input Features.....	5
Overvoltage Protection.....	5
Filters.....	8
UV Shutdown.....	9
Fault Indication.....	10
Overvoltage Limit .....	11
Overcurrent Limit.....	11
Fault Timer.....	12
Mosfet Selection.....	12
Thermal Considerations.....	12
Additional Characteristics.....	15
Conclusions.....	16
References.....	17
Annexes.....	19
Finish Assembly Photos.....	19
Revision History.....	19

## Abstract

On May 2022 I made the first version (REV:A) of the module and after some testing and debugging I decided to make a second version (REV:B) that I finish in Dec 2023. This version only differs from the previous on the value and quantity of bulk capacitors.

As you may know, it only requires a little amount of voltage increase at the input of an unprotected sensitive electronic circuit to damage it. The best way to protect it is to use a device capable of withstand overvoltage events under a certain threshold while providing a safe voltage level at the output.

Along this document you will find all the information and considerations needed to build a reliable protection circuit. Some calcs are included also, to bring confidence that the circuit will behave as expected under certain conditions.

## What is a Surge-Stopper?

A surge stopper is a device capable of withstand voltage transients at its input while maintaining a safe voltage on the output, so all components connected to it are protected.

This kind of devices are used across multiple environments including industrial, automotive and military. The point is keeping safe important electronic components from voltage variations, so when the transient disappears, the circuit continue with its normal operation.

In most of the cases they are placed at the input of a circuit, they are rated to work up to a certain level of voltage and the output can be programmed or predefined.

# Module Characteristics

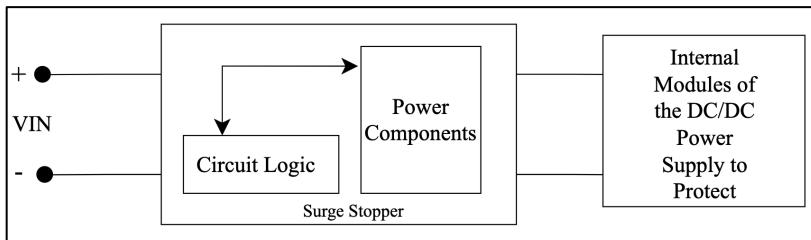


Figure 1 Module Function

VIN has a rated voltage of 12V and cannot exceed 40V. Above 13V the module is configured to shutdown its output until input voltage return to the specified value. The maximum current the module is able to work is 10A. Figure 1 shows a diagram of his function.

To protect the input from reverse polarity I added two 4-pin connectors (J1-J4) [1].

## Input Features

### Overvoltage Protection

There are two unidirectional TVS diodes connected in parallel (D1-D9) [2] to suppress any voltage spike that may occur. I choose unidirectional type because voltage in the circuit is always positive. The design contemplates the exposure to random non-repetitive exponential overvoltage with an amplitude of 100V ( $V_p$ ) and a duration of 8ms ( $t_d$ ) at 10% of peak voltage (standard wave – see Figure 2).

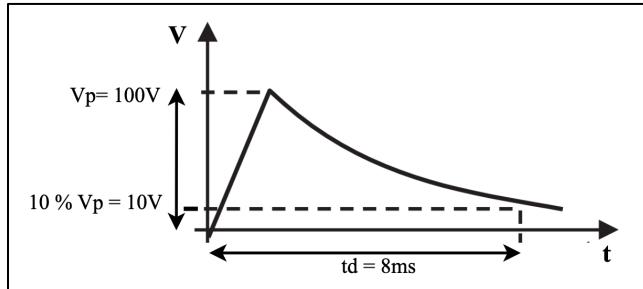


Figure 2 Surge

Let's see all the math involved to show the diodes are able to protect the rest of the circuit from non-repetitive exponential overvoltages.

D1-D9 characteristics are:

- .  $V_R = 24V$
- .  $V_{BR \min} = 26.7V$
- .  $V_{BR \max} = 29.5V$
- .  $V_C \max = 38.9V$  for  $I_{PP} = 16A$  at 10/1000 us exponential waveform
- .  $I_{PPM} = 16A$
- . Power capability: 600W at 10/1000  $\mu s$  exponential waveform

The equivalent internal impedance ( $Z$ ) of the surge source is  $5.5\Omega$  and the maximum working temperature is  $125^\circ\text{C}$ .  $\text{VIN}$  cannot exceed  $40\text{V}$ .

In this scenario, as diodes are connected in parallel and peak current of the surge (calculated in the next paragraph) will not exceed  $I_{PPM}$  in any of the diodes, voltage will be the same across them, same as the current through it also. All calcs will refer for D1.

TVS peak pulse power can be calculated using this formula:

$$P_{PP} = V_C \times I_P$$

$$I_P = V_P - V_C / Z = 100\text{V} - 38.9\text{V} / 5.5\Omega = 11.11\text{A}$$

$$P_{PP} = 38.9\text{V} \times 11.11\text{A} = 432.18\text{W}$$

Now, we need to extrapolate this value to  $125^\circ\text{C}$  because datasheet specifies it at  $25^\circ\text{C}$ .

At  $125^\circ\text{C}$  power capability is around 79%, approximately  $475\text{W}$  according to diode datasheet graphic (see Figure 3) so ratio is  $475\text{W} / 600\text{W} = 0.79$

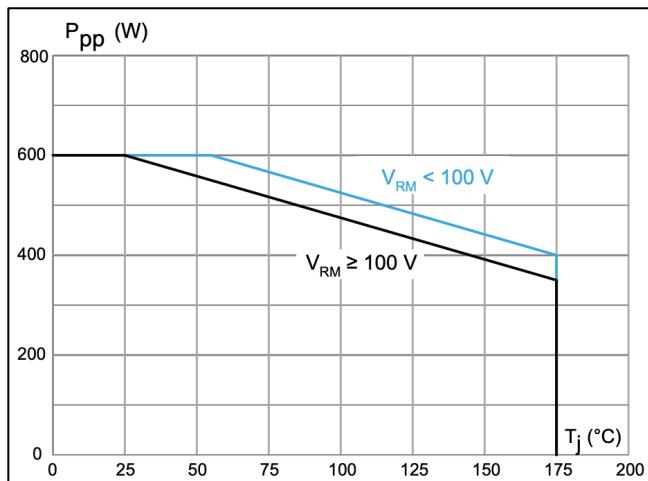


Figure 3 Peak Pulse Power Derating Curve

To estimate  $t_p$  value, is necessary to define pulse duration. This type of pulse match most of the standards used for the protection devices. Duration time is defined at 50% of exponential peak current through TVS diode when surge is applied (See Figure 4 extracted from diode datasheet).

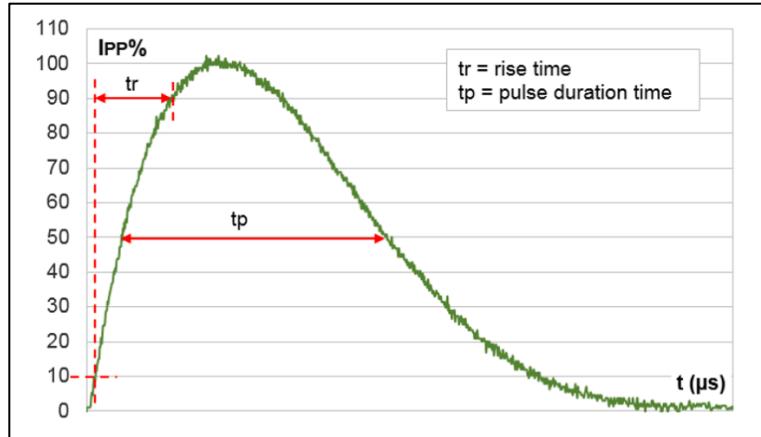


Figure 4 Pulse Definition for Electrical Characteristics

Based on  $t_d$  definition on Figure 2 and for terms of simplification, we will consider only exponential decreasing voltage using this equation:  $v(t) = V_p \times e^{-t/\tau}$

Now we can calculate the constant time Tau ( $\tau$ ) using these equations:

$$v(t_d) = 10\% \times V_p = V_p \times e^{-t_d/\tau}$$

$$\tau = -t_d / \ln 0.1$$

$$\tau = -8\text{ms} / \ln 0.1 = 3.47\text{ms}$$

When surge is applied to TVS diode, the current flow through it only when  $v(t)$  is higher than his voltage breakdown  $V_{BR}$ . Current formula is given by this equation:

$$i(t) = (v(t) - V_{BR}) / Z = (V_p \times e^{-t/\tau} - V_{BR}) / Z$$

Next,  $t_p$  value can be obtained using these equations:

$$i(t_p) = (V_p \times e^{-t_p/\tau} - V_{BR}) / Z$$

$$\text{For } t_p \text{ value, } i(t_p) = I_p / 2 \text{ so, } i(t_p) = I_p / 2 = (V_p \times e^{-t_p/\tau} - V_{BR}) / Z$$

$$t_p = -\tau \times \ln(((Z \times (I_p / 2)) + V_{BR}) / V_p) = -3.47\text{ms} \times \ln(((5.5\Omega \times (11.11\text{A} / 2)) + 29.5\text{V}) / 100\text{V}) = -3.47\text{ms} \times \ln(0.6) = 1.77\text{ms}$$

Last step is calculate the clamping voltage at 1.77ms using this formula:

$$V_{CL} = V_{BR} + R_D \times I_p$$

$R_D$  can be estimated using the table from Figure 5 extracted from diode datasheet.

As SMA6F24A is not plotted I use SMA6F33A. Between 1ms and 1.8ms  $R_D$  ratio is  $\approx 1.38$  (at 1ms  $R_D = 0.8\Omega$  and at 1.8ms =  $1.1\Omega$ ).

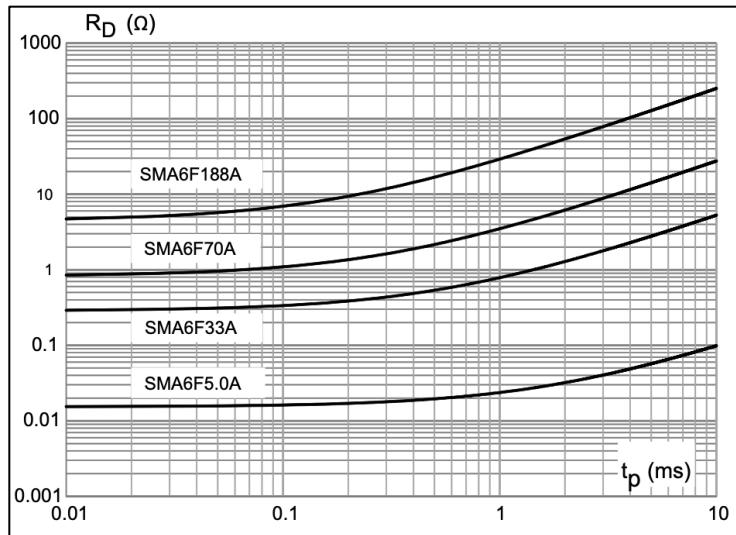


Figure 5 Dynamic Resistance vs Pulse Duration

Maximum  $R_D$  of SMA6F24A at 1ms is  $0.588\Omega$ , so at 1.77ms will be  $0.811\Omega$ .

$$V_{CL} = V_{BR} + R_D \text{ (at 1.77ms)} \times I_P = 29.5V + 0.811\Omega \times 11.11A = 29.5 + 9.01 = 38.51V$$

Finally, is necessary to adjust this value at maximum working temperature ( $125^\circ C$ ) using this equation:  $V_C(T_j) = V_C(25^\circ C) \times (1 + \alpha T \times (T_j - 25^\circ C))$  with  $\alpha T$  = temperature coefficient. For this diode  $\alpha T = 0.0001$  according to datasheet.

$$V_C(125^\circ C) = 38.51V \times (1 + (9.6 / 10000) \times (125^\circ C - 25^\circ C)) = 38.51V \times 1.096 = 42.2V$$

Using this equation, we can get peak pulse power of the diode at 1.77ms:

$$P_{PP} = V_C \times I_P = 38.51V \times 5.555A = 213.92W$$

This value is obtained at  $25^\circ C$ , we have to consider maximum working temperature ( $125^\circ C$ ), so applying the derating for the temperature  $P_{PP} = 213.92W \times 0.79 = 169W$ .

After getting these results we can see that TVS diodes SMA6F24A are appropriate for this scenario in terms of power capability and, during surges the clamping voltage will be below 40V (always maintaining an ambient temperature below  $125^\circ C$  as voltage not exceed the maximum allowed value).

## Filters

During start-up, noise from different sources may be present. In order to prevent a false shutdown from the controller, I use a snubber circuit (R2-C1). By using this passive circuit, high frequencies are shunted to GND.

## UV Shutdown

IC1 is a surge stopper [3] that among its functions has the capability of entering in a low current mode if complementary SHDN pin is pulled low. The input voltage threshold is similar to a TTL input.

Using a 9.1V zener diode (D3) [4] connected to VIN and a  $47\text{K}\Omega$  resistor (R5) [5] in series with D3, when  $\text{VIN} = 10.5\text{V}$ , the voltage of the zener-resistor joint is around 1.5V respect to ground, making IC1 stay on low current mode. As long as this value is incremented above 1.7V, (minimum voltage input threshold for SHDN complementary input based on IC1 datasheet) the IC goes into normal operation.

Resistor R5 is used to limit the current on the zener diode. Current on R5 is given by:

$$I_{R5} = V_{R5} / R_5 \text{ and } V_{R5} = \text{VIN} - V_Z \text{ with } V_Z \text{ voltage of the zener diode.}$$

$$I_{R5} = (12\text{V} - 9.1\text{V}) / 47000\Omega = 0.00006\text{A}.$$

$$\text{Power dissipation on R5 is obtained by: } P_{R5} = V_{R5} \times I_{R5} = 2.9\text{V} \times 0.00006\text{A} = 0.00017\text{W}.$$

According to datasheet, maximum power dissipation of D3 is 0.5W and maximum current is given by:  $I_{D3} = P_{D3} / V_{D3} = 0.5\text{W} / 9.1\text{V} = 0.055\text{A}$ .

When  $\text{VIN} = 12\text{V}$ , maximum power on D3 is  $P_{D3} = V_{D3} \times I_{R5} = 9.1\text{V} \times 0.00006\text{A} = 0.00055\text{W}$ .

When  $\text{VIN} = 40\text{V}$ ,  $I_{R5} = 40\text{V} - 9.1\text{V} / 47000\Omega = 0.00066\text{A}$  so  $P_{D3} = 9.1\text{V} \times 0.00066\text{A} = 0.0060\text{W}$ .

Power on R5 will be:  $P_{R5} = V_{R5} \times I_{R5} = 40\text{V} - 9.1\text{V} \times 0.00066\text{A} = 0.020\text{W}$ .

With this values, even when VIN reaches its maximum threshold, maximum ratings will not be exceeded on D3 and R5 at  $25^\circ\text{C}$ .

At  $125^\circ\text{C}$ , according to temperature table of D3 datasheet showed on Figure 6, if VIN gets to  $40\text{V}$ ,  $P_{D3}$  will be under 0.1W.

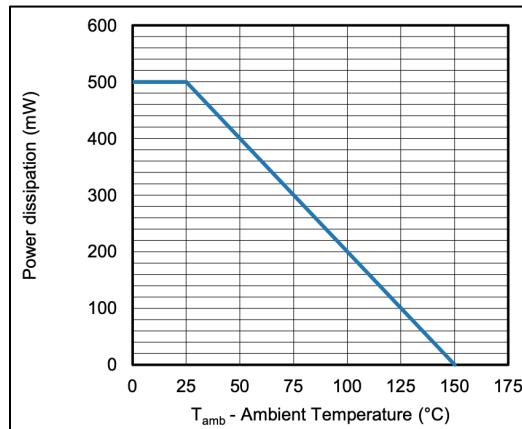


Figure 6 Admissible Power Dissipation vs. Ambient Temperature

On R3, according to temperature table extracted from resistor datasheet and showed on Figure 7,

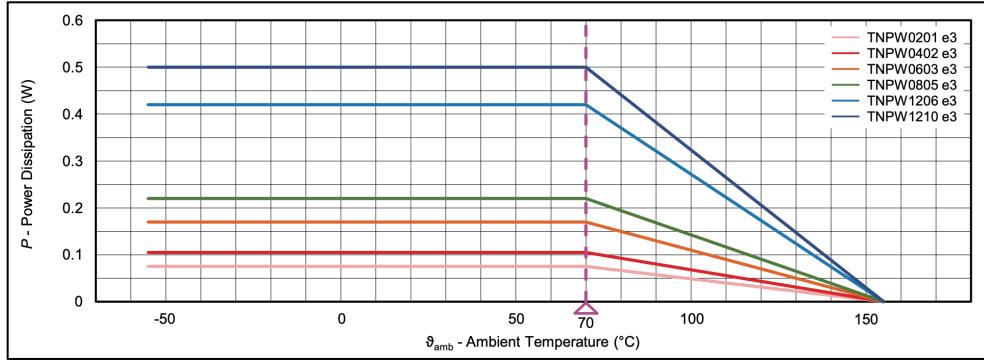


Figure 7 Derating General Operation

it's clearly that at 125°C maximum power dissipation is a little below of 0.1W (showed on green line). Same as D3, even when  $V_{IN} = 40V$ , maximum power rate on R5 is never reached.

## Fault Indication

IC1 has a complementary FLT pin to show when an overcurrent or overvoltage happens. A NPN transistor (Q2) [6] is used with a  $1K\Omega$  resistor (R7) to provide a constant current to D4, since FLT pin can sink up to 3mA enough to drive a led diode. Q2 base pin is feeded from a stable 5.6V from the joint of a  $22K\Omega$  resistor (R6) and a 5.6V zener diode (D5) [7].

When  $V_{IN} = 12V$ :

$V_B = V_{D5} = 5.6V$  with  $V_B$  base voltage of Q2.

$V_E = V_B - V_{BE} = 5.6V - 0.6V = 5V$  with  $V_E$  emitter voltage and  $V_{BE}$  base-emitter voltage of Q2.

Current on R7 is  $I_{R7} = V_E - V_{D4} / R_7$  with  $V_{D4}$  forward voltage of D4 (around 1.8V).

$I_{R7} = 5V - 1.8V / 1000\Omega = 0.0032A$ , the same current FLT pin can sink.

When  $V_{IN} = 40V$ :

$I_{R6} = V_{IN} - V_{D5} / R_6 = 40V - 5.6V / 22000\Omega = 0.0016A$ .

$P_{R6} = I_{R6}^2 \times R_6 = 0.0016^2 A \times 22000\Omega = 0.056W$ .

$P_{D5} = I_{R6}^2 \times V_{D5} = 0.0016^2 A \times 5.6V = 0.0000143W = 0.0143mW$ .

According to diode datasheet, maximum power is 300mW. If  $V_{IN}$  reaches 40V,  $P_{D5}$  will be under this value.

On Q2, base and emitter voltage remain with the same values as when  $V_{IN} = 12V$ .

$V_{CE}$  voltage is  $V_{CE} = V_{IN} - (V_B - V_{BE})$  with  $V_{CE}$  voltage of collector-emitter.

$V_{CE} = 40V - (5.6V - 0.6V) = 35V$ .

$V_{CB} = V_{CE} - V_{BE}$  with  $V_{CB}$  collector-base voltage.

$V_{CB} = 35V - 0.6V = 34.4V$ .

According to datasheet, maximum  $V_{CE}$  voltage cannot exceed 160V and  $V_{CB}$  cannot be above 180V, so even when  $VIN = 40V$ , transistor is protected in terms of maximum voltage values.

## Overvoltage Limit

Since IC1 includes fault latchoff, I configure an overvoltage limit ( $V_{REG}$ ) of 13.25V. If  $VIN$  reaches this value, output is shutdown.

To simplify resistor value calcs, I will use  $R_A$  and  $R_B$  to represent R12, R13 and R14 resistors and at the end, I will substitute the values.

First, I calculate  $R_A$  and  $R_B$  values so FB pin of IC1 stay at 1.25V:

$$V_{REG} = 1.25V \times (R_A + R_B) / R_B = 13.25V$$

Set a  $250\mu A$  of current between  $R_A$  and  $R_B$  if the event happens.

$$With this condition, R_B = 1.25V / 250\mu A = 5K\Omega$$

Replacing this value on the first equation we have:

$$V_{REG} = 1.25V \times (R_A + 5K\Omega) / 5K\Omega = 13.25V$$

$$1.25V \times (R_A + 5K\Omega) = 13.25V \times 5K\Omega$$

$$R_A + 5K\Omega = 13.25V \times 5K\Omega / 1.25V$$

$$R_A = (13.25V \times 5K\Omega / 1.25V) - 5K\Omega$$

$$R_A = 48K\Omega$$

Replacing  $R_A$  and  $R_B$  values we have:

$$R_A = R12 + R13 \text{ and } R_B = R14.$$

Taking into account resistor availability at that moment with 0.1% tolerance I get:

$$R12 = 43K\Omega$$

$$R13 = 5K\Omega$$

$$R14 = 5K\Omega$$

## Overcurrent Limit

IC1 senses an overcurrent condition by monitoring the voltage across a sense resistor placed between VCC and SNS pins. A current limit circuit controls the GATE pin to limit the sense voltage to 0.050V.

The value of the current sense resistor is obtained using this formula:  $R_{SNS} = 0.050V / I_{LIM}$  where  $I_{LIM}$  is the maximum current the module can handle.

I decided to set a current limit of 10A, so  $R_{SNS} = 0.050V / 10A = 0.005\Omega$ . I use three resistors in parallel (R3, R15, R16) [8] [9] to achieve the desired value.

These 4 terminal current sense resistors are used to ensure higher current measurement accuracy. On this application note [10], the use of this type of resistors is explained with more detail.

## Fault Timer

When an overcurrent or overvoltage event happens, a current source charges up TMR pin of IC1. Current level depends on the voltage drop across drain and source pins of the mosfet handled by IC1.

TMR pin allows to connect a capacitor (C2) to set the delay time period before the mosfet is turned off. Also, this capacitor sets the cool down period before the mosfet is turned on again after the fault condition disappear.

Capacitor value ( $C_{TMR}$ ) is obtained from this formula:  $t_{WARNING} = C_{TMR} \times 100mV / 5\mu A$  where  $t_{WARNING}$  is the interval between FLT complementary pin is on low state and the mosfet turn off. For a 1ms warning time,  $C_{TMR} = 1ms \times 5\mu A / 100mV = 50nF$ .

## Mosfet Selection

IC1 drives a N-channel mosfet to manage the load current. The most important features when selecting it are:

- on-resistance  $R_{DS(ON)}$
- maximum drain-source voltage  $V_{(BR)DSS}$
- threshold voltage
- SOA

I decided to use SQM100N10-10 (Q1) [11] Automotive N-Channel Mosfet. According to datasheet  $R_{DS(ON)} = 0.0105\Omega$ ,  $V_{(BR)DSS} = 100V$  and  $V_{GS} \pm 20V$ .

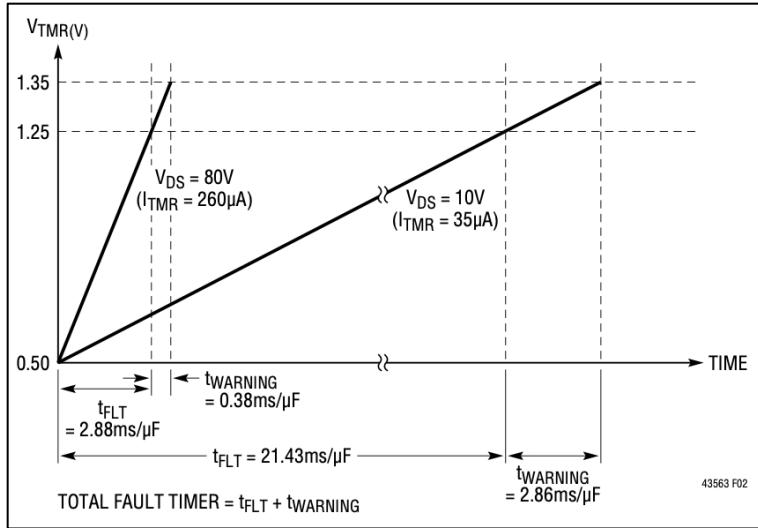
When an overvoltage or overcurrent happens, GATE pin of IC1 regulates either the output voltage or the current through the mosfet. SOA curves must be considered together with the selected capacitor attached to TMR pin to assure the mosfet won't get damaged during this fault conditions.

## Thermal Considerations

Q1 must be chosen making sure is able to withstand an output short condition when  $VIN = 12V$ . During an overcurrent event, timer current of IC1 start at  $4\mu A$  when  $V_{DS}$  is  $0.5V$  or less but increases up to  $260\mu A$  when  $V_{DS}$  reaches  $80V$  with  $V_{DS}$  the drain-source voltage of Q1.

To calculate total overcurrent fault time (toc), is necessary to get first the current at TMR pin when  $VIN = 12V$  using a simple rule of three:  $I_{TMR} = 12V \times 260\mu A / 80V = 39\mu A$ .

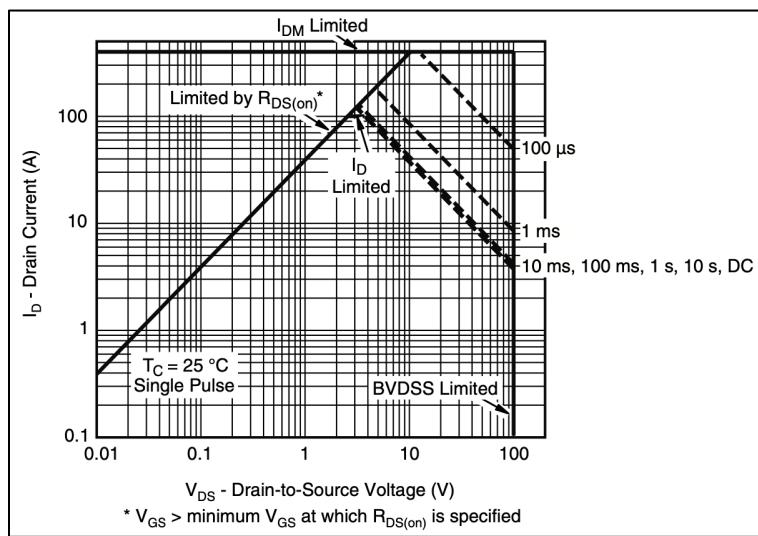
$toc = C_{TMR} \times 0.85V / I_{TMR} = 50nF \times 0.85V / 39\mu A = 1.089ms$  with  $0.85V$  the difference between the maximum and minimum voltage of TMR pin ( $V_{TMR}$ ) according to Figure 8 extracted from IC1 datasheet.



Power dissipation on Q1 is obtained by:

$P_D = V_{IN} \times V_{SNS} / R_{SNS} = 12V \times 0.050V / 0.005\Omega = 120W$  with  $V_{SNS}$  the voltage across VCC and SNS pins of IC1 during an overcurrent event.

Having  $t_{oc}$  and  $P_D$ , looking at Safe Operating Area (SOA) of Q1 in Figure 9 extracted from mosfet datasheet, if we trace a vertical line from  $V_{DS} = 12V$  and intersect with 1ms dotted line, maximum current it's about 80A.



This allows to confirm that if an overcurrent event happens, the mosfet will tolerate it without damage.

Now let's see if mosfet junction temperature stays below its maximum value when working up to 10A. According to datasheet:

- $I_D = 100A$  (continuous drain current at  $25^\circ\text{C}$ )
- $P_D = 375\text{W}$  (power dissipation at  $25^\circ\text{C}$ )
- $T_J = 175^\circ\text{C}$  (maximum junction temperature)

Effective temperature differential [12] is given by  $\Delta T = P \times \theta$  with:

- .  $P$  = total device power dissipation (W)
- .  $\theta$  = total thermal resistance ( $^\circ\text{C/W}$ )

Junction temperature is given by:  $T_J = T_A + (P \times \theta_{JA})$  with:

- .  $T_A$  = ambient temperature
- .  $\theta_{JA}$  junction-ambient thermal resistance.

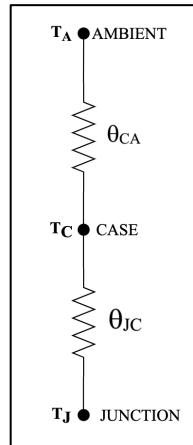


Figure 10 Thermal Relationships

$\theta_{JA} = \theta_{JC} + \theta_{CA}$  as is shown on Figure 10 with:

- .  $\theta_{JC}$  = junction-case thermal resistance
- .  $\theta_{CA}$  = case-ambient thermal resistance

Pcb where mosfet is soldered act as a heatsink. The heat is dissipated through it to the ambient air by convection/radiation so  $\theta_{CA} = \theta_{CS} + \theta_{SA}$  with:

- .  $\theta_{CS}$  = case-sink thermal resistance
- .  $\theta_{SA}$  = sink-ambient thermal resistance

In resume,  $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$

We can assume  $\theta_{CS}$  from the junction of Q1 to the surface of the pcb is small enough compared to  $\theta_{SA}$  as elements are soldered. Replacing  $\theta_{JA}$  gives us  $T_J = T_A + (P \times (\theta_{JC} + \theta_{SA}))$ .

A widely published figure for the heat transfer coefficient [13] from pcb surface ( $h$ ) to air is  $10\text{W/m}^2\text{K}$ . In order to take  $h$  into thermal resistance from board surface to the ambient air ( $\theta_{SA}$ ), the inverse is taken and then converted from square meters to square inches. Finally, the result is divided by the surface area.

$$\theta_{SA} = ((1/h) / \text{surface area}) = (0.1 \text{ m}^2\text{K/W} / \text{surface area}) \times (1550 \text{ in}^2 / 1\text{m}^2) = 155 \text{ in}^2\text{K/W} / \text{surface area}$$

If convective heat transfer is present from both sides of the board,  $\theta_{SA}$  is reduced by half.

On mosfet datasheet  $\theta_{JC} = 0.4^\circ\text{C/W}$ . If we want to limit Q1 junction temperature to a 40 degree rise in temperature for 1W of power dissipation:

$$\theta_{SA} = (\theta_{JA} - \theta_{JC}) / P_D = (40^\circ\text{C} - 0.4^\circ\text{C}) / 1\text{W} = 39.6^\circ\text{C/W}$$

The required board area will be:

$$\text{board area} = 155 \text{ in}^2\text{C/W} / 2 \times \theta_{SA} = 155 \text{ in}^2\text{C/W} / 2 \times 39.6^\circ\text{C/W} = 1.96 \text{ in}^2$$

Converting to mm<sup>2</sup>,  
 $\text{board area} = 1.96 \times 645.2 = 1264.51\text{mm}^2$

I make the design on a 4-layer pcb, 1oz copper each one. Surface where mosfet is soldered has 21.59mm x 26.51mm of dimension duplicated along the 4 layers, interconnected through vias.

Inside the enclosure where the module is set, ambient temperature will go up to  $35^\circ\text{C}$  due to a dc fan always turned on.

Mosfet power dissipation at 10A is:  $P = I^2_{DS} \times R_{DS(on)} = 10^2\text{A} \times 0.0105\Omega = 1.05\text{W}$ .

With all thermal's resistance information we have:

$$T_J = 35^\circ\text{C} + (1.05\text{W} \times (0.4^\circ\text{C/W} + 39.6^\circ\text{C/W})) = 35^\circ\text{C} + (1.05\text{W} \times 40^\circ\text{C/W}) = 77^\circ\text{C}$$

If temperature inside the enclosure reach to  $125^\circ\text{C}$ ,

$$T_J = 125^\circ\text{C} + (1.05\text{W} \times (0.4^\circ\text{C/W} + 39.6^\circ\text{C/W})) = 125^\circ\text{C} + (1.05\text{W} \times 40^\circ\text{C/W}) = 167^\circ\text{C}$$

According to this result, we can see that Q1 working at 10A will not exceed its maximum junction temperature.

## Additional Characteristics

According to IC1 datasheet, a total bulk capacitance of at least  $22\mu\text{F}$  is needed close of source pin of Q1. I decided to use aluminum polymer capacitors (C3, C4) [14] of  $47\mu\text{F}$ .

To avoid reverse polarity connections on the output, I use same type 4-pin connectors (J2, J3) as used on the input.

The overvoltage lockout components (D6, R8, R9) are used for protecting Q1 during bench testing by preventing autoretry when VIN exceeds 18V approximately. IC1 model used on this design latches off during faults (not autoretry like LT4356-2). I added this components for testing purposes but can be omitted.

## Conclusions

After testing the second version of the module (REV:B) on different scenarios, I consider it offers a good starting point to protect sensitive electronic circuits.

Design flexibility is offered on input and output parameters to suit the needs of the system where it will be installed.

A good soldering station is required to solder IC1 as distance between pins is only 0.5mm.

## References

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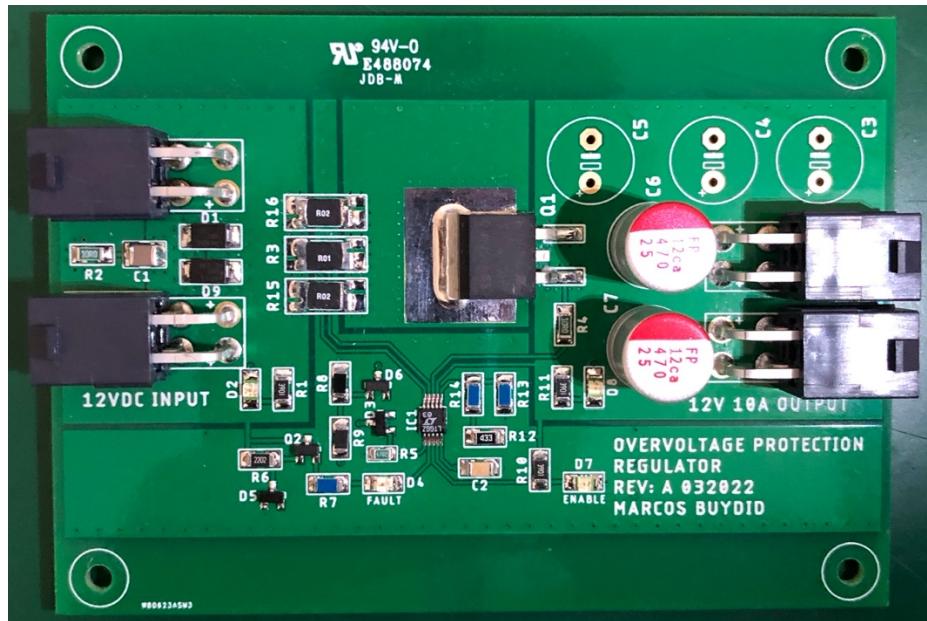
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## Annexes

### Finish Assembly Photos



Module Upper View

As you can notice on the pcb, revision is labeled “A” and not “B”. As I explain at the beginning of this document, difference between revisions only differ in the quantity and value of bulk capacitors.

### Revision History

Date	Version	Changes
Aug-2024	1	First version