A Fully Integrated Class-E CMOS Amplifier with a Class-F Driver Stage

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Abstract: This report presents a fully integrated two-stage 1.9 GHz class-E amplifier, implemented by 0.18 μm CMOS technologies. By using the switching operation mode of a class-E amplifier, the dc power dissipation can be reduced, and this amplifier delivers a 16.3 dBm output power at 1.9 GHz, with a maximum power-added efficiency (PAE) of 70% from a 2-V dc supply voltage. This monolithic amplifier includes the matching and biasing circuit, where no external components are required.

I. INTRODUCTION

With the rapid expansion of wireless personal communications, the high performance and low cost single-chip transceivers are sincerely expected. In the receiver function, the low-noise amplifier, voltage-controlled oscillator, mixer have been reported in the integrated form by CMOS technologies [1]. However, the integration of CMOS power amplifier remains a difficult challenge. The main requirements for a power amplifier used in the CMOS rf transceiver are high efficiency and low supply voltage. An efficient power amplifier is desirable for a wireless system because the dominant power consumption in the transceiver is coming from the power amplifier. For considering the low-cost and low-power issues, the implementation of a high efficiency power amplifier is a challenging target by using the CMOS technologies.

The switching mode amplifier is the preferred selection for its excellent power-added efficiency (PAE), where the voltage and the current waveforms are basically out of the phase, and the dc power consumption can therefore be reduced. The PAE is defined by the output power minus the input power, divided by the supply power. Since the transistor is used as a switch in a class-E amplifier, it is important to have a low-loss operation at high frequencies. In the past, the rf power amplifier is implemented usually by using GaAs MESFET or SOI LDMOS [2-3], which is due to the low-loss microwave switching features in an insulating substrate. However in the CMOS technologies, the bulk silicon substrates present a significant loss in high frequency operation, which may degrade the switching characteristic in the class-E amplifier design. In this work, we particularly used the CMOS deep n-well configuration to provide a good isolation between passive components and transistors. Since the class-E amplifier is performed in a switching mode operation, it is an important issue to shape the input waveform for turning the transistor on and off. To obtain the shortest transition time from one switching state to the other, a square waveform should be applied into the class-E amplifier. This function can be realized by using the class-F amplifier as a driver stage, which can generate appropriate harmonics of the input signals and combining them into a square waveform.

For those published high efficiency amplifiers, implemented by CMOS technologies have used the off-chip external components to reduce the signal loss in the Si substrates [4-6]. In this study, we use the advanced 0.18 μm CMOS technologies to fabricate and characterize a fully integrated, where no external components is required, CMOS class-E amplifier operating at 1.9 GHz.

II. CLASS-E AMPLIFIER DESIGN

Fig. 1 shows the circuit schematics of this 1.9

GHz class-E amplifier with a class-F driver stage. In the class-F driver stage, a 60 μm gate-width transistor M_1 was used as an amplifier with two parallel L-C pairs in series with the drain, one pair tuned to the first harmonic and the second one tuned to the third harmonic of the input frequency. It therefore generates a square-like waveform on the drain terminal of transistor M_1. The L_b, C_b and L_{g1} are the input matching networks. In the class-E stage, the L_1-C_1 filter is designed to pass and reshape the sinusoidal fundamental frequencies to the load. The L_{dc} is used as a rf choke, connecting the transistor M_2 to the supply voltage V_{dd}. The capacitor C_p is connected in parallel with the transistor M_2, providing the charge-discharge function of the switching mode operation.

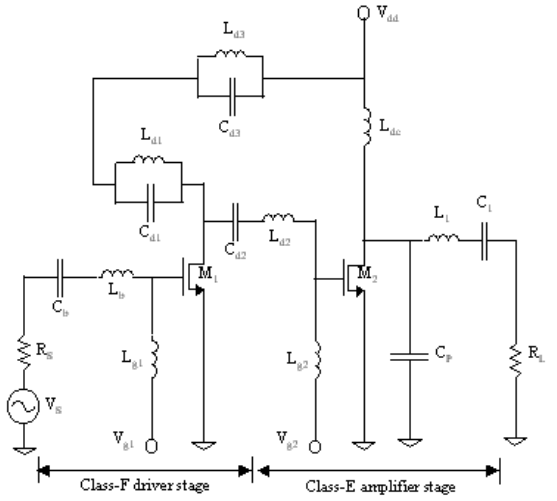

Figure 1: Schematics of the integrated CMOS class-E amplifier with a class-F driving stage.

The circuit performance was simulated by using the Agilent ADS™, where the modified home-made BSIM3v3 rf model for 0.18 μm CMOS was used, and the simulated waveforms are shown in Fig. 2. The V_{d1} represents the approximate square waveform in the drain terminal of the class-F driving stage. During the t_1 time interval, the transistor M_2 working as an opened mode, the dc current flows through the inductor L_{dc} and starts to charge the capacitor C_p. It results in a voltage drop across the transistor M_2 (V_{d2} in Fig. 2), and the I_{d2} through the transistor M_2 consequently approaches to the zero current. During the time interval of t_2, the transistor M_2 working as a closed mode, the capacitor C_p will be discharged through the current of M_2, and the voltage across the M_2, i.e. V_{d2}, is therefore approaching zero. Since the high current waveform mainly overlaps with the zero voltage waveform and vice versa in the other period, the power dissipation in the transistor M_2 is zero in principle. In consequence, the power-added efficiency (PAE) can be improved significantly. As shown in Fig. 2, the drain current I_{d2} through the transistor M_2 consists of both a capacitive current and a resistive current. A large portion of current I_{d2} mainly overlaps with the approximately zero voltage of V_{d2} in the t_2 interval, so the power dissipation can be reduced effectively, resulting in an efficiency improvement.

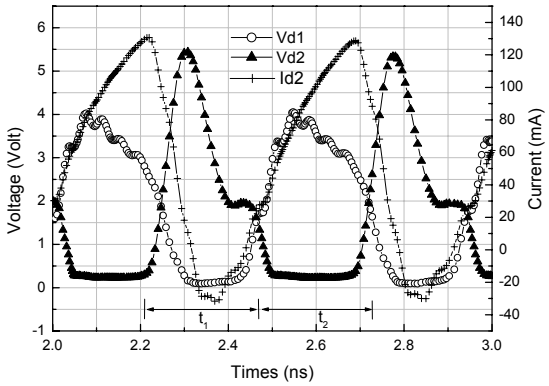

Figure 2: Simulated output waveforms of the switching mode transistor M_2 with an input signal of 1.9 GHz.

However, under the high frequencies operation, the unforgettable transition time of switching causes a certain amount of power loss. In order to minimize the power loss in the above-mentioned mechanism, the class-E amplifier is designed to ensure no overlap of nonzero switch voltage and nonzero switch current, i.e. the zero of $V_{ds}(t)$ and $dV_{ds}(t)/dt$ [7]. In a practical situation, the transistor M_2 has its finite on-resistance, and the transition time from the off-state to the on-state and vice-versa are not negligible. These factors cause the certain amount of power dissipation in the switch resulting in a reduction of the amplifier power efficiency [8]. For the sake of achieving the highest efficiency, we can choose a wider transistor to reduce the resistance, but it also introduces a larger parasitic capacitance to limit the transition speed. Since the on-resistance affects the maximum efficiency, and the parasitic capacitance limits the maximum operating frequency, there is a trade-off in selecting the size of the transistor as far as the efficiency and bandwidth are concerned. In this study, we used the gate-width of 400 μm NMOS transistor in the

class-E amplifier, which is compromised by these two aspects.

III. CHARACTERISTICS OF CMOS CLASS-E AMPLIFIER

In addition to the active transistor devices, the performance of the on-chip spiral inductors on Si substrates is critical in the high efficiency amplifier design. In order to achieve a good isolation between passive components and transistors, we used the deep n-well placed beneath the spiral inductors. The deep n-well provides a built-in p-n junction potential to isolate the cross-talk leakage signals. Comparing with the 5.5 turns squared and circular spiral inductors, the maximum Q-value is up to 9.7 with an inductance of 5.7 nH for a circular-shaped inductor, corresponding to a 12% improvement from the square-shaped one. As to the inductor equivalent circuit model, the circular-shaped inductor exhibits lower parasitics (R_s, C_p, C_{ox}) and a lower substrate loss (R_{sub}, C_{sub}). Since the performance of the circular-shaped spiral inductor is better than that of the square-shaped spiral inductor, the circular-shaped spiral inductors are preferred in our monolithic CMOS amplifier designs.

The photograph of the CMOS class-E power amplifier is shown in Fig. 3, where the matching and biasing circuits are all included, and the total chip area is 1.36×1.49 mm^2. The output power was measured by using the spectrum analyzer. By using the switching mode, this amplifier delivers a 16.3 dBm output power to a 50-Ω load at 1.9 GHz. Fig. 4 shows the measured output power, power gain and PAE as a function of input power. The maximum PAE is 70%, and the maximum linear power gain is 15.9 dB from a 2-V dc supply voltage. As shown in Fig. 5, the measured maximum output powers and PAEs versus the supply dc voltage (V_{dd}) reveal that changing the supply voltage from 1.0 V to 2.3 V, the output power increases from 7.4 dBm to 16.5 dBm. By increasing the dc supply voltage, the dc power consumption also increases, and the highest PAE is achieved at a dc voltage of 2V. Fig. 6 shows the measured output powers and PAEs of this CMOS amplifier versus the operating frequencies. In the range of 90 MHz bandwidth (from 1.86 GHz to 1.95 GHz), the variations of output power and PAE are relatively small, which can be applied in the 1.9 GHz band wireless system applications.

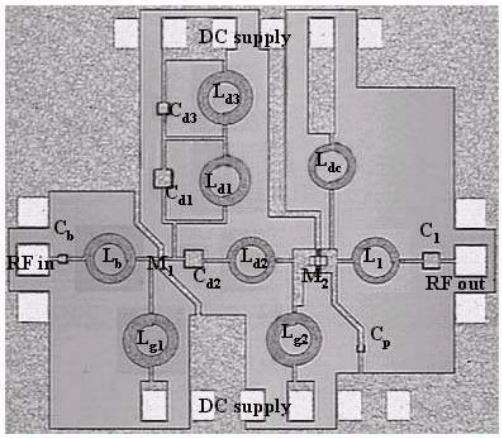

Figure 3: Photograph of the fabricated CMOS class-E amplifier (chip area: 1.36×1.49 mm^2).

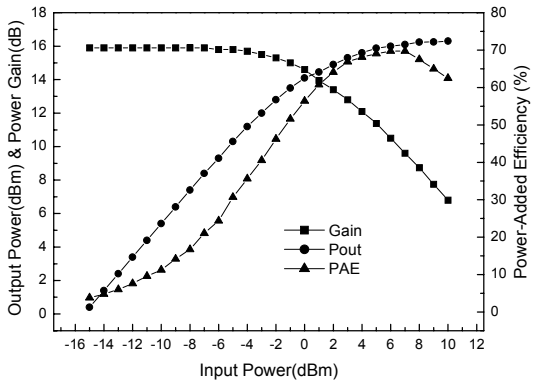

Figure 4: Measured output power, power gain and PAE of the CMOS class-E amplifier as a function of input power with a supply voltage of 2 V.

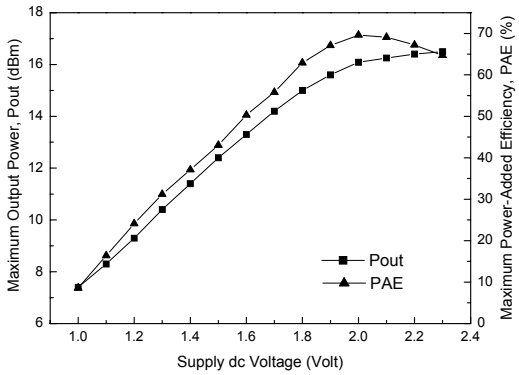

Figure .5: Measured output powers and PAEs of the CMOS class-E amplifier as a function of the supply voltages.

	Frequency (MHz)	Technology (μm)	Supply voltage (V)	Output power (dBm)	PAE (%)	Area (mm^2)	Required external components
Ref. [4]	700	0.35	2.3	30.0	62	2.6	Yes
Ref. [5]	900	0.25	2.5	29.5	41	4.0	Yes
Ref. [6]	1900	0.35	2.0	30.0	48	0.6	Yes
This work	1900	0.18	2.0	16.3	70	2.0	No

TABLE Ⅰ PERFORMANCE COMPARISONS OF THE REPORTED CMOS CLASS-E AMPLIFIERS

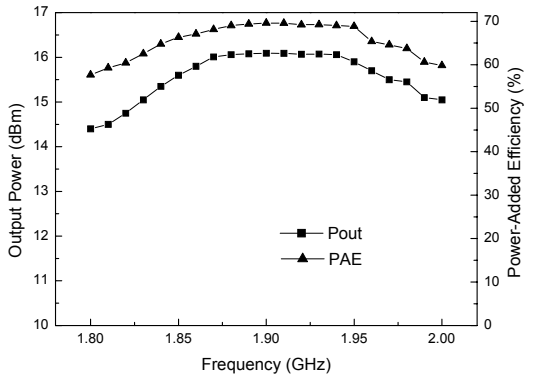

Figure .6: Measured output powers and PAEs of the CMOS class-E amplifier as a function of the operation frequencies.

Comparing to the performance of the other published CMOS class-E amplifiers summarized in Tab. I, our amplifier presents the highest operational frequency and the PAE value, which is responsible for using the advanced 0.18 μm technologies. In addition, no external component is required in our circuit, where all the matching and biasing circuits are fully integrated in a chip.

IV. CONCLUSIONS

In this study, a fully integrated CMOS class-E amplifier operating at 1.9 GHz fabricated by 0.18 μm CMOS technologies has been designed and characterized. The experimental results demonstrate that this amplifier delivers a 16.3 dBm output power, with a 70% maximum PAE from a 2-V dc voltage supply. It therefore provides a potential application of CMOS class-E amplifier for a low-voltage and high-efficiency microwave amplifier circuit.

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