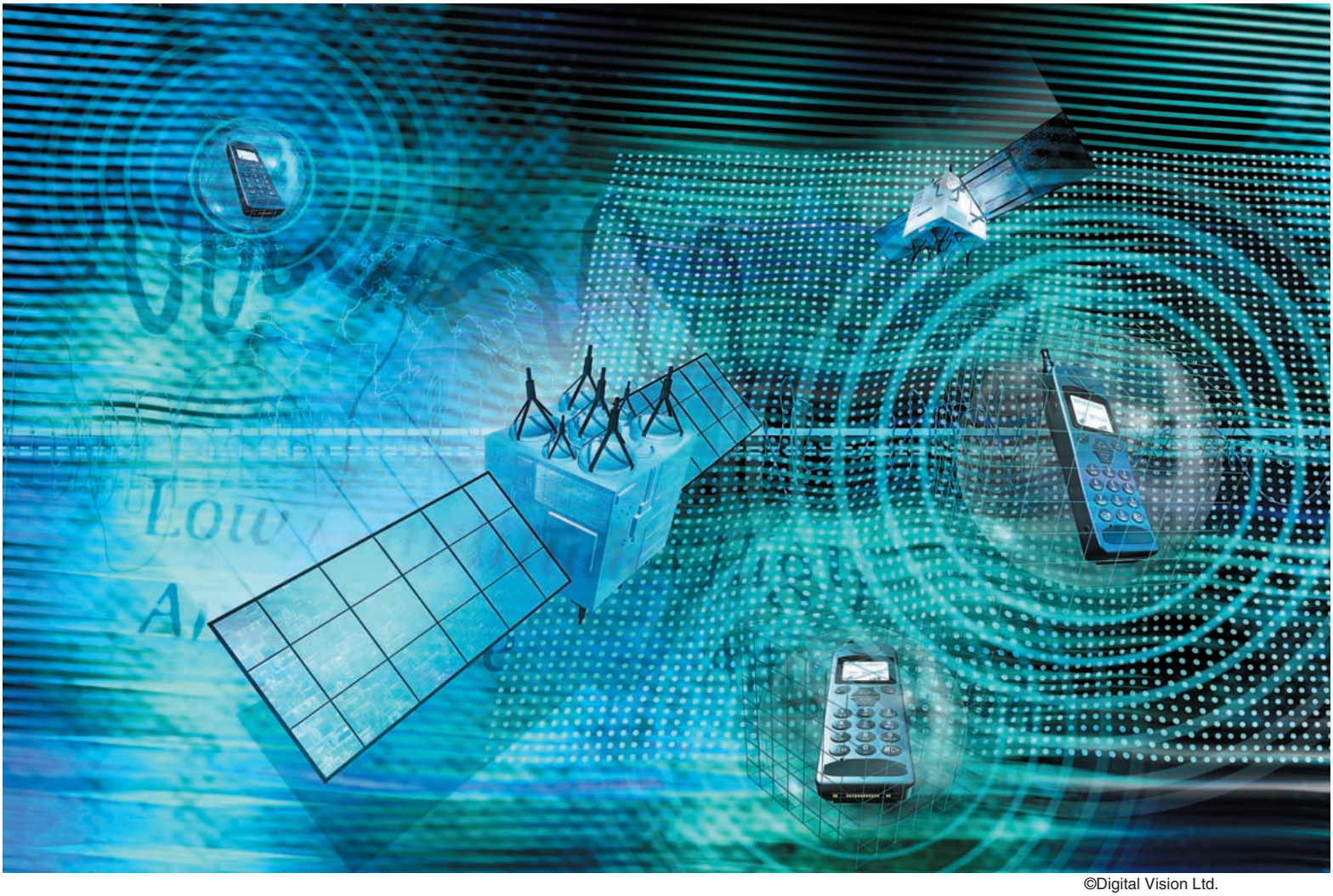
Advanced Phase-Locked-Loop Oscillators



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In the past decade, a rapidly increased demand in the development of microwave, millimeter-wave, wireless, and mobile communication systems can be observed. There is hardly any other area of these techniques in which such enormous changes, like those of nonlinear network design, could be recognized. Recently, the active devices and their technology have moved from classical solutions to solid-state performances and their integration. Nowadays, the monolithic integrated circuits (MMIC) are becoming predominant, and classical circuit design has shifted to advanced. This enables improvement of the technical parameters of these circuits at high yield, rapid growth of the markets, and, at the same time, reduction of costs. The most important subsystems in microwave, millimeter-wave, wireless, and mobile communication systems are the amplifiers, oscillators, mixers, phase shifters, and attenuators.

This article presents a very sophisticated subclass of these subsystems, namely oscillators, that use the phase-locked loop (PLL) technique. Some basic features and several application examples are presented that enable locking in the oscillator signal for each frequency offset. If the oscillator is used on its fundamental frequency, a high spectral purity is achieved without additional distortion. Furthermore, it can be increased by the filter function of the loop.

An integrated 70 GHz synthesizer is introduced and discussed, and a microwave synthesizer module and its technical behavior is described. Several measured results supported by analytical considerations show the applicability and the high performance of the PLLs introduced.

How Does the PLL Technique Work?

The PLL technique has had wide application in the past to solve various problems occurring in frequency sources [1], [2]. In the range of millimeter-wave frequencies, one of the most important tasks is the synchronization of the electronic tunable oscillator. Analog and digital frequency prescalers are commercially available up to the higher microwave frequency band, which is not satisfactory for millimeter-wave purposes [3], [4]. Hence, the output signal must be multiplied and filtered to reach higher frequencies [5]. These processes cause a reduction of oscillator performance, especially as there are problems with the purity of the output signal and the decrease of output power [6]-[8].

As a starting point, a double PLL is considered [9], which is coupled by a harmonic mixer (Figure 1). The

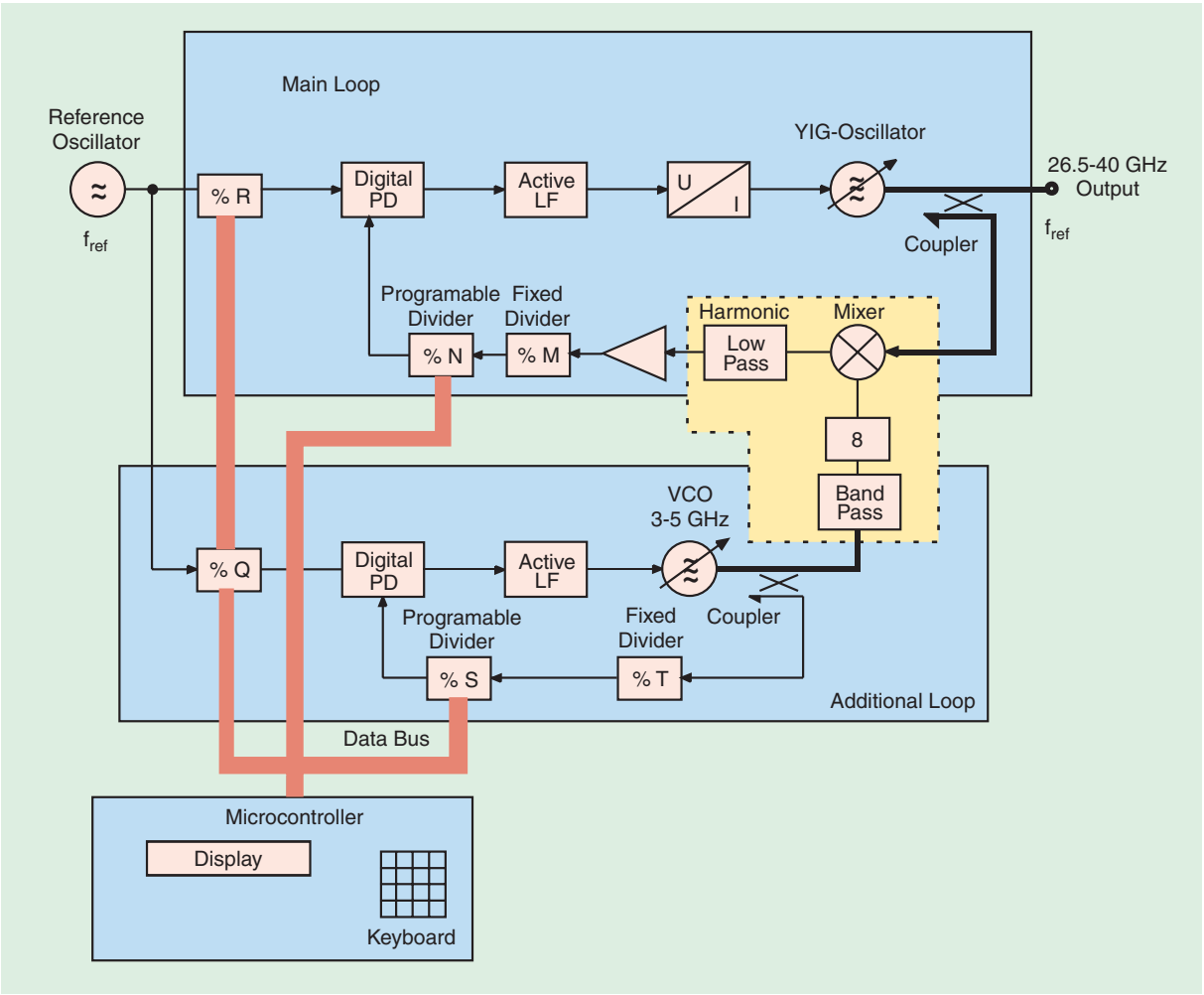

Figure 1. *Block diagram of the PLL system.*

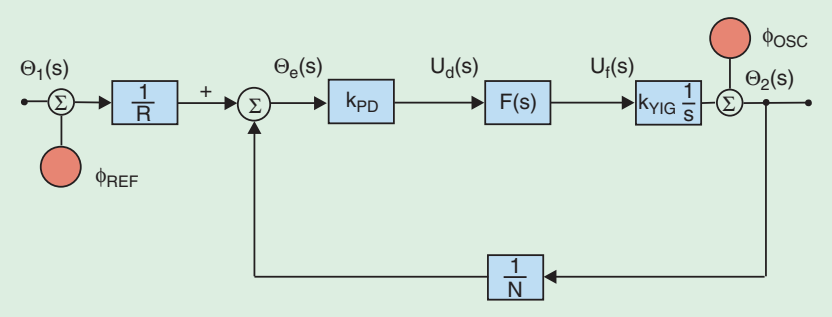

Figure 2. *Basic PLL-loop.*

main loop contains the elements that are necessary to stabilize the YIG oscillator, which works in the frequency range of 26.5 to 40 GHz, while the additional loop is of the same construction and stabilizes a voltage-controlled oscillator (VCO) at a frequency of 3 to 5 GHz. The output signal of the additional loop downconverts the output signal of the YIG oscillator by the harmonic mixer, enabling the use of frequency dividers.

In the feedback loops of both PLLs, fixed frequency-dividers (M, Q) are installed to convert the intermediate frequency and the output signal of the VCO, respectively, to a frequency range in which digital frequency dividers (N, S) can be applied. The reference oscillator is used for both PLLs, and its frequency is also divided by digital frequency divider before it is put on the phase detector. The factor M/R determines the step width of the frequency at which the YIG oscillator is stabilized.

A programmable divider switches the frequency in a large range, if the edge frequency of the harmonic mixer is below the edge frequency of the low-pass filter. So the frequency f_{RF} of the output signal can be calculated by

$$f_{RF} = 8 \cdot \frac{f_{ref} T}{Q} \cdot S + \frac{f_{ref} M}{R} \cdot N \tag{1}$$

where the positive integers $T, S, M, N, \ldots$ are the division ratios and f_{ref} is the reference frequency.

In this PLL, digital phase detectors (PD) are applied that contain an enhancement of the digital circuit and cover two latches in connection with two RS flip-flops. These allow the PD to recognize which one of both input signals is the first to carry out a change of the signal level, and the outlet "up" or "down" is dependent on the recognized change (negative logic).

This PLL system has two important properties. Both the hold-in range $\Delta\omega_H$ and the pull-in range $\Delta\omega_p$ are infinite [2]. This means that the following relations are valid

$$\Delta\omega_H \rightarrow \infty, \tag{2}$$

$$\Delta\omega_p \rightarrow \infty. \tag{3}$$

Thus, there is no restriction in the frequency range at which the double PLL works.

The double-PLL circuit has been realized with following operating parameters:

- Frequency range from 26.5 to 40 GHz should be comprised with a channel spacing of 50 kHz
- Reference oscillator frequency is 10 MHz.

Next, the locked state of this system should be analyzed. In an approximation of first order, a linearized model for both above mentioned PLLs can be obtained (Figure 2).

For the determination of the transfer function of the system, the Laplace transformation is applied. The transfer function of the active lowpass filter is

$$F(s) = \frac{1 + s\tau_2}{s\tau_1}, \tag{4}$$

where τ_1 and τ_2 are the time constants of the loop filter.

Referring to the flow diagram in Figure 2, the phase transfer function for each of these PLLs is given by

$$H(s) = \frac{N}{R} \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}. \tag{5}$$

The parameters ω_n and ξ are described as:

$$\omega_n = \sqrt{\frac{k_{PD} \cdot k_{YIG}}{N\tau_1}} \tag{6}$$

$$\xi = \frac{\tau_2}{2}\omega_n, \tag{7}$$

where k_{PD} and k_{YIG} are the transmission coefficients of the phase detector and the YIG oscillator, respectively.

Complementary, the phase error transfer function yields:

$$H_e(s) = \frac{\Theta_e(s)}{\Theta_1(s)} = \frac{1}{R} \frac{s^2}{s^2 + 2\xi\omega_n s + \omega_n^2}, \tag{8}$$

with $\Theta e(s)$ and $\Theta 1(s)$ the Laplace transforms of the phase error and the input phase, respectively.

The PLL can be optimized due to its damping factor. In the optimal case, it has a value of $\xi = 1/\sqrt{2}$, which is well know from the analog computer simulations [7].

The linearized model in Figure 2 also renders possible the calculation of the influence of the PLL on the oscillator's phase noise [8]. For this reason, two noise sources are added to the block diagram in Figure 2: phase noise of the reference oscillator (ϕ_{REF}) at the input

and the phase noise of the YIG-oscillator (ϕ_{osc}) at the output of the system. This leads to the output phase noise equation:

$$L_{\phi}(\omega) = \left(\frac{N}{R}\right)^2 \frac{\omega_n^4 + (2\xi\omega_n)^2\omega^2}{(\omega_n^2 - \omega^2)^2 + (2\xi\omega_n)^2\omega^2} L_{\phi_{REF}}(\omega) + \frac{\omega^2}{(\omega_n^2 - \omega^2)^2 + (2\xi\omega_n)^2\omega^2} L_{\phi_{OSC}}(\omega), \quad (9)$$

with the associated one-side spectral noise power densities, $L_{\phi REF}$ and $L_{\phi OSC}$, respectively.

All these features are summarized in a software tool, which allows the extraction of the values of the resistors and the capacitor needed for dimensioning the loop filter (LF). These quantities are optimized due to the best value of the damping factor ζ and to a user-defined setting time. The designer simply types in the phase noise given by the data of the oscillators and receives the output phase noise as a result.

The stability of the system is investigated by the help of the Bode-diagram (Figure 3) of the local oscillator open loop. The magnitude shows a medium frequency of 2.7 kHz, while the phase has a reserve of 78.5° at this frequency. This indicates the stability of the whole system.

In Figure 4, the long-term stability of the system is plotted for different lock conditions (locked/unlocked). It can be observed that in the locked state a long-term error of ± 10 Hz is reached.

For the realized PLL, the phase noise relations were measured and plotted (Figure 5). The upper curve shows the single-sided spectral phase noise density of the YIG oscillator in an unlocked condition, whereby the lower curve represents the locked condition. The peaks between 50 Hz and 1 kHz arise from a public power network and a wave peak about 36 kHz from a voltage source used to control the YIG oscillator. Phase noise degrades by 30 dB/decade and is reduced by approximately 50 dBc/Hz compared to the free-running YIG.

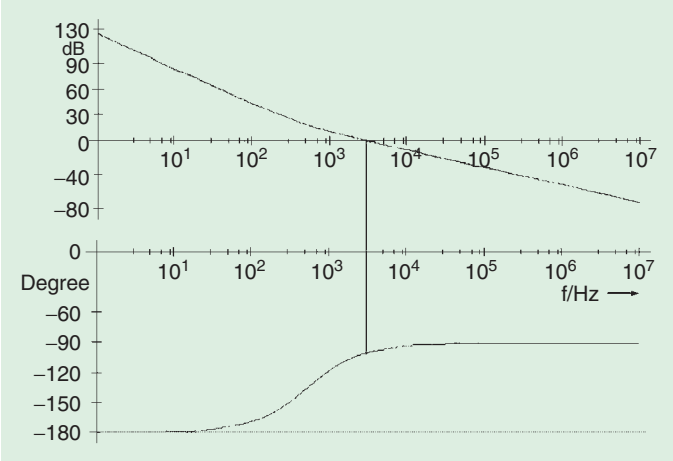

Figure 3. *Simulated Bode diagram of local oscillators open loop.*

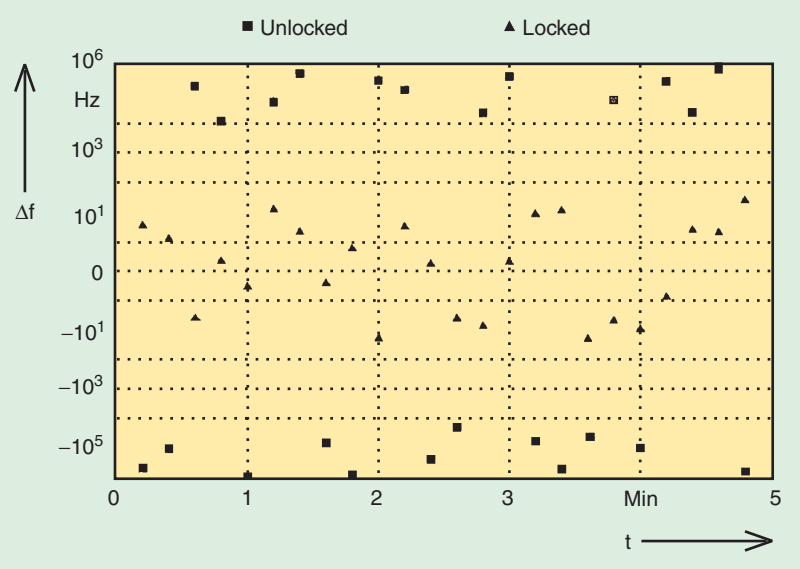

Figure 4. *Measured frequency stability for different lock conditions.*

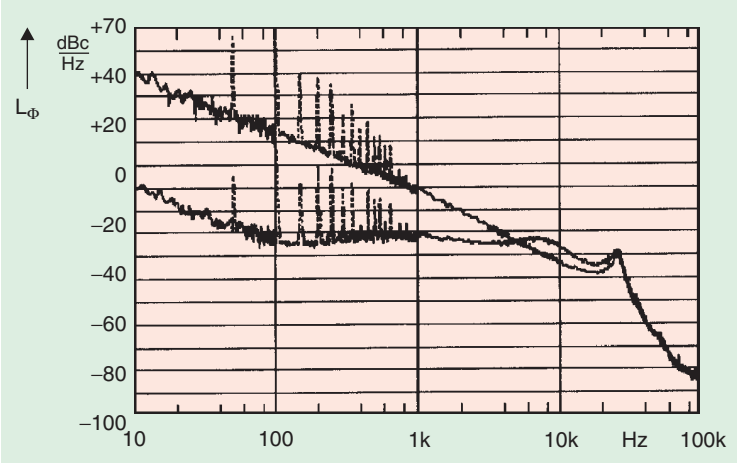

Figure 5. *The measured output one side spectral noise density for different lock conditions.*

Integrated Phase-Locked Oscillators

This section focuses on an application at 70 GHz that is used for the representation of the international Volt [10].

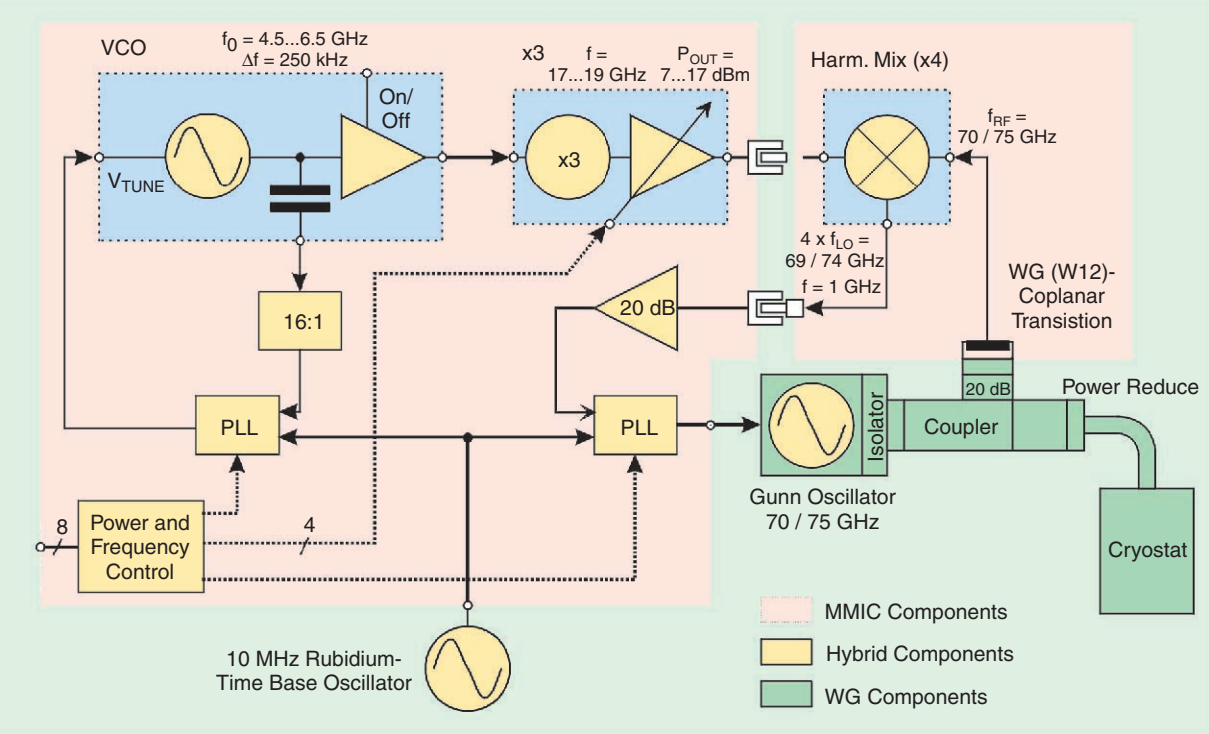

Figure 6. *Schematic of the proposed 70 GHz synthesizer.*

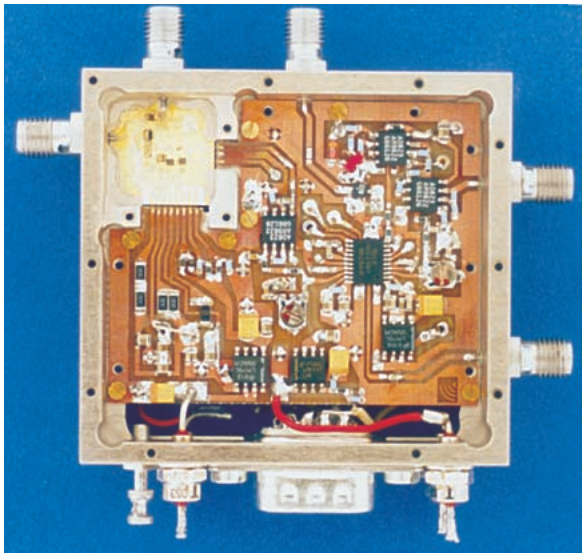

Figure 7. *The 18 GHz VCO module.*

Cooled Josephson Junctions create very fine constant voltage steps. Thus, approximately 10,000 junctions in series and a frequency of 70 GHz is needed in order to generate a voltage of 10 V. Although 70 GHz easily can be generated using a Gunn oscillator, this approach does not deliver the accuracy of 10^{-10} necessary for the created frequency, which means ± 5 Hz. A rather expensive way to stabilize the frequency is a frequency-lock counter (FLC). Therefore, a 70 GHz synthesizer with a tuning range from 70 to 75 GHz in steps of 1 MHz, including two hybrid PLLs with the overall accuracy of ± 5 Hz (Figure 6), was used.

The synthesizer includes a 6 GHz oscillator, which is stabilized versus a rubidium time-base oscillator by the first PLL. Together with the following frequency times three multiplier, the first chip acts as a voltage controlled oscillator (VCO) with an operating frequency from 17 to 19 GHz. The amplified signal then serves as an input signal for the harmonic mixer. The 4th harmonic of the 18 GHz VCO is used as the mixer's LO signal. With the RF signal coming from the Gunn oscillator, an IF signal around 1 GHz is generated, which is directly fed into a second PLL. Also this signal is compared to the rubidium time-base oscillator.

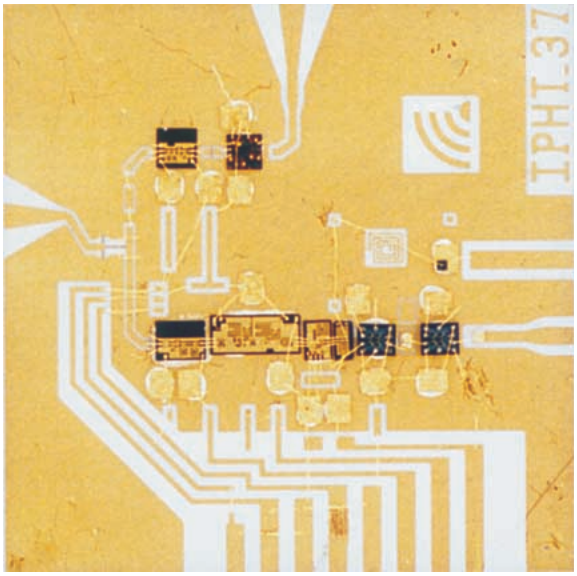

Figure 8. *Magnification of the MMICs included in the 18 GHz module.*

Using the second PLL, frequency steps of 1 MHz are possible for the Gunn oscillator. Figure 7 shows the assembly of the 18 GHz VCO module.

The MMICs can be seen in the upper left region of Figure 8. They are assembled on ceramic. The PLLs and other tuning elements are placed on FR4 substrate. The module size is $60 \times 55 \times 23$ mm^3.

A long-term measurement was carried out with all modules for more than 3.5 hours. The stability of various Gunn oscillators' output signals is excellent, as can be seen for a 75 GHz Gunn oscillator (Figure 9). The nominal frequency is shifted by 4.1 Hz, which seems to be systematically due to the FLC. The maximum deviation is + 9 Hz / - 2 Hz; the standard deviation is ± 1.4 Hz.

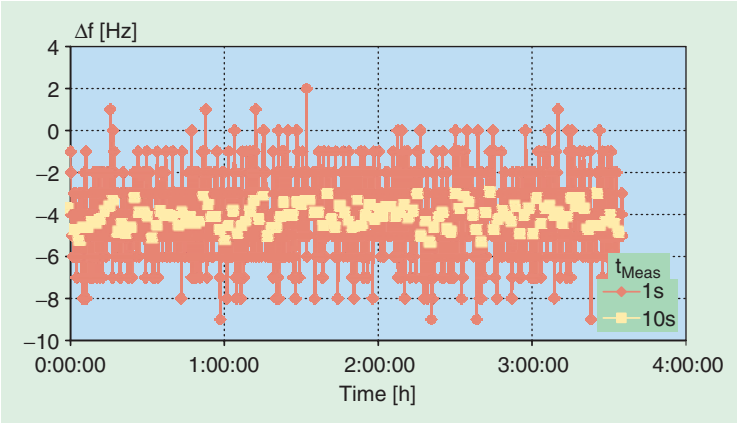

Figure 9. *Long-term measurements of the stabilized Gunn oscillator.*

Microwave Synthesizer Module

As a second example, a high precision frequency oscillator module in the range of 13 to 18 GHz is discussed in this section. Both frequency as well as output power can be controlled by a PC interface.

The basic functionality is shown in Figure 10. Using a sampling phase detector, the frequency of an external microwave VCO is mixed down into the intermediate frequency range (< 100 MHz). This IF signal will be compared to the reference signal. A second PLL generates the input signal for the sampling phase detector.

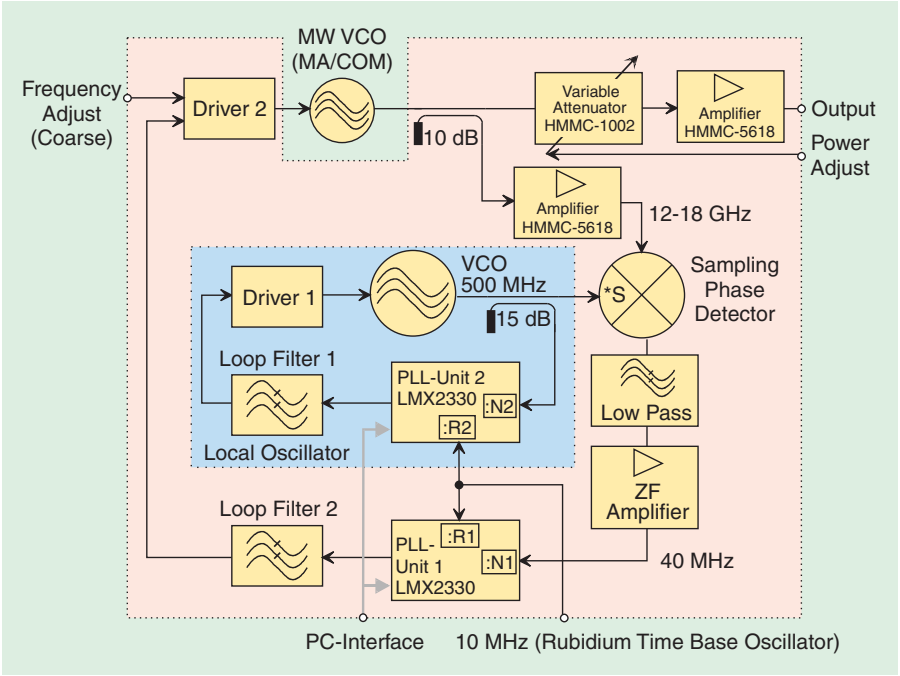

Figure 10. *Oscillator module with sampling phase detector.*

A part of the VCO signal is decoupled by a directional coupler and amplified. By a sampling phase detector, this signal will be mixed with harmonics of the LO signal. This generates frequencies as given by:

$$f_{ZF} = \pm S \cdot f_{LO} \pm f_{VCO} \tag{10}$$

(The sampling phase detector generates all harmonics of the LO signal up to $S > 50$). The LO frequency is tuneable by a second PLL in the frequency range from 400 to 500 MHz. For the LO frequency the following is valid:

$$f_{LO} = \frac{N2}{R2} \cdot f_{REF}. \tag{11}$$

The lowest signal of the Sampling Phase Detector is based on the difference of the frequencies $S \cdot f_{LO}$ and f_{VCO}. By this the following intermediate frequency is generated

$$f_{ZF1} = S \cdot f_{LO} - f_{VCO} \tag{12a}$$

if $S \cdot f_{LO} > f_{VCO}$ is valid, or

$$f_{ZF2} = f_{VCO} - S \cdot f_{LO} \tag{12b}$$

if $S \cdot f_{LO} < f_{VCO}$ is valid.

The LO frequency will be fixed in a way that the lowest mixing frequency product of the sampling phase detector appears in the range of approximately 40 MHz. After a low-pass filter, this frequency will be amplified and compared to the reference frequency, a 10 MHz rubidium frequency source (PLL 1). It follows:

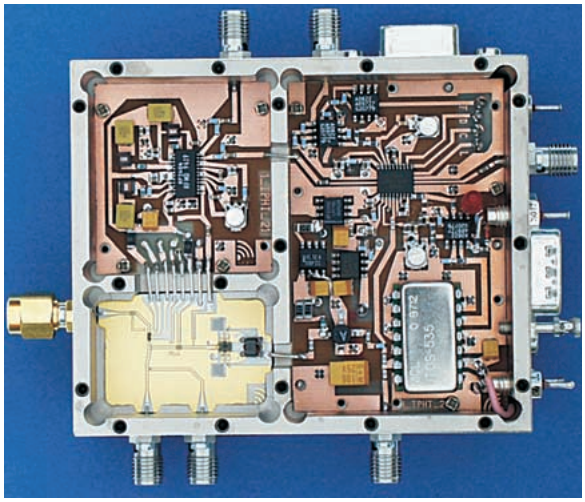

Figure 11. *Realized module.*

$$f_{ZF} = \frac{N1}{R1} \cdot f_{REF} \,. \tag{13}$$

PLL 1 generates a tuning voltage to control the VCO frequency unless (13) is fulfilled. In the following, the case $S \cdot f_{LO} < f_{VCO}$ is considered for the calculation of the output frequency f_{VCO}. In the other case, $S \cdot f_{LO} > f_{VCO}$, analogous conditions are valid. Following (12), the output frequency of the VCO is:

$$f_{VCO} = S \cdot f_{LO} + f_{ZF2} = \left(S \cdot \frac{N_2}{R_2} + \frac{N_1}{R_1} \right) \cdot f_{REF}. \tag{14}$$

As the sampling phase detector generates all harmonics of the LO signal, for different factors S different output frequencies can be generated, all of them with the same IF frequencies. To avoid this nonuniqueness, the PLL is only responsible for the fine-tuning of the VCO frequency. A digital/analog converter generates a bias signal for rough tuning of the working frequency. As the periodicity of the IF frequency is caused by the LO-frequency, the frequency shift of the VCO by the PLL has to be limited to a smaller range than the smallest IF frequency.

Our module is designed for PLL frequencies of 1 MHz (PLL 1) and 100 kHz (PLL 2). It follows

$$R_1 = \frac{10\text{MHz}}{1\text{MHz}} = 10 \tag{15}$$

$$R_2 = \frac{10\text{MHz}}{100\text{kHz}} = 100. \tag{16}$$

An output frequency of 18,040 MHz based on a LO frequency will be realized. Then a mixing of the output signal with the 36 harmonic frequency of the LO signal is necessary (36 · 500 MHz=18,000 MHz).

The factor N_2 of PLL 2 will be according to (11):

$$N_2 = \frac{500\text{MHz}}{100\text{kHz}} = 5{,}000, \tag{17}$$

whereas for the factor N_1 of PLL 1 yields (12):

$$N_1 = \frac{40\text{MHz}}{1\text{MHz}} = 40, \tag{18}$$

respectively.

It follows for the output frequency of the module:

$$f_{VCO} = \left(36 \cdot \frac{5{,}000}{100} + \frac{40}{10} \right)$$
$$f_{REF} = 1{,}804 \cdot 10 \text{ MHz} = 18{,}040 \text{ MHz}. \tag{19}$$

The minimal frequency step of the output frequency is equal to the phase-compare frequency of the IF signal, i.e., 1 MHz.

Figure 11 shows the produced module discussed above according to the block diagram given by Figure 10. It should be mentioned, however, that not only the output frequency but also the output power of the module is controlled digitally. The VCO signal passes a variable damping unit, which is controlled by a digital/analog converter. After the damping unit, the signal is amplified by an integrated circuit, generating an output power $P_{\text{out, max}} > 13$ dBm.

Acknowledgment

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