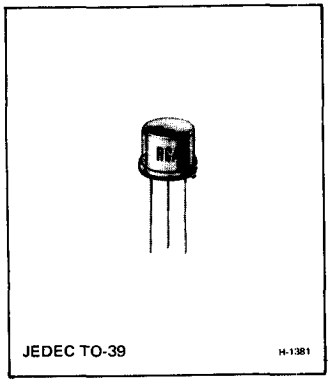
RCA Solid State Division

RF Power Transistors

2N3866



Silicon N-P-N Overlay Transistor

High-Gain Driver for VHF/UHF Applications in Military and Industrial Communications Equipment

Features

- **High Power Gain, Unneutralized Class C Amplifier**
  - **1 W output at 400 MHz (10 dB gain)**
  - **1 W output at 250 MHz (15 dB gain)**
  - **1 W output at 175 MHz (17 dB gain)**
  - **1 W output at 100 MHz (20 dB gain)**
- **Low Output Capacitance**
  C_{obo} = 3 pF max.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

*	COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55 V
	COLLECTOR-TO-EMITTER VOLTAGE:		
	With external base-to-emitter resistance (R_{BE}) = 10Ω	V_{CER}	55 V
*	With base open	V_{CEO}	30 V
*	EMITTER-TO-BASE VOLTAGE	V_{EBO}	3.5 V
*	CONTINUOUS COLLECTOR CURRENT	I_C	0.4 A
*	CONTINUOUS BASE CURRENT	I_B	0.4 A
*	TRANSISTOR DISSIPATION	P_T	
	At case temperature up to 25°C		5 W
	At case temperatures above 25°C		See Fig. 4
*	TEMPERATURE RANGE:		
	Storage & Operating (Junction)		−65 to +200 °C
*	LEAD TEMPERATURE		
	At distances ≥ 1/16 in. (1.58 mm) from seating plane for 10 s max.		230 °C

* In accordance with JEDEC registration data format JS-6 RDF-3.

RCA-2N3866 is an epitaxial silicon n-p-n planar transistor employing an advanced version of the RCA-developed "overlay" emitter-electrode design. This electrode consists of many isolated emitter sites connected together through the use of a diffused-grid structure and a metal overlay which is deposited on a silicon oxide insulating layer by means of a photo-etching technique. This overlay design provides a very high emitter periphery-to-emitter area ratio resulting in low output capacitance, high rf current handling capability, and substantially higher power gain.

The 2N3866 is intended for class-A, -B, or -C amplifier, frequency-multiplier, or oscillator circuits: it may be used in output, driver, or pre-driver stages in vhf and uhf equipment.

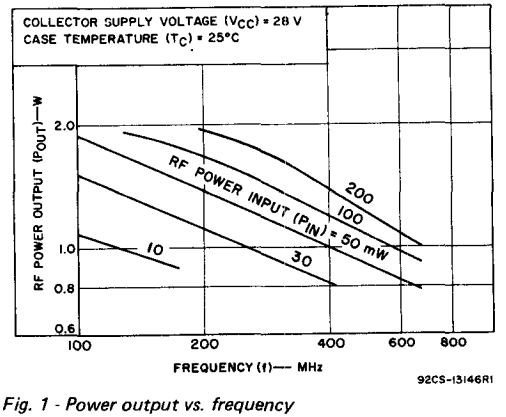
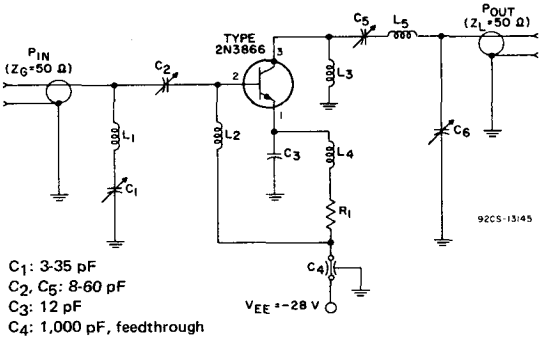


Fig. 1 - Power output vs. frequency



C_1: 3-35 pF
C_2, C_5: 8-60 pF
C_3: 12 pF
C_4: 1,000 pF, feedthrough
C_6: 0.9-7 pF
L_1: 2 turns No. 18 wire, 1/4" ID, 1/8" long
L_2: Ferrite rf choke, 1 turn, Z = 450Ω
L_3, L_4: RF choke, 0.1 μH
L_5: 2-1/2 turns, No. 18 wire, 1/4" ID, 3/16" long
R_1: 5.6Ω, 1 W

Fig. 2 - RF amplifier circuit for power output test (400-MHz operation)

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C

STATIC

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		DC Voltage (V)		DC Current (mA)					
		V_{CE}	V_{EB}	I_E	I_B	I_C	Min.	Max.	
* Collector-Cutoff Current:									
Base-emitter junction reverse biased	I_{CEX}	55	1.5				–	0.1	mA
T_C = 200°C		30	1.5				–	0.1	
Base open	I_{CEO}	28			0		–	20	μA
* Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	55	–	V
* Collector-to-Emitter Breakdown Voltage:									
With base open	$V_{(BR)CEO}$				0	5	30	–	V
With base connected to emitter through 10-ohm resistor	$V_{(BR)CER}$		0			5	55	–	
* Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	3.5	–	V
* Emitter-Cutoff Current	I_{EBO}		3.5				–	0.1	mA
* Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$				20	100	–	1.0	V
* DC Forward-Current Transfer Ratio	h_{FE}	5 5				360 50	5 10	– 200	
Thermal Resistance: (Junction-to-Case)	$\theta_{J\text{-}C}$						–	35	°C/W

DYNAMIC

TEST & CONDITIONS	SYMBOL	FREQUENCY MHz	LIMITS		UNITS
			MINIMUM	MAXIMUM	
Power Output (V_{CC} = 28 V): P_{IE} = 0.1 W	P_{OE}	400	1.0	–	W
Large-Signal Common-Emitter Power Gain (V_{CC} = 28 V): P_{IE} = 0.1 W	G_{PE}	400	10	–	dB
* Collector Efficiency (V_{CC} = 28 V): P_{IE} = 0.1 W, P_{OE} = 1 W, Source Impedance = 50Ω	η_C	400	45	–	%
* Magnitude of Common-Emitter, Small Signal, Short-Circuit Forward-Current Transfer Ratio I_C = 50 mA, V_{CE} = 15 V	$\lvert h_{fe} \rvert$	200	2.5	–	
* Available Amplifier Signal Input Power, P_{OE} = 1 W, Source Impedance = 50Ω (See Fig. 2)	P_i	400	–	0.1	W
* Common-Base Output Capacitance (V_{CB} = 28 V)	C_{obo}	1	–	3	pF

* In accordance with JEDEC registration data format JS-6 RDF-3

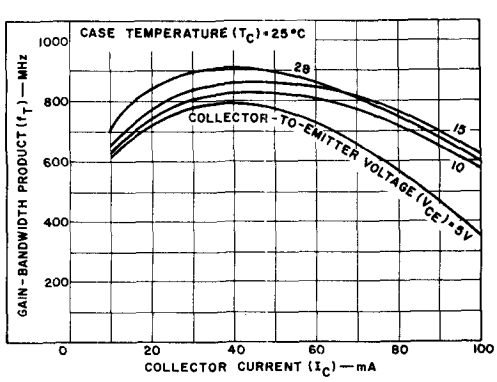


Fig. 3 - Gain-bandwidth product vs. collector current

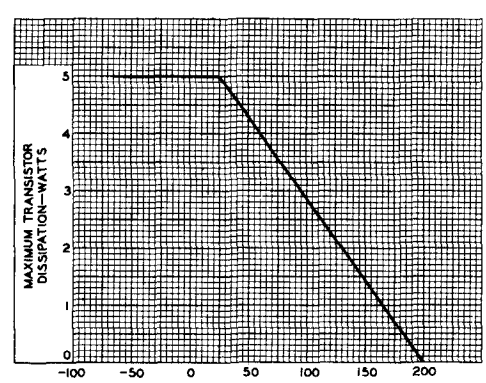


Fig. 4 - Dissipation derating curve

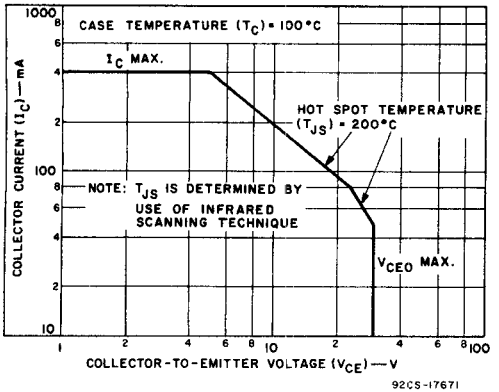


Fig. 5 - Safe area for dc operation

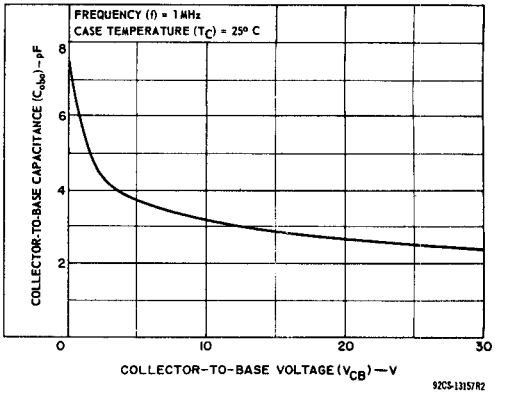


Fig. 6 - Variation of collector-to-base capacitance

DESIGN DATA

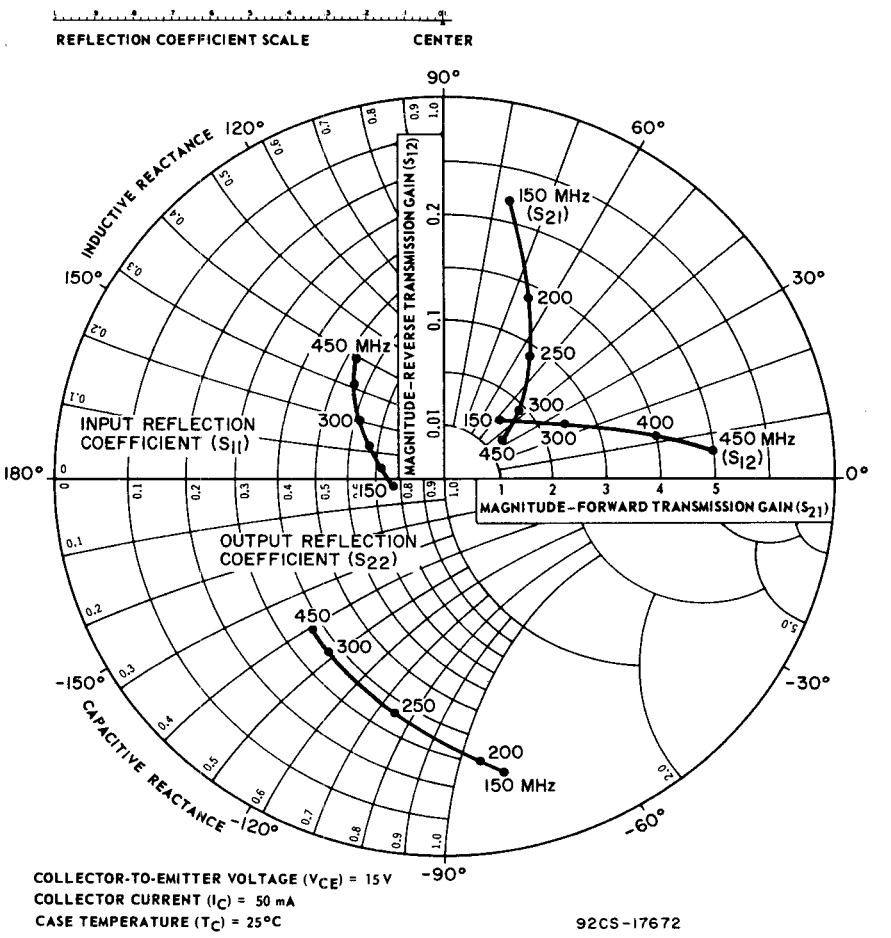


Fig. 7 - Typical S parameters vs. frequency

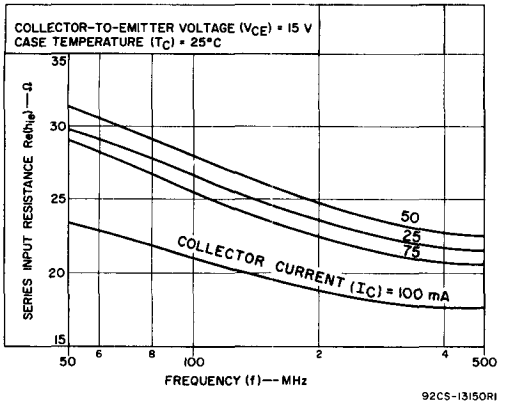


Fig. 8 - Typical series input resistance vs. frequency

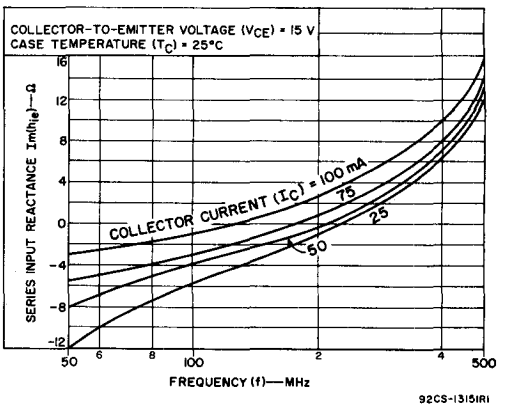


Fig. 9 - Typical series input reactance vs. frequency

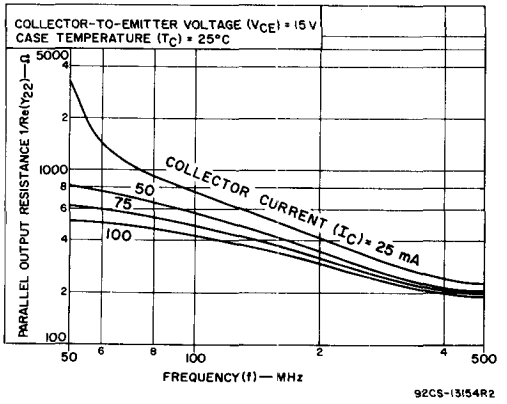


Fig. 10 - Typical parallel output resistance vs. frequency

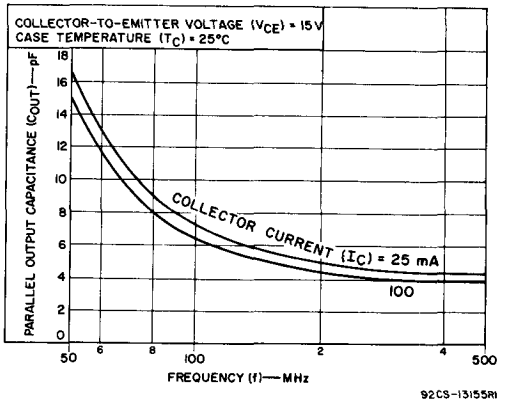
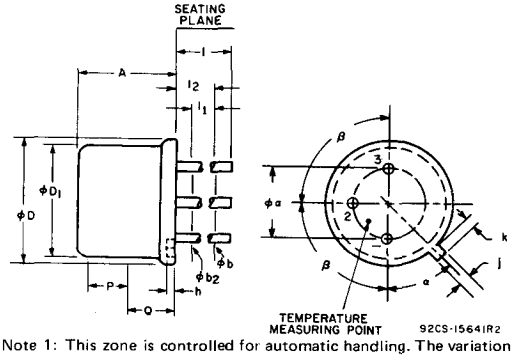


Fig. 11 - Typical parallel output capacitance vs. frequency

DIMENSIONAL OUTLINE
JEDEC No. TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD_1	0.315	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500	0.562	12.70	14.27	2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.5 in (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.