A Multiple Modulator Fractional Divider

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***Abstract*—Fractional-*N* synthesis allows a PLL to achieve arbitrarily fine frequency resolution. Because the technique modulates the instantaneous divide ratio, fractional-*N* synthesizers suffer from fractional spurs. Various cancellation schemes allow fractional spur reduction to about −70 dBc at the expense of hardware cost and complexity.**

Recent advances in oversampling A/D conversion technology can be incorporated into fractional-*N* synthesis, allowing the spectrum of error energy to be shaped so that fractional synthesis error energy is pushed away from the carrier. Based on this new technology, a CMOS integrated fractional-*N* divider was successfully developed. A complete fractional-*N* PPL was constructed utilizing only the CMOS divider, a dual modulus prescaler, a simple loop filter, and VCO. The resulting PLL exhibits no fractional spurs.

I. Review of Fractional-*N* Synthesis

In a conventional PLL (Fig. 1) $f_{vco} = N * f_{ref}$. The divide ratio N must be an integer and therefore the frequency resolution of the locked loop is f_{ref}. Fine frequency resolution requires a small f_{ref} and a correspondingly small loop bandwidth. Narrow loop bandwidths are undesirable because of long switching times, inadequate suppression of vco phase noise, and susceptibility to hum and noise.

Fractional-*N* synthesis was developed to allow a phase-locked loop to have frequency resolution finer than f_{ref} [1], [2]. In a fractional-*N* divider, the integer divide ratio is periodically altered from N, to $N + 1$ (Fig. 2). The resulting average divide ratio will be increased from N by the duty cycle of the $N + 1$ division.

$$\begin{aligned}\text{average } f_{vco} &= \frac{1}{(T_N + T_{N+1})}\left[T_N * N * f_{ref}\right. \\ &\quad \left. + T_{N+1} * (N + 1) * f_{ref}\right] \\ &= [N + T_{N+1}/(T_N + T_{N+1})] * f_{ref} \\ &= (N.f) * f_{ref}\end{aligned}$$

where N denotes the integer portion of the divide ratio and $.f$ is the fractional component of the average divide ratio.

Typically, the overflow from an accumulator is used to modulate the instantaneous divide ratio (Fig. 3) [3]. Given that

a) VCO frequency $= N.f * f_{ref}$,
b) Accumulator maximum capacity $= C - 1$,
c) $X = .f * C$ (so that $X/C = .f$),

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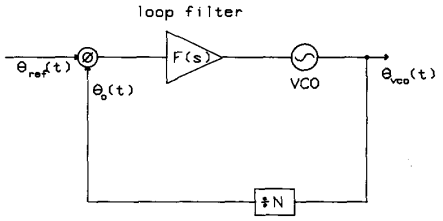

Fig. 1. Basic PLL.

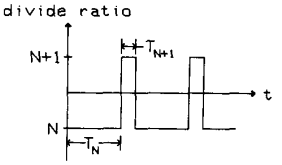

Fig. 2. Alternating divide ratio of fractional-*N* PLL.

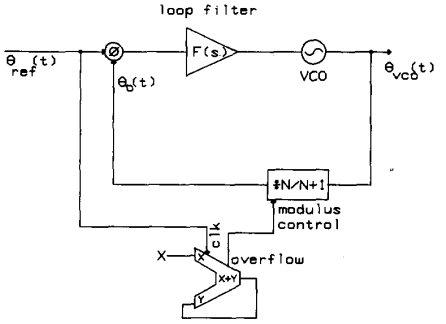

Fig. 3. Fractional-*N* PLL showing accumulator control of divide ratio.

then, while the divider is programmed to divide by N, the VCO signal at the phase detector will be at a frequency of $f_{ref} + (.f/N) * f_{ref}$ and the loop phase error will begin to advance at a rate of $2\pi * (.f/N) * f_{ref}$ rad/s. The phase error, referred to the VCO, advances at a rate of $2\pi * .f * f_{ref}$ rad/s. Because the accumulator is summing the same fraction as the VCO phase-error/reference-cycle, an accumulator overflow corresponds to a VCO phase error exceeding 2π radians and indicates the need to remove 2π of phase from the VCO output; accomplished by changing the divider modulus to $N + 1$ for a single reference cycle.

This periodic modification of the divider modulus gives rise to a sawtooth phase error (Fig. 4). If unfiltered, the phase error causes severe spurious tones (fractional spurs) at all multiples of the offset frequency ($.f * f_{ref}$).

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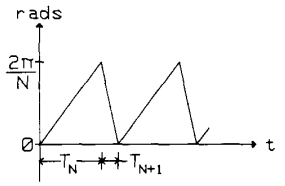

Fig. 4. Sawtooth phase error of conventional fractional-N synthesis.

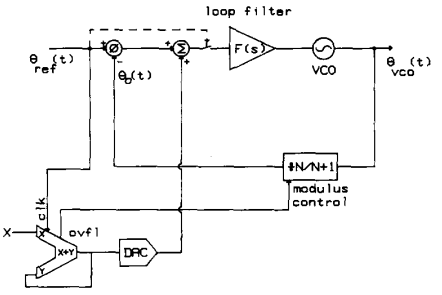

Fig. 5. Fractional-N PLL incorporating phase interpolation.

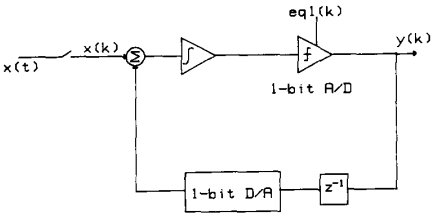

Fig. 6. Sigma-delta modulator.

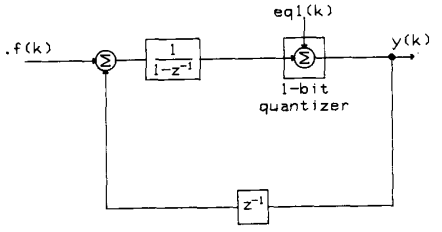

Fig. 7. Sigma-delta modulator suitable for fractional-N synthesis.

Fortunately, it is easy to predict what the phase error will be at any given time and a compensating signal can be summed into the PLL to cancel the error signal (Fig. 5) [4]. The phase detector output is sampled to allow settling of the interpolation DAC every reference cycle. This form of correction is called phase interpolation and fractional spurs are reduced to the extent that the phase interpolation signal exactly matches the phase error. Through the use of precision DAC's and carefully designed phase detector and sampler circuitry, fractional spurs of -70 dBc can be achieved. The complexity and expense of the interpolation circuitry make this form of fractional-N synthesis unsuitable in many applications.

II. A New Approach to Fractional Division

Interpolative A/D converters primarily based on sigma-delta modulators, have recently been developed into a viable technology for low frequency measurement and audio systems [5]–[7]. Interpolative A–D converters operate by greatly oversampling the input with a coarse (usually 1-bit) converter and then digitally filtering the 1-bit output stream to eliminate out-of-band quantization noise. S/N is further enhanced by embedding the 1-bit converter in a recursive filter structure which shapes the quantization noise present at the converter output so that most of the noise energy lies outside the band of interest and will be removed during filtering.

The same concept may be applied to fractional-N synthesis. Fractional-N synthesis attempts to achieve fine frequency resolution through manipulation of a coarse, integer divider. The desired fractional frequency is analogous to the analog input of an A–D. The integer-restricted divider is analogous to the 1-bit converter utilized in interpolative A–D converters. Consequently, most of the recent developments in interpolative A–D converter technology are also applicable to fractional-N synthesis.

A multistage, sigma-delta modulator architecture based on the work of Matsuya *et al.* [5] was chosen to implement the new fractional-N divider. Fig. 6 shows the basic modulator used in sigma-delta A–D converters. $x(k)$ is the modulator input, $y(k)$ is the modulator output, and $e_{q1}(k)$ is the quantization error added by the 1-bit A/D. In fractional-N synthesis applications, the input to the sigma-delta modulator is the desired fractional offset, which is a digital word. Consequently, the integrator may be digitally implemented and the 1-bit D-A is not required. Fig. 7 shows a sigma-delta modulator suitable for fractional-N synthesis.

$$Y(z) = \frac{1/(1 - z^{-1})}{1 + z^{-1}/(1 - z^{-1})}(.F(z)) + \frac{1}{1 + z^{-1}/(1 - z^{-1})}E_{q1}(z) = .F(z) + (1 - z^{-1})E_{q1}(z) \quad (1)$$

where $Y(z)$, $.F(z)$ and $E_{q1}(z)$ are the Z-transforms of $y(k)$, $.f(k)$, and $e_{q1}(k)$, respectively.

A block diagram of a three-modulator fractional divider is shown in Fig. 8. System behavior is assumed sufficiently random to justify modeling each 1-bit quantizer as a unity gain element with added quantization noise [8]. $N.F$ is the desired rational divide ratio and $N_{div}(k)$ is the actual sequence presented to the integer restricted divider. Using

$$N_1(z) = (1 - z^{-1})E_{q1}(z) + .F(z) \quad (1)$$

$$N_2(z) = -E_{q1}(z) + (1 - z^{-1})E_{q2}(z) \quad (2)$$

$$N_2'(z) = -(1 - z^{-1})E_{q1}(z) + (1 - z^{-1})^2E_{q2}(z) \quad (3)$$

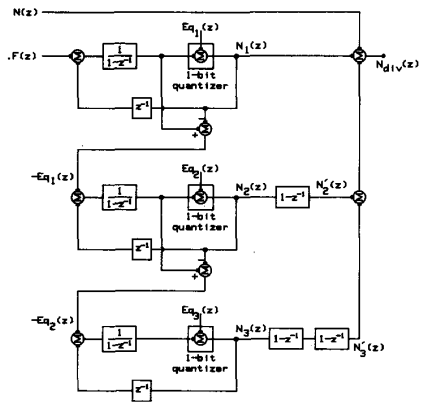

Fig. 8. 3-modulator fractional-N divider.

$$N_3(z) = -E_{q2}(z) + (1 - z^{-1})E_{q3}(z) \quad (4)$$

$$N_3'(z) = -(1 - z^{-1})^2E_{q2}(z) + (1 - z^{-1})^3E_{q3}(z) \quad (5)$$

$$N_{\text{div}}(z) = N(z) + N_1(z) + N_2'(z) + N_3'(z)$$

$$= N.f(z) + (1 - z^{-1})^3E_{q3}(z) \quad (6)$$

In a locked PPL,

$$f_{\text{out}}(k) = N_{\text{div}}(k)f_{\text{ref}}. \quad (7)$$

Using (7), we can then write

$$F_{\text{out}}(z) = N.F(z)f_{\text{ref}} + (1 - z^{-1})^3f_{\text{ref}}E_{q3}(z) \quad (8)$$

where the first term of (8) is the desired frequency, and the second term represents frequency noise due to fractional division. This form is not useful for frequency synthesis applications and needs to be converted into single-sideband phase noise, $\mathcal{L}(f)$.

Each of the 1-bit quantizers is assumed to have uniform quantization error. The error power is then $(\delta)^2/12$; where δ is the minimum stepsize of the quantizer. Because we are quantizing to integers, $\delta = 1$ and the quantization error power $= 1/12$. This power is spread over a bandwidth of f_{ref}. Consequently, the power spectral density (PSD) of $e_{q3} = 1/(12f_{\text{ref}})$. Defining, $v(z) \equiv$ frequency fluctuations of $F_{\text{out}}(z)$

$$S_v(z) = |(1 - z^{-1})^3f_{\text{ref}}|^2(1/12f_{\text{ref}}) \quad (9)$$

$$= |1 - z^{-1}|^6(f_{\text{ref}}/12). \quad (10)$$

We want phase fluctuations, not frequency fluctuations.

$$\phi(t) = \int \omega(t)\,dt = 2\pi \int \nu t\,dt.$$

Employing a simple rectangular integration to represent $\int dt$ in the z-domain,

$$\Phi(z) = \frac{T_sW(z)}{1 - z^{-1}} = \frac{2\pi T_sv(z)}{1 - z^{-1}}, \quad (11)$$

where T_s is the sample period.

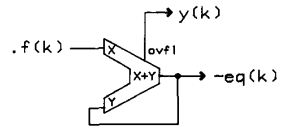

Fig. 9. An accumulator regarded as a sigma-delta modulator.

Using $T_s = 1/f_{\text{ref}}$ and (10) in (11), we obtain

$$S_\Phi(z) = \frac{(2\pi)^2}{|1 - z^{-1}|^2f_{\text{ref}}^2} * \frac{|1 - z^{-1}|^6f_{\text{ref}}}{12}$$

$$= \frac{(2\pi)^2}{12f_{\text{ref}}}|1 - z^{-1}|^4 \text{ rad}^2/\text{Hz}. \quad (12)$$

If $S_\phi(f)$ is a two-sided PSD, then; $\mathcal{L}(f) = S_\phi(f)$. Therefore,

$$\mathcal{L}(z) = \frac{(2\pi)^2}{12f_{\text{ref}}}|1 - z^{-1}|^4 \text{ rad}^2/\text{Hz}. \quad (13)$$

Converting to the frequency domain and generalizing to any number of modulator sections,

$$\mathcal{L}(f) = \frac{(2\pi)^2}{12f_{\text{ref}}}[2 \sin (\pi f/f_{\text{ref}})]^{2(m-1)} \text{ rad}^2/\text{Hz}, \quad (14)$$

where m is the number of modulator sections.

Typically we are concerned with offset ranges small compared to the reference frequency allowing;

$$\mathcal{L}(f) \approx \frac{(2\pi)^2}{12f_{\text{ref}}}\left[\frac{f}{f_{\text{ref}}/2\pi}\right]^{2(m-1)} \text{ rad}^2/\text{Hz}. \quad (15)$$

Equation (15) gives the colored quantization noise produced by the multiple modulator synthesis technique. Instead of discrete spurs, error energy produced by the fractional division will be manifested as noise. This noise must be filtered prior to the VCO to prevent unacceptable degradation of spectral purity. Interpolative A–D converters utilize digital filters to remove out-of-band quantization noise. In a fractional-N synthesis application, the PLL lowpass characteristic may be utilized to filter the quantization noise. A circuit example is given in Section IV.

The system of Fig. 8 can be simplified when it is recognized that an accumulator is a compact realization of the sigma-delta modulator. Fig. 9 shows an accumulator based sigma-delta modulator. The feedback of Fig. 7 occurs implicitly in the internal logic of the accumulator. Incorporating accumulators into the three-stage sigma-delta modulator yields Fig. 10. The topology of Fig. 10 is readily amenable to integration. The multiple modulator fractional-N control system reduces to a forward path of accumulators and a reverse path of differentiators.

III. Fractional Divider Implementation

An IC was conceived to implement all the digital functions of a PLL incorporating a multiple modulator fractional divider. The part is fabricated in a 1.5-μm, 5-V

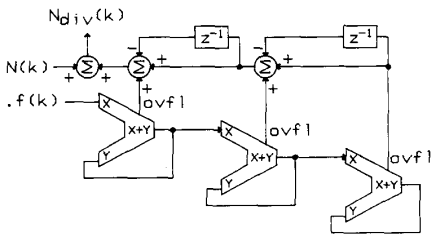

Fig. 10. Multiple modulator divider implemented with accumulators.

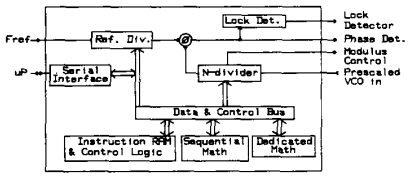

Fig. 11. Block diagram of the fractional-N IC.

CMOS process and packaged in a 44-pin plastic leaded chip carrier. The part dissipates 75 mW when clocked at 15 MHz.

Fig. 11 illustrates the overall block diagram of the IC. This diagram can be broken down into two distinct sections:

1) Basic Synthesizer
   a) N divider
   b) Phase Frequency Detector
   c) Reference Divider
   d) Out of Lock Detector
   e) Serial Interface
2) Computation and Control
   a) Sequential Math Section
   b) Dedicated Math Section
   c) Data Flow Control

Not shown in Fig. 11 but included on the IC, is circuitry to support FM inside the PLL bandwidth, synthesized sweep, and a general purpose 12-bit parallel data bus for control of external peripheral devices.

A. Basic Synthesizer

Although the basic synthesizer looks very much like the parts available from Motorola [11], Fujitsu [12], and others, significant differences exist, particularly in the N divider. Those who have built and tested fractional N PLL's know the importance of avoiding spurious coupling from the N divider, reference divider, and the fraction computation logic onto the edges presented to the phase detector. With this in mind, the following basic premise governed the architecture of the N divider and mathematical sections of the IC.

"Avoid spurious coupling of divider and computation events to the phase detector edges by restricting both to separate times within the PLL cycle."

This, coupled with the following two observations, resulted in the general PLL cycle requirements illustrated in Fig. 12.

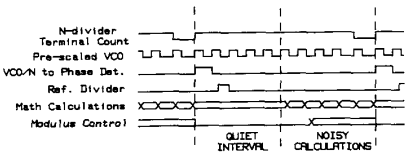

Fig. 12. Timing diagram of the basic PLL cycle.

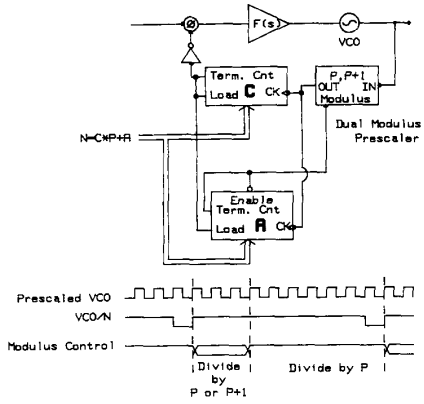

Fig. 13. Prescalar controller with modulus changes referenced to the beginning of the reference cycle.

a) To reduce the delay of FM, sweep, and other external requests, the requests should be sampled and their associated calculations executed at the last possible moment before the N-divider is reloaded.
b) The VCO/N edge placement must represent exactly the number of VCO cycles calculated by the sigma-delta modulators. No incidental PM can be allowed to modulate the VCO/N edge.

The start of the reference cycle is "quiet" and reserved for the phase detector edges. The last portion of the cycle is reserved for the noisy calculations and prescalar modulus control changes.

The N-divider controller is based on the well known dual modulus prescalar [13] technique. In a typical prescaler based divider, prescaler modulus changes are referred to the beginning of the reference cycle as illustrated in Fig. 13. However, unlike most dividers found in single chip synthesizers, the new IC references changes of the prescalar modulus to the end of the PLL reference cycle (Fig. 14) to facilitate time separation of phase detector edges and noisy computations. Instead of using two counters to generate prescalar modulus control, a counter and comparator are used. The Q outputs of the down counter are compared to the value stored in the modulus control register. Although other dual modulus dividers have been built, based on a single counter and comparators [14], they do not function to reference the modulus control changes to the end of the PLL cycle.

B. Computation and Control

Consider the implementation of three-modulator divider illustrated in Fig. 10. In addition let the desired

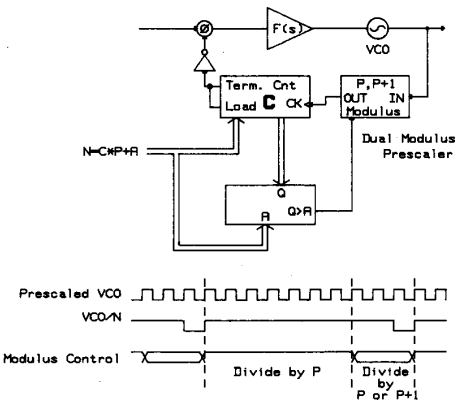

Fig. 14. Prescalar controller with modulus changes referenced to the end of the reference cycle.

fractional resolution require a 24-bit word width in each modulator and an N-value less than 4096. The major logic required to implement this is cataloged as follows:

1) 3 24-bit adders,
2) 4 24-bit registers,
3) 6 24-bit data paths,
4) 2 $1 - z^{-1}$ operators,
5) 1 12-bit adder,
6) 3 12-bit data paths.

This could be a large integration problem. Since multiple prescalar output cycles are available every PLL cycle, a sequential approach to the accumulations was chosen. This approach complicates IC control but saves considerable die area. The number of prescalar output cycles per PLL cycle are limited, so the small valued computations such as the $1 - z^{-1}$ operators are implemented in dedicated logic. The $1 - z^{-1}$ operators can be scaled, since their peak numeric value is bounded (i.e., $+1$, -1 for the third modulator section). This further reduces die requirements.

The control section, in addition to scheduling accumulations, is required to fetch dedicated computations into the sequential section and pass new values off to the N divider and peripherals used in FM [15] and sweep functions. The state machine required to implement the sequential math and control could have been implemented in PLA, ROM, or RAM. Cell-based RAM was selected for its obvious versatility as well as overall speed when compared to available cell-based ROM. The IC has a 16-instruction control RAM which must be programmed upon application of power to the part. RAM-based control hastened development of the part and its intended application because it was easy to reconfigure the IC for experimentation. The RAM-based control also provides flexibility to PLL designers who, with the IC, can program unique combinations of correction, specialized sweep, and FM or PM.

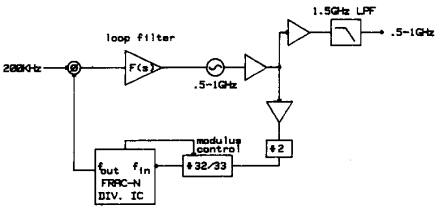

Fig. 15. 0.5–1-GHz fractional-N PLL.

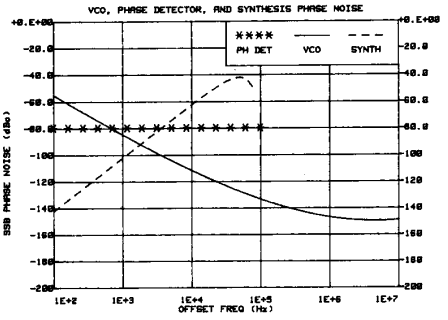

Fig. 16. Phase noise sources in the 0.5–1-GHz PLL.

IV. Complete Fractional-N Synthesis PLL

The new fractional-N divider was used to construct a 0.15–1-GHz PLL (Fig. 15). The divider IC was programmed to implement a 3-modulator interpolative divider. An external 32/33 prescalar was utilized in conjunction with the fractional-divider IC to implement the N-divider function. The prescaler is preceeded by a divide-by-2 because the 32/33 prescalar is not able to toggle at 1 GHz.

The VCO is a single band, 0.5–1-GHz, varactor tuned transistor oscillator. The loop f_{ref} is 200 KHz. In addition to the normal phase control objectives, the loop filter must also provide adequate rejection of the synthesis noise. The predicted synthesis noise is overlaid on a plot of the free-running VCO phase noise (Fig. 16) to determine the loop filter design parameters. The synthesis noise plotted in Fig. 16 is increased 6 dB over (14) because of the divide-by-2 prescaler between the VCO and the fractional divider circuit. Note how the fractional division error energy has been pushed away from the carrier. In this case, the error energy intersects the VCO phase noise at an offset greater than where the phase detector noise intersects the VCO phase noise. Notice also that the error energy rises at 40-dB/decade. For this application, the servo requirements were satisfied with a type II, second-order loop of approximately 750 Hz bandwidth. The filtering requirements were met by adding two additional real-axis poles (1.8 kHz, 3 kHz) to the loop filter.

The results of a phase noise measurement on the locked loop are given in Fig. 17. The fractional divider was programmed for a frequency offset of 2 kHz. None of the traditional 2 kHz (and multiples thereof) spurs are present.

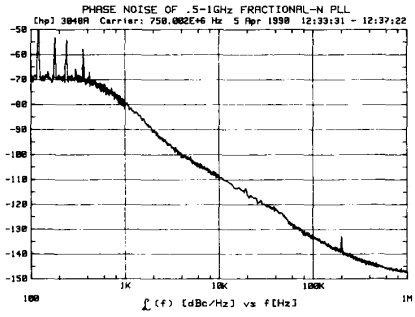

Fig. 17. Measured phase noise of the PLL.

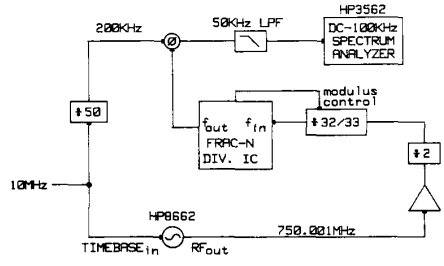

Fig. 18. Apparatus to measure synthesis noise of new fractional-N technique.

Equation (14) was verified with the apparatus of Fig. 18. $N.f$ was chosen to divide the applied RF (750.001 MHz) down to the reference frequency (200 KHz). The baseband noise recorded on the spectrum analyzer was adjusted by the reciprocal of the low-pass filter gain, which was measured separately. Results are given in Fig. 19. The noise floor of the measurement system was approximately -80 dBc.

The mathematical prediction of synthesis error energy (14) relies on a uniform quantization noise model. The reader may rightly wonder if this is justifiable. Several authors [9], [10] have addressed the exact output spectra of a sigma–delta modulator but have limited their analyses to single-stage modulators. For single-stage modulators, the output spectra is strongly dependent on the dc input to the modulator and a quantization noise model is not appropriate [9]. Heuristically, higher order coders decrease the correlation between the input signal and the quantization error [10], permitting a quantization noise model.

We found the three-stage ΣDM to comply with the uniform noise model if the first accumulator experiences activity in, or near, the LSB bit position. Inputs which excite only bits near the MSB position, such as $.f = 0.5$, 0.75, 0.25, etc., result in a limit cycle of short duration and insufficient randomness to decorrelate the quantization error. Fortunately, it is easy to always add 1 LSB to the desired frequency offset if the desired $.f$ does not already have the LSB set. Because the accumulator length is so large, a 1-LSB frequency error is easily tolerable. In our test circuit utilizing a 24-bit accumulator, 1 LSB corresponds to 0.0238 Hz, or 4.77×10^{-5} ppm worst case.

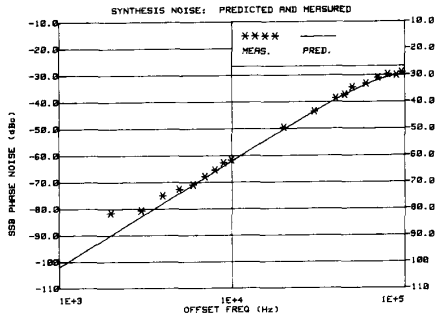

Fig. 19. Theoretical and measured synthesis noise.

V. Summary

A new technique for fractional-N synthesis has been developed. The technique causes error energy to be converted into colored noise instead of discrete spurious tones. The noise energy is suppressed at small offsets, allowing the remaining error to be rejected by simple filtering. The technique provides a tremendous advantage in cost, size, and complexity over traditional fractional-N synthesis techniques which utilize error correction. The prototype circuit achieved a 2.5 times reduction in size with respect to previous generation fractional-N synthesis circuits.

Acknowledgment

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