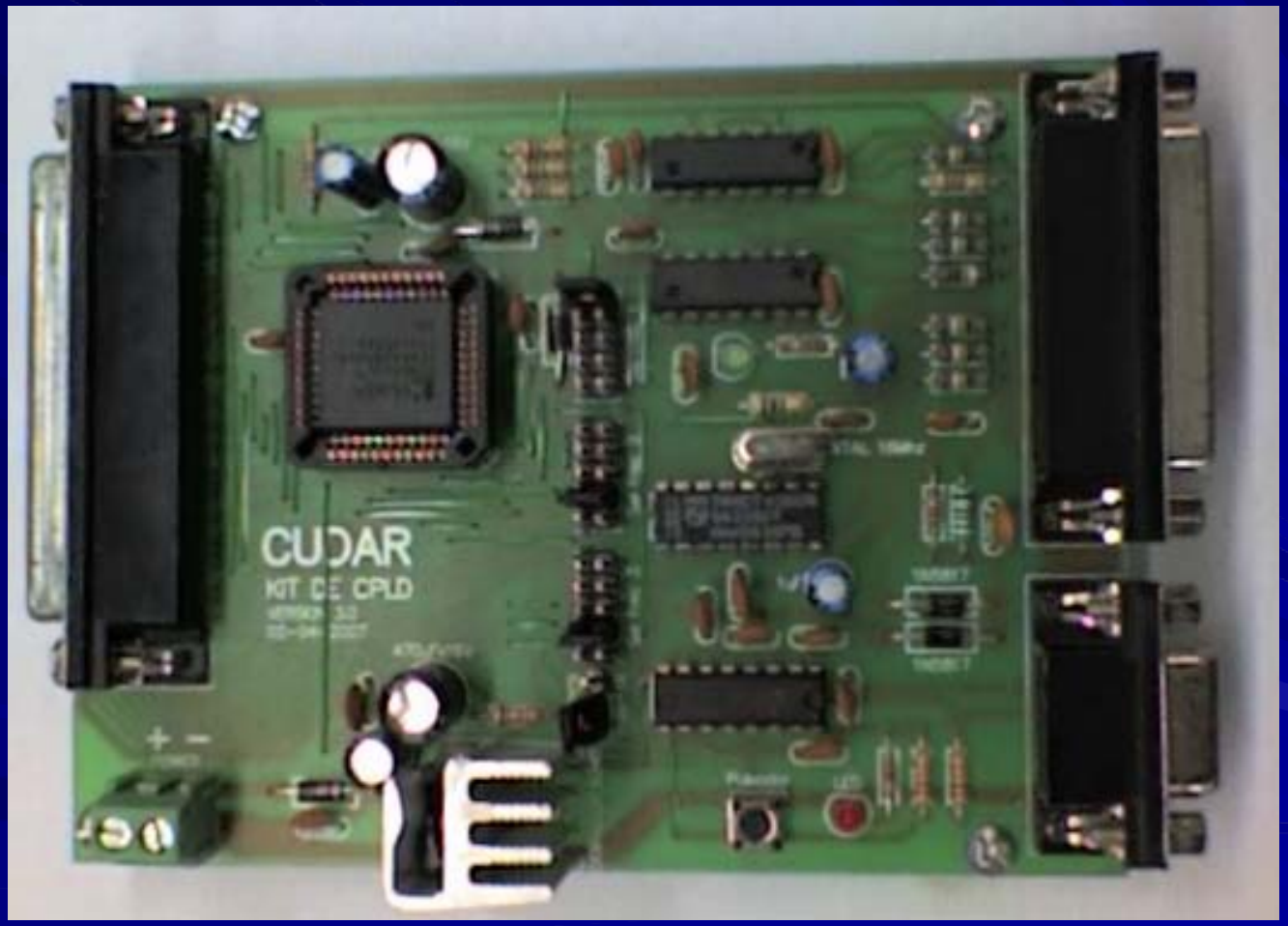
TECNICAS DIGITALES I

KIT CPLD

XC9572XL

Kit de desarrollo



Características Electricas

Absolute Maximum Ratings(2)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 5.5	V
T_{STG}	Storage temperature (ambient)(3)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. External I/O voltage may not exceed V_{CCINT} by 4.0V.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb-free packages, see XAPP427.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to 70°C	3.0	3.6	V
		Industrial T_A = –40°C to +85°C	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.80	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCIO}	V

Reprogramación y Condiciones de operación

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{CCIO} = Max; V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} Min < V_{IN} < 5.5V	-	±50	µA
C_{IN}	I/O capacitance	V_{IN} = GND; f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_{IN} = GND, No load; f = 1.0 MHz	20 (Typical)		mA

Arquitectura del CPLD

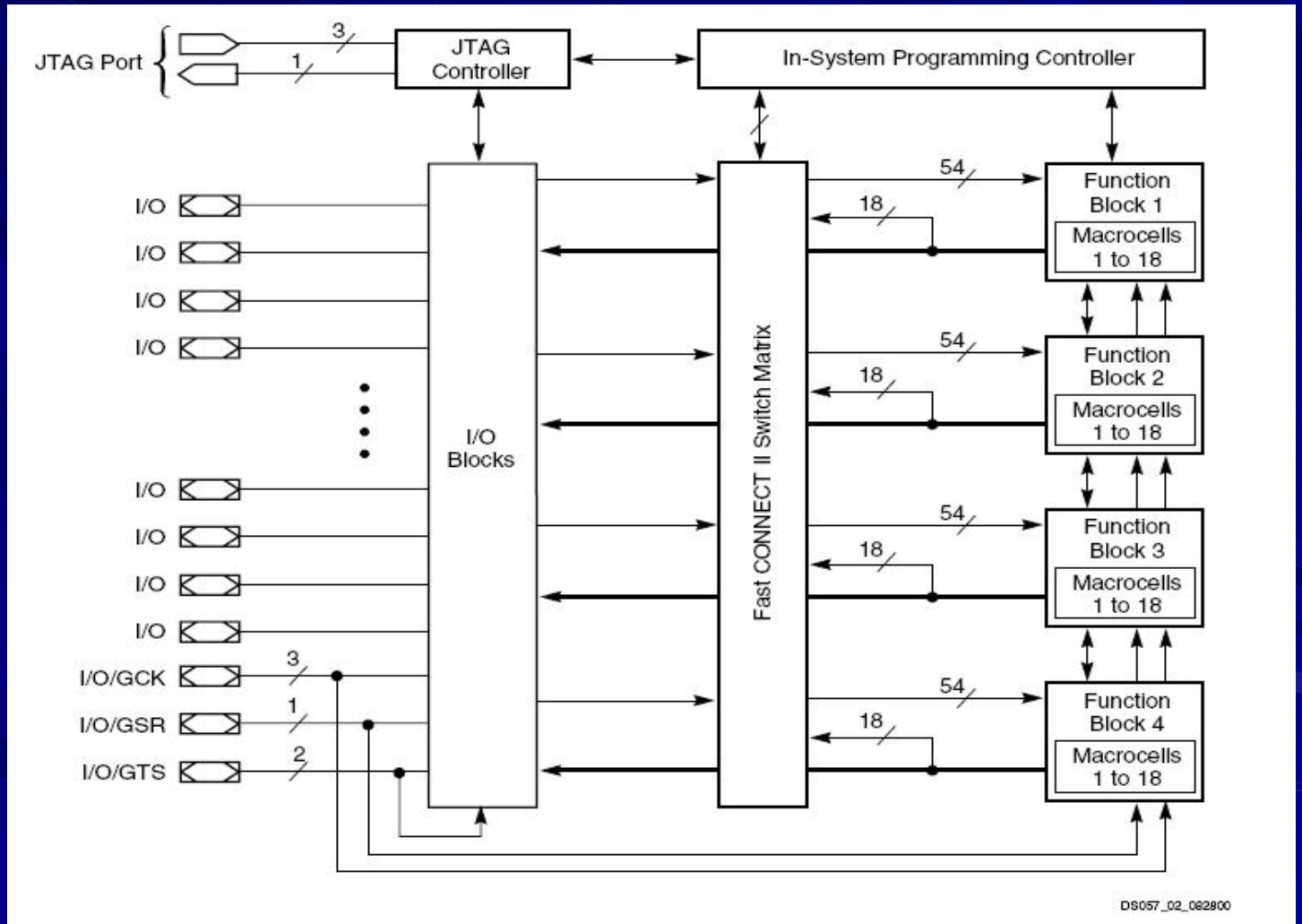


Figure 2: **XC9572XL Architecture**

Bloque Funcional

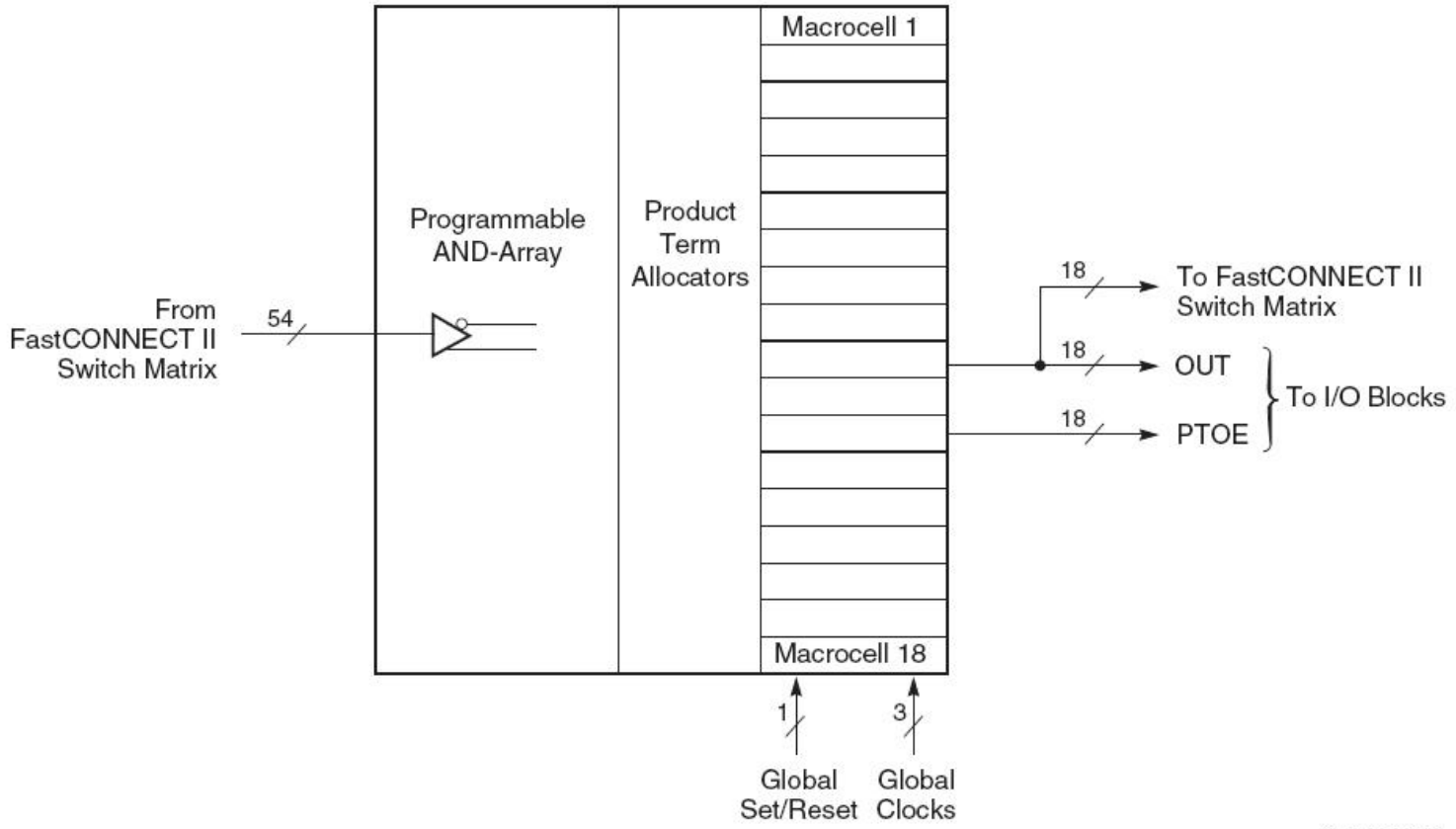


Figure 2: **XC9500XL Function Block**

Macrocelda

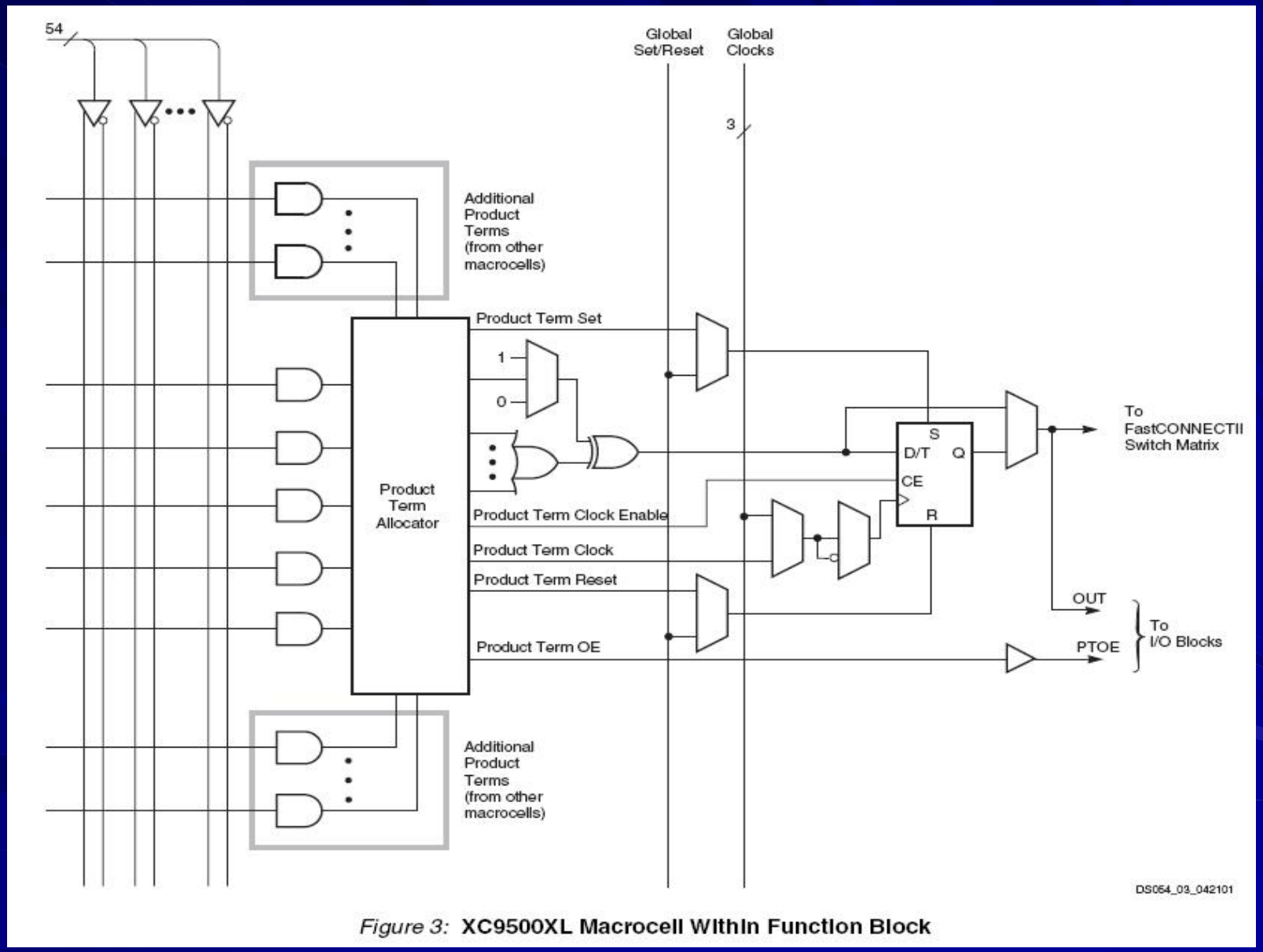


Figure 3: **XC9500XL Macrocell Within Function Block**

Circuito SET-RESET

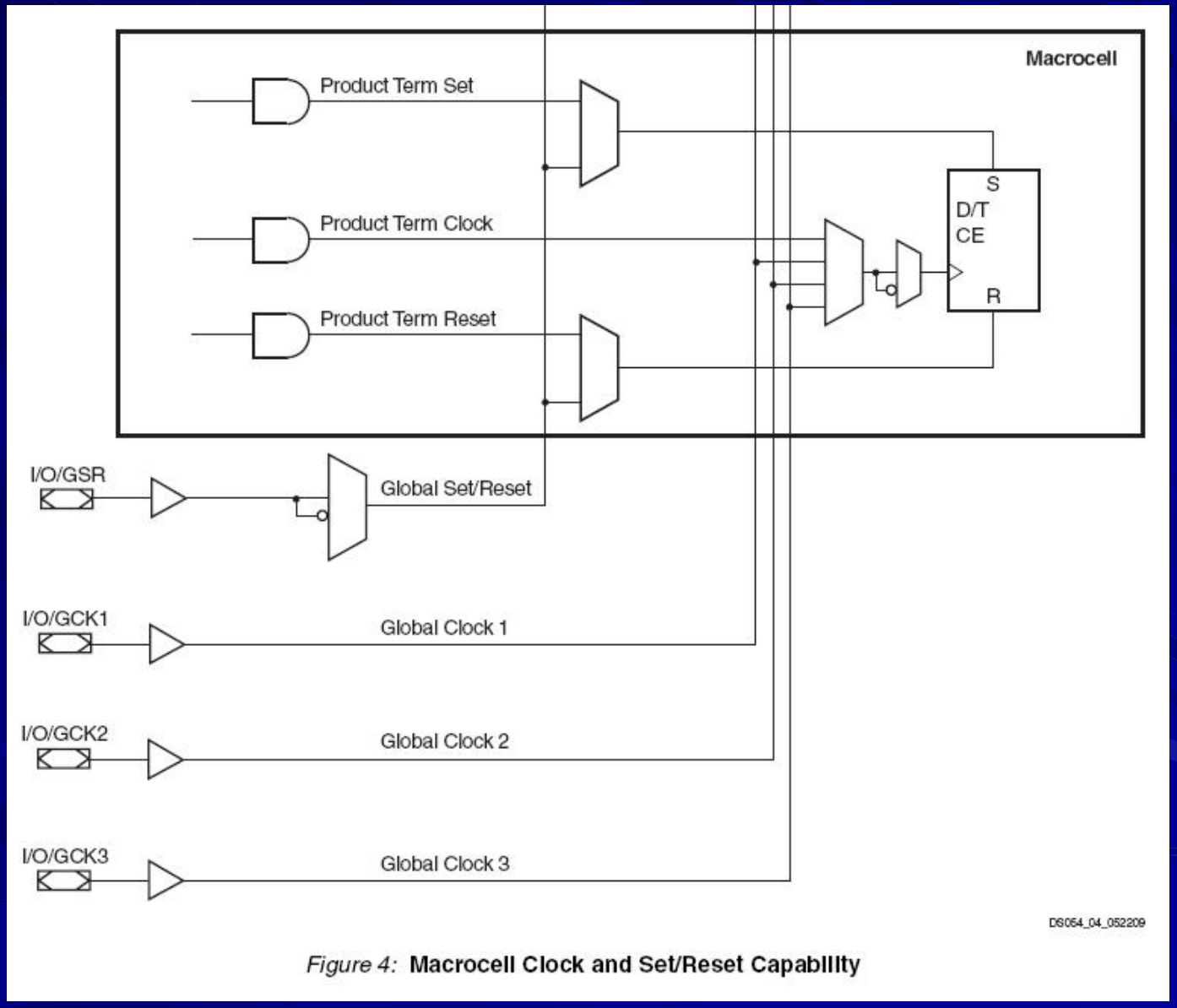
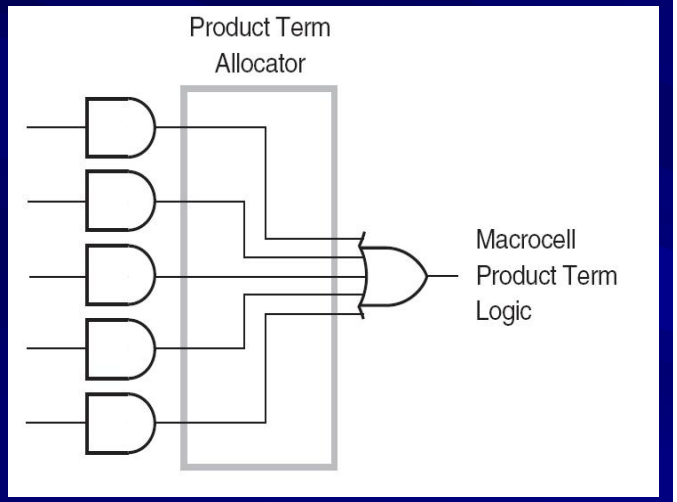


Figure 4: **Macrocell Clock and Set/Reset Capability**



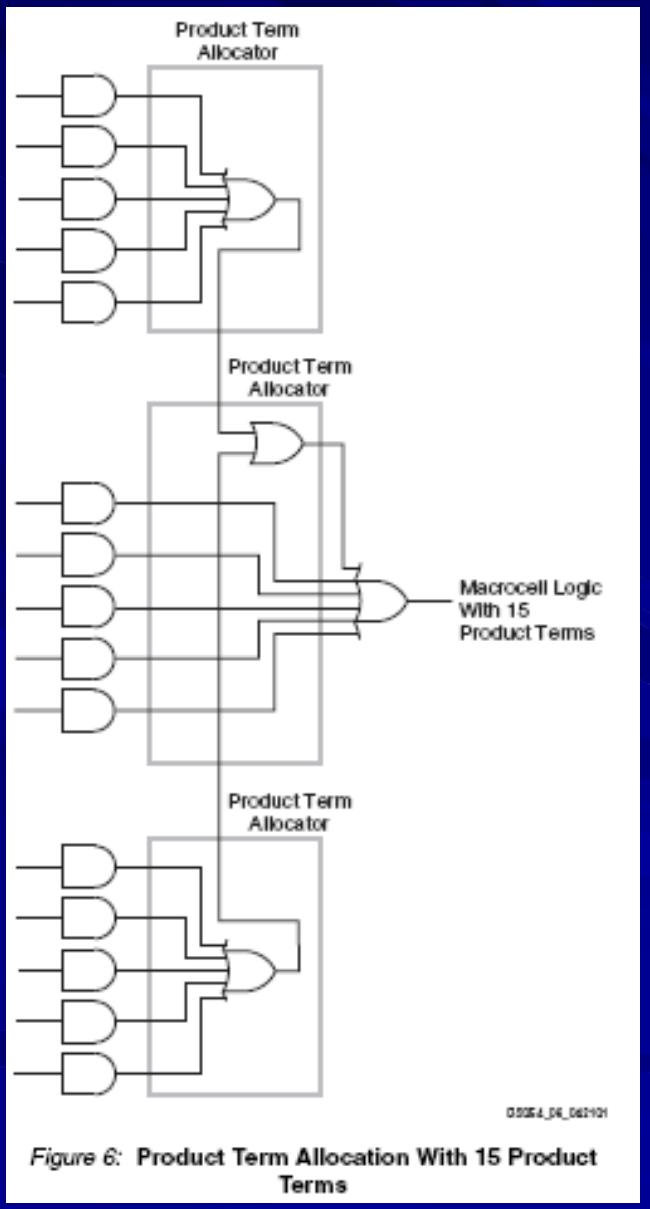


Figure 6: **Product Term Allocation With 15 Product Terms**

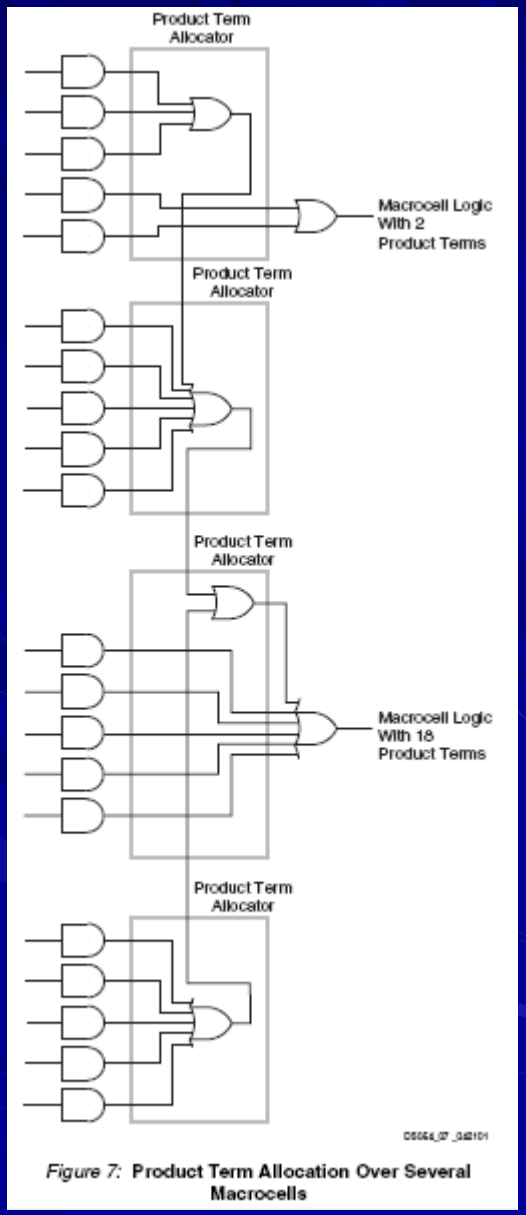


Figure 7: **Product Term Allocation Over Several Macrocells**

Lógica

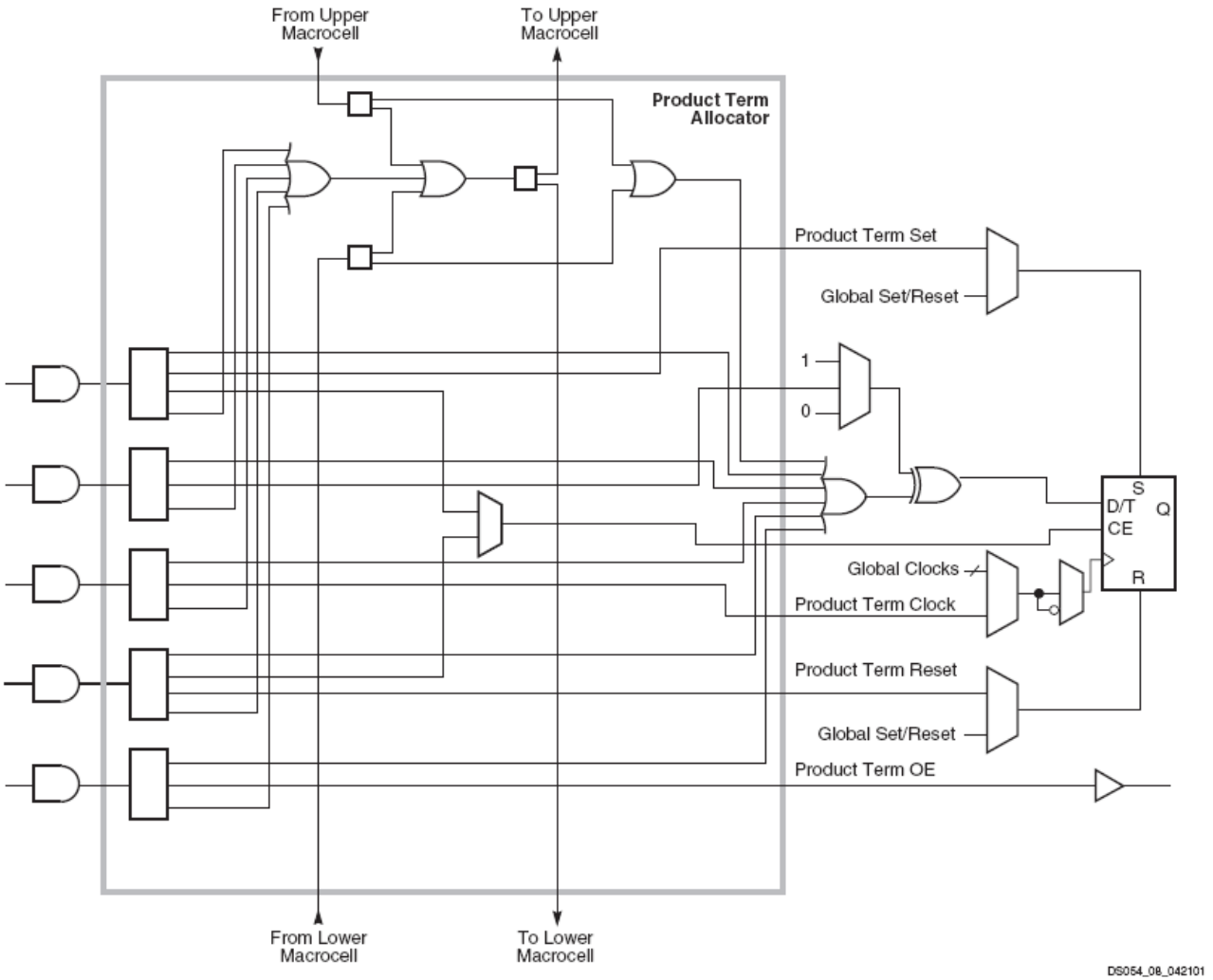


Figure 8: **Product Term Allocator Logic**

Matriz de interconexión

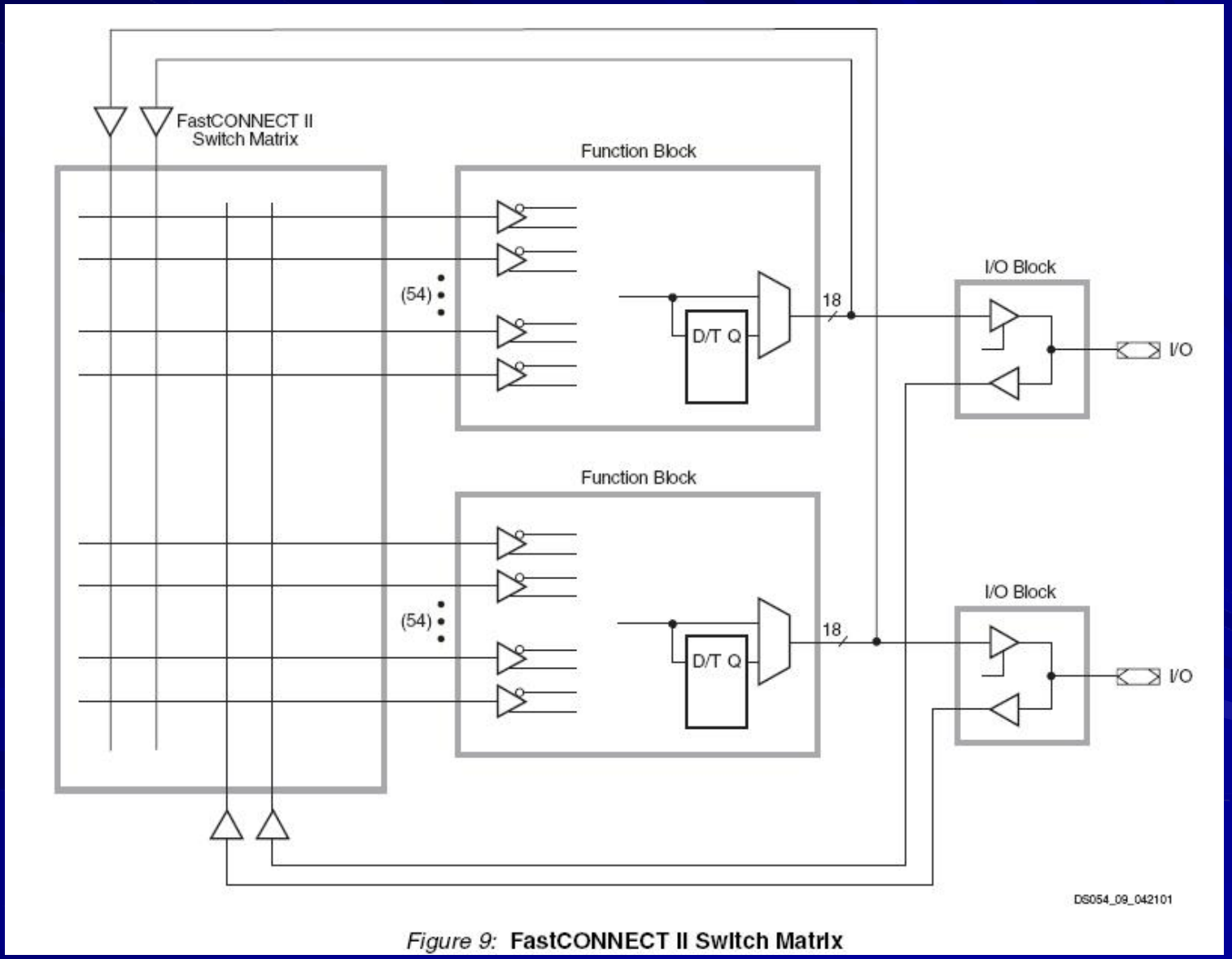


Figure 9: **FastCONNECT II Switch Matrix**

Bloque de I/O

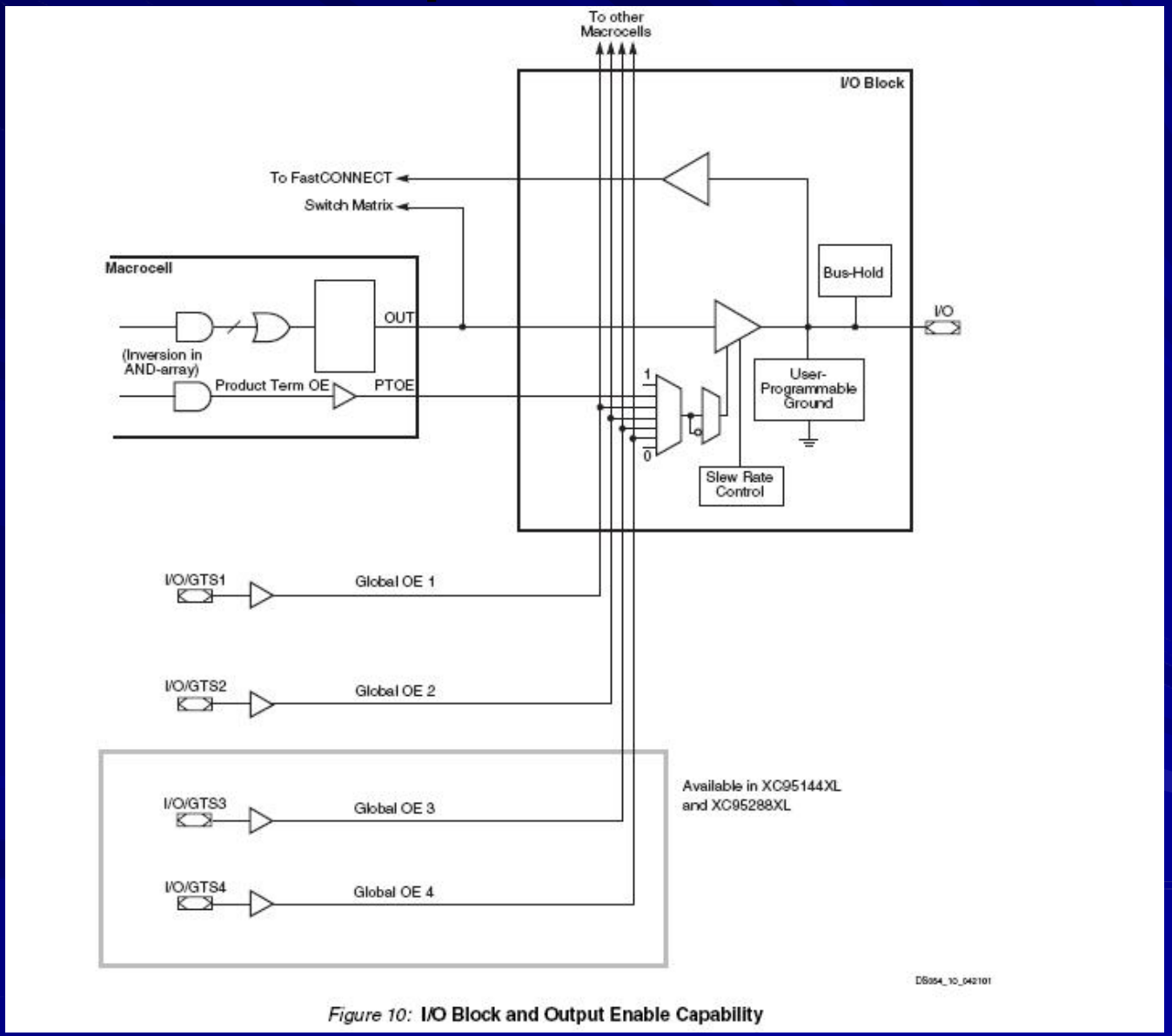
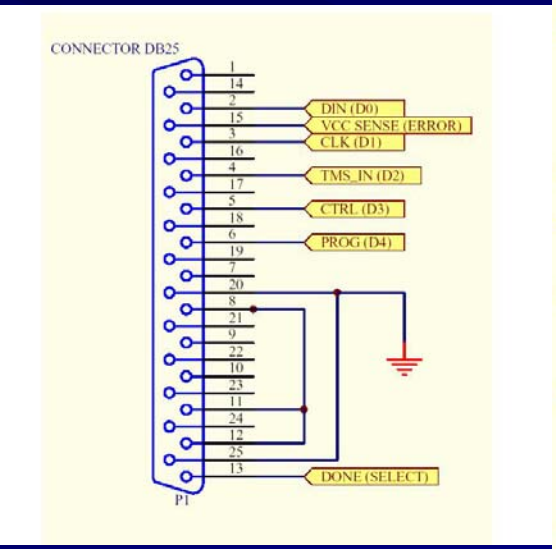
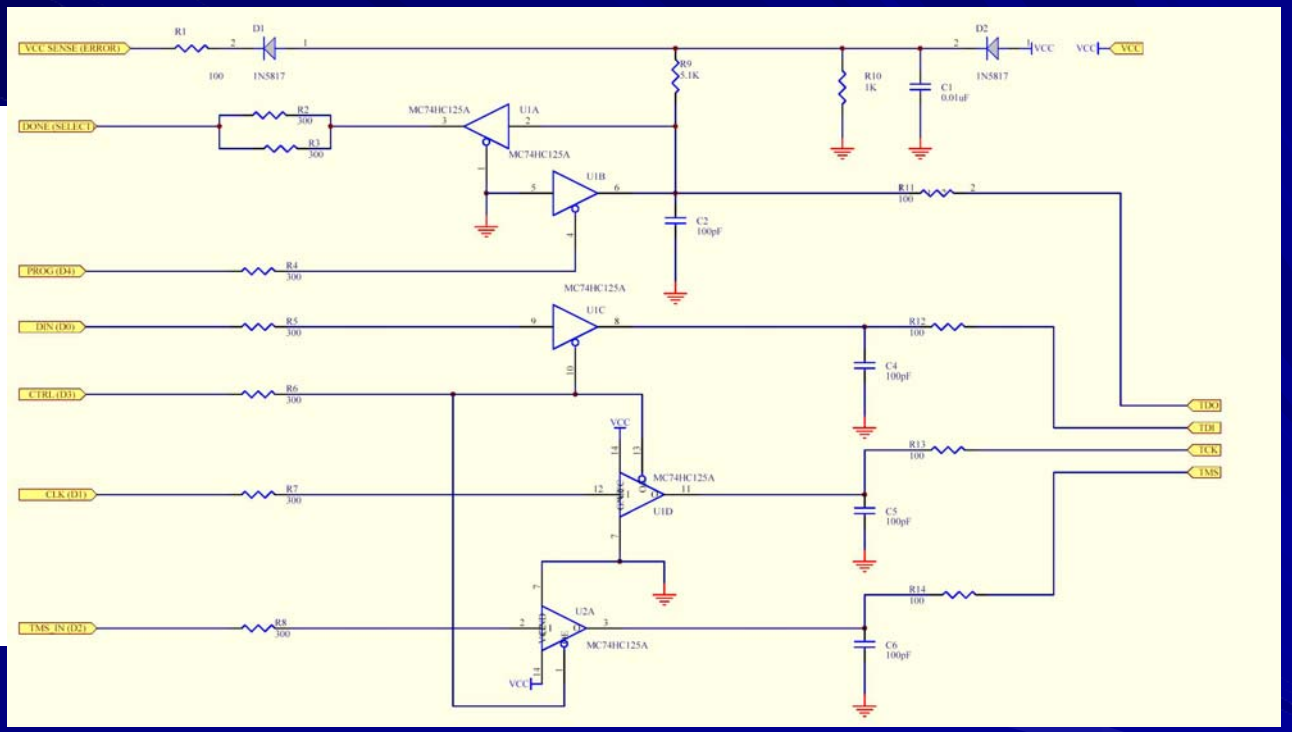


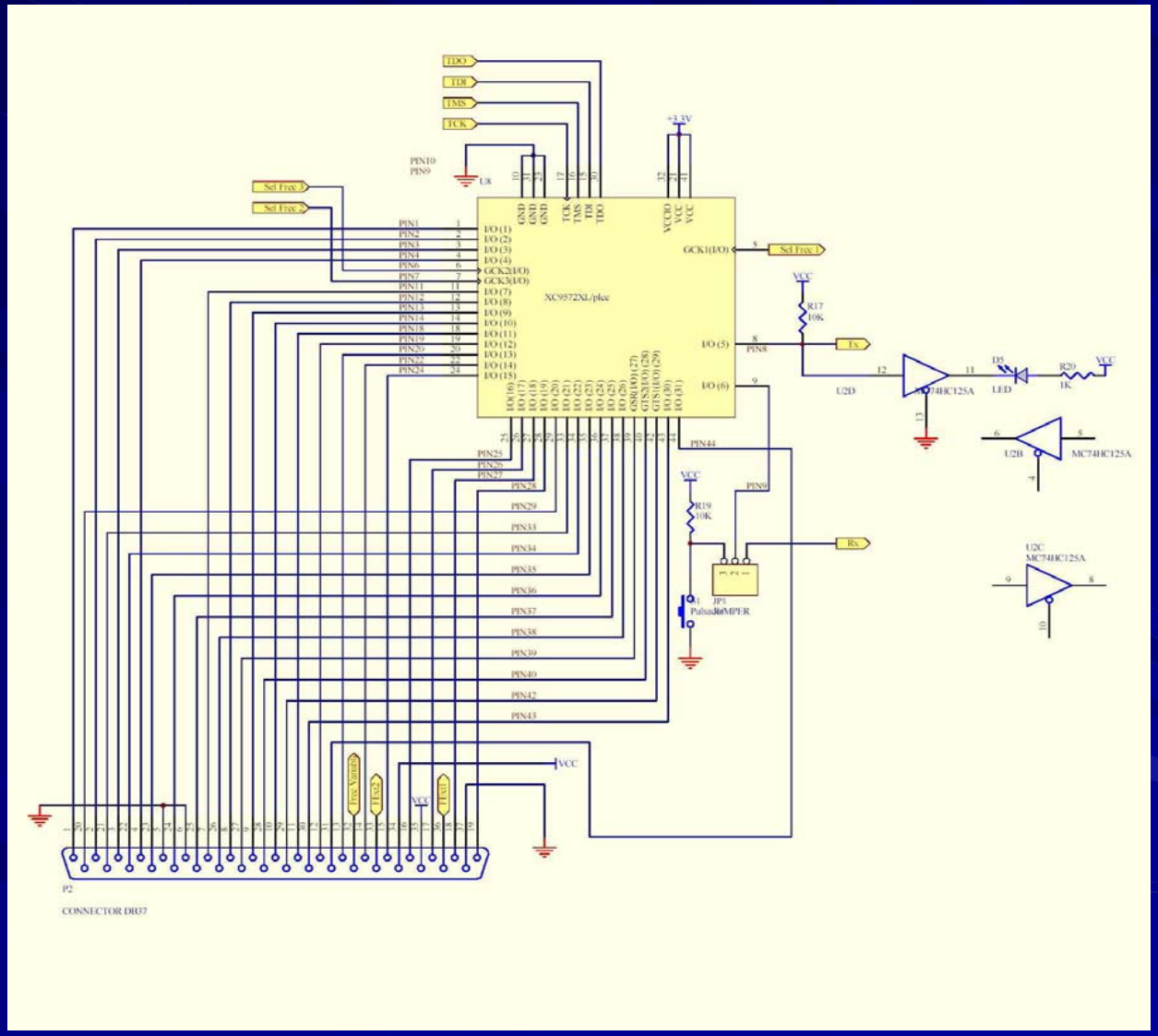
Figure 10: **I/O Block and Output Enable Capability**

Puerto de grabación

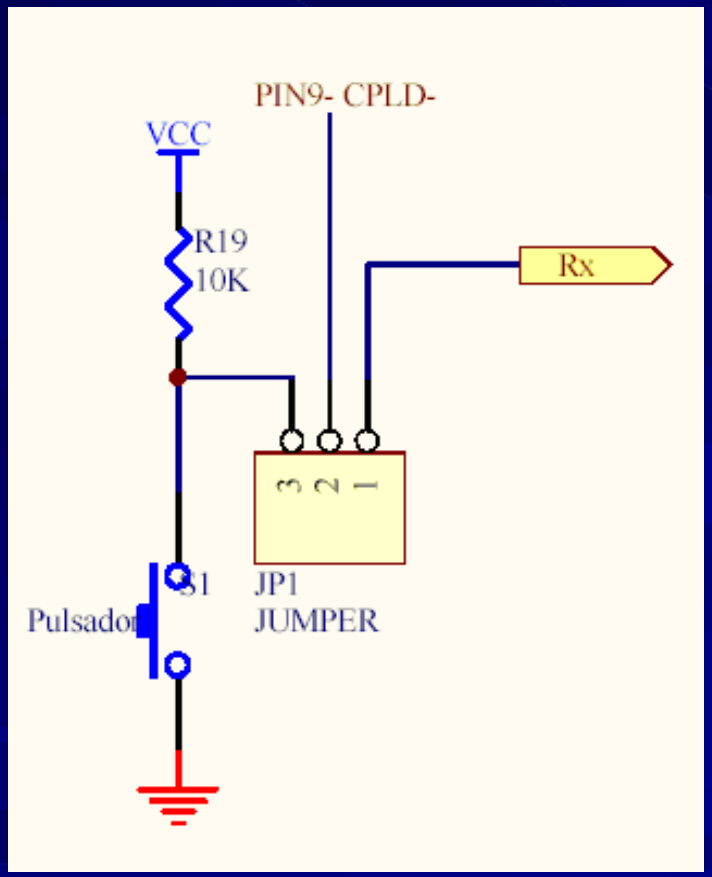


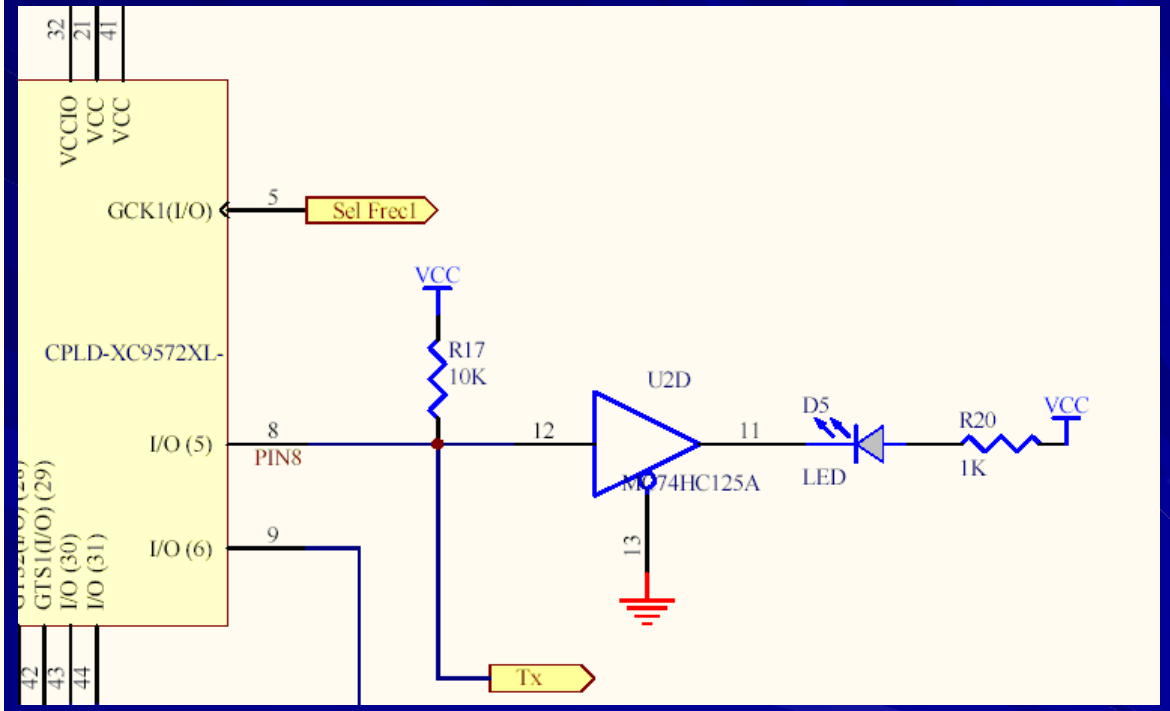


Circuito CPLD



Circuito de Prueba

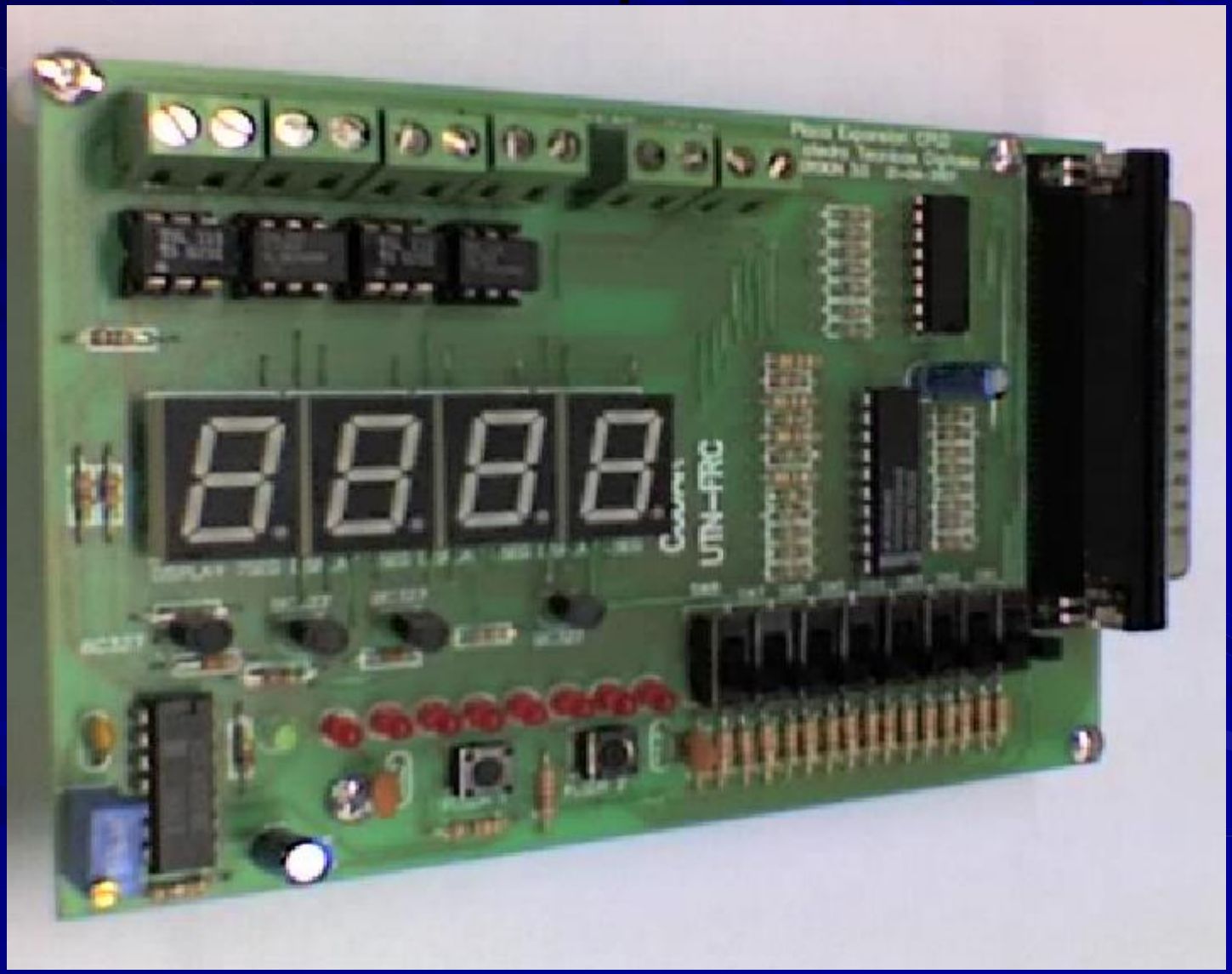




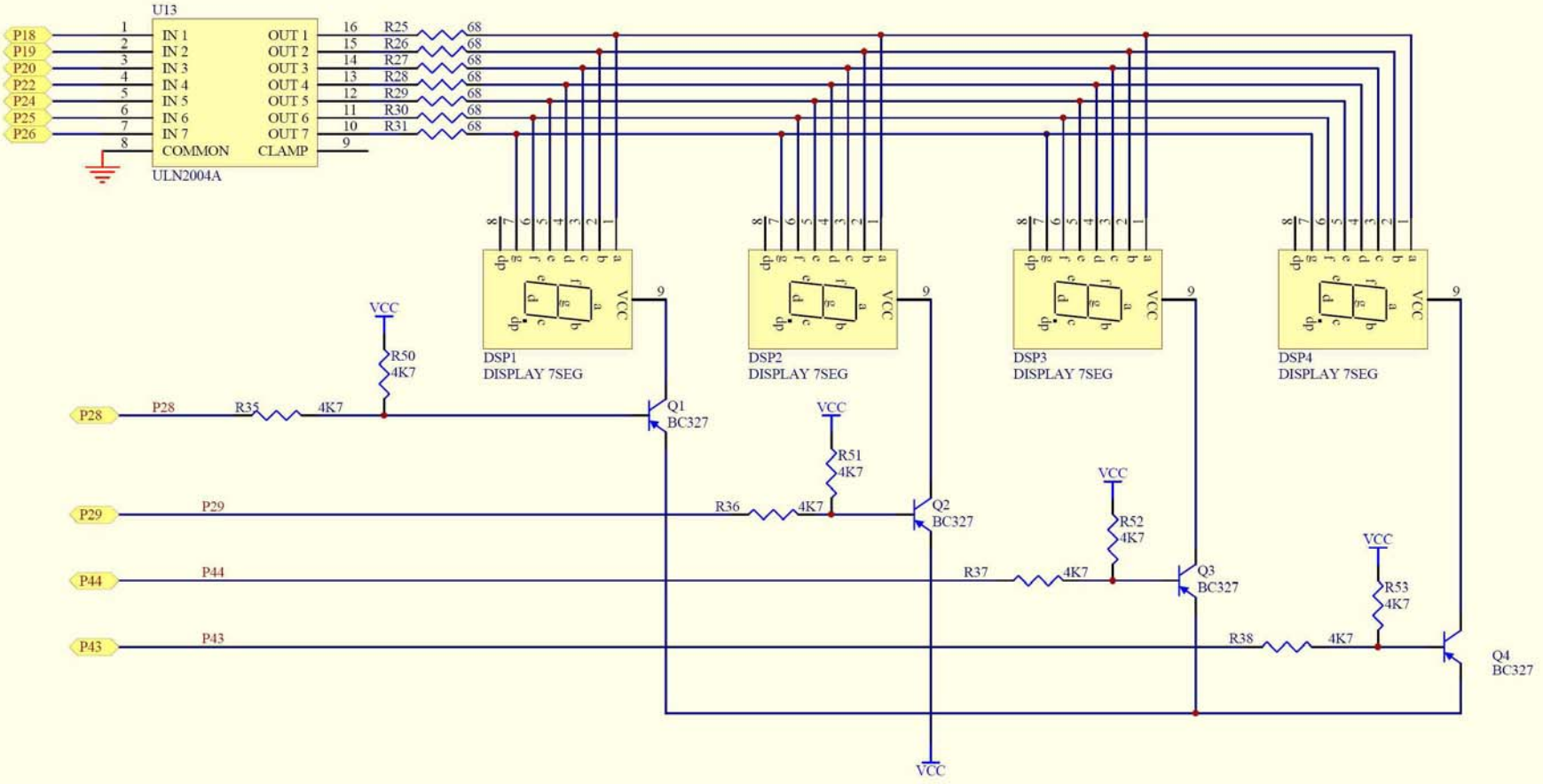
UCF

```
#PACE: Start of Constraints generated by PACE
#PACE: Start of PACE I/O Pin Assignments
NET "clk1"  LOC = "P5"  ;
NET "clk2"  LOC = "P7"  ;
NET "clk3"  LOC = "P6"  ;
NET "led_tx_prog"  LOC = "P8"  ;
NET "leds<0>"  LOC = "P1"  ;
NET "leds<1>"  LOC = "P2"  ;
NET "leds<2>"  LOC = "P3"  ;
NET "leds<3>"  LOC = "P4"  ;
NET "leds<4>"  LOC = "P11"  ;
NET "leds<5>"  LOC = "P12"  ;
NET "leds<6>"  LOC = "P13"  ;
NET "leds<7>"  LOC = "P14"  ;
#NET "pulsador1" LOC = "P27" ;
#NET "pulsador2" LOC = "P33" ;
NET "pulsador_rx_prog"  LOC = "P9"  ;
```

Placa Expansión



Display


U13
P18
P19
P20
P22
P24
P25
P26
IN 1
IN 2
IN 3
IN 4
IN 5
IN 6
IN 7
COMMON
OUT 1
OUT 2
OUT 3
OUT 4
OUT 5
OUT 6
OUT 7
CLAMP
ULN2004A
R25
R26
R27
R28
R29
R30
R31
68
DSP1
DSP2
DSP3
DSP4
DISPLAY 7SEG
VCC
R50
4K7
R51
R52
R53
P28
P29
P44
P43
R35
R36
R37
R38
Q1
Q2
Q3
Q4
BC327