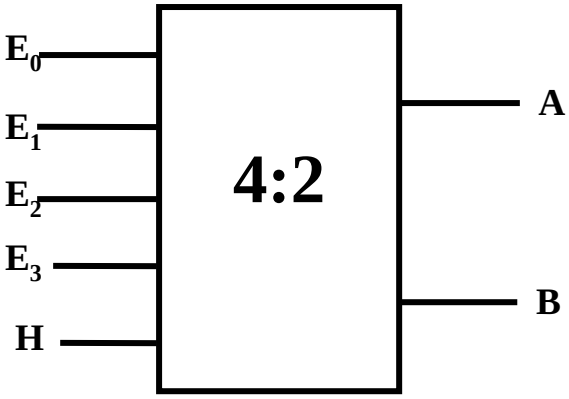
CODIFICADORES

.SIN PRIORIDAD

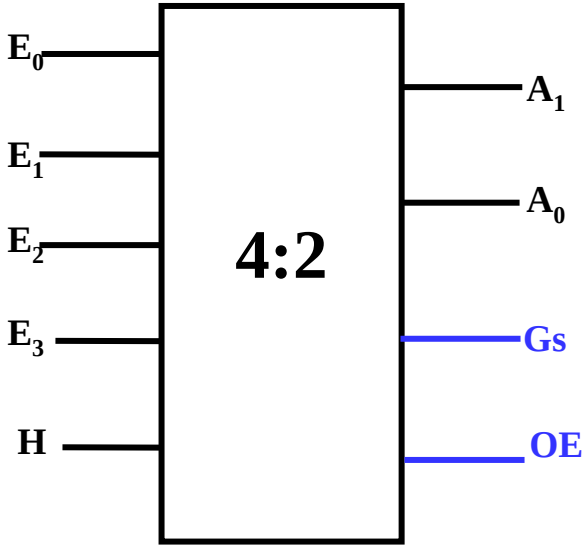


H	E_i	A	B
0	X	0	0
1	E_0	0	0
1	E_1	0	1
1	E_2	1	0
1	E_3	1	1

$$A = H(E_2 + E_3)$$

$$B = H(E_1 + E_3)$$

.CON PRIORIDAD



H	E_0	E_1	E_2	E_3	A_1	A_0	Gs	OE
0	x	x	x	x	0	0	0	0
1	0	0	0	0	0	0	0	1
1	x	x	x	1	1	1	1	0
1	x	x	1	0	1	0	1	0
1	x	1	0	0	0	1	1	0
1	1	0	0	0	0	0	1	0

MODELO VHDL

ENTRADAS				SALIDAS		
w3	w2	w1	w0	y1	y0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	x	x	x	1	1	1

W0 : **la mas baja prioridad**

W3 : la mas alta prioridad

d : don’t care

```
LIBRARY ieee;
USE ieee.std_logic_1164.all ;

ENTITY priority IS
        PORT ( w    : IN    STD_LOGIC_VECTOR(3 DOWNTO 0) ;
               y    : OUT  STD_LOGIC- _VECTOR(1 DOWNTO 0) ;
               z    : OUT  STD_LOGIC ) ;
END priority ;

ARCHITECTURE Behavior OF priority IS
BEGIN
    y <=  “11”  WHEN w(3) = ‘1’ ELSE,
          “10”  WHEN w(2) = ‘1’ ELSE,
          “01”  WHEN w(1) = ‘1’ ELSE,
          “00” ;

    z <= ‘0’ WHEN w = “0000” ELSE ‘1’ ;
END Behavior ;
```