VHDL

STD_LOGIC
STD_LOGIC_VECTOR
SIGNAL
WITH – SELECT
Conversor de códigos

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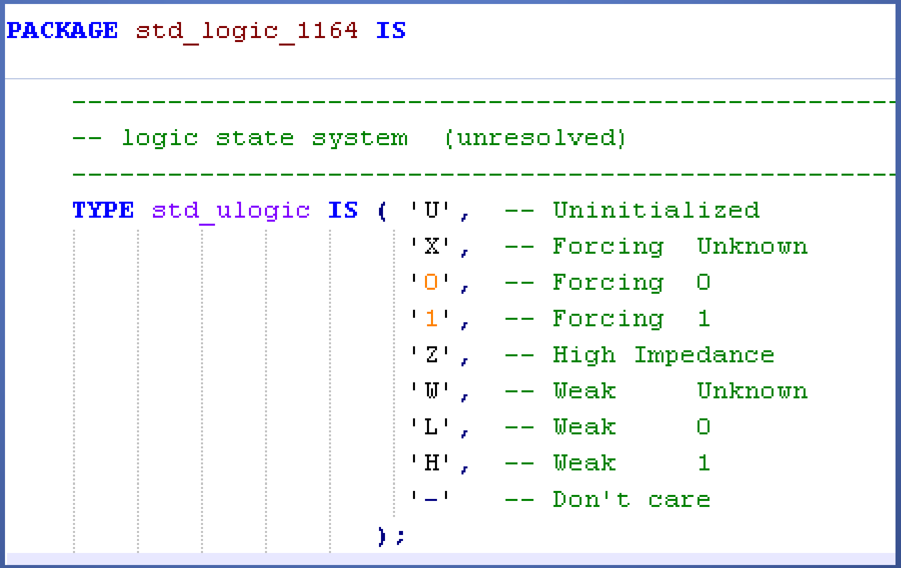
VHDL STD_LOGIC

IEEE 1164

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

STD_LOGIC

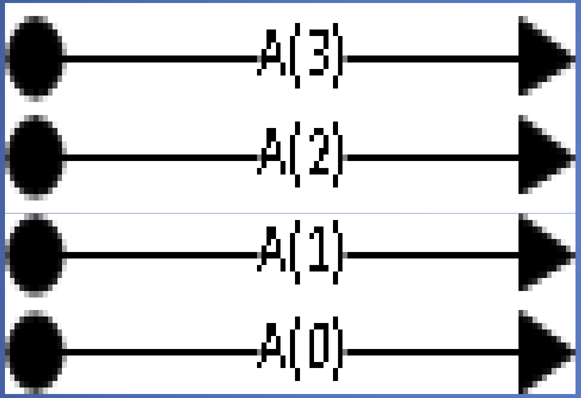


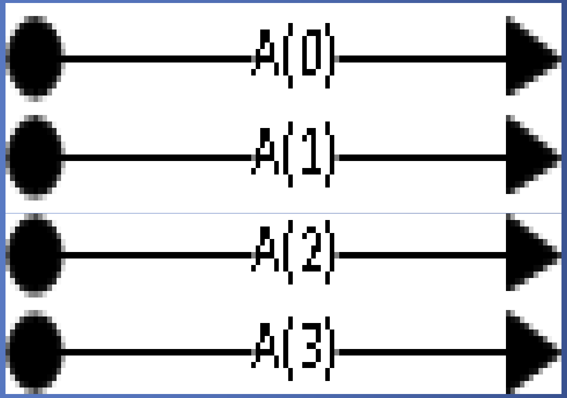
```
PACKAGE std_logic_1164 IS

    -------------------------------------------------------------------
    -- logic state system  (unresolved)
    -------------------------------------------------------------------
    TYPE std_ulogic IS ( 'U',  -- Uninitialized
                         'X',  -- Forcing  Unknown
                         '0',  -- Forcing  0
                         '1',  -- Forcing  1
                         'Z',  -- High Impedance
                         'W',  -- Weak     Unknown
                         'L',  -- Weak     0
                         'H',  -- Weak     1
                         '-'   -- Don't care
                       );
```

VHDL STD_LOGIC

STD_LOGIC_VECTOR

A : std_logic_vector(3 downto 0) | A : std_logic_vector(0 to 3)





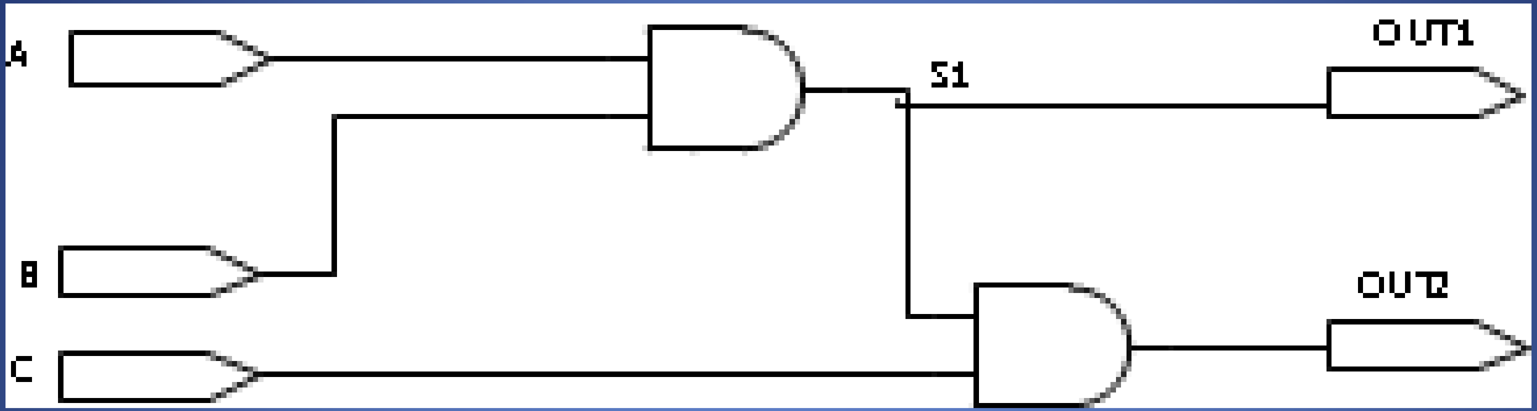
A(0) <=‘1’;

dato<=A(0) & A1 (3) & A1(5) ; -- Concatenación

VHDL SIGNALS

- Signals:
    - Se declaran dentro de la arquitectura.
    - Tienen las mismas propiedades que los puertos.
    - No salen fuera de la arquitectura.
    - Son cables y señales internas del dispositivo.
    - Se asignan igual que los puertos.
    - Son bidireccionales.
- Declaración
- <nombre>: tipo;
- D : std_logic;
- D2: std_logic_vector(0 to 10);
- D3. std_logic_vector(10 downto 0)

VHDL SIGNALS



```
Entity compuerta is
   Port ( A : in  STD_LOGIC;
             B: STD_LOGIC;
             C: STD_LOGIC;
             OUT1 : OUT std_logic;
             OUT2. OUT std_logic);
end compuerta;
```

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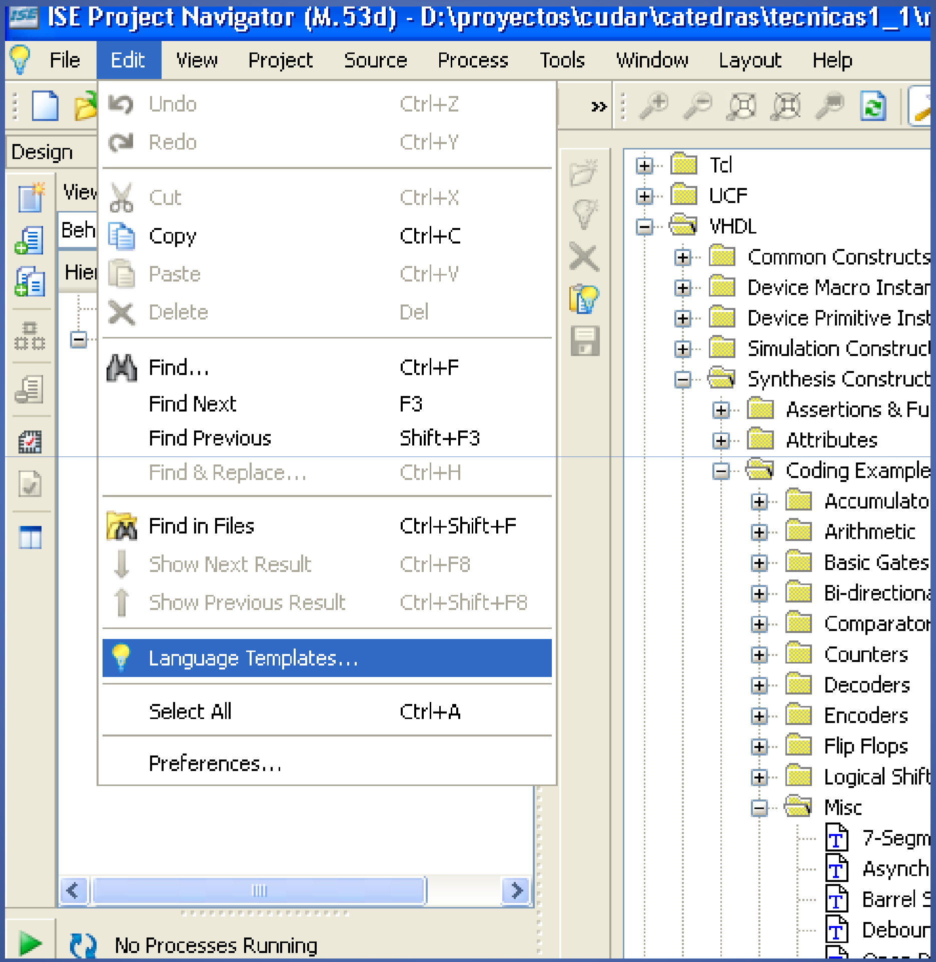
VHDL SIGNALS

```
architecture Behavioral of compuerta is
Signal S1: std_logic;
begin
out1<=S1;
S1<= A and B;
OUT2<=  S1 and C;
end Behavioral;
```

VHDL – ISE TEMPLATES



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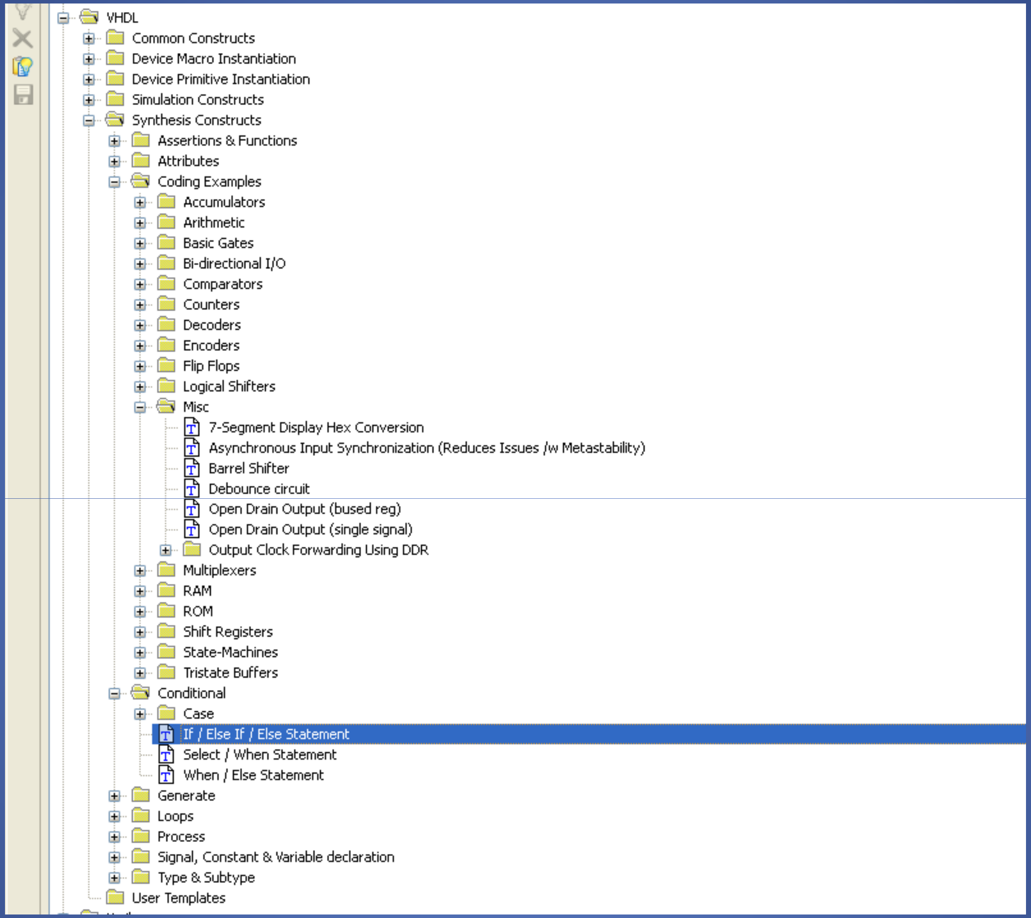
VHDL – ISE TEMPLATES



- VHDL
  - Common Constructs
  - Device Macro Instantiation
  - Device Primitive Instantiation
  - Simulation Constructs
  - Synthesis Constructs
    - Assertions & Functions
    - Attributes
    - Coding Examples
      - Accumulators
      - Arithmetic
      - Basic Gates
      - Bi-directional I/O
      - Comparators
      - Counters
      - Decoders
      - Encoders
      - Flip Flops
      - Logical Shifters
      - Misc
        - 7-Segment Display Hex Conversion
        - Asynchronous Input Synchronization (Reduces Issues /w Metastability)
        - Barrel Shifter
        - Debounce circuit
        - Open Drain Output (bused reg)
        - Open Drain Output (single signal)
        - Output Clock Forwarding Using DDR
      - Multiplexers
      - RAM
      - ROM
      - Shift Registers
      - State-Machines
      - Tristate Buffers
    - Conditional
      - Case
      - If / Else If / Else Statement
      - Select / When Statement
      - When / Else Statement
    - Generate
    - Loops
    - Process
    - Signal, Constant & Variable declaration
    - Type & Subtype
  - User Templates

TEMPLATE

```
with <choice_expression> select
   <name> <= <expression> when <choices>,
         <expression> when <choices>,
         <expression> when others;
```

TEMPLATE HEX-7SEG

```
with HEX select
 LED<= "1111001" when "0001",   --1
      "0100100" when "0010",   --2
      "0110000" when "0011",   --3
      "0011001" when "0100",   --4
      "0010010" when "0101",   --5
      "0000010" when "0110",   --6
      "1111000" when "0111",   --7
      "0000000" when "1000",   --8
      "0010000" when "1001",   --9
      "0001000" when "1010",   --A
      "0000011" when "1011",   --b
      "1000110" when "1100",   --C
      "0100001" when "1101",   --d
      "0000110" when "1110",   --E
      "0001110" when "1111",   --F
      "1000000" when others;   --0
```

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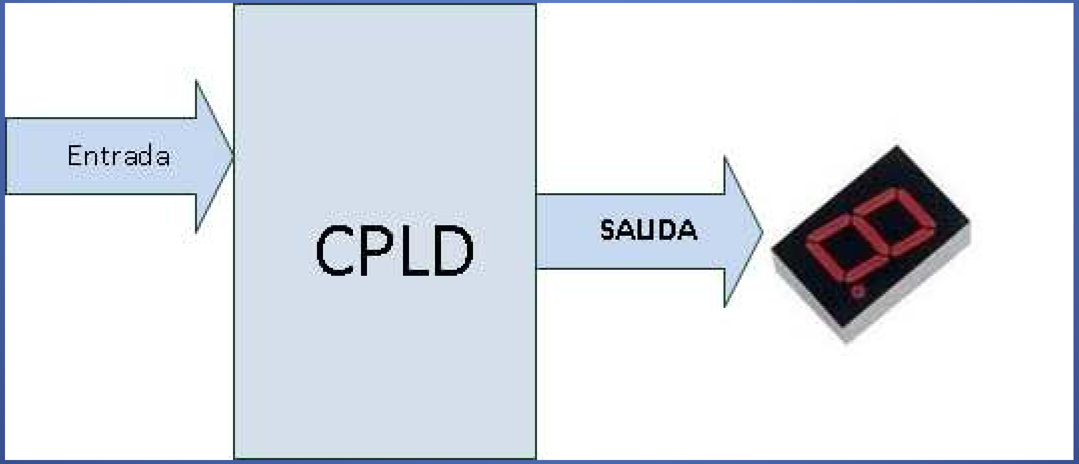
Entidad

```
entity bcd_7segment is
   Port ( Entrada : in  STD_LOGIC_VECTOR (3 downto 0);
          Salida : out  STD_LOGIC_VECTOR (6 downto 0));
end bcd_7segment;
```



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Arquitectura

```
architecture Behavioral of bcd_7segment is

begin
   with Entrada SELect
  Salida<= "1111001" when "0001",  --1
       "0100100" when "0010",   --2
       "0110000" when "0011",   --3
       "0011001" when "0100",   --4
       "0010010" when "0101",   --5
       "0000010" when "0110",   --6
       "1111000" when "0111",   --7
       "0000000" when "1000",   --8
       "0010000" when "1001",   --9
        "1000000" when others;   --0
end Behavioral;
```

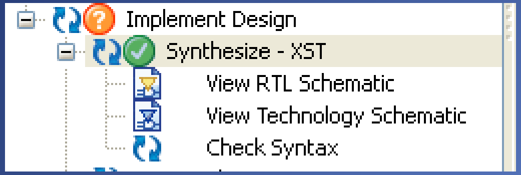
when - else

```
<name> <= <expression> when <condition> else
        <expression> when <condition> else
        <expression>;
```

Arquitectura

```
architecture Behavioral of bcd_7segment is
begin
        Salida<= "1111001" when Entrada="0001" else  --1
            "0100100" when Entrada="0010" else   --2
            "0110000" when Entrada="0011" else --3
            "0011001" when Entrada="0100" else  --4
            "0010010" when Entrada="0101" else  --5
            "0000010" when Entrada="0110" else  --6
            "1111000" when Entrada="0111" else  --7
            "0000000" when Entrada="1000" else   --8
            "0010000" when Entrada="1001" else   --9
            "1000000" ;   --0
end Behavioral;
```

Rtl schematic



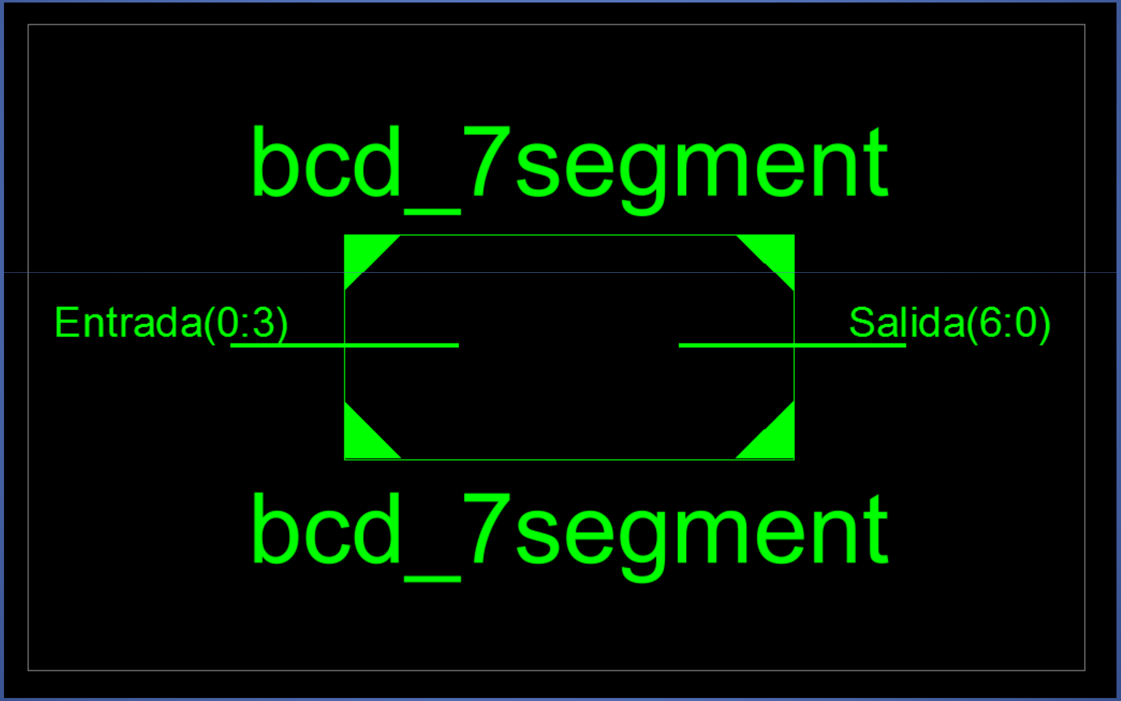
Implement Design

Synthesize - XST

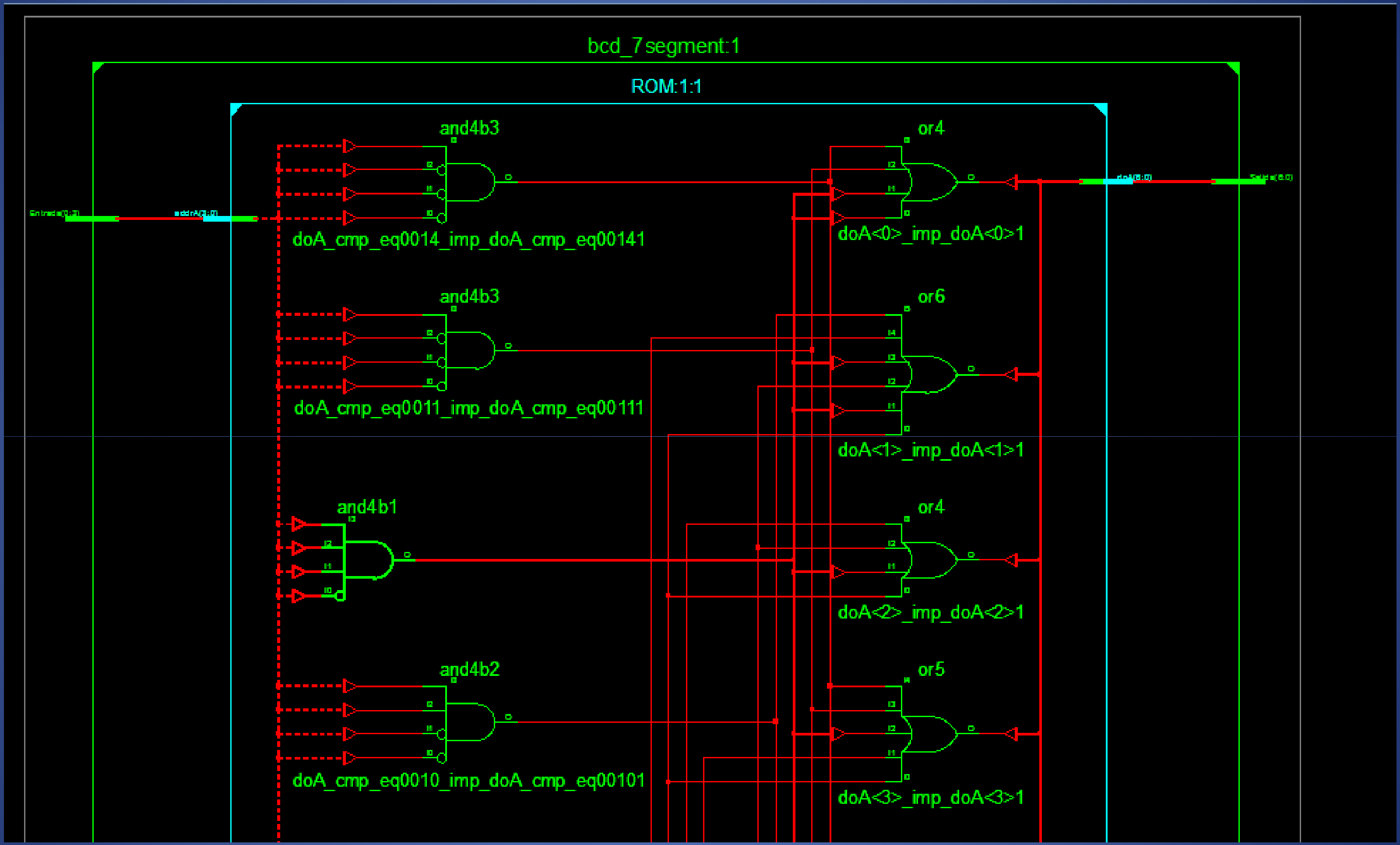
View RTL Schematic

View Technology Schematic

Check Syntax



RTL schematic



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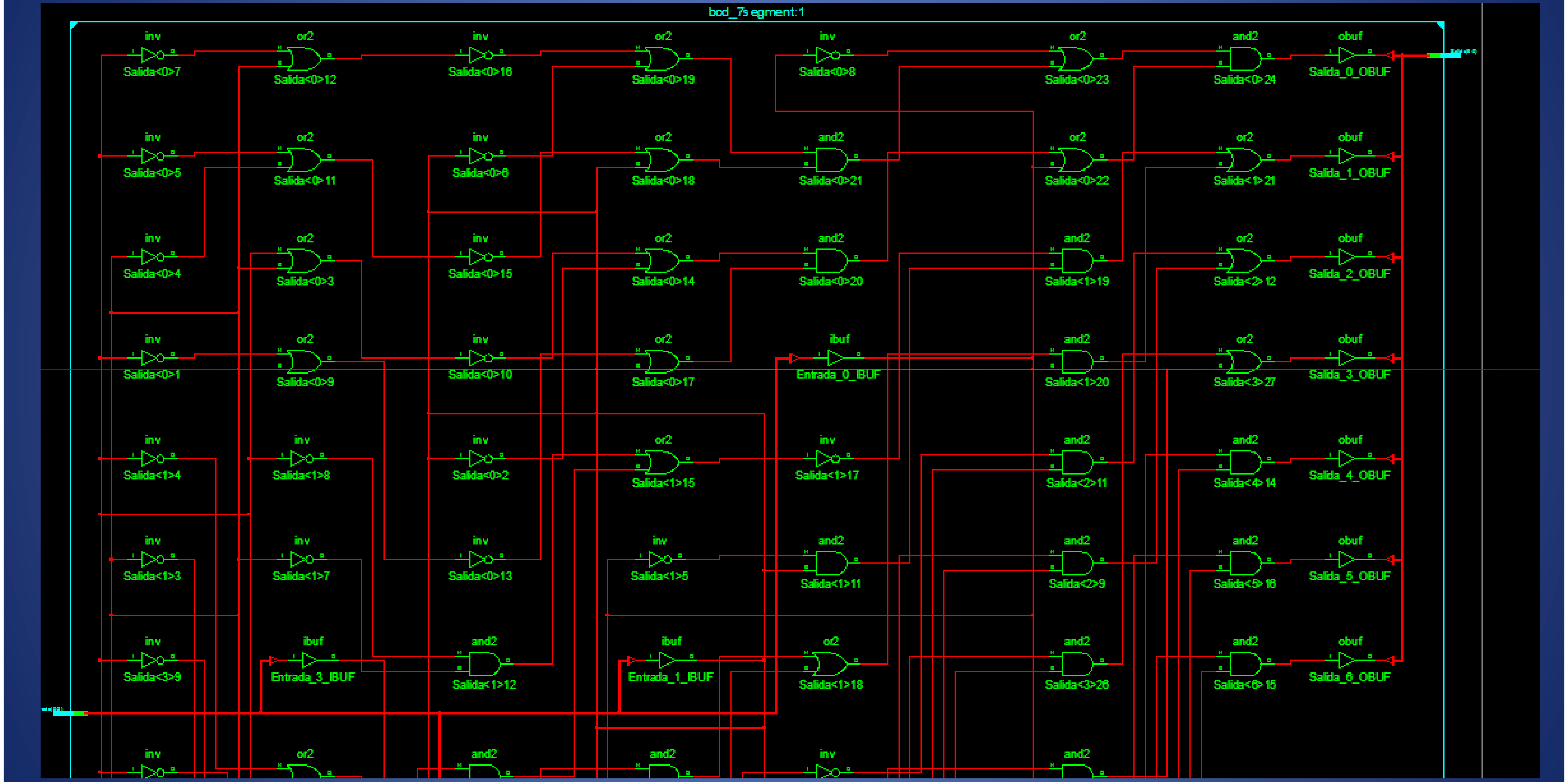
Technology schematic



Practica

Codificador y Decodificador hamming.

Transmisor

- Ingresar al codificador con un bit vector.
- Generar las paridades.
- Transmitir Dato usando signals.

Receptor

- Armar cada grupo con el operador concatenación.
- Utilizando WITH- SELECT O WHEN-ELSE generar la palabra de control en un vector.
- Utilizar los componentes del vector para corregir el dato. (el mismo vector de error puede entrar en un conversor BCD-7SEG para indicar el bit de error)