

Resumen teorico con ejer de final

Se encuentran las maquinas de estado de las guias de automatas(solo diagramas de estado), ejercicios de shift register con un poco de teorico extracto del libro de caballero(la parte que esta bien).

La parte de sumadores es sacado del brown, la de caballero no sirve pa bosta esta mal varios .

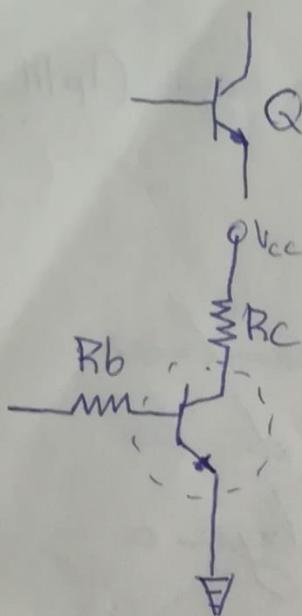
El teorico de osciladores de los temas mas salideros (casi todos), tambien de las filminas de toledo.

Tambien estan los mux, con distintos casos de implementacion.

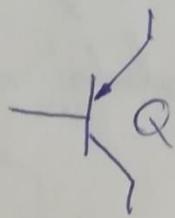
Haming, explicado como resolverlo.

Transistor NPN y PNP

NPN



PNP



Margen de Rueda

Es el margen q' se especifica a maxima corriente en la entrada, cuya margen si es superada no se hace buenos los niveles logicos en la salida, tambien produce efectos indeseables en la salida.

Rueda en ~~alto~~ Alto

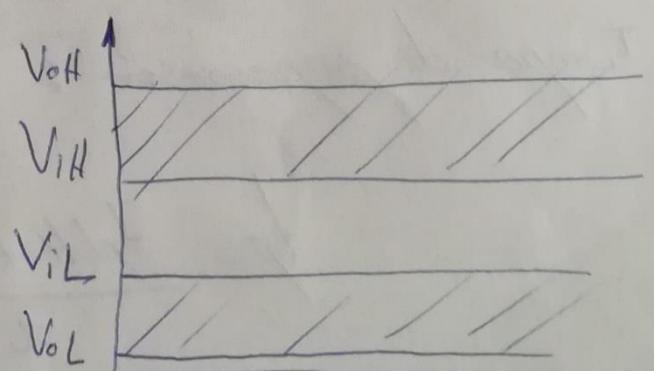
~~MRH = Voh - Vil~~

$$MRH = V_{OH} - V_{IL}$$

Rueda en bajo

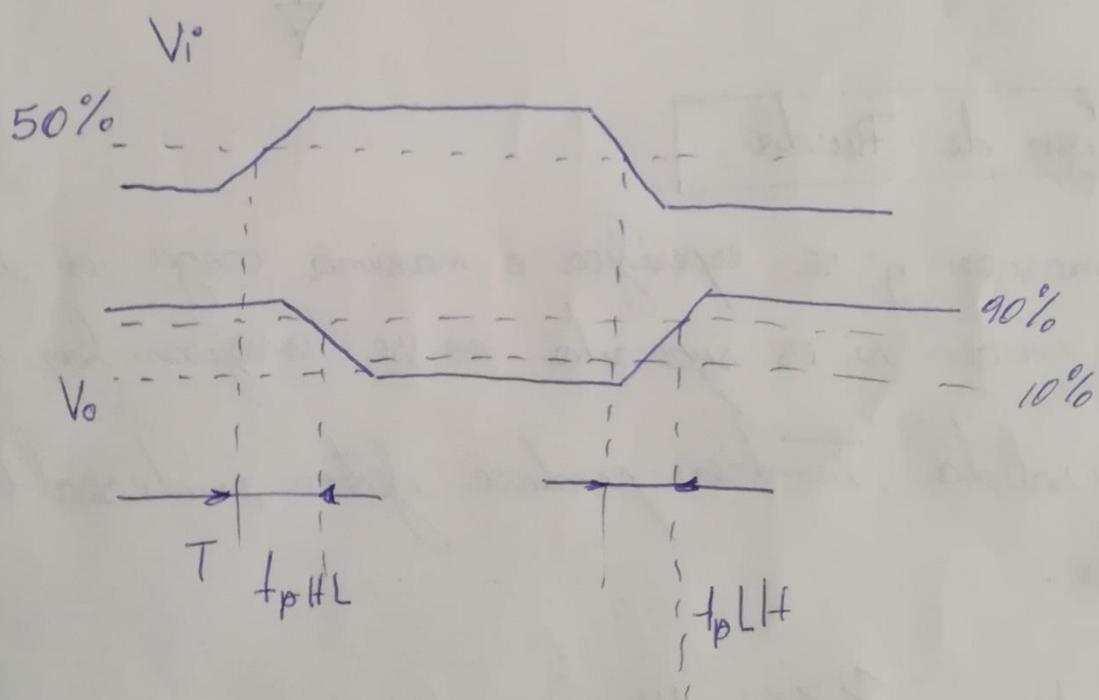
~~MRL = Vol(max) - Vil(min)~~

$$MRL = V_{IL} - V_{OL}$$



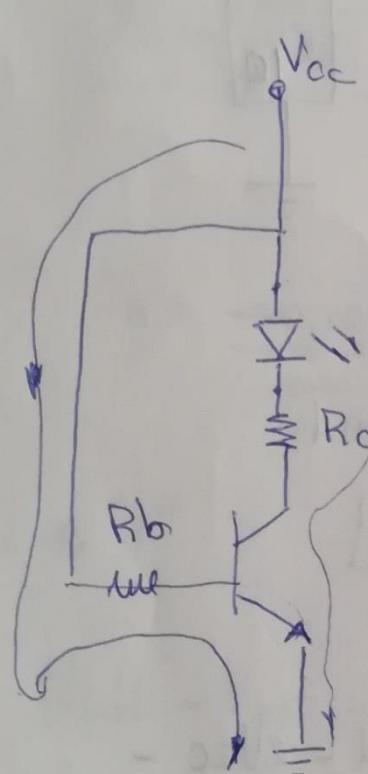
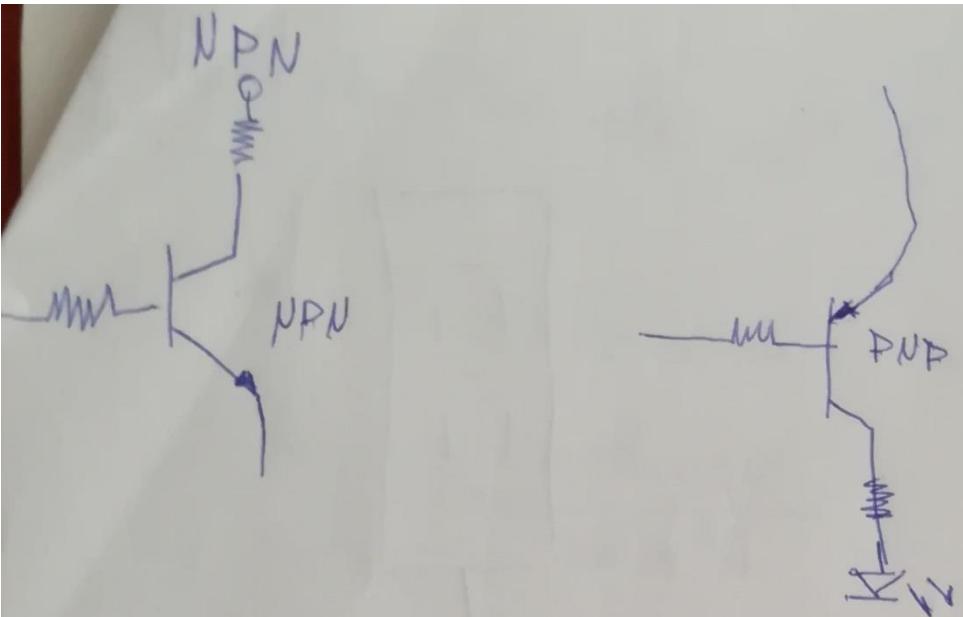
Tiempo de subida: es el tiempo entre el cambio de la entrada y el correspondiente cambio en la salida, cuando la salida cambia de alta a baja (t_{pHL})

Tiempo de bajada: es el tiempo entre el cambio de la entrada y el correspondiente cambio de la salida, cuando la salida cambia de baja a alta t_{pLH}



Tiempo de propagación: es el promedio de t_{pHL} y t_{pLH}

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$



$$B = 200$$

$$I_{LED} = 10mA$$

$$V_{CC} = 5V$$

$$I_B \cdot B = I_C$$

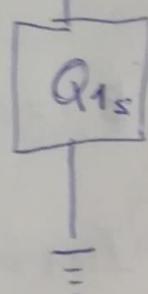
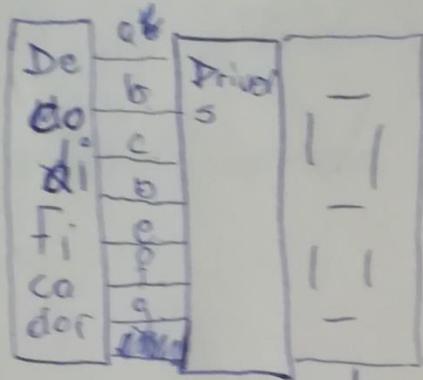
$$V_{CC} - V_{LED} - V_{R_C} - V_{CE} = 0$$

$$V_R = V_{CC} - V_{LED} - V_{CE}$$

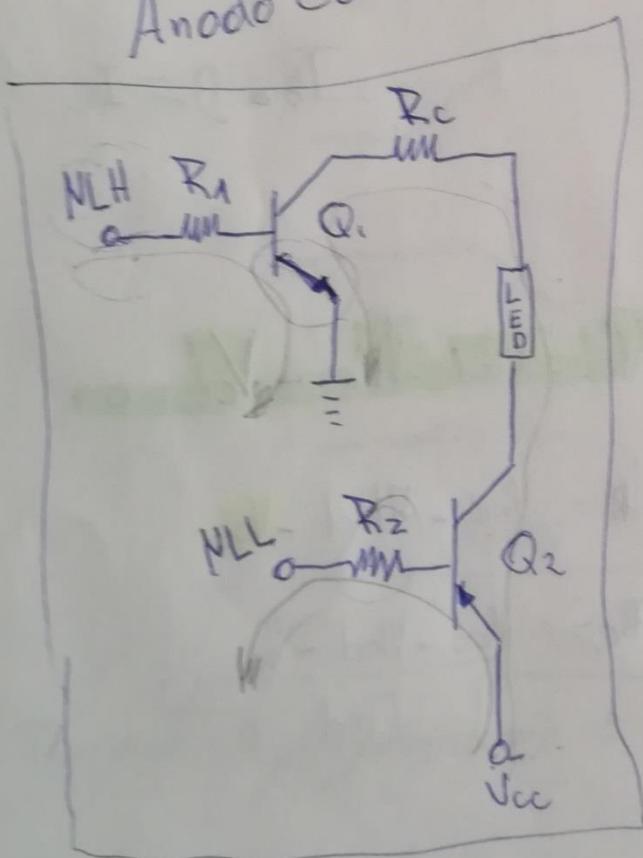
$$R_C = \frac{V_{CC} - V_{LED} - V_{CE}}{I_{LED}}$$

$$V_{CC} - V_{R_B} - V_{BE} = 0$$

preguntar Guillermo?



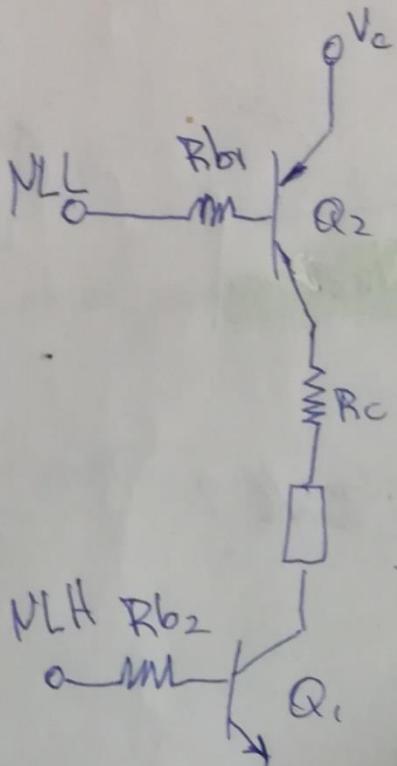
Anodo Comum



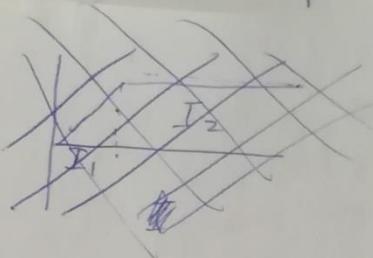
$$I_c = 10, 10mA$$

$$I_c = 100mA$$

$$V_{cc} - V_{Led} - 2V_{EC} -$$



$$V_{CC} - 2V_{CE} - V_{LED} = V_{RC} = 0$$



$$V_{RC} = V_{CC} - 2 \cdot V_{CE} - V_{LED}$$

$$R_C = \frac{5V - 0,4V - 1,5V}{100 \cdot 10^{-3} A}$$

$$\boxed{R_C = 31 \Omega}$$

$$I_B = \frac{100 \cdot 10^{-3} A}{100} = 1,10^{-3} A$$

Mollo 1

$$NLH - V_{BE} - V_{RB1} = 0$$

$$I_{B1} = \frac{I_C}{B}$$

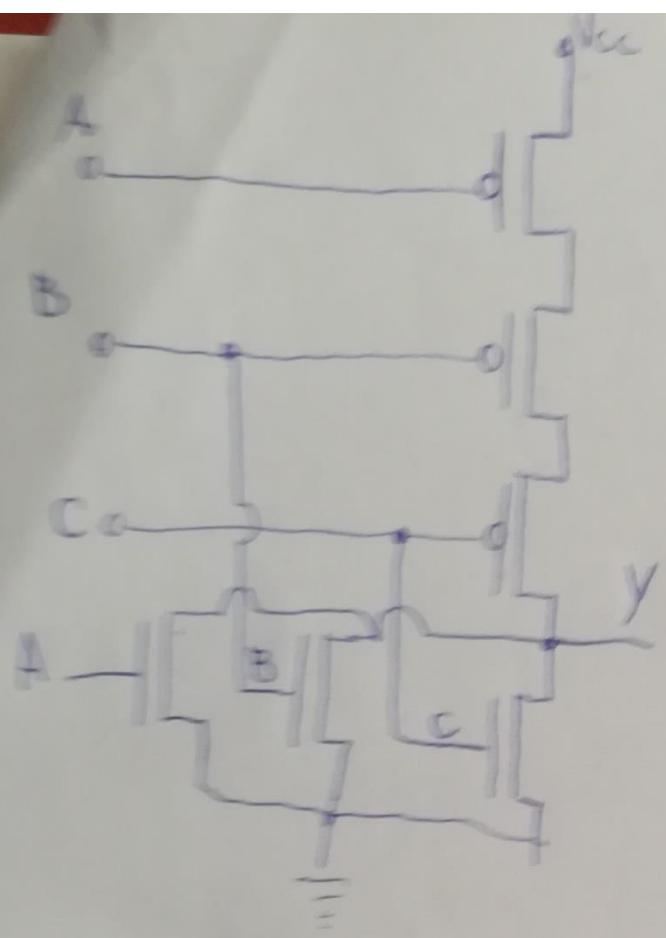
Mollo 2

$$V_{CC} - NLL - V_{BE} - V_{RC} = 0$$

$$V_{RB2} = \frac{V_{CC} - NLL - V_{BE}}{I_B}$$

remontas

$$I_{B2} = \frac{I_C}{B} \cdot \gamma$$



| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

| | 0 | 1 |
|----|---|---|
| 00 | 1 | 0 |
| 01 | 0 | 0 |
| 10 | 0 | 0 |
| 11 | 0 | 0 |

$$F = \bar{A} \bar{B} \bar{C}$$



$$I_{OH} = -400 \mu A$$

$$I_{OL} = 16 mA$$

$$V_{OH} = 3,3 V$$

$$V_{OL} = 0,5 V$$

$$t_{PLH} = 3,4 ns$$

$$t_{PHL} = 3 ns$$

$$I_{IH} = 40 \mu A$$

$$V_{IH} = 1,9 V$$

$$V_{CC} = 6 V$$

$$I_{CC} = 1,5 mA$$

$$V_{iL} = 1 V$$

$$I_{iL} = 1,6 mA$$

$$P_{max} = ?$$

$$M_A = ?$$

$$P_{an\ out} = ?$$

$$P_{max} = ?$$

$$\cancel{M_{BH} = \sqrt{V_H - V_L}}$$

$$V_H = V_{OH(max)} - V_{iH(min)}$$

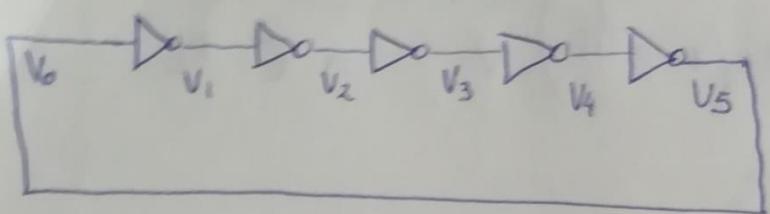
$$V_L = V_{iL(max)} - V_{OL(max)}$$

$$P_{an\ out} = \frac{I_{OH(max)}}{I_{iH(max)}} \text{ (alto)}$$

$$P_{an\ out} = \frac{I_{OL}}{I_{iL}} = \text{ (baja)}$$

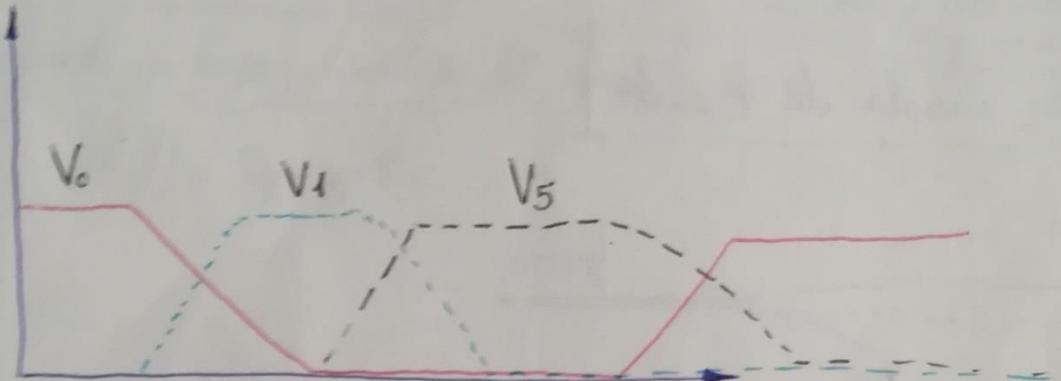
$$\Phi = I_{CC} \cdot V_{CC}$$

Temporización

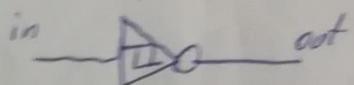


$$T = 2 \cdot t_p \cdot N$$

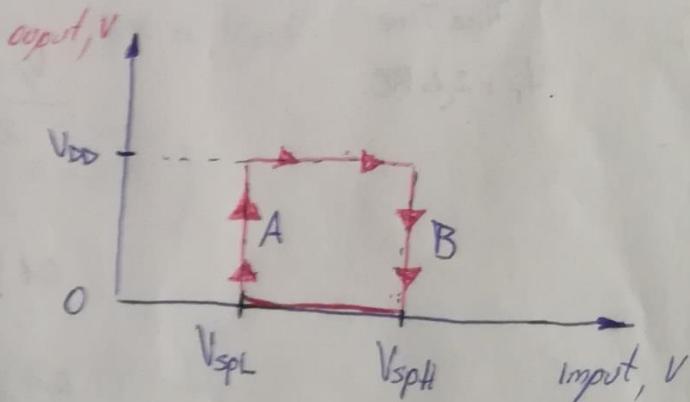
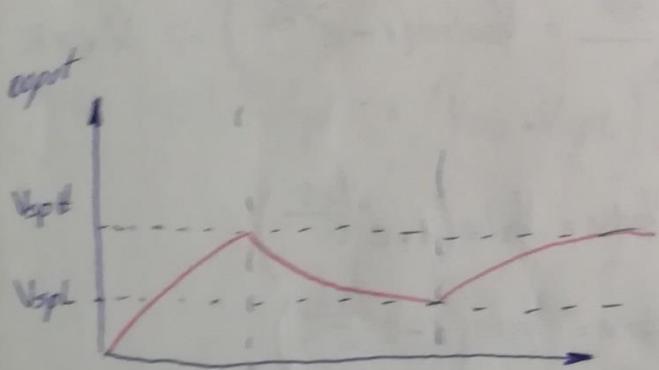
$$2 \cdot N \cdot t_p \gg t_f + t_r$$



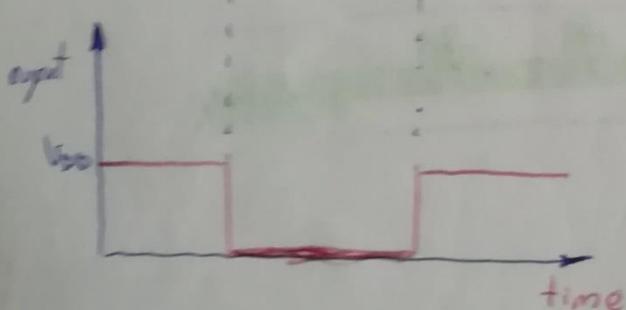
Trigger Shmitt



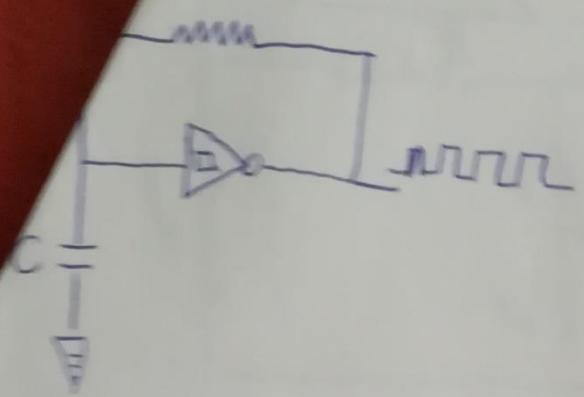
Características de transición



$$\text{Hysteresis} \Rightarrow V_H = V_{spH} - V_{spL}$$



Sp = switching point



$$f_{osc} = \frac{1}{t_1 + t_2}$$

$$t_1 = RC \cdot \ln \left[\frac{V_{spH}}{V_{spl}} \right]$$

$$t_2 = RC \cdot \ln \left[\frac{V_{dd} - V_{spl}}{V_{dd} - V_{spH}} \right]$$

Compara a baja, el voltaje del capacitor V_{spH}

$$V_c(t) = V_{spH} \cdot e^{-\frac{t}{RC}}$$

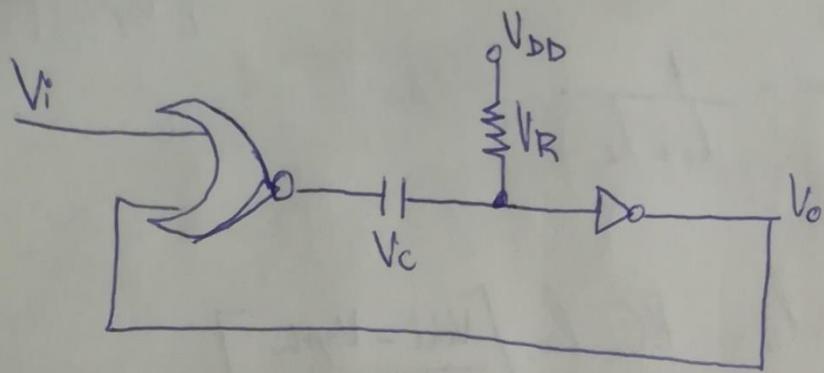
Tiempo de descarga del capacitor V_{spH} a V_{spl}

$$t_1 = RC \cdot \ln \left[\frac{V_{spH}}{V_{spl}} \right]$$

Similarmente la de carga. V_{spl} a V_{spH}

$$V_c(t) = V_{spl} + (V_{dd} - V_{spl}) \left(1 - e^{-\frac{t}{RC}} \right)$$

$$t_2 = RC \cdot \ln \left[\frac{V_{dd} - V_{spl}}{V_{dd} - V_{spH}} \right]$$



$$V_R = V_P + (V_S - V_P) e^{-\frac{t}{C}}$$

$$V_P = V_{DD}$$

$$V_S = 0$$

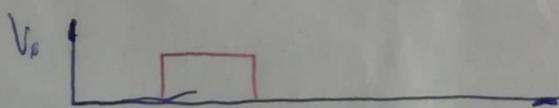
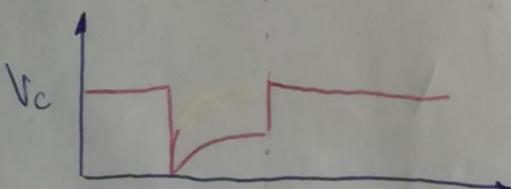
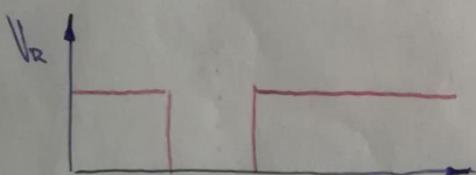
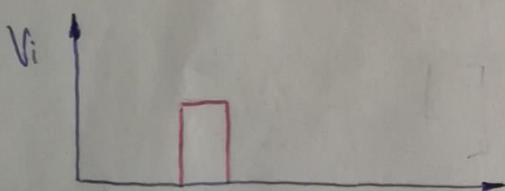
$$\frac{V_{DD}}{2} = V_{DD} - V_{DD} \cdot e^{-\frac{t}{C}}$$

$$V_R = \frac{V_{DD}}{2}$$

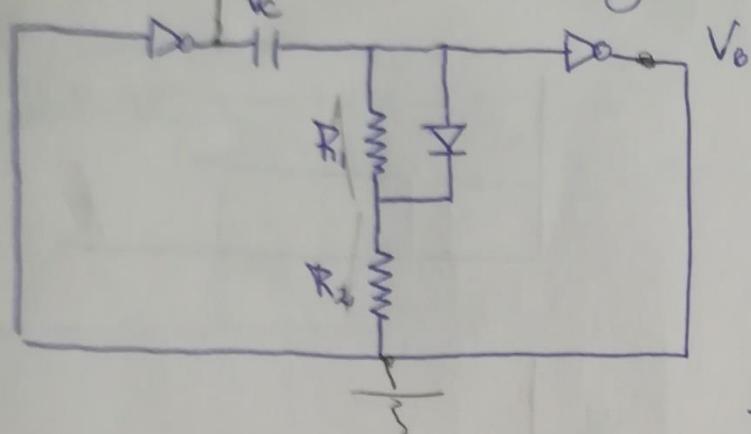
$$\frac{1}{2} - 1 = -e^{-\frac{t}{C}}$$

$$+\frac{1}{2} = +e^{-\frac{t}{C}}$$

$$\ln\left(\frac{1}{2}\right) = -\frac{t}{C} \cdot \ln(e)$$



con 2 inversores de 15 k Ω y ciclo de trabajo



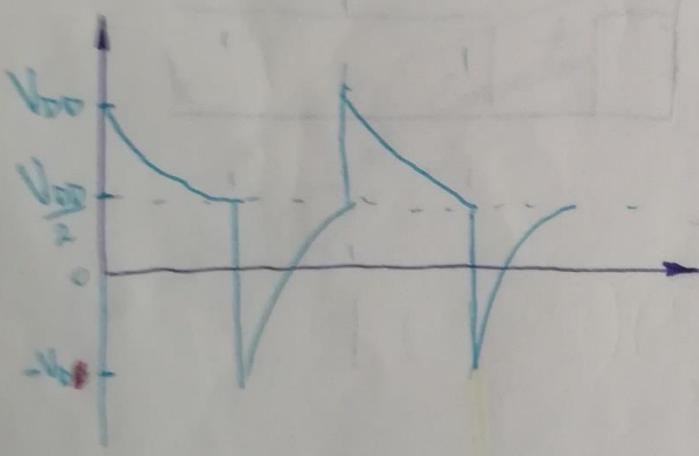
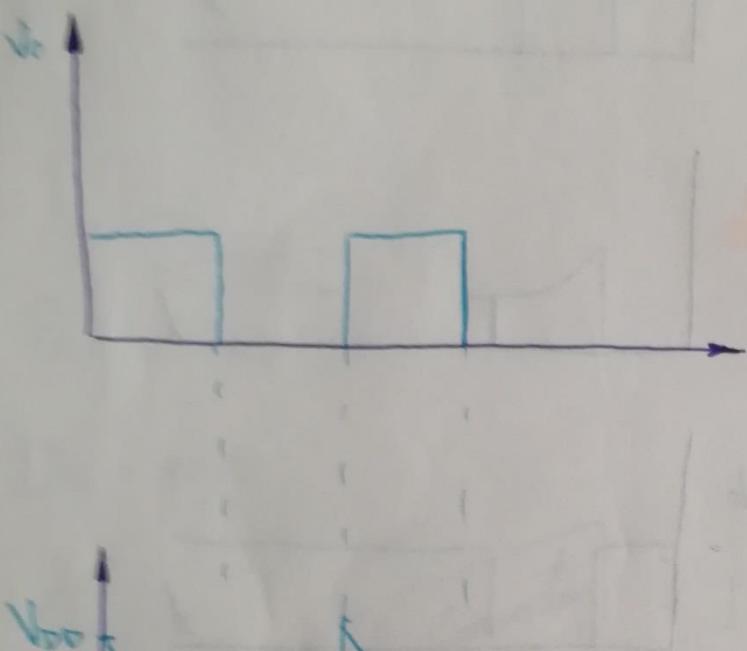
$$T = T_1 + T_2 \quad \wedge \quad T = \frac{1}{f_{\text{rec.}}}$$

$$T_1 = R_2 \cdot C \cdot 0,69$$

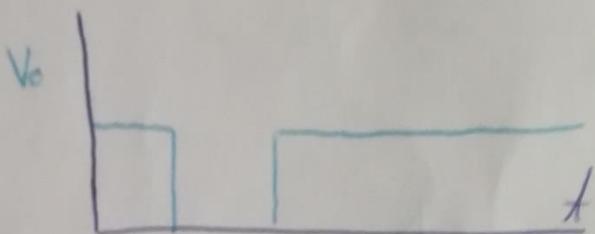
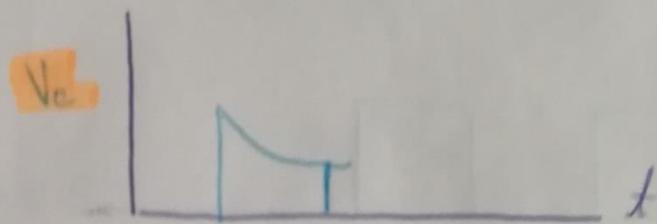
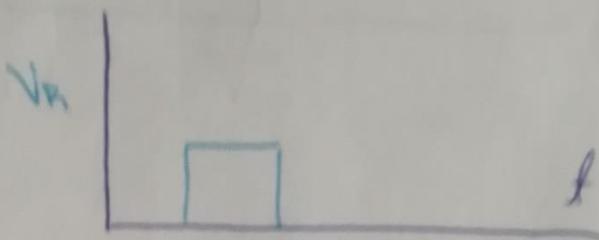
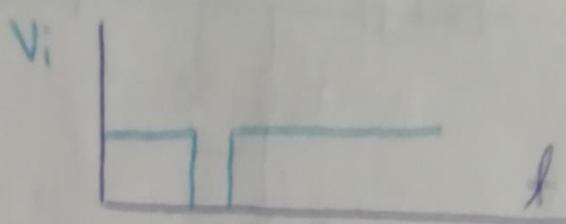
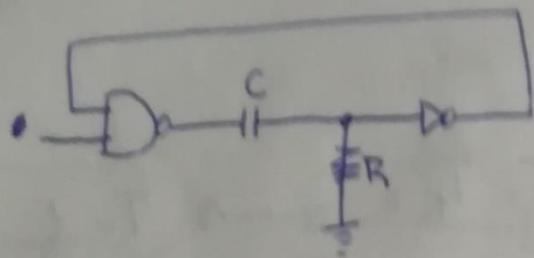
$$T_2 = (R_2 + R_1) \cdot C \cdot 0,69$$

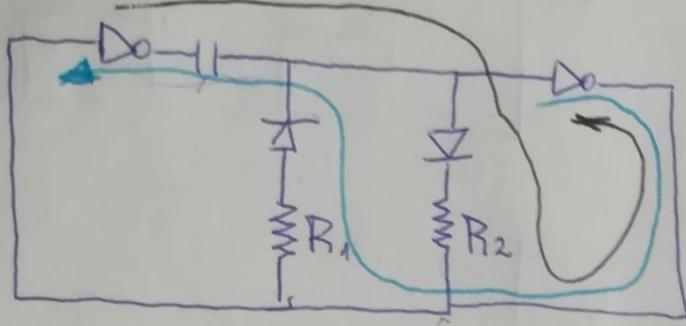
$T_1 = \text{carga}$

$T_2 = \text{descarga}$



Monostable de pulso negativo





$$T_1 = R_1 \cdot C \cdot 0,69$$

$$T_2 = R_2 \cdot C \cdot 0,69$$

D_c = ciclo de trabajo

$$D_c = \frac{T_1}{T} \cdot 100$$

Datos

$$f_r = 20 \text{ kHz}$$

$$D_c = 25\%$$

se debe fijar el capacitor

$$D_c = \frac{T_1}{T} \cdot 100\%$$

$$T_1 = \frac{D_c \cdot T}{100\%}$$

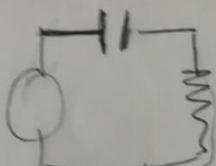
$$T_1 = \frac{25\% \cdot 0,00005 \text{ seg}}{100\%}$$

$$T_1 = 0,0000125 \text{ seg}$$

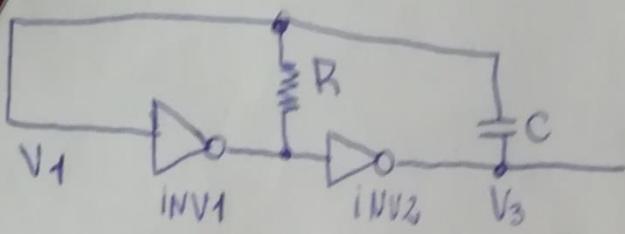
$$T = T_1 + T_2$$

$$T_2 = 0,00005 \text{ seg} - 0,0000125$$

$$T_2 = 0,0000375 \text{ seg}$$



Circuito Multivibrador



$$V_c(t) = V_1(t) - V_3(t) = (V_{DD} + V_{sp1}) e^{-\frac{t}{RC}} - V_{DD}$$

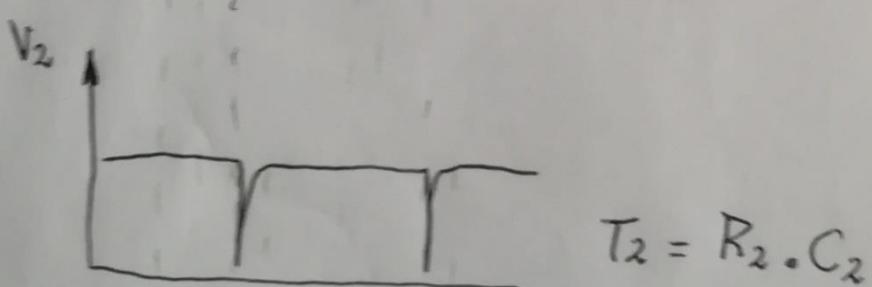
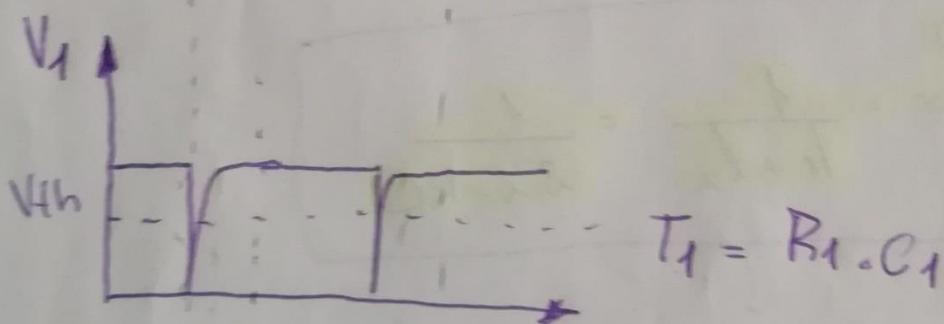
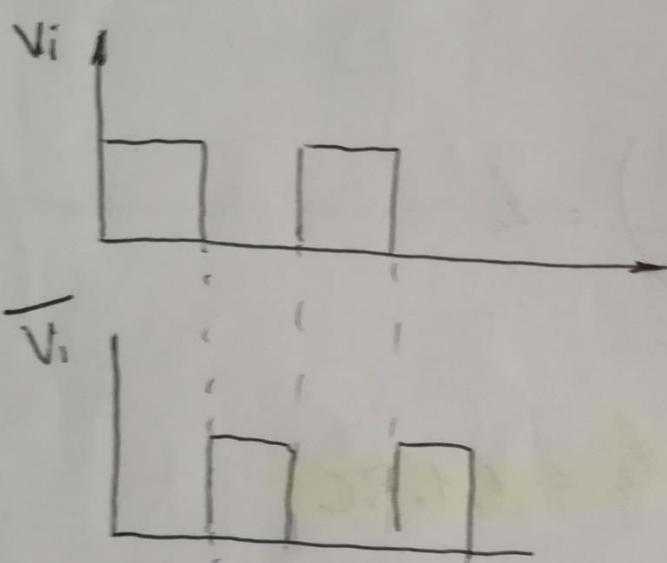
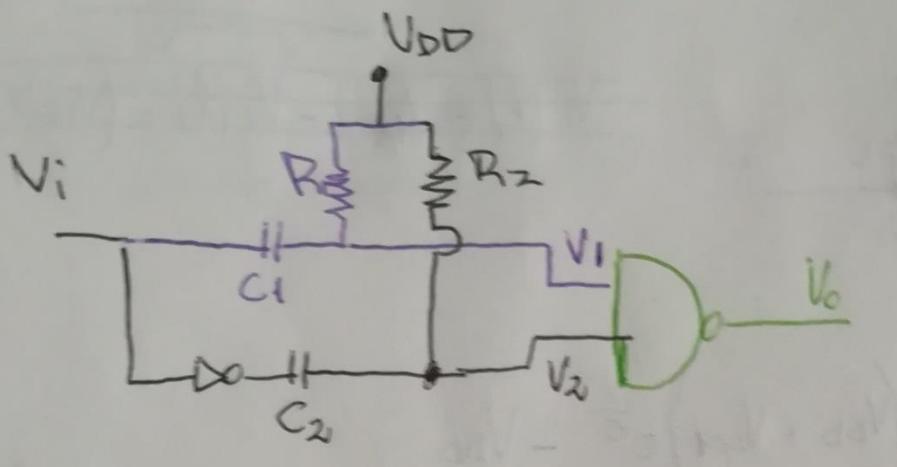
$$V_c(t) = V_1(t) - \overbrace{V_3(t)}^{V_{DD}} = (V_{DD} + V_{sp1}) e^{-\frac{t}{RC}} - V_{DD}$$

$$t_1 = RC \cdot \ln \left(\frac{V_{DD} + V_{sp1}}{V_{sp1}} \right) = t_2$$

$$V_{sp1} = \frac{V_{DD}}{2}$$

$$t_1 = t_2 = 1,1 \cdot RC$$

$$P_{osc} = \frac{1}{t_1 + t_2} = \frac{1}{2,2 \cdot RC}$$



Máquinas de Estado

Shift – register

Contadores

Las maquinas fueron ojeadas por Gutiérrez, se suponen que están bien o por lo menos para el ¡!!!!

No puse tablas de transición xq son muy largas!!!

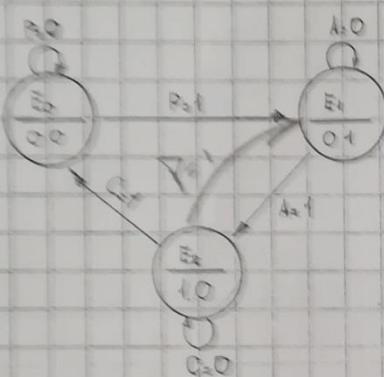
Tampoco VHDL, xq a partir de 2018 se toma verilog

Q. Puerta (Sin sensor de Personas)

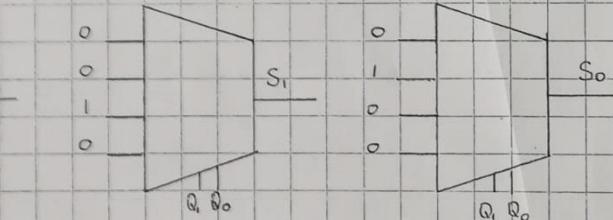
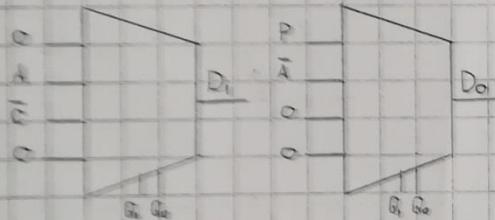
| Entradas | Descripción |
|----------|----------------|
| P | Pulsador |
| A | Sensor Abierto |
| C | Sensor Cerrado |

| SALIDAS | Descripción |
|-------------------|---------------|
| S ₀ =1 | Cierra Puerta |
| S ₁ =1 | Abre Puerta |
| S ₀ =0 | Espesa |
| S ₀ =0 | |

| Estado | Q ₁ Q ₀ |
|----------------|-------------------------------|
| E ₀ | 0 0 |
| E ₁ | 0 1 |
| E ₂ | 1 0 |



| Qt | Qt+1 | FF-D | D ₁ D ₀ | S ₁ S ₀ |
|-------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|
| P A C | Q ₁ Q ₀ | Q ₁ Q ₀ | 0 0 | 0 0 |
| 0 X X | 0 0 | 0 0 | 0 0 | 0 0 |
| 1 X X | 0 0 | 0 1 | 0 1 | 0 1 |
| X 0 X | 0 1 | 0 1 | 0 1 | 0 1 |
| X 1 X | 0 1 | 1 0 | 1 0 | 0 1 |
| X X 0 | 1 0 | 1 0 | 1 0 | 1 0 |
| X X 1 | 1 0 | 0 0 | 0 0 | 1 0 |

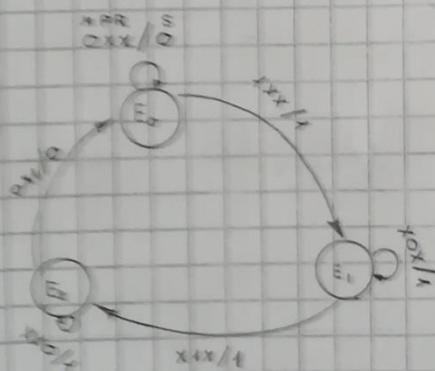


| Entradas | Descripción |
|----------|-------------|
| M | Marcha |
| P | Parada |
| R | Sensor F.C |

Salida

| SALIDA | DESCRIPCIÓN |
|--------|----------------------|
| S=0 | Desactiva Parabrisas |
| S=1 | Activa Parabrisas |
| | |

| ESTADO | Q ₁ Q ₀ |
|----------------|-------------------------------|
| E ₀ | 0 0 |
| E ₁ | 0 1 |
| E ₂ | 1 0 |

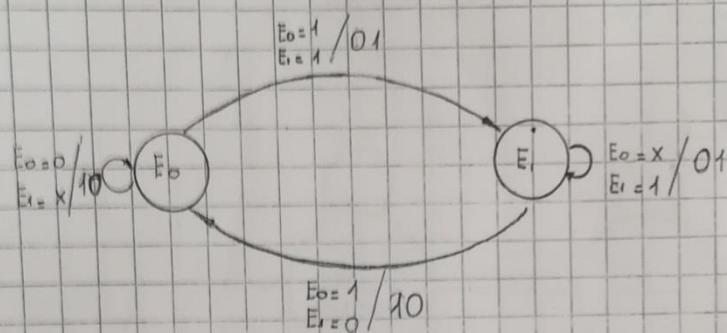


| M P R | Qt | Qt+1 | FF-D | D ₁ D ₀ | S |
|-------|-----|------|------|-------------------------------|-------|
| 0 X X | 0 0 | 0 0 | 0 0 | 0 0 | 0 |
| 1 X X | 0 0 | 0 1 | 0 1 | 0 1 | 1 |
| X 0 X | 0 1 | 0 1 | 0 1 | 0 1 | 1 X 0 |
| X 1 X | 0 1 | 1 0 | 1 0 | 1 0 | 1 X 1 |
| 0 X 0 | 1 0 | 1 0 | 1 0 | 1 0 | 1 X 0 |
| 0 X 1 | 1 0 | 0 0 | 0 0 | 0 0 | 0 X 1 |
| 1 X 0 | 1 0 | 1 0 | 1 0 | 1 0 | 1 |
| 1 X 1 | 1 0 | 1 0 | 1 0 | 1 0 | 1 |

(4)

| Entradas | Descripción |
|----------|-------------------|
| E_0 | 1º Sensor (Corto) |
| E_1 | 2º Sensor (Largo) |

| SALIDAS | Descripción |
|---------|-------------|
| $A = 1$ | Vía A |
| $B = 1$ | Vía B |
| $A = 0$ | Esp |
| $B = 0$ | Esp |

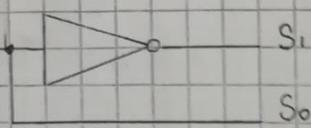
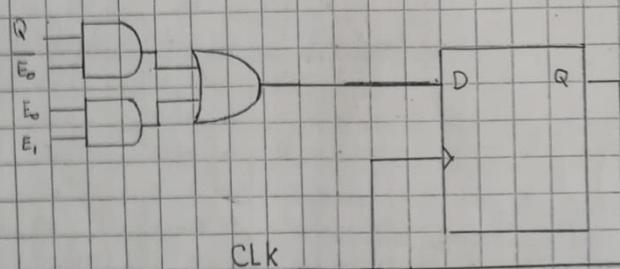


| Estado | Q |
|--------|---|
| E_0 | 0 |
| E_1 | 1 |

| E_0 | E_1 | Q_t | | Q_{t+1} | | D | S_1, S_0 |
|-------|-------|-------|-----------|-----------|-----------|---|------------|
| | | Q | \bar{Q} | Q | \bar{Q} | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

$$D = \begin{array}{ccccc} E_0 & E_1 & Q & \bar{Q} \\ \hline 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 0 \end{array} = Q \cdot \bar{E}_0 + \bar{E}_0 \cdot E_1 = S_0 = D$$

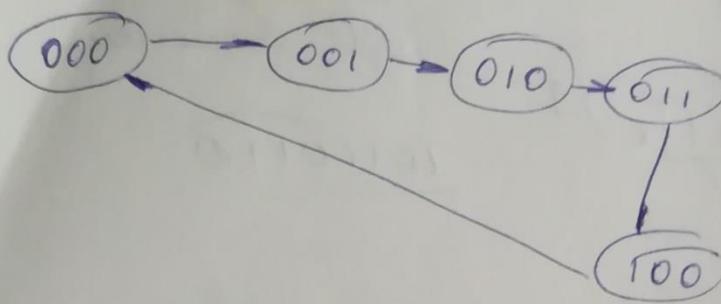
$$S_1 = \begin{array}{ccccc} E_0 & E_1 & Q & \bar{Q} \\ \hline 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 \end{array} =$$



Contadores

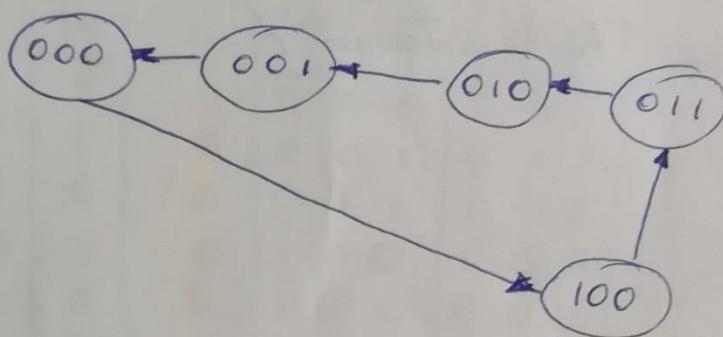
Contador UP

Modulo 5



Contador Down

Modulo 5



Contador Up-Down

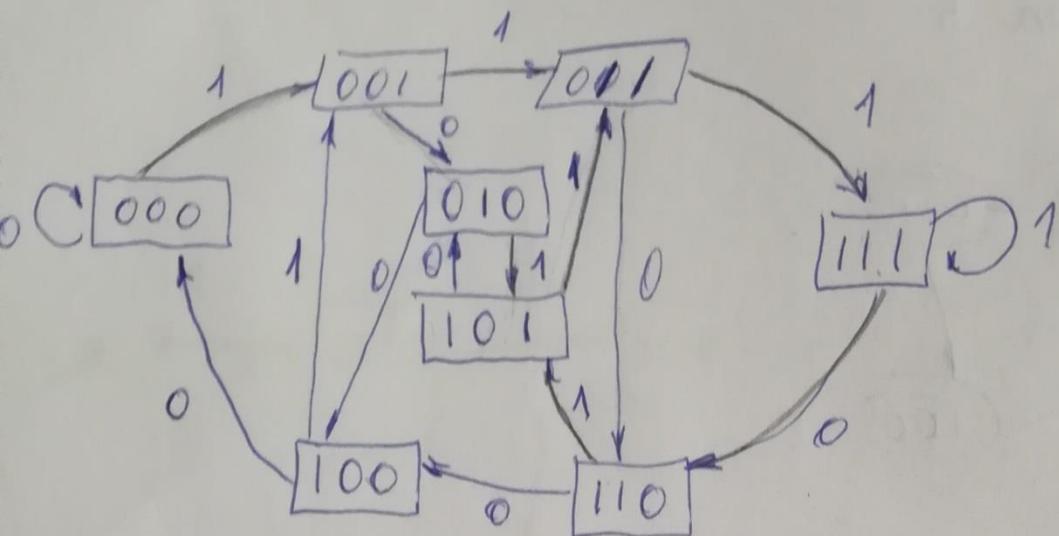
Modulo 5

$x = 0 \Rightarrow \text{up}$

$x = 1 \Rightarrow \text{down}$

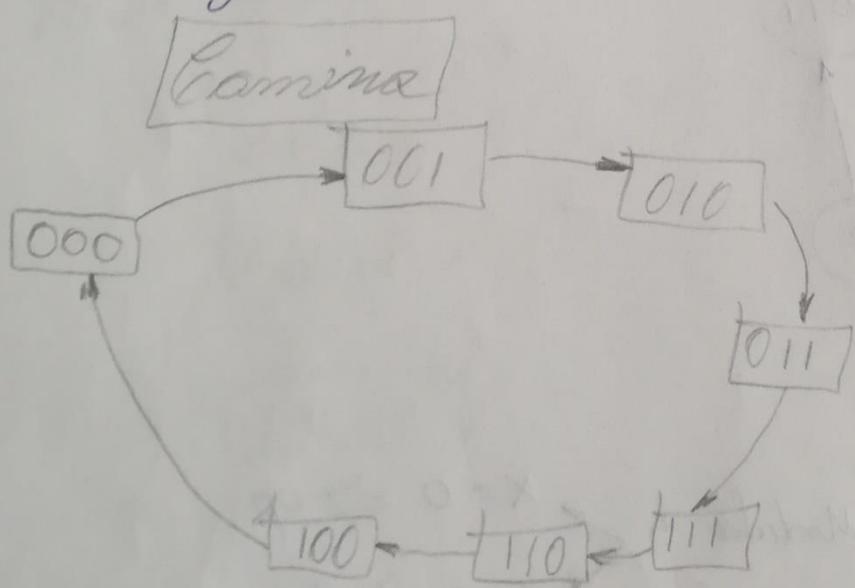
| x | Q(t) | | | $Q(t+1)$ | | |
|---------|----------------|----------------|----------------|----------------|----------------|----------------|
| | Q ₁ | Q ₂ | Q ₃ | Q ₁ | Q ₂ | Q ₃ |
| 0 0 0 0 | 0 0 1 | | | | | |
| 0 0 0 1 | 0 1 0 | | | | | |
| 0 0 1 0 | 0 1 1 | | | | | |
| 0 0 1 1 | 1 0 0 | | | | | |
| 0 1 0 0 | 0 0 0 | | | | | |
| X X X | X X X | | | | | |
| 1 1 0 0 | 0 1 1 | | | | | |
| 1 0 1 1 | 0 1 0 | | | | | |
| 1 0 1 0 | 0 0 1 | | | | | |
| 1 0 0 1 | 0 0 0 | | | | | |
| 1 0 0 0 | 1 0 0 | | | | | |
| X X X | X X X | | | | | |

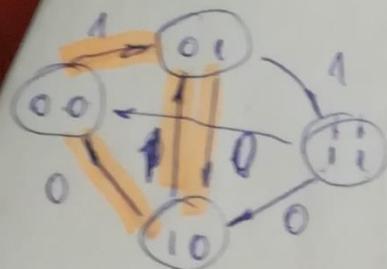
Shift-Register



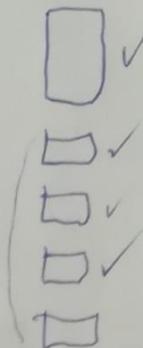
Generar la
siguiente secuencia:
10110110

Se debe tomar 8 caminos por la cantidad de bits
; no confundir la secuencia con Realimentación !





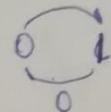
| $Q_1 Q_0$ | $Q(t+1)$ | P_o | P_u |
|-----------|----------|-------|-------|
| 00 | 01 | 1 | 0 |
| 01 | 10 | 0 | 0 |
| 10 | 00 | 0 | 0 |
| 11 | XX | X | 1 |



$B \geq n + K$

| $Q_1 Q_0$ | 00 | 01 | 11 | 10 |
|-----------|----|----|----|----|
| 00 | 11 | X | | |
| 01 | | XX | | |
| 11 | | | 11 | |
| 10 | 1 | 1 | 1 | 1 |

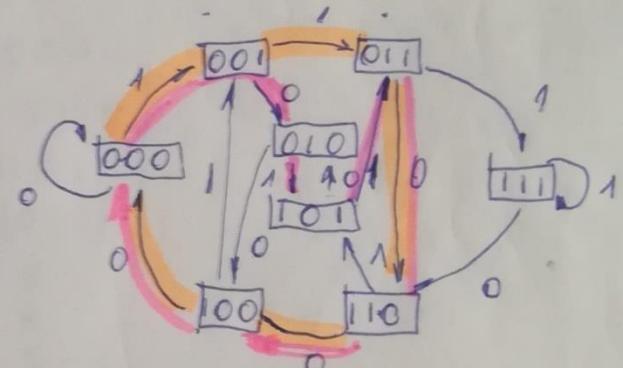
$$P_o = Q_2 Q_0 + \bar{Q}_0 Q_2 + \bar{m}_2 \bar{Q}_2 - \bar{Q}_1$$



14

$Q(t) \quad Q(t+1)$

| | P_u | m | $Q_2 \quad Q_1 \quad Q_0$ | $\bar{Q}_2 \quad \bar{Q}_1 \quad \bar{Q}_0$ | Salidas |
|---|-------|-----|---------------------------|---|---------|
| 0 | 1 | 0 | 0 0 0 | 0 0 1 | |
| 0 | 1 | 0 | 0 0 1 | 0 1 1 | |
| 0 | 0 | 0 | 0 1 1 | 1 1 0 | |
| 0 | 0 | 0 | 1 1 0 | 1 0 0 | |
| 0 | 0 | 0 | 1 0 0 | 0 0 0 | |
| - | - | - | - | - | - |
| 0 | 1 | - | 0 0 0 | 0 0 1 | |
| 0 | 0 | - | 0 0 1 | 0 1 0 | |
| 0 | 1 | - | 0 1 0 | 1 0 1 | |
| 0 | 1 | - | 1 0 1 | 0 1 1 | |
| 0 | 0 | - | 0 1 1 | 1 1 0 | |
| 0 | 0 | - | 1 1 0 | 1 0 0 | |
| 0 | 0 | - | 1 0 0 | 0 0 0 | |



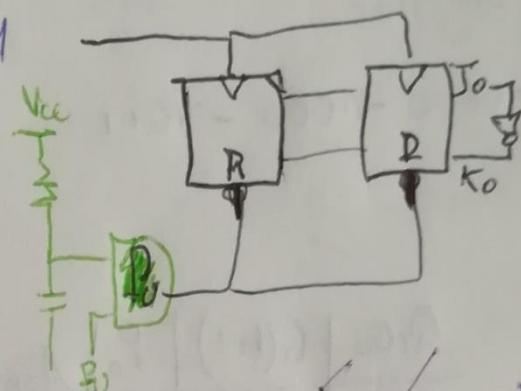
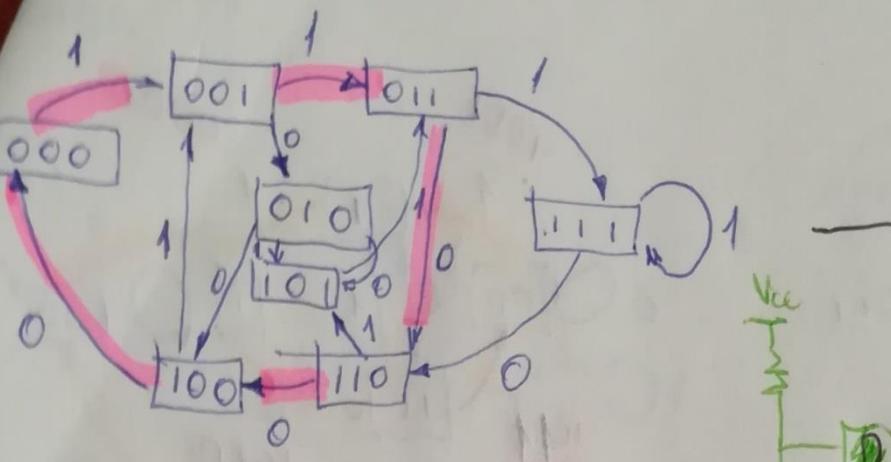
| $Q_1 Q_0$ | 00 | 01 | 11 | 10 |
|-----------|----|----|----|----|
| 00 | 0 | 0 | 0 | * |
| 01 | 0 | * | * | 0 |
| 11 | 0 | 0 | * | 0 |
| 10 | 0 | 0 | 0 | 0 |

$$P_u = \bar{m}_2 \bar{Q}_2 \bar{Q}_1 \bar{Q}_0 + \bar{m}_2 Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0$$

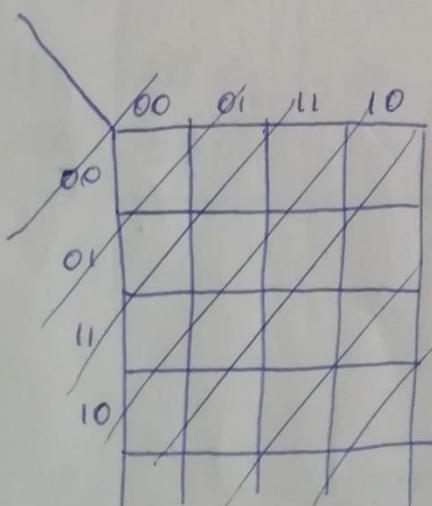
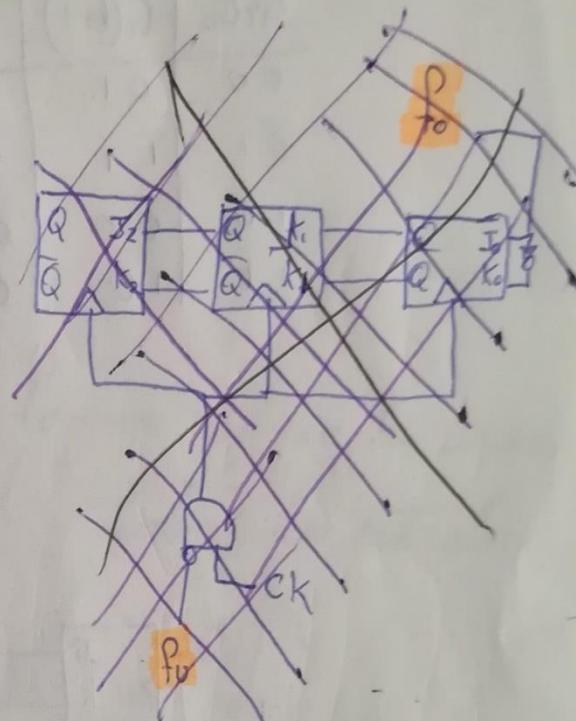
$$P_o =$$

* Preguntar: ¿Qué pasa con las salidas?

¿en J_o van ~~xx~~ donde estan los E_o no



| $Q(t)$ | $Q(t+1)$ | P_0 | P_U | Salidas |
|--------|----------|-------|-------|---------|
| 000 | 001 | 1 | 0 | 11011 |
| 001 | 011 | 1 | 0 | 00110 |
| 011 | 110 | 0 | 0 | 1.0110 |
| 110 | 100 | 0 | 0 | 11011 |
| 100 | 000 | 0 | 0 | 00011 |
| XXX | XXX | X | 1 | X |
| . | . | . | . | X |
| . | . | . | 1 | X |



| $Q_2 Q_1$ | Q_0 | f_O |
|-----------|-------|-------|
| 00 | 0 | 1 |
| 01 | X | 0 |
| 11 | 0 | X |
| 10 | 0 | X |

$$f_O = \bar{Q}_2 \bar{Q}_1$$

| $Q_2 Q_1$ | Q_0 | f_U |
|-----------|-------|-------|
| 00 | 0 | 0 |
| 01 | 1 | 0 |
| 11 | 0 | 1 |

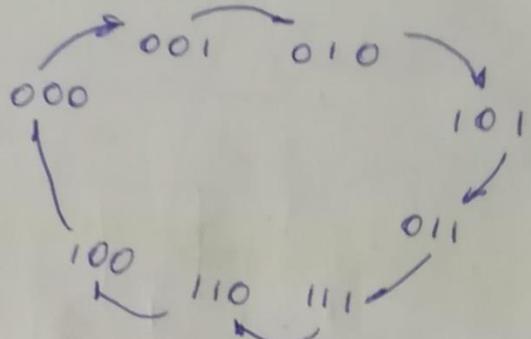
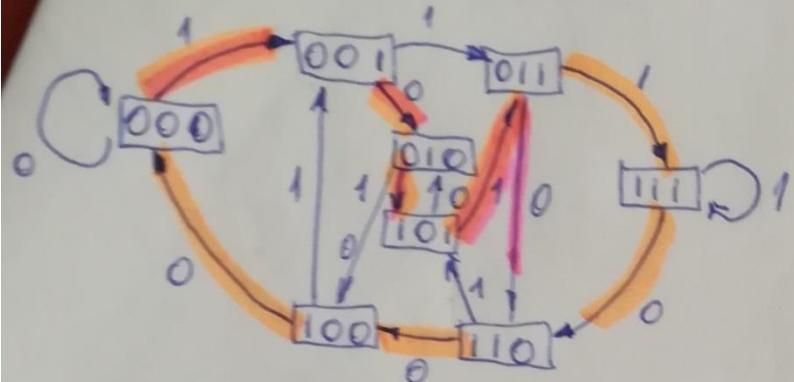
$$f_U = Q_2 Q_0$$

01 00 1011

anterior

actual

siguiente



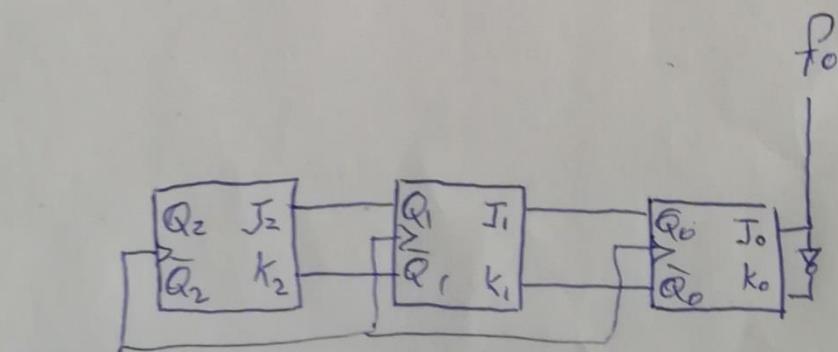
f_0

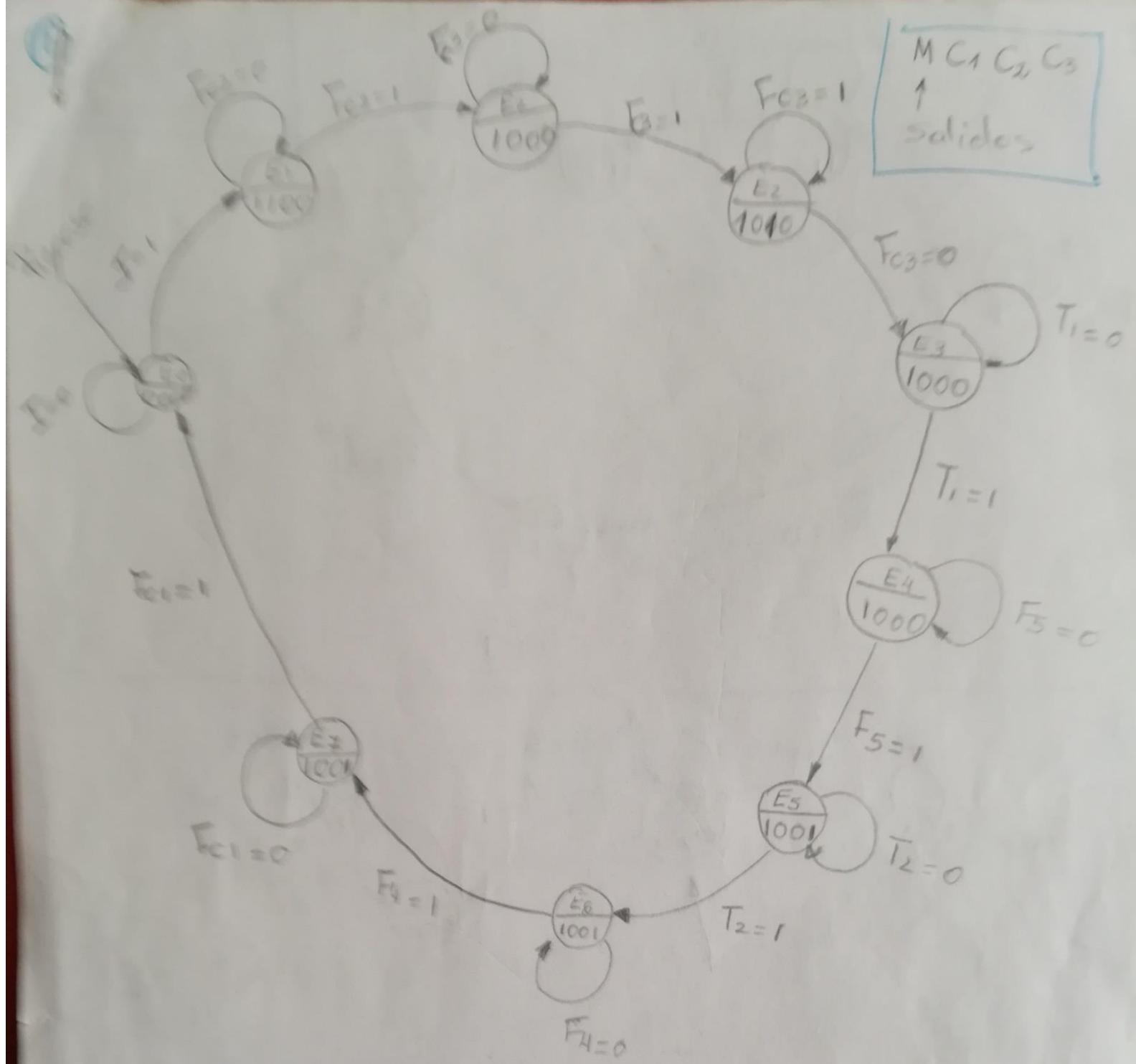
| $Q(t)$ | $Q(t+1)$ | Asignación | Asig |
|--------|----------|-----------------------|-----------------|
| 000 | 001 | 1 ✓ | 0 |
| 001 | 010 | 0 ✓ | 1 |
| 010 | 101 | 1 ✓ | 0 |
| 101 | 011 | 1 ✓ | 0 |
| 011 | 111 | 0 ✓ | 1 |
| 111 | 110 | 0 | 0 |
| 110 | 100 | 0 | 1 |
| 100 | 000 | 0 | 1 |

$P_V = \text{no hay } x \text{ que se usan}$
 todos los estados

| Q_2 | $Q_1 Q_0$ |
|-------|-------------|
| 0 | 00 01 11 10 |
| 1 | 01 10 00 01 |

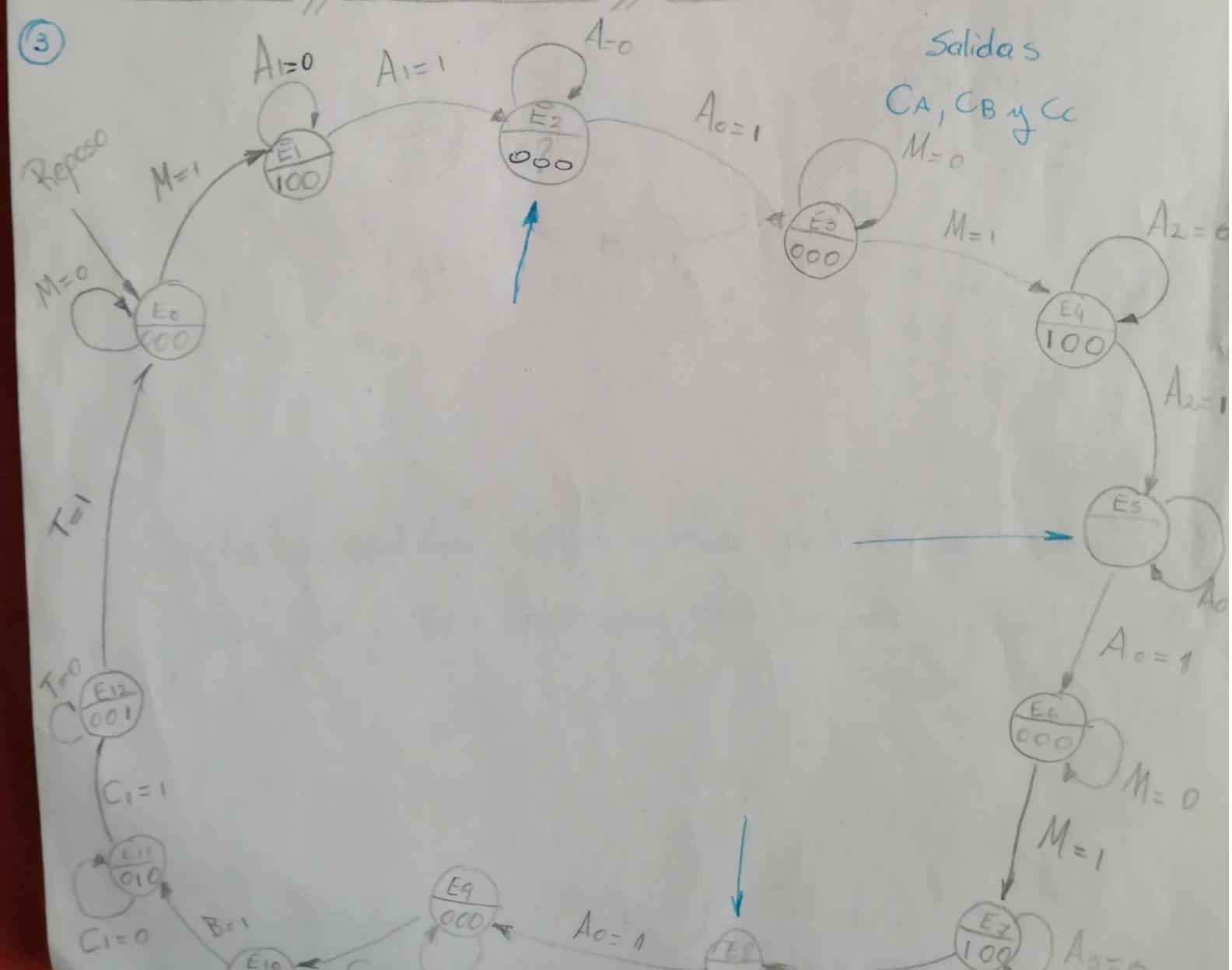
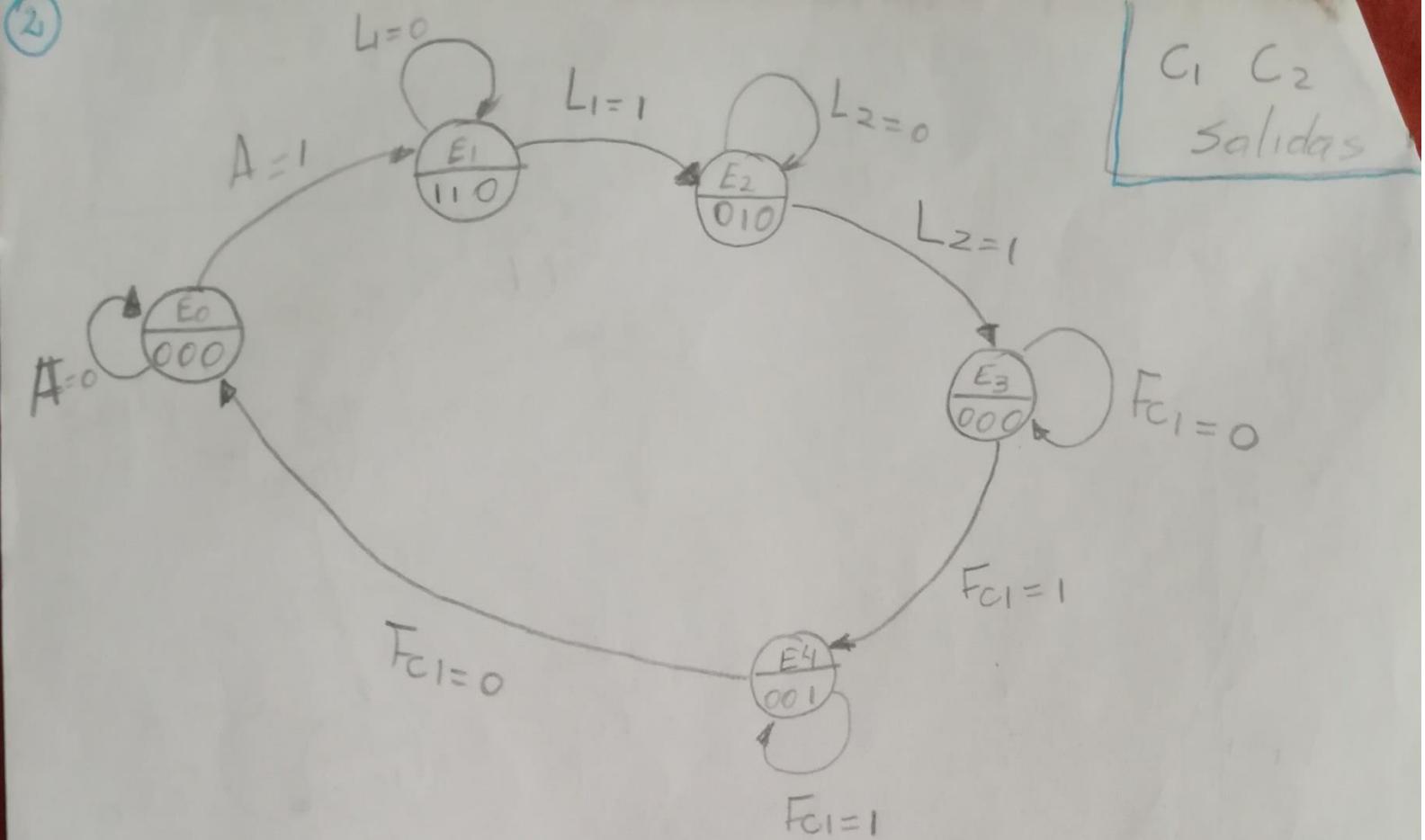
$$f_0 = \bar{Q}_2 \bar{Q}_0 + Q_2 \bar{Q}_1 Q_0 + \bar{Q}_2 Q_1$$



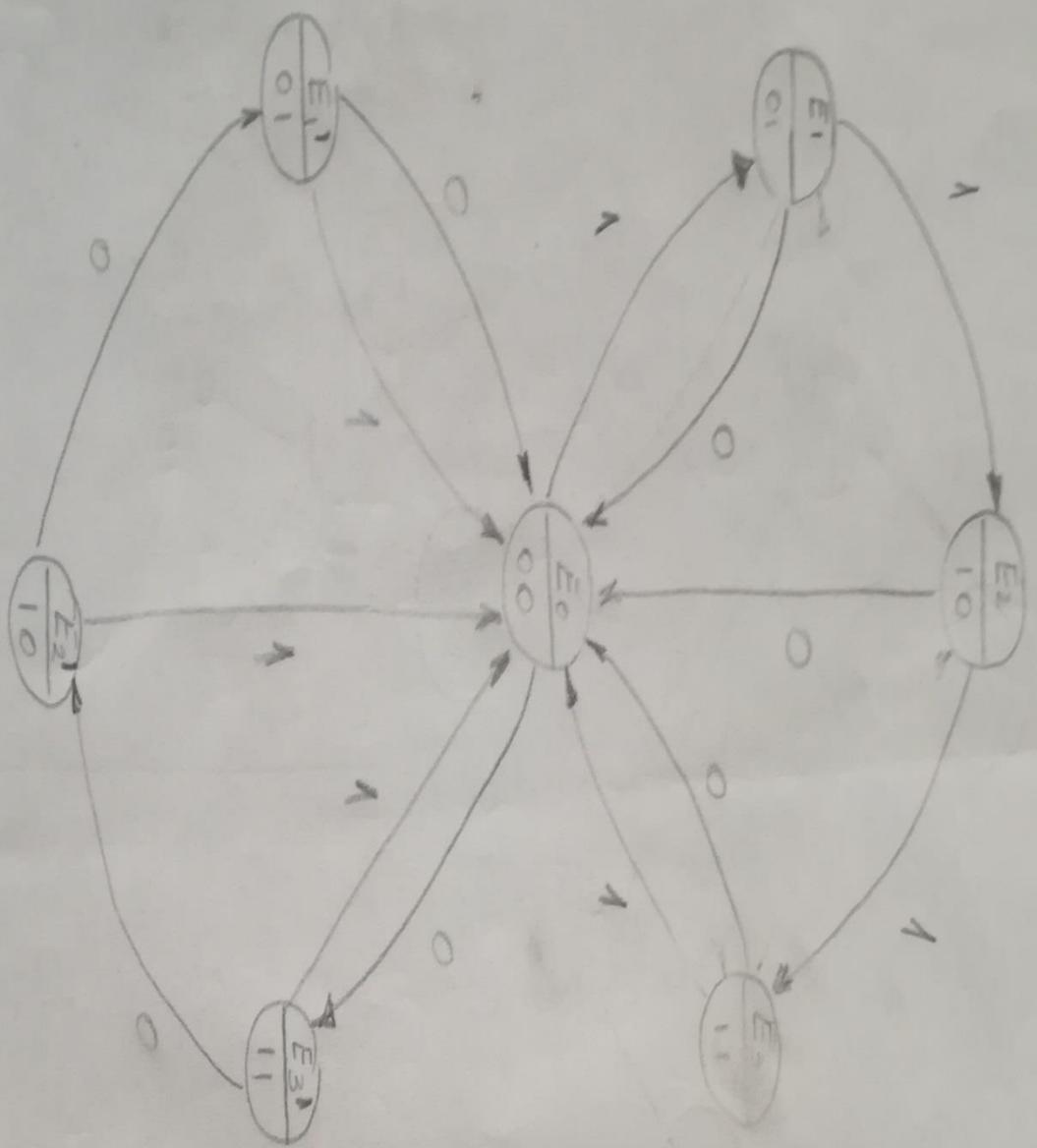


Preguntas

- ① ¿Cuando los cilindros suben o bajan salidas es 1?
- ② ¿El motor bomba esta prendido hasta el final?



Ejer 4



⑥ Comparar 2 números de 2 bits cada uno, indicar cuando es mayor, menor o igual, tabla de verdad, minimizar con NAND e implementar el circuito.

c

| A | B | F_1 | F_2 | F_3 |
|---|---|-------|-------|-------|
|---|---|-------|-------|-------|

| A | B | C | D | $A > B$ | $A < B$ | $A = B$ |
|---|---|---|---|---------|---------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |

Se toma los números binarios de 2 en 2 y luego se los compara.

Se pone "1" cuando se cumple la condición.

e

CD F_1

| AB | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 00 | | | | |
| 01 | 1 | | | |
| 11 | 1 | 1 | | |
| 10 | 1 | 1 | 1 | |

CD F_2

| AB | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 00 | | | | |
| 01 | 1 | | | |
| 11 | 1 | 1 | | |
| 10 | 1 | 1 | 1 | |

| | AB | CD | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|----|
| 00 | 1 | | | | | |
| 01 | | 1 | | | | |
| 11 | | | 1 | | | |
| 10 | | | | 1 | | |

| | AB | CD | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|----|
| 00 | | | | | | |
| 01 | | | | | | |
| 11 | | | | | | |
| 10 | | | | | | |

F₃

$$F_1 = A\bar{C} + B\bar{C}\bar{D} + AB\bar{D}$$

$$F_2 = \bar{A}C + \bar{B}CD + \bar{A}\bar{B}D$$

$$F_3 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}D + ABCD + A\bar{B}C\bar{D}$$

Ahora convertir las funciones F₁, F₂ y F₃ en compuertos "NAND"

$$\underline{F_1 = A\bar{C} + B\bar{C}\bar{D} + AB\bar{D}} = (\bar{A}\bar{C}) (\bar{B}\bar{C}\bar{D}) (\bar{A}B\bar{D})$$

$$\underline{F_2 = \bar{A}C + \bar{B}CD + \bar{A}\bar{B}D} = (\bar{A}C) (\bar{B}CD) (\bar{A}\bar{B}D)$$

$$\underline{F_3 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}D + ABCD + A\bar{B}C\bar{D}}$$

$$\underline{F_3 = (\bar{A}\bar{B}\bar{C}\bar{D}) (\bar{A}B\bar{C}D) (ABCD) (A\bar{B}C\bar{D})}$$

No tener como de dibujar /

| | A | B | C |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

F_2

| | AB | CD | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|----|
| 00 | | | | | | |
| 01 | | | / | / | / | / |
| 11 | | | / | / | / | / |
| 10 | | | | | | |

| | AB | CD | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|----|
| 00 | | | | | / | / |
| 01 | | | | / | / | / |
| 11 | | | | / | / | / |
| 10 | | | | / | / | / |

⑧ Determine los valores de bit de paridad para poder transmitir en código Hamming el siguiente dato 101100101. Realice el circuito transmisor con conjuectores

101100101

m = cantidad de bits

$$m = 9$$

$$2^k > m + k + 1$$

$$16 > 9 + 4 + 1$$

$$16 > 14 \quad \checkmark$$

Como la cantidad depende m y k
se usa 13 columnas
estas 2 nisetocan.

| d_9 | d_8 | d_7 | d_6 | d_5 | k_4 | d_4 | d_3 | d_2 | k_3 | d_1 | k_2 | k_1 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | - |
| - | - | - | 0 | 0 | 0 | 0 | 0 | - | - | 0 | 0 | 0 |
| - | - | 0 | 0 | - | 0 | 0 | - | 0 | 0 | - | 0 | 0 |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |
| - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - |

Los bits 0000 se eliminan xq significa q' no existe error!

$$16 > \begin{matrix} 2^4 \\ 2^3 \\ 2^2 \\ 2^1 \\ 2^0 \end{matrix}$$

↑
ese no

| | | | |
|-------|-------|-------|-------|
| 8 | 4 | 2 | 1 |
| k_4 | k_3 | k_2 | k_1 |

indica la posición de los bits donde van las "K"

$$G_1 = k_1 \oplus d_1 \oplus d_2 \oplus d_4 \oplus d_5 \oplus d_7 \oplus d_9$$

$$G_2 = k_2 \oplus d_1 \oplus d_3 \oplus d_4 \oplus d_6 \oplus d_7$$

$$G_3 = k_3 \oplus d_2 \oplus d_3 \oplus d_4 \oplus d_8 \oplus d_9$$

- * En los columnas donde el dato a transmitir es cero la hacemos totalmente cero los "1"
- * En G_1 hacemos $q' k_1$ sea "cero", en G_2 $q' k_2$ sea "cero", G_3 $q' k_3$ sea "cero" y así hasta llegar al último "k"

En estas columnas
los "1" se hacen
cero

| 1 0 1 1 0 k ₄ 0 1 0 k ₃ 1 k ₂ k ₁ | G ₄ |
|---|----------------|
| - - - - - 0 0 0 0 0 0 0 0 | G ₃ |
| - - 0 0 0 0 - - - 0 0 0 | G ₂ |
| - - 0 - 0 - 0 - 0 - 0 - 0 - | G ₁ |

La tabla nos quedara

| 1 0 1 1 0 k ₄ 0 1 0 k ₃ 1 k ₂ k ₁ | G ₄ |
|---|----------------|
| - 0 - 0 0 0 0 0 0 0 0 0 | G ₃ |
| - 0 0 0 0 0 0 - 0 0 0 0 | G ₂ |
| - 0 - 0 0 0 0 0 0 - 0 0 | G ₁ |

$$G_1 = 1+1+1 = 1$$

$$G_2 = 1+1+1+1 = 0$$

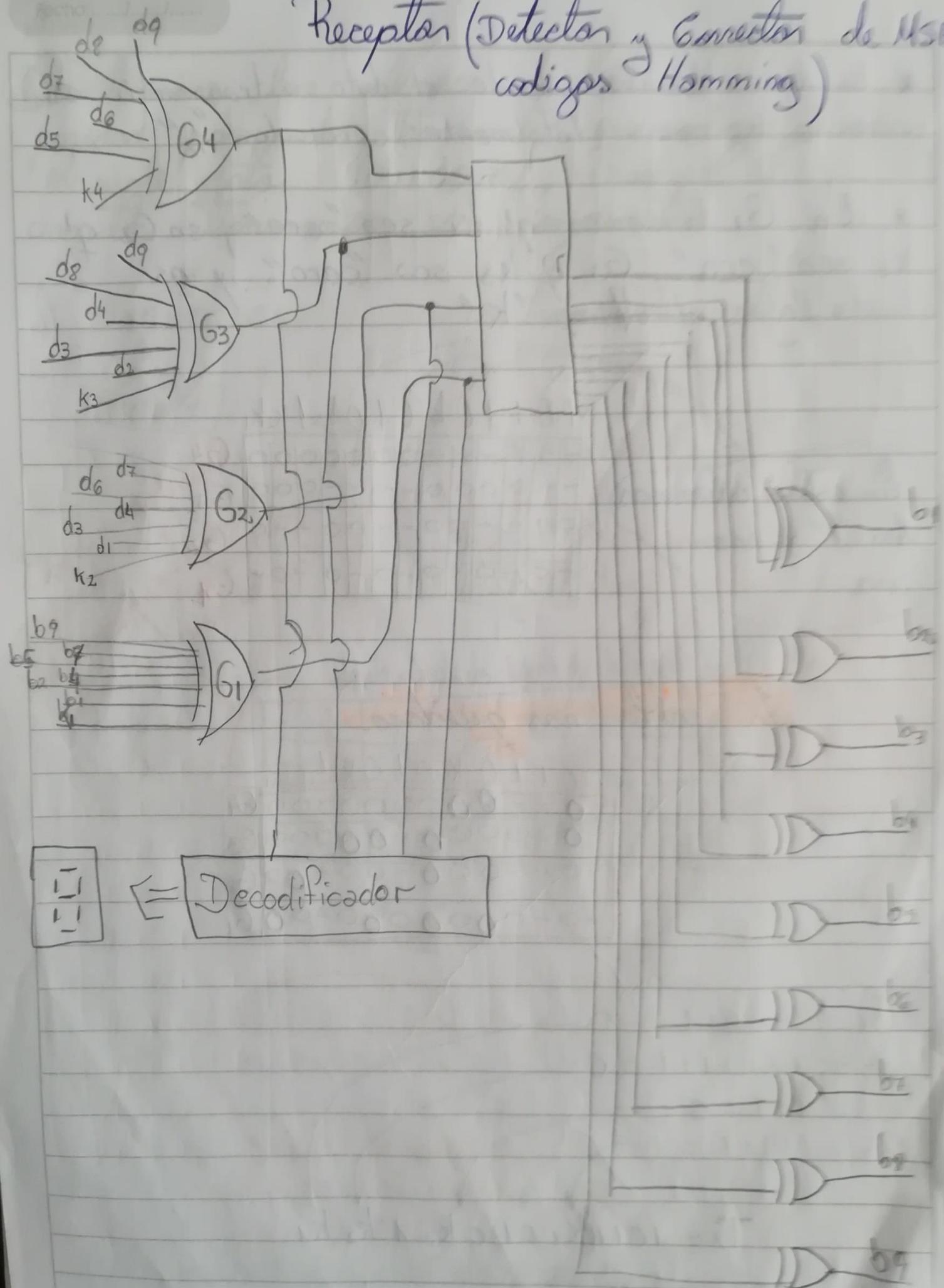
$$G_3 = 1+1 = 0$$

$$G_4 = 1+1+1 = 1$$

$$Tx = 10110k_4 010k_3 1k_2 k_1$$

| |
|--------------------|
| Tx = 1011010100101 |
|--------------------|

Receptor (Detector y Corrector de MSB codigos Hamming)

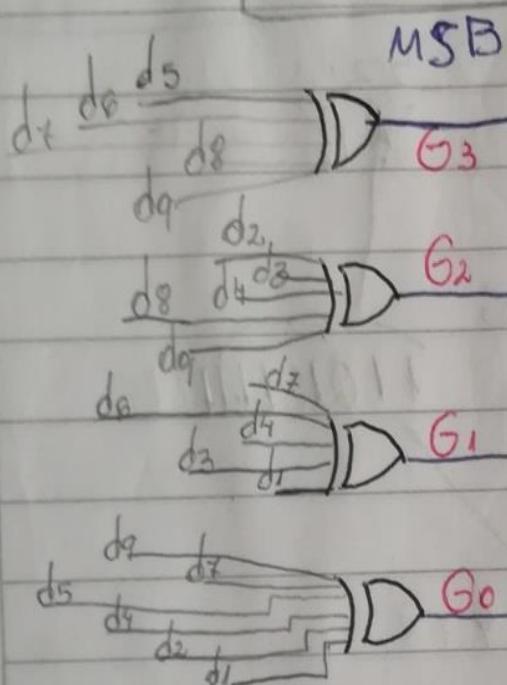


Transmisor

(Generador de Códigos de Hamming) $d_9 d_8 d_7 d_6 d_5 k_4 d_4 d_3 d_2 k_3 d_1 k_2 k_1$

LSB

Generador
de informa
ción



MSB

G_3

G_2

G_1

G_0

⑪ Diseñar un conversor codiga de BCD a Ex3

- Realizar la tabla de verdad
- Minimizar

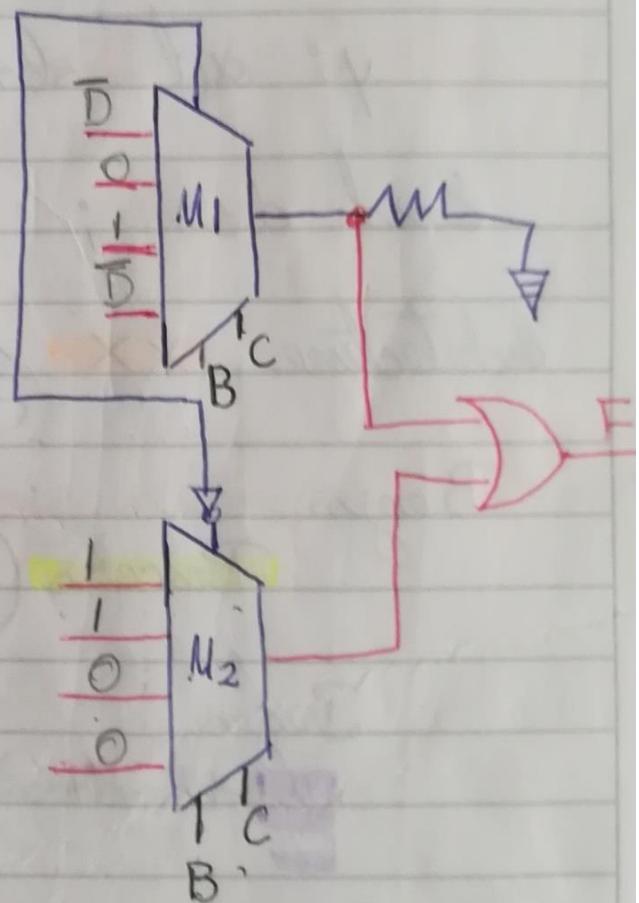
- Implementar con compuertas NAND/NAND

| A B C D | X ₀ | X ₁ | X ₂ | X ₃ |
|---------|----------------|----------------|----------------|----------------|
| 0 0 0 0 | 0 | 0 | 1 | 1 |
| 0 0 0 1 | 0 | 1 | 0 | 0 |
| 0 0 1 0 | 0 | 1 | 0 | 1 |
| 0 0 1 1 | 0 | 1 | 1 | 0 |
| 0 1 0 0 | 0 | 1 | 1 | 1 |
| 0 1 0 1 | 1 | 0 | 0 | 0 |
| 0 1 1 0 | 1 | 0 | 0 | 1 |
| 0 1 1 1 | 1 | 0 | 1 | 0 |
| 1 0 0 0 | 1 | 0 | 1 | 1 |
| 1 0 0 1 | 1 | 1 | 0 | 0 |
| 1 0 1 0 | x | x | x | x |
| 1 0 1 1 | x | x | x | x |
| 1 1 0 0 | x | x | x | x |
| 1 1 0 1 | x | x | x | x |
| 1 1 1 0 | x | x | x | x |
| 1 1 1 1 | x | x | x | x |

(18) Resolver las sigtes funciones utilizando dos multiplexores de 4:1, uno de los multiplexores queda en alta impedancia y el otro queda en 0 cuando la señal ENABLE se encuentra en alta

$$F = \overline{M_0}, M_1, M_2, M_3, M_8, M_{12}, M_{13}, M_{14}$$

| A | B | C | D | F |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |



⑯ Resolver la siguiente función lógica
utilizando dos Mux de 4:1. Usted
tiene un multiplexor tipo M_1 y otro M_2

Mux 1

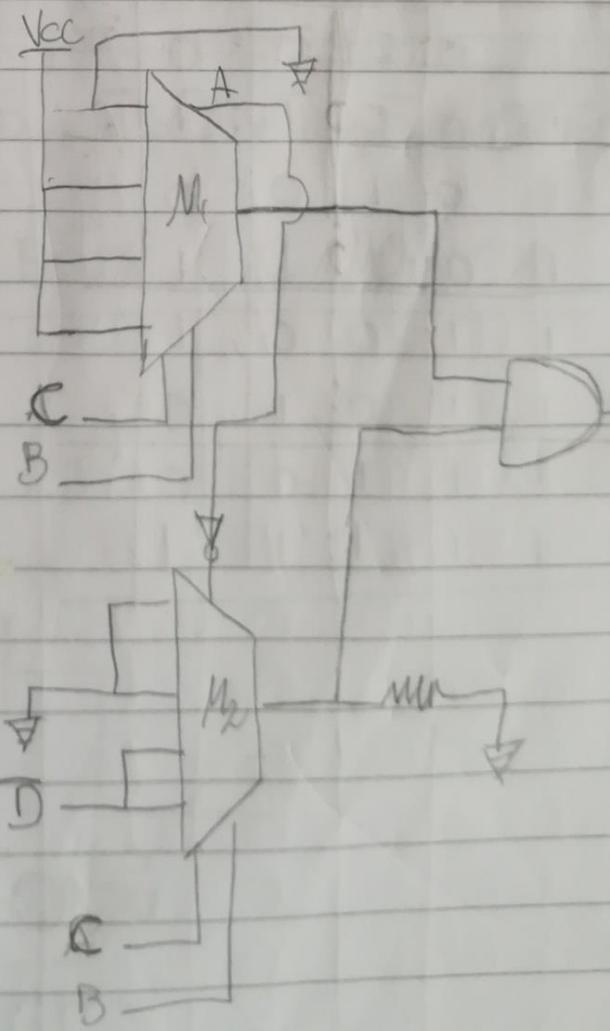
| CE | A | B | out |
|----|---|---|-----------------|
| 1 | X | X | 1 |
| 0 | 0 | 0 | In ₀ |
| 0 | 0 | 1 | In ₁ |
| 0 | 1 | 0 | In ₂ |
| 0 | 1 | 1 | In ₃ |

Mux 2

| CE | A | B | out |
|----|---|---|-----------------|
| 0 | X | X | Z |
| 1 | 0 | 0 | In ₀ |
| 1 | 0 | 1 | In ₁ |
| 1 | 1 | 0 | In ₂ |
| 1 | 1 | 1 | In ₃ |

$$F = \overline{\Pi} 0, 2, 4, 5, 6, 7, 14, 15$$

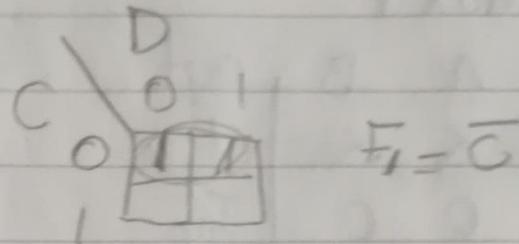
| A | B | C | D | F |
|-------|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| <hr/> | | | | |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| <hr/> | | | | |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| <hr/> | | | | |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| <hr/> | | | | |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| <hr/> | | | | |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| <hr/> | | | | |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| <hr/> | | | | |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |
| <hr/> | | | | |



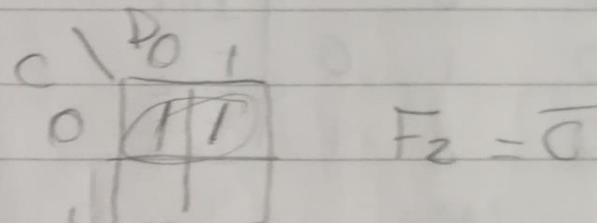
10) Implementar con Max de 4 Entradas la siguiente función

$$F = \sum 0, 1, 4, 5, 9, 11, 12, 15$$

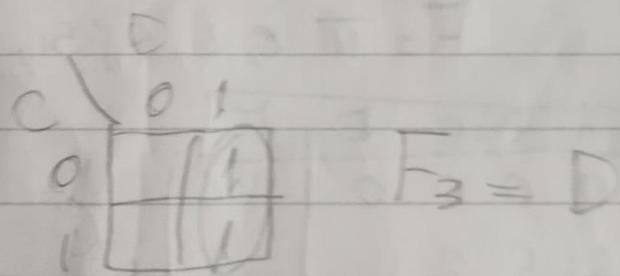
| A | B | C | D | F |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |



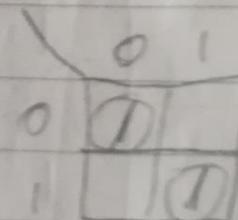
$$F_1 = \bar{C}$$



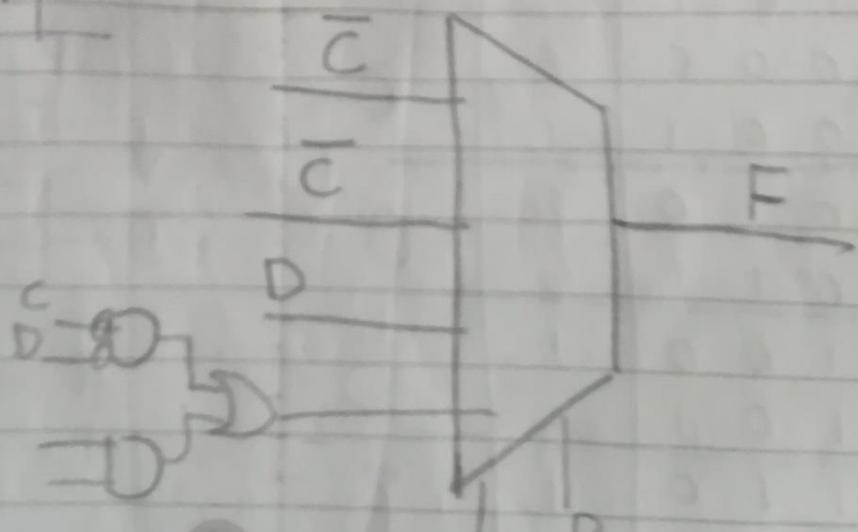
$$F_2 = \bar{D}$$



$$F_3 = D$$



$$F_4 = \bar{C} \bar{D}$$



(21) Expresar las sigles. función lógica de 4 variables en su forma canónica, como suma de productos, minimizar por Karnaugh. Implementar utilizando 2 multiplexores de 4:1 cuya tabla se presenta en tabla 1.

| A | B | C | D | F |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

$$F = \overline{D} \cdot 0, 1, 4, 5, 6, 8, 11, 12, 13, 14$$

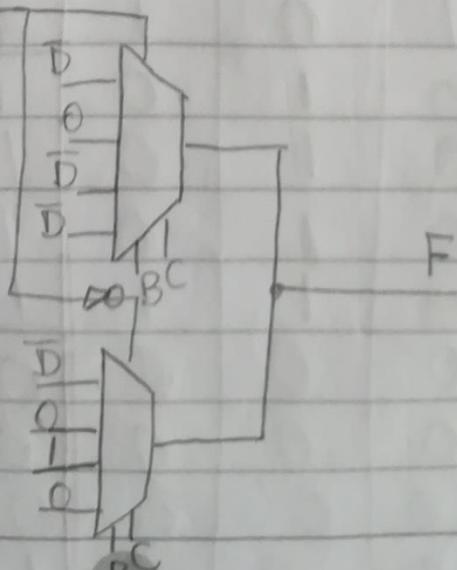
| CD | AB | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|
| 00 | 00 | 1 | | | |
| 01 | 01 | | 1 | | |
| 11 | 11 | | | 1 | 1 |
| 10 | 10 | | | | 1 |

$$F = AB\bar{C} + B\bar{C}D + B\bar{C}\bar{D} + \bar{A}BC\bar{D}$$

$$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}D$$

+ $A\bar{B}\bar{C}D$ CANONICA

| E | A | B | out |
|---|---|---|----------------|
| 0 | 0 | 0 | 1 ₀ |
| 0 | 0 | 1 | 1 ₁ |
| 0 | 1 | 0 | 1 ₂ |
| 0 | 1 | 1 | 1 ₃ |
| 1 | x | x | z |



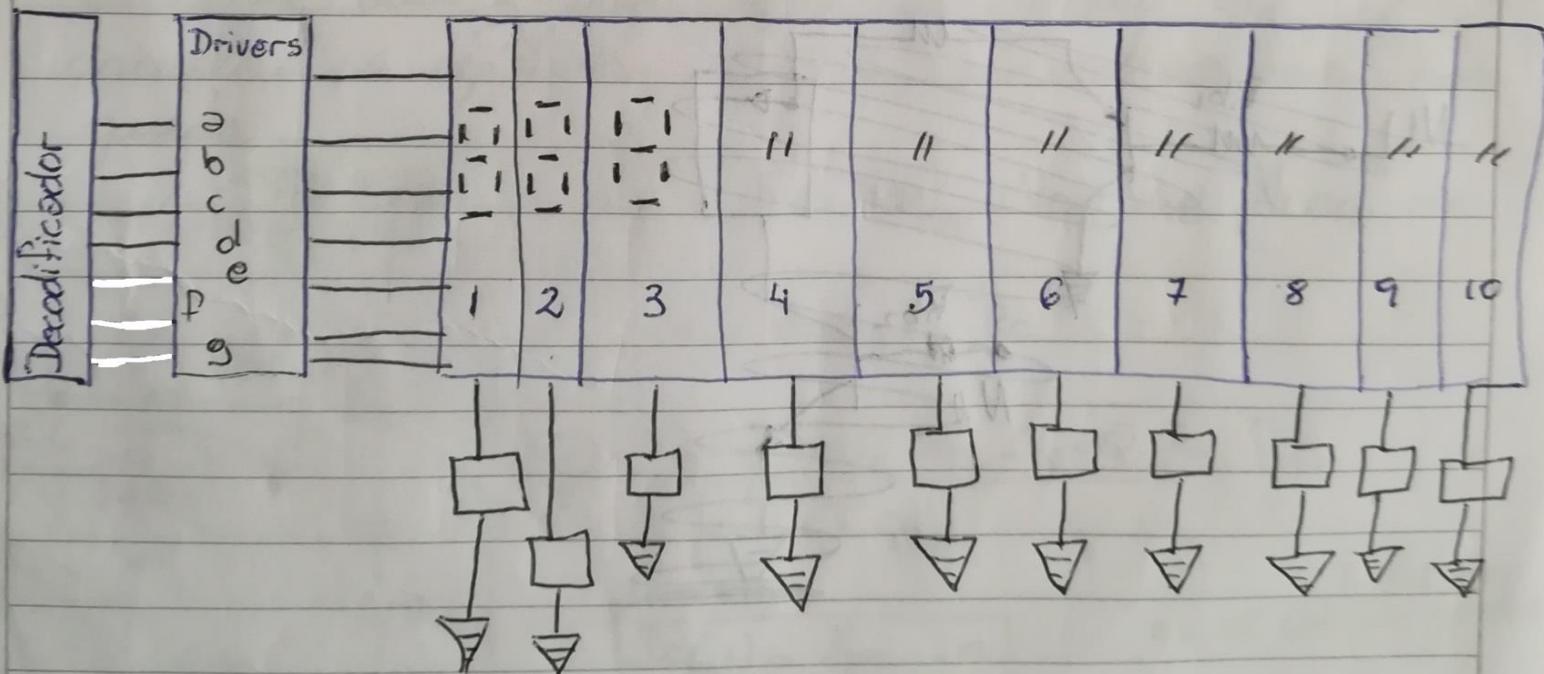
Diseñar drivers necesarios para activar "10" display de 7 segmentos, (modo común), sistema multiplicador. La "I" p_rm_as de los segmentos es 20 mA.

Realizar el diagrama en bloque del sistema
Dibujar cada uno de los drivers necesarios
Realizar la selección de los componentes y el cálculo de la potencia disipada en los mismos

- a) $\beta = 100$
- b) $V_{CC} = 5V$
- c) $V_{CE} = 0.2V$

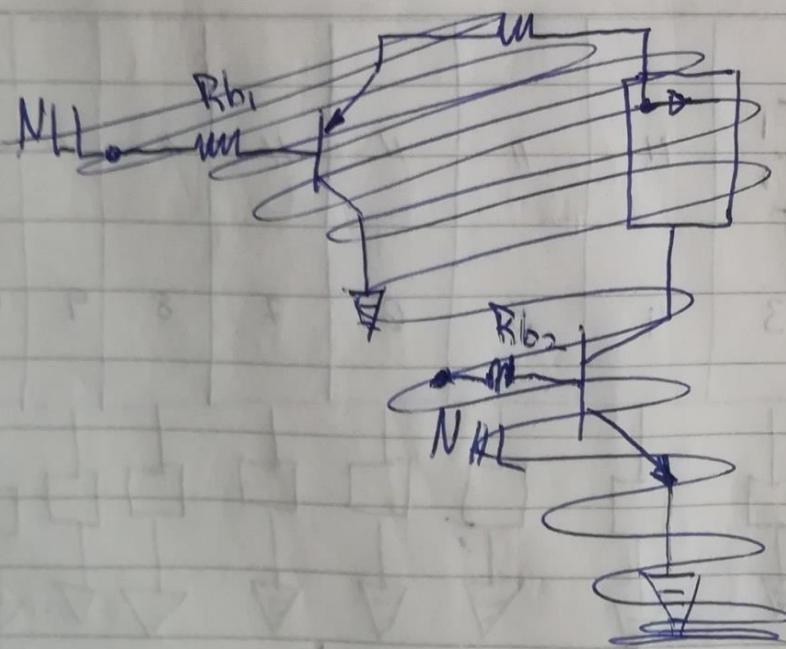
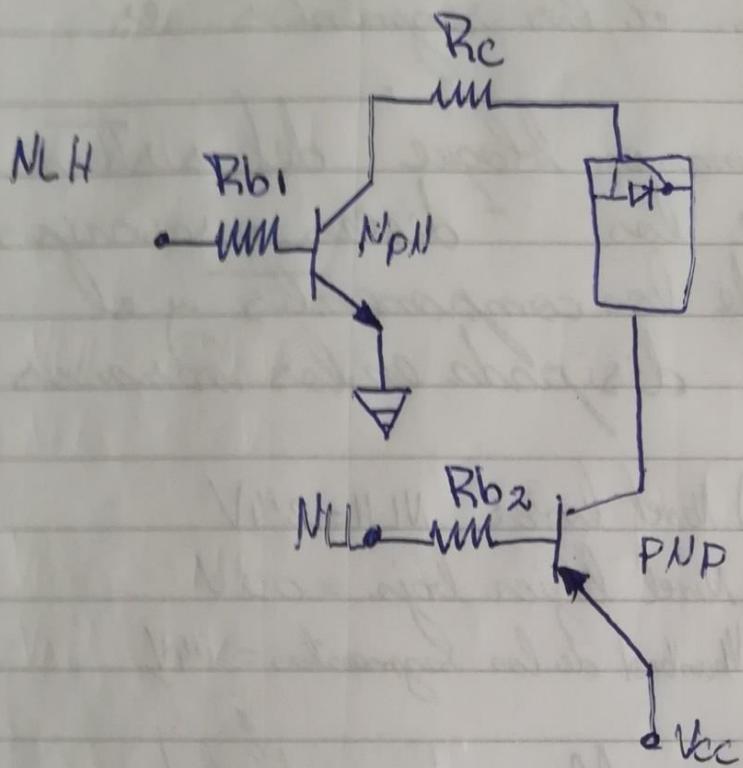
- d) Nivel lógica NLH = 2.4V
- e) Nivel lógica baja = 0.2V
- f) Umbral de los segmentos = 1.4V

~~Diagrama~~ Diagrama en bloque del led

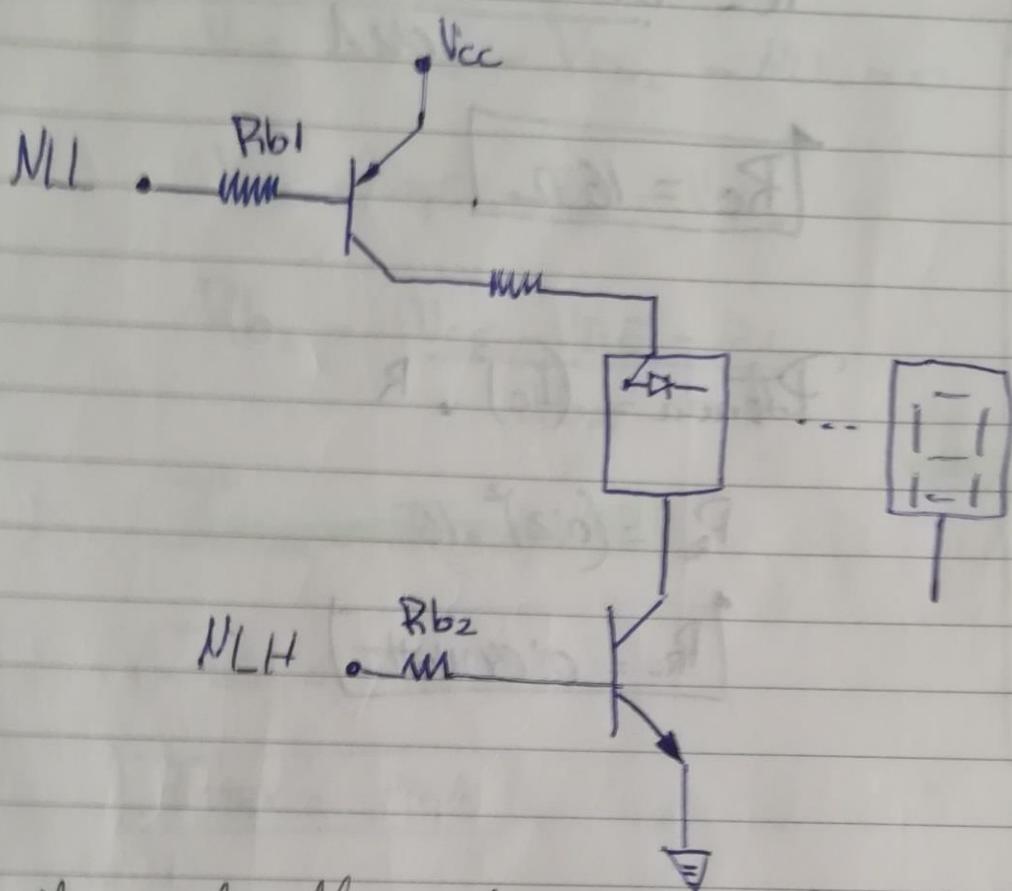


cheque

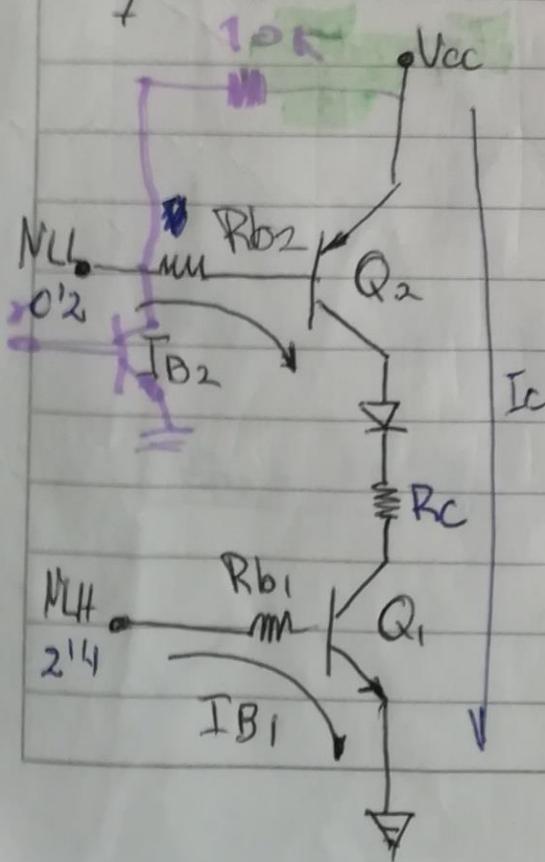
② Modo Comum



Catodo Común



El nivel alta y baja serán las entradas V_{dd} , el circuito se repite 10 veces, si redimensionamos nos quedará



$$V_{cc} - V_{ceQ_2} - V_D - V_{RC} - V_{ceQ_1} = 0$$

Lo q' busco es "Rc"

$$\frac{V_{cc} - V_{ceQ_2} - V_D - V_{ceQ_1}}{I_{C(ed)}} = R_c$$

$$I_{C(ed)} = I_{prom \cdot n}$$

$n = n^{\circ}$ de segmentos
display

$$I_{C(ed)} = 0,02A \cdot 10$$

$$I_{C(ed)} = 0,2A$$

Datos

$$V_{CC} = 5V$$

$$\beta = 100$$

$$I_{\text{prom}} = 20 \text{ mA}$$

$$V_{CC \text{ sat}} = 0.2V$$

$$N_{LH} = 2.4V$$

$$N_{LL} = 0.2V$$

$$V_{LED} = 1.4$$

$$V_{BE} = 0.7$$

$$R_E = \frac{5V - 0.2 - 1.4 - 0.2V}{0.2A}$$

$$R_E = 16 \Omega$$

$$\text{Potencia} = (I_C)^2 \cdot R$$

$$P_{RE} = (0.2)^2 \cdot 16$$

$$P_{RE} = 0.64 \text{ Watt}$$

(2)

Malla p/ R_{B1}

$$V_{BB} - V_{BE} - V_{B1} = 0$$

$$I_{B1} = \frac{I_C}{B}$$

$$\frac{2.4 - 0.7}{0.2A} = R_1$$

$$R_{B1} = 850 \Omega$$

$$P_{RB1} = \left(\frac{0.2 \text{ mA}}{100} \right)^2 \cdot 850 \Omega$$

$$P_{RB1} = 0.0034 \text{ W}$$

Malla p/ calcular R_{b2}

$$V_{CC} - V_{BE} - V_{Rb2} - NLL = 0$$

$$V_{CC} - V_{BE} - NLL = V_{Rb2}$$

$$R_{b2} = \frac{V_{CC} - V_{BE} - NLL}{I_{b2}}$$

$$I_{max} = I_{d(Led)} \cdot n'$$

n' = numero de segmentos

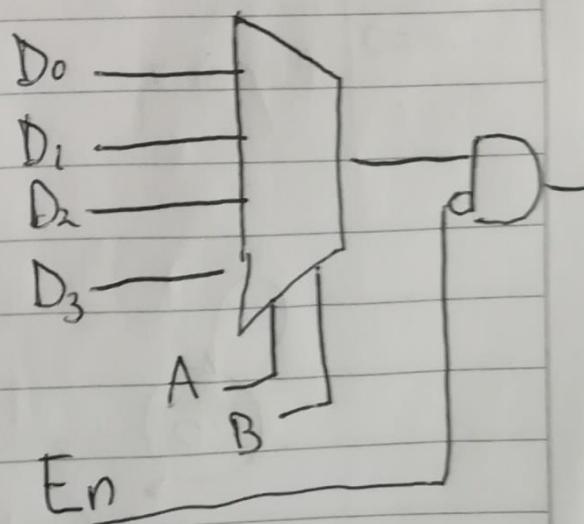
$$I_{max} = 7.012 A$$

$$\boxed{I_{max} = 114 A}$$

$$I_{b2} = \frac{I_{max}}{100}$$

$$I_{b2} = \frac{114}{100}$$

$$\boxed{I_{b2} = 0.114 A}$$



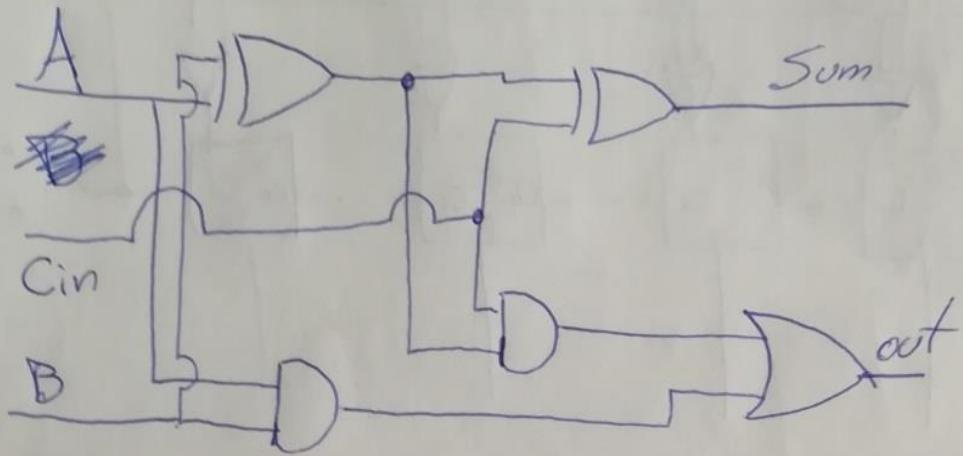
$$R_{b2} = \frac{5V - 0.7V - 0.2V}{0.114 A}$$

$$R_{b2} = 2921.8 \Omega$$

Aritmética Diseño de sumadores - Típicos de parcial y final

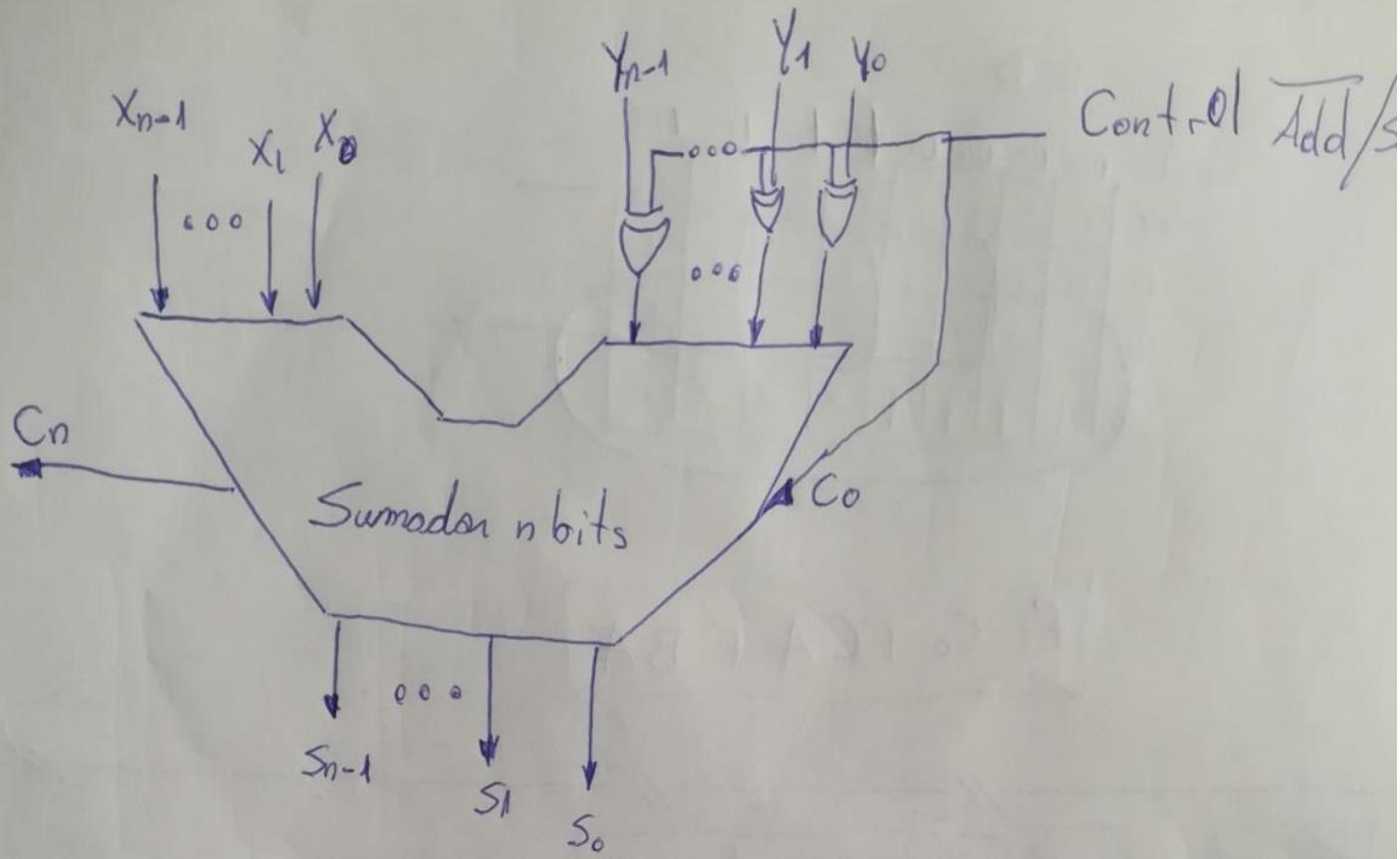
Como los del libro de caballero están mal algunos (varios muchos ejer), rompi las pelotas a guille para que me enseñara, como resultado salió esto

Sumador completa de 1 bit



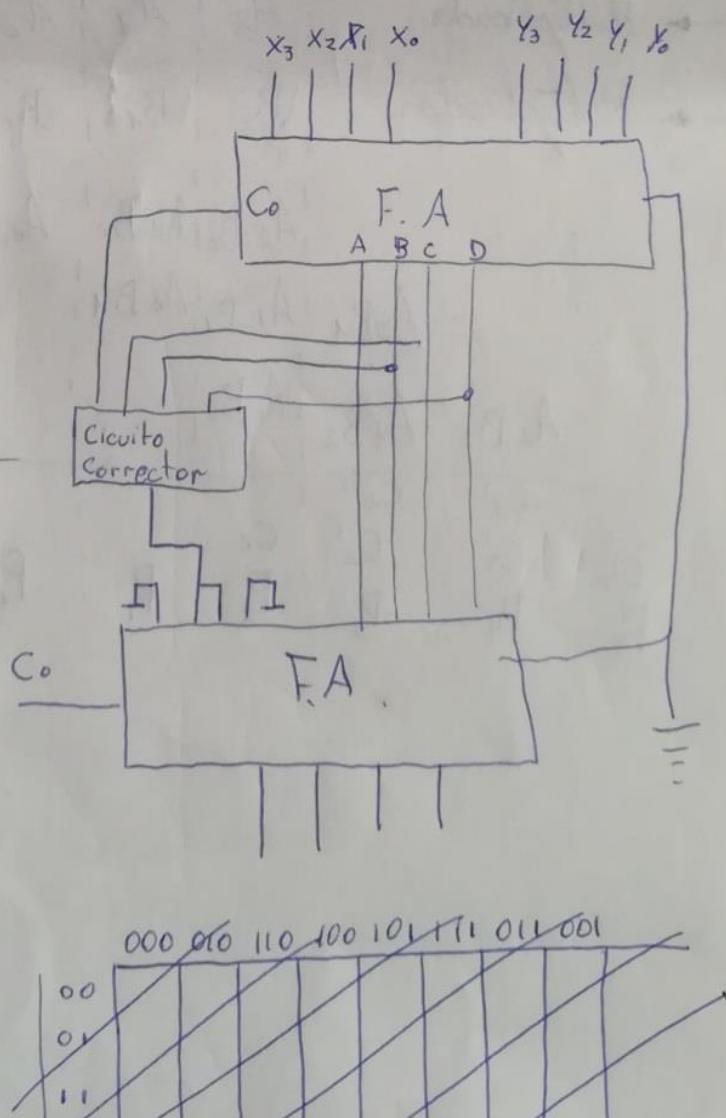
Unidad Sumadora y restadora

- para la resta es necesario un complemento A_2
 - los operandos " x " e " y "
 - " y " Funciona como sustraendo en la resta
 - Los resultados de las compuertas XOR representan " y " si $\overline{\text{Add/Sub}} = 0$
 - Si $\overline{\text{Add/Sub}} = 1$ representa el complemento A_1 de " y "
 - $\overline{\text{Add/Sub}}$ tambien se conecta al acarre C_0
- $C_0 = 1$ se realiza la resta, x lo lanza sumo el 1 q' necesita para el complemento A_2



Sumador BCD con detalles

| C_0 | A | B | C | D | |
|-------|-----|-----|-----|-----|---|
| 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 0 | 0 | 0 |
| 6 | 0 | 1 | 0 | 1 | 0 |
| 7 | 0 | 1 | 1 | 0 | 0 |
| 8 | 0 | 1 | 1 | 1 | 0 |
| 9 | 1 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 0 | 1 | 0 |
| | 0 | 1 | 0 | 0 | 1 |
| | 0 | 1 | 0 | 1 | 1 |
| | 0 | 1 | 1 | 0 | 0 |
| | 0 | 1 | 1 | 0 | 1 |
| | 0 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 0 | 0 | 0 |
| | 1 | 0 | 0 | 1 | 1 |
| | 1 | 0 | 1 | 0 | 0 |
| | 1 | 0 | 1 | 0 | 1 |
| | 1 | 0 | 1 | 1 | 1 |



| | | BCD | | | | | | | | | |
|----------------|---|----------------|---|-----|-----|-----|-----|-----|-----|-----|-----|
| | | C ₀ | A | 000 | 001 | 011 | 010 | 110 | 111 | 101 | 100 |
| C ₀ | A | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 01 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 11 | X | X | X | X | X | X | X | X | X | X | X |
| 10 | 1 | 1 | 1 | 1 | X | X | X | X | X | X | X |

$$F = C_0 + CA + BA$$

Circuito de Multiplicación Binaria

→ Multiplicanda

| | | |
|----------------|----------------|----------------|
| A ₂ | A ₁ | A ₀ |
|----------------|----------------|----------------|

→ Multiplicador

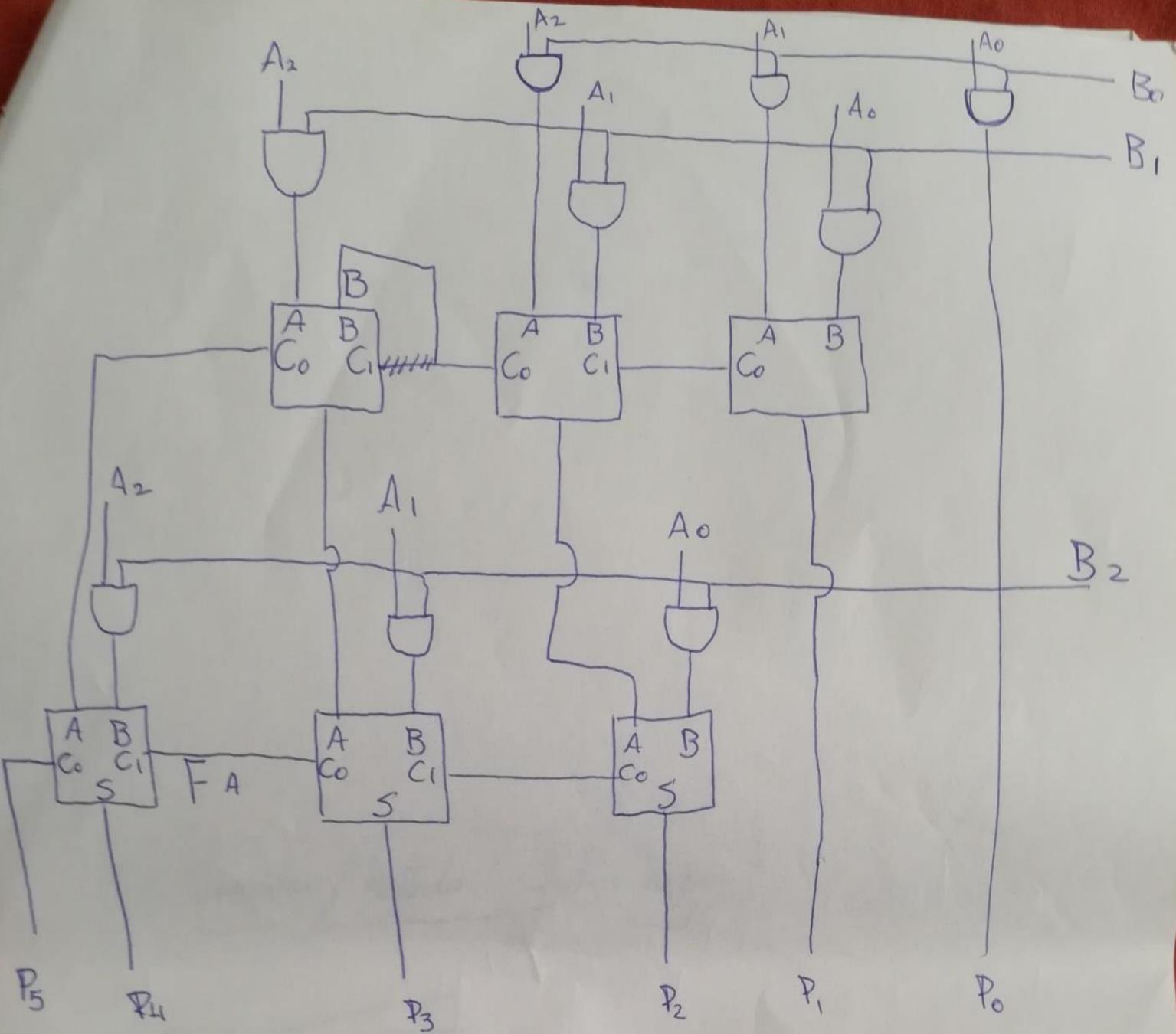
| | | |
|----------------|----------------|----------------|
| B ₂ | B ₁ | B ₀ |
|----------------|----------------|----------------|

| | | |
|--------------------------------|--------------------------------|--------------------------------|
| A ₂ .B ₀ | A ₁ .B ₀ | A ₀ .B ₀ |
|--------------------------------|--------------------------------|--------------------------------|

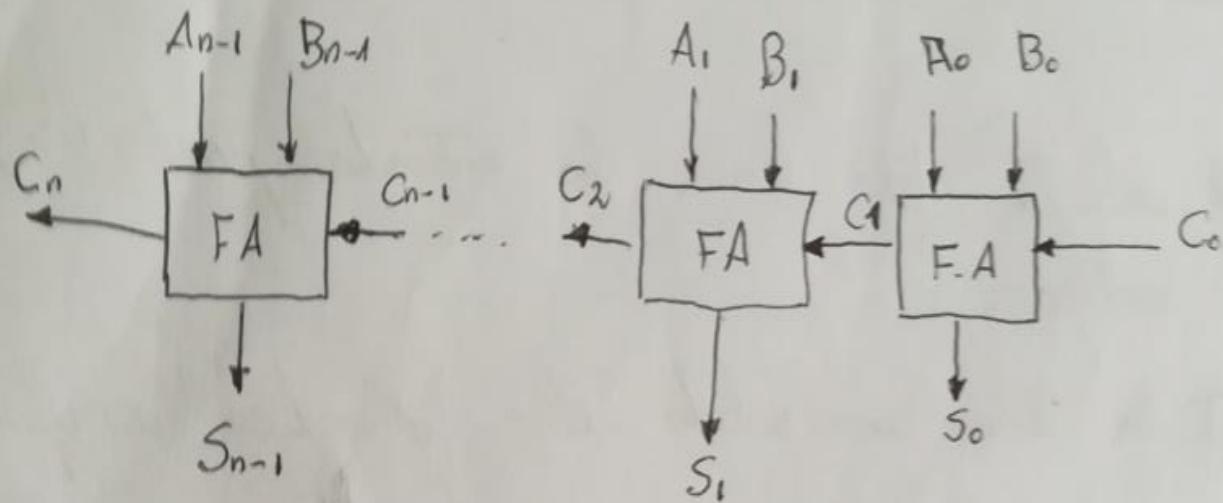
| | | |
|------------------------------------|------------------------------------|------------------------------------|
| (A ₂ .B ₁) | (A ₁ .B ₁) | (A ₀ .B ₁) |
|------------------------------------|------------------------------------|------------------------------------|

| | | |
|------------------------------------|------------------------------------|------------------------------------|
| (A ₂ .B ₂) | (A ₁ .B ₂) | (A ₀ .B ₂) |
|------------------------------------|------------------------------------|------------------------------------|

| | | | |
|----------------|----------------|----------------|----------------|
| C ₃ | C ₂ | C ₁ | P ₀ |
| C ₄ | C ₃ | C ₂ | P ₁ |
| P ₅ | D ₄ | P ₃ | P ₂ |



Ejemplo de Diseño

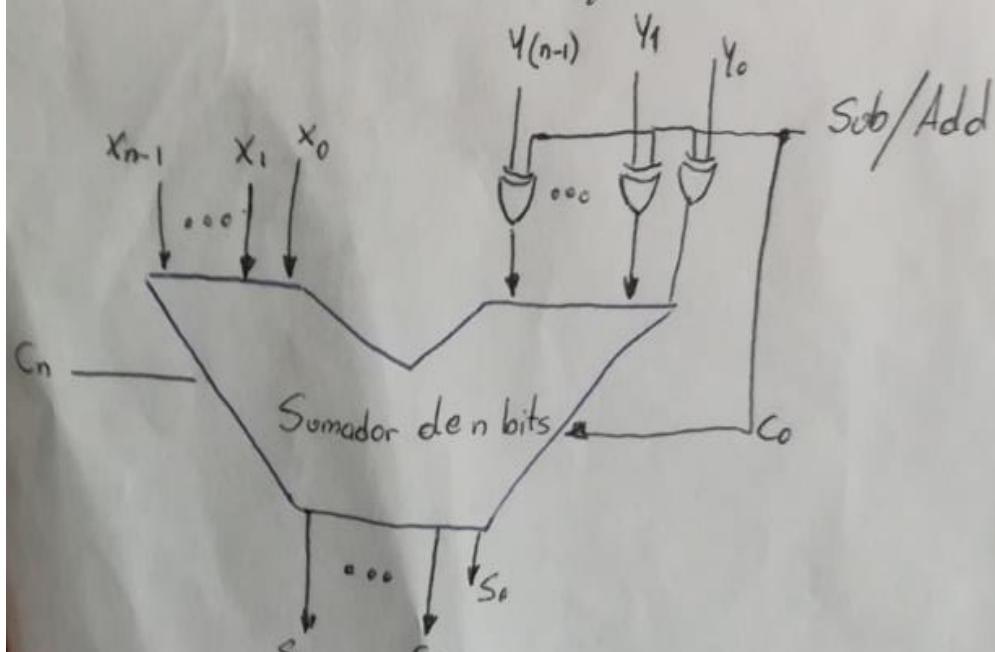


Sumadores de n -bits con acarreo en cascada.

Con signo

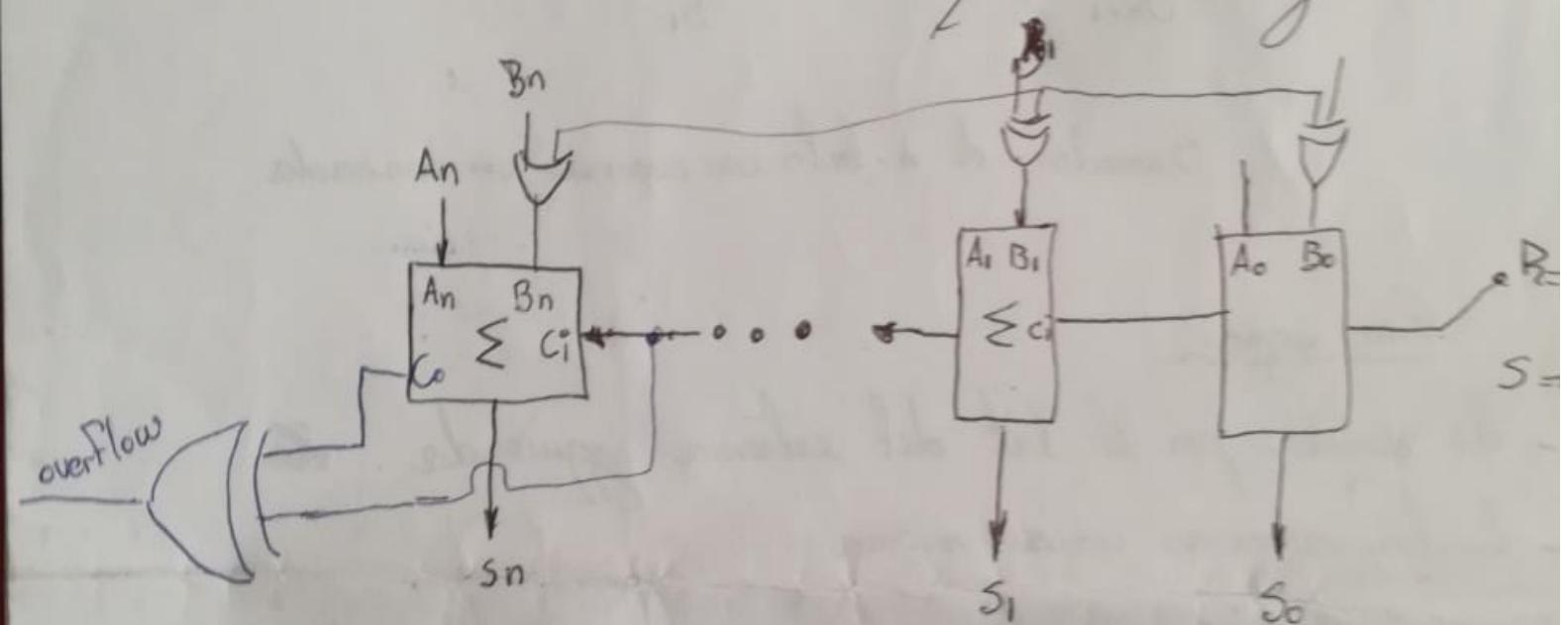
- Se denota por el bit del extremo izquierda.
- En los numeros con signo

Unidad Sumadora / Restadora



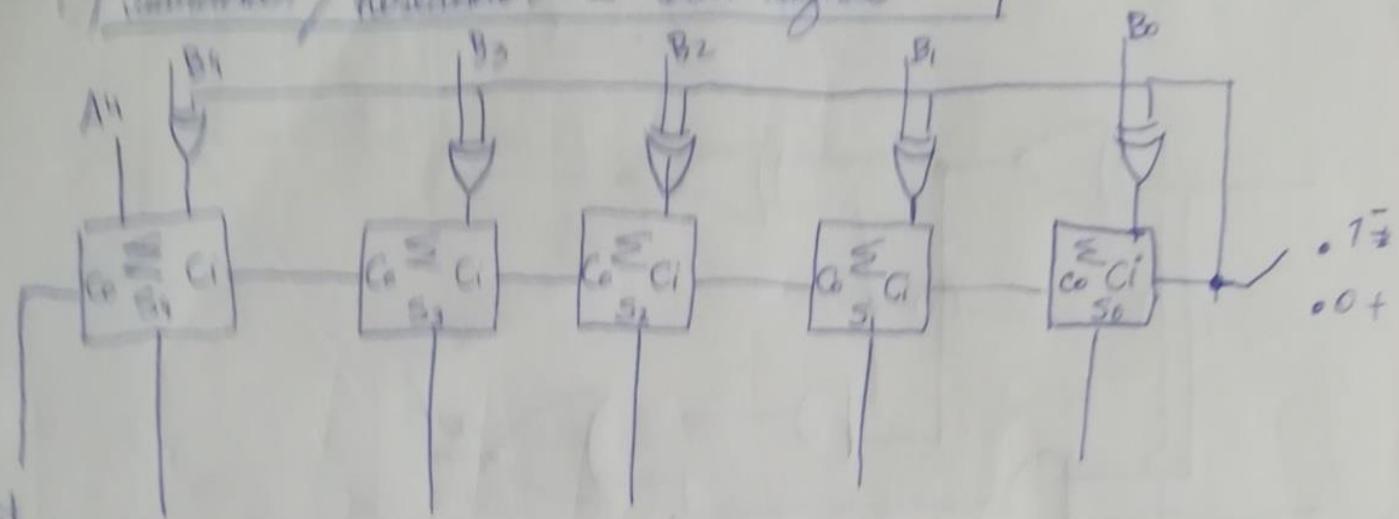
* Diseñe un sumador binario, los n° están en complemento A₂

- El circuito debe tener la entrada para la operación a realizar
- Debe tener una salida extra que indica overflow.



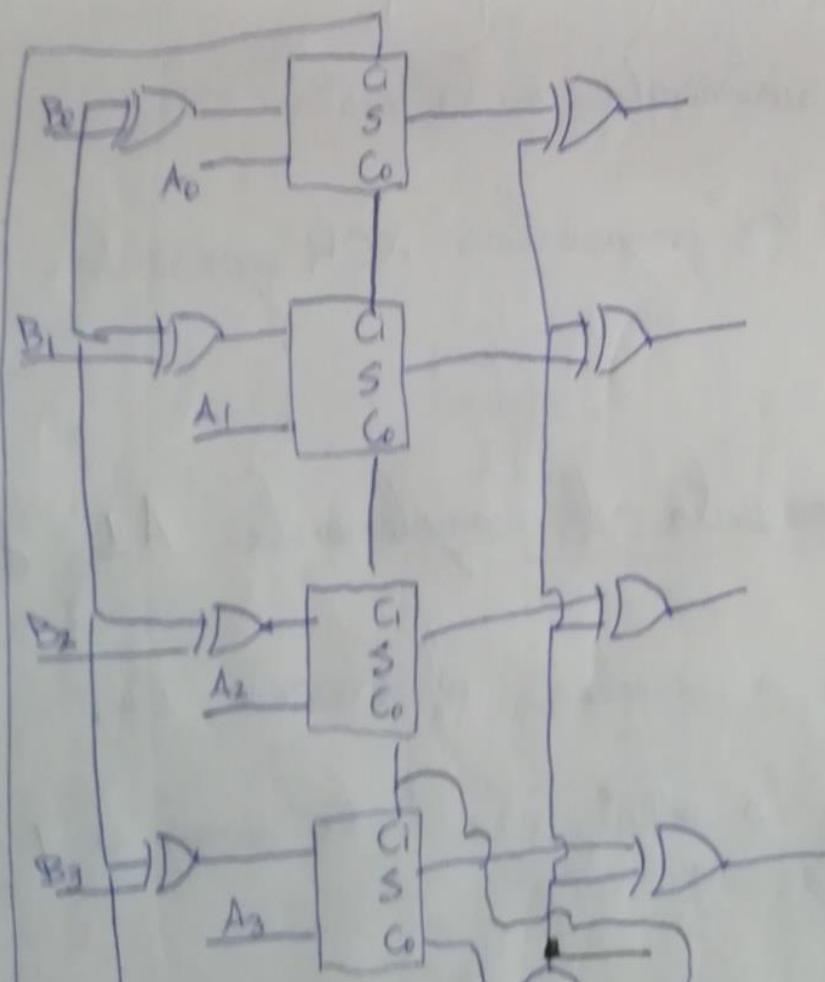
Resumen de sumador

Sumador / Restador - Con signo

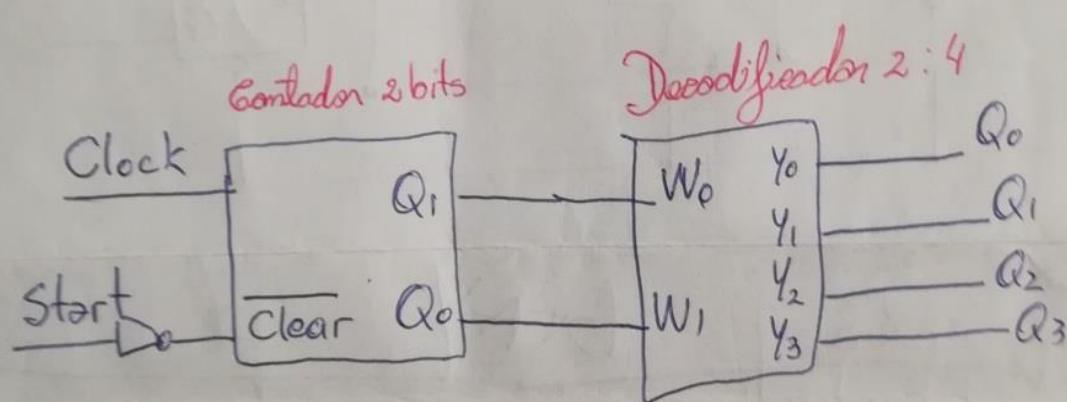
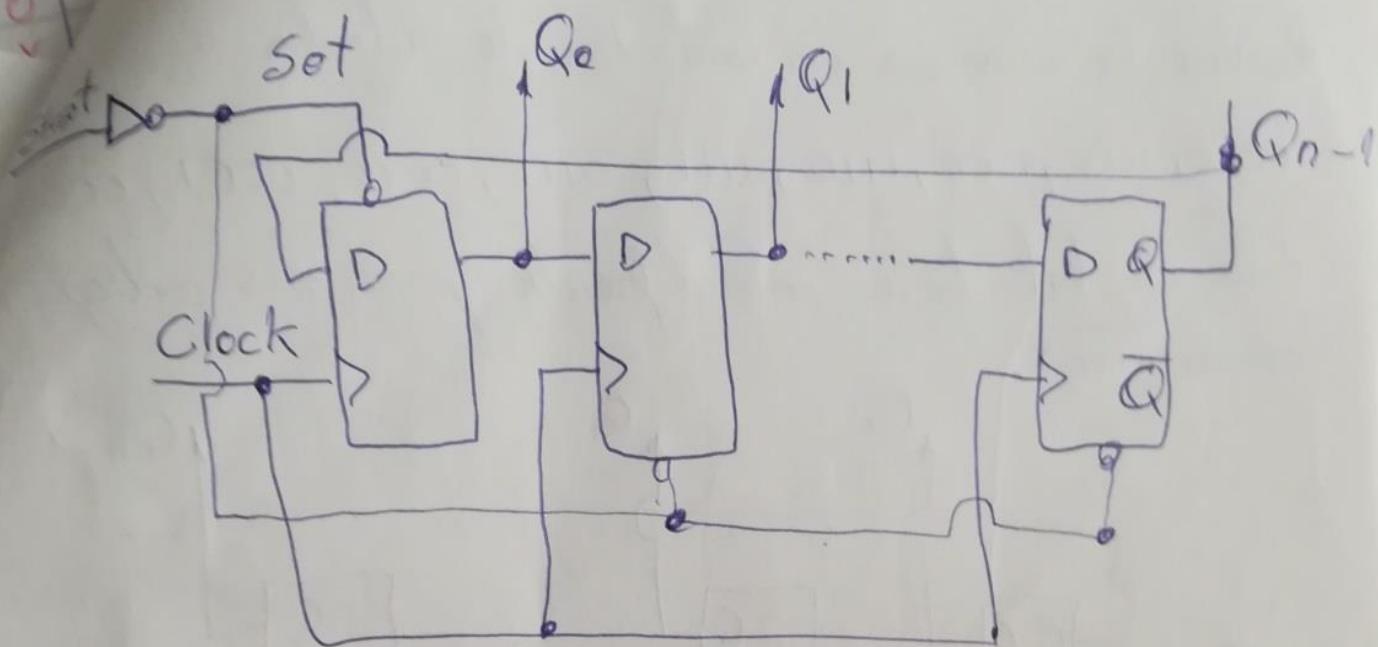


Bit
del
signo

Sumador / Restador - Sin signo



Contador Anilla



los códigos posibles serán Q_0, Q_1, Q_2, Q_3
 $1000, 0100, 0010, 0001$. Solo habrá un solo 1
"codificación de 1 activo" es el nombre

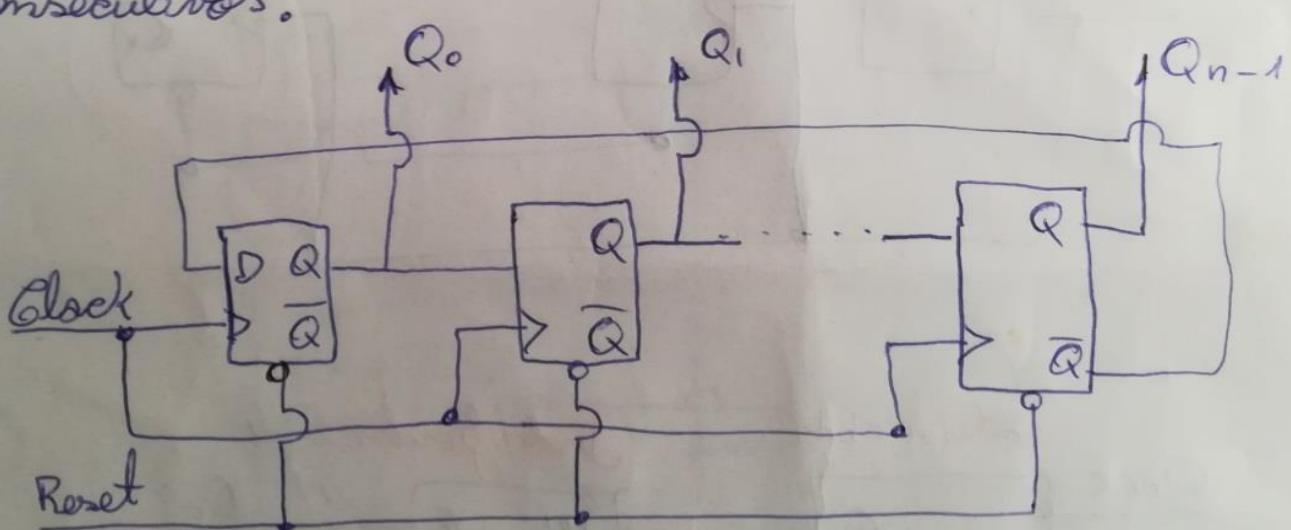
Funcionamiento: inicia inyectando un "1" en la Q_0 de la primera F.F., lo que se logra utilizando la señal de control Start, que pone a 1 el FF del extremo izquierdo y borra los otros FF. hasta dejarlos en cero. Todo ocurre después del frente positivo.

Contador Johnson

Produce la secuencia un contador de 4 bits

0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000

Solo un bit tiene valor diferente para dos códigos consecutivos.



Fin .