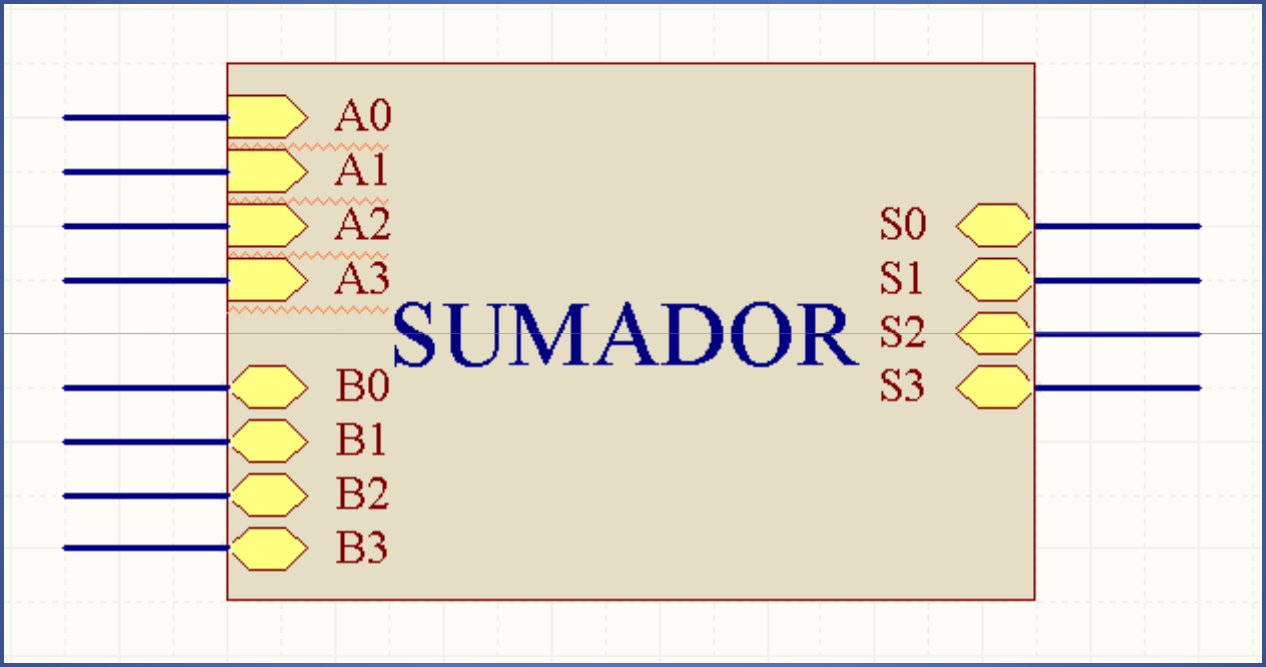
VHDL

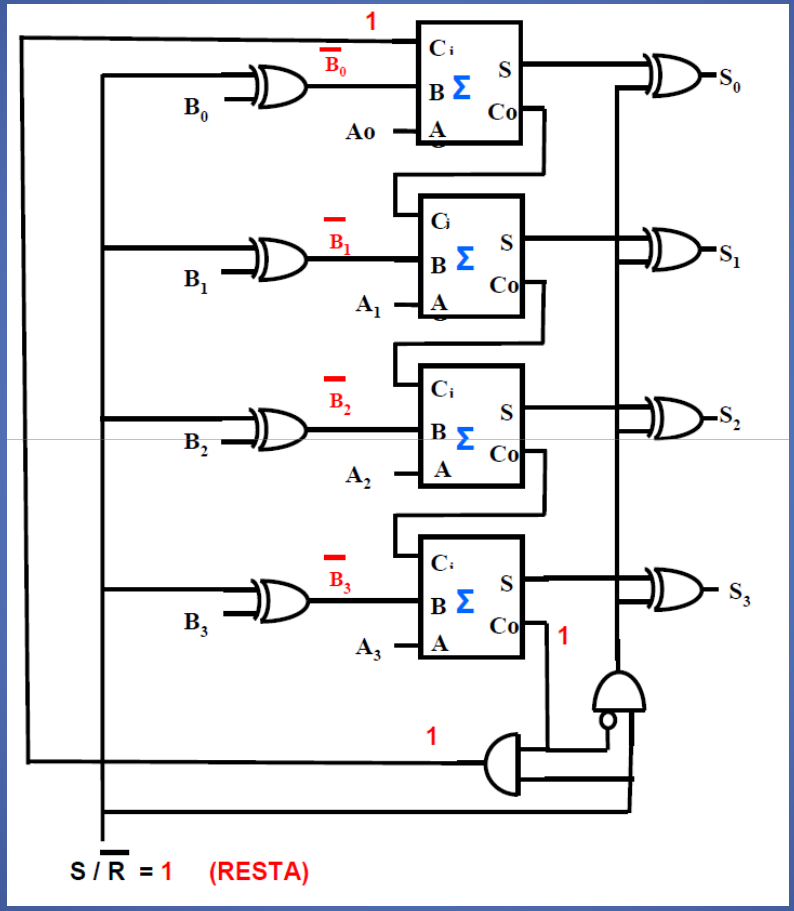
INSTANCIACION DE COMPONENTES
ARITMETICA BINARIA

Técnicas Digitales I -Ing. Francisco G. Gutiérrez 2012

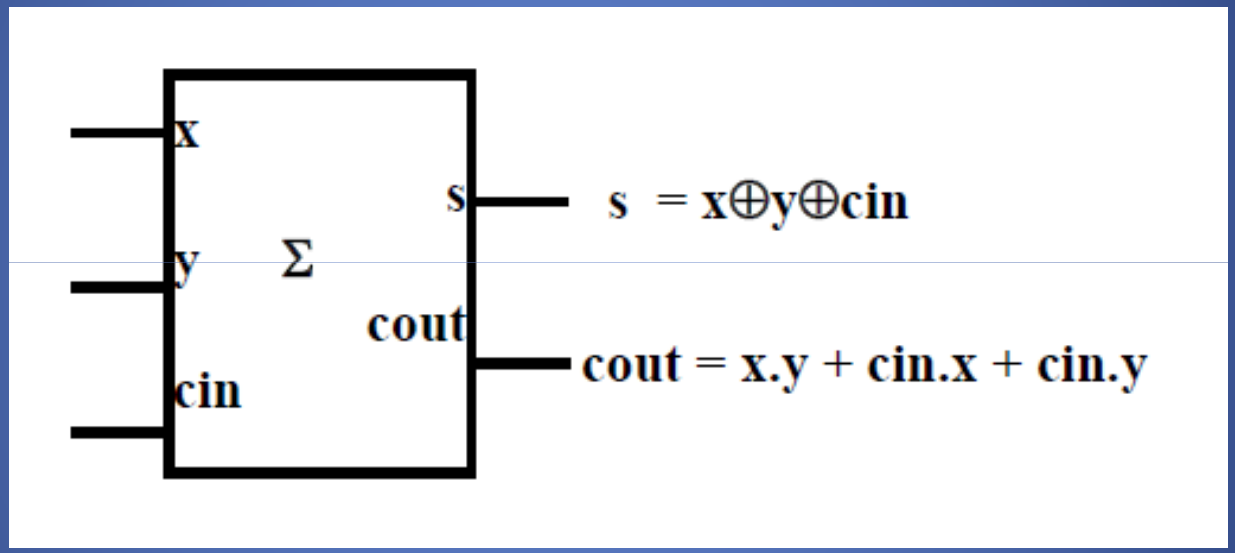
Concepto



Concepto


1
$\overline{B_0}$
B_0
Ao
Ci
B Σ
A
S
Co
S_0
$\overline{B_1}$
B_1
A_1
S_1
$\overline{B_2}$
B_2
A_2
S_2
$\overline{B_3}$
B_3
A_3
S_3
1
1
S / $\overline{R}$ = 1 (RESTA)

Definición de un componente
Esquema del componente



Definición de un componente
Descripcion del componente

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY sumador1Bit IS
PORT (cin, x, y : IN STD_LOGIC;
s, cout : OUT STD_LOGIC);
END sumador1bit;

ARCHITECTURE LogicFunc OF fulladd IS
BEGIN
s <= (x XOR y XOR cin);
cout<= (x AND y) OR (cin AND x) OR ( cin AND Y);
END LogicFunc;
```

Definición de un componente component

```
ARCHITECTURE behavior OF sumador_Test_sumador_vhd_tb IS
COMPONENT sumador 1Bit
PORT(
        cin, x, y : IN STD_LOGIC;
        s, cout : OUT STD_LOGIC);
);
BEGIN
```

Conexión del componente port map

```
BEGIN
Componente1: sumador PORT MAP(
Cin => A(0),
x => B(0),
y => Cin(0),
S => s(0),
Cout => Cout(0)
);
```

Sumador de 4 bit

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY sumado 4 bit IS
PORT (
            cin, x, y : IN STD_LOGIC_VECTOR(3 downto 0);
            s, cout : OUT STD_LOGIC_VECTOR(3 downto
0));
END fulladd;

ARCHITECTURE LogicFunc OF fulladd IS

BEGIN
Componente1: sumador PORT MAP…..
Componente2: sumador PORT MAP ….
Componente3: sumador PORT MAP….
Componente4: sumador PORT MAP….
```

VHDL – USO DE LA LIBRERÍA use IEEE.STD_LOGIC_SIGNED.ALL;

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity bcd_7segment is
    Port (      numero1: in std_logic_vector(3 downto 0);
                numero2: in std_logic_vector(3 downto 0);
                suma: OUT std_logic_vector(3 downto 0));
end bcd_7segment;

architecture Behavioral of bcd_7segment is
begin
                suma<=numero1+numero2;
end Behavioral;
```

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