

1. Multiplicador básico

Elementos de hardware

+-----+-----+-----+-----+-----+						Report Cell Usage:		
+-----+-----+-----+-----+-----+						+-----+-----+-----+		
Site Type Used Fixed Available Util%						Cell Count		
+-----+-----+-----+-----+-----+						+-----+-----+-----+		
Slice LUTs* 16 0 20800 0.08						1 CARRY4 2		
LUT as Logic 16 0 20800 0.08						2 LUT2 3		
LUT as Memory 0 0 9600 0.00						3 LUT3 1		
Slice Registers 0 0 41600 0.00						4 LUT4 4		
Register as Flip Flop 0 0 41600 0.00						5 LUT5 1		
Register as Latch 0 0 41600 0.00						6 LUT6 10		
F7 Muxes 0 0 16300 0.00						7 IBUF 8		
F8 Muxes 0 0 8150 0.00						8 OBUF 8		
+-----+-----+-----+-----+-----+						+-----+-----+-----+		

Caminos

Síntesis

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
↳ Path 1	∞	5	4	13	Y[1]	Z[6]	8.457	5.944	2.512
↳ Path 2	∞	5	4	13	Y[1]	Z[5]	8.347	5.835	2.512
↳ Path 3	∞	5	4	13	Y[1]	Z[7]	8.259	5.747	2.512
↳ Path 4	∞	5	4	13	Y[1]	Z[4]	8.153	5.641	2.512
↳ Path 5	∞	4	3	13	Y[1]	Z[3]	7.810	5.737	2.073
↳ Path 6	∞	4	3	13	X[1]	Z[2]	7.470	5.870	1.599
↳ Path 7	∞	4	3	10	X[0]	Z[1]	7.312	5.713	1.599
↳ Path 8	∞	4	3	10	X[0]	Z[0]	7.099	5.500	1.599

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
↳ Path 9	∞	4	3	9	X[3]	Z[7]	2.253	1.578	0.674	-∞
↳ Path 10	∞	4	3	11	Y[2]	Z[2]	2.268	1.594	0.674	-∞
↳ Path 11	∞	4	3	9	X[3]	Z[6]	2.272	1.598	0.674	-∞
↳ Path 12	∞	4	3	9	Y[0]	Z[0]	2.274	1.600	0.674	-∞
↳ Path 13	∞	4	3	9	X[3]	Z[3]	2.275	1.601	0.674	-∞
↳ Path 14	∞	4	3	9	X[3]	Z[4]	2.276	1.601	0.674	-∞
↳ Path 15	∞	4	3	9	X[3]	Z[5]	2.279	1.605	0.674	-∞
↳ Path 16	∞	4	3	9	Y[0]	Z[1]	2.297	1.622	0.674	-∞

Implementación

Name	Slack ^{^1}	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
↳ Path 1	∞	6	4	11	Y[2]	Z[6]	10.819	6.022	4.797	∞
↳ Path 2	∞	5	3	13	X[1]	Z[7]	10.755	5.967	4.788	∞
↳ Path 3	∞	6	4	11	Y[2]	Z[4]	10.740	6.004	4.736	∞
↳ Path 4	∞	6	4	11	Y[2]	Z[5]	10.732	6.126	4.606	∞
↳ Path 5	∞	5	3	11	Y[2]	Z[3]	10.424	5.637	4.787	∞
↳ Path 6	∞	4	2	10	X[0]	Z[1]	10.049	5.513	4.536	∞
↳ Path 7	∞	4	2	10	X[0]	Z[2]	9.666	5.836	3.830	∞
↳ Path 8	∞	4	2	9	Y[0]	Z[0]	8.678	5.502	3.177	∞

Name	Slack ^{^1}	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
↳ Path 9	∞	4	2	8	X[2]	Z[2]	2.484	1.608	0.876	-∞
↳ Path 10	∞	4	2	10	X[0]	Z[0]	2.518	1.604	0.914	-∞
↳ Path 11	∞	4	2	13	X[1]	Z[6]	2.535	1.611	0.925	-∞
↳ Path 12	∞	4	2	9	X[3]	Z[3]	2.543	1.600	0.943	-∞
↳ Path 13	∞	4	2	9	Y[0]	Z[5]	2.548	1.606	0.941	-∞
↳ Path 14	∞	4	2	9	X[3]	Z[4]	2.553	1.603	0.950	-∞
↳ Path 15	∞	4	2	13	X[1]	Z[7]	2.573	1.590	0.983	-∞
↳ Path 16	∞	4	2	13	Y[1]	Z[1]	2.895	1.637	1.259	-∞

2. Multiplicador con sumadores

Elementos de hardware

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	15	0	20800	0.07
LUT as Logic	15	0	20800	0.07
LUT as Memory	0	0	9600	0.00
Slice Registers	0	0	41600	0.00
Register as Flip Flop	0	0	41600	0.00
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

Report Cell Usage:

Cell	Count
LUT2	1
LUT4	6
LUT6	11
IBUF	8
OBUF	8

Caminos

Síntesis

SYNTHESIZED DESIGN - xc7a35tcbg236-1

Tcl ConsoleMessagesLogReportsDesign RunsTiming

SYNTHESIZED DESIGN - xc7a35tcbg236-1

Tcl ConsoleMessagesLogReportsDesign RunsTiming

Unconstrained Paths - NONE - NONE - Hold

General Information

Timer Settings

Design Timing Summary

Check Timing (0)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

Unconstrained Paths

NONE to NONE

Setup (8)

Hold (8)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
↳ Path 9	∞	3	2	7	X[3]	Z[7]	2.138	1.463	0.674	-∞	input port clock
↳ Path 10	∞	3	2	8	Y[2]	Z[2]	2.139	1.465	0.674	-∞	input port clock
↳ Path 11	∞	3	2	7	X[3]	Z[6]	2.143	1.469	0.674	-∞	input port clock
↳ Path 12	∞	3	2	7	Y[0]	Z[0]	2.144	1.470	0.674	-∞	input port clock
↳ Path 13	∞	3	2	8	Y[2]	Z[3]	2.147	1.473	0.674	-∞	input port clock
↳ Path 14	∞	3	2	7	Y[3]	Z[4]	2.156	1.482	0.674	-∞	input port clock
↳ Path 15	∞	3	2	7	Y[3]	Z[5]	2.162	1.487	0.674	-∞	input port clock
↳ Path 16	∞	3	2	7	Y[0]	Z[1]	2.168	1.493	0.674	-∞	input port clock

Implementación

Name	Slack ^{^1}	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
↳ Path 1	∞	6	5	12	X[1]	Z[6]	11.331	5.693	5.638	∞
↳ Path 2	∞	6	5	12	X[1]	Z[7]	11.299	5.688	5.611	∞
↳ Path 3	∞	6	5	12	X[1]	Z[5]	10.965	5.702	5.263	∞
↳ Path 4	∞	5	4	10	X[2]	Z[4]	10.712	5.574	5.138	∞
↳ Path 5	∞	4	3	8	Y[2]	Z[3]	9.397	5.207	4.191	∞
↳ Path 6	∞	3	2	9	X[0]	Z[1]	9.042	5.107	3.935	∞
↳ Path 7	∞	3	2	9	X[0]	Z[0]	8.693	5.312	3.381	∞
↳ Path 8	∞	3	2	9	X[0]	Z[2]	8.434	5.078	3.356	∞

Name	Slack ^{^1}	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
↳ Path 9	∞	3	2	10	X[2]	Z[2]	2.313	1.479	0.834	-∞
↳ Path 10	∞	3	2	7	Y[3]	Z[7]	2.316	1.474	0.842	-∞
↳ Path 11	∞	3	2	7	Y[3]	Z[6]	2.330	1.479	0.851	-∞
↳ Path 12	∞	3	2	7	Y[3]	Z[5]	2.394	1.487	0.907	-∞
↳ Path 13	∞	3	2	7	Y[0]	Z[0]	2.405	1.535	0.870	-∞
↳ Path 14	∞	3	2	9	X[0]	Z[3]	2.479	1.476	1.003	-∞
↳ Path 15	∞	3	2	12	X[1]	Z[4]	2.530	1.543	0.987	-∞
↳ Path 16	∞	3	2	7	Y[0]	Z[1]	2.590	1.494	1.095	-∞