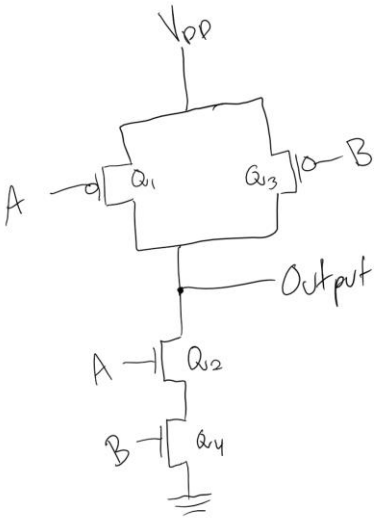
Marcus Domingo
ECE-301-002 HW7A

1. AND gate CMOS:



2. Function table for the give CMOS circuit:

A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	F
0	0	0	ON	OFF	ON	OFF	ON	OFF	0
0	0	1	ON	OFF	ON	OFF	OFF	ON	0
0	1	0	ON	OFF	OFF	ON	ON	OFF	0
0	1	1	ON	OFF	OFF	ON	OFF	ON	0
1	0	0	OFF	ON	ON	OFF	ON	OFF	0
1	0	1	OFF	ON	ON	OFF	OFF	ON	0
1	1	0	OFF	ON	OFF	ON	ON	OFF	0
1	1	1	OFF	ON	OFF	ON	OFF	ON	1

3. Given input analyzation of the given CMOS circuit:

A	B	C	D	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	F
0	0	1	0	ON	OFF	ON	OFF	OFF	ON	ON	OFF	1
0	1	0	0	ON	OFF	OFF	ON	ON	OFF	ON	OFF	0
1	1	0	0	OFF	ON	OFF	ON	ON	OFF	ON	OFF	1

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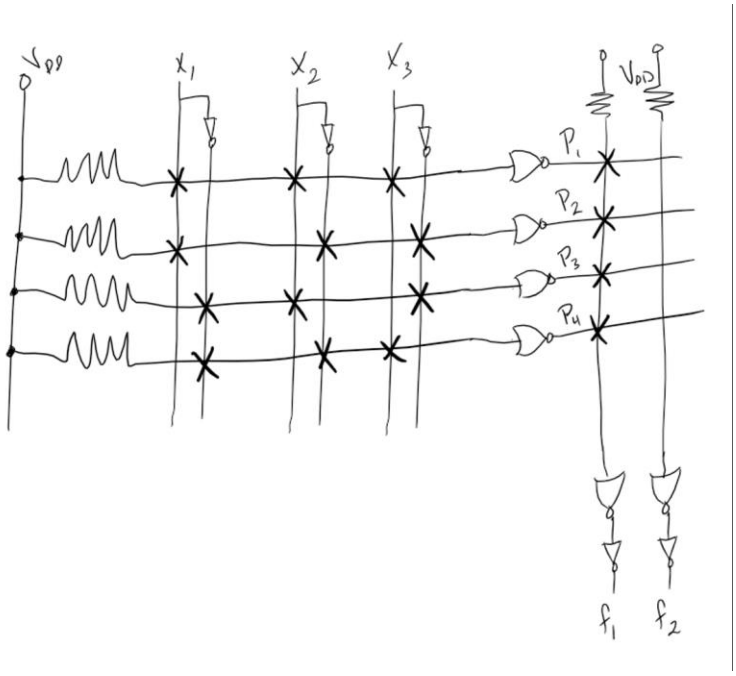
4. **3.37:** $f_1(x_1, x_2, x_3) = \sum m(0,3,5,6) = \overline{x_1 x_2 x_3} + \overline{x_1} x_2 x_3 + x_1 \overline{x_2} x_3 + x_1 x_2 \overline{x_3}$



5. **3.39:**