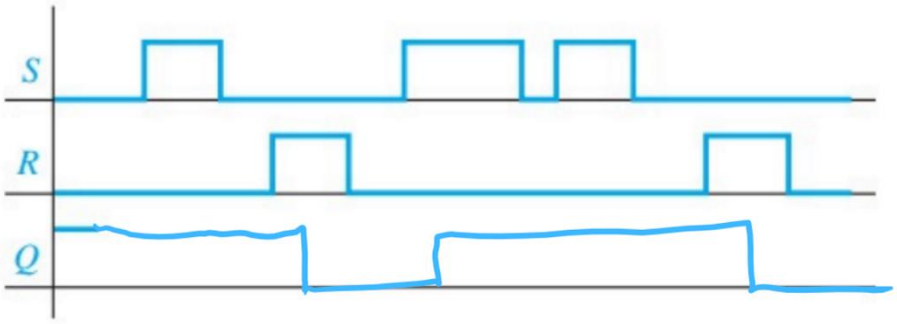
Marcus Domingo
ECE-301-002 HW8

1.



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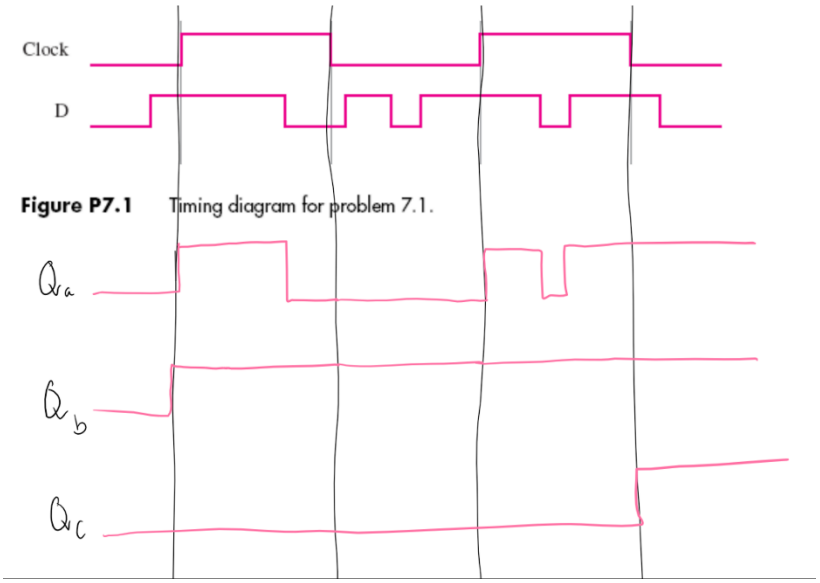
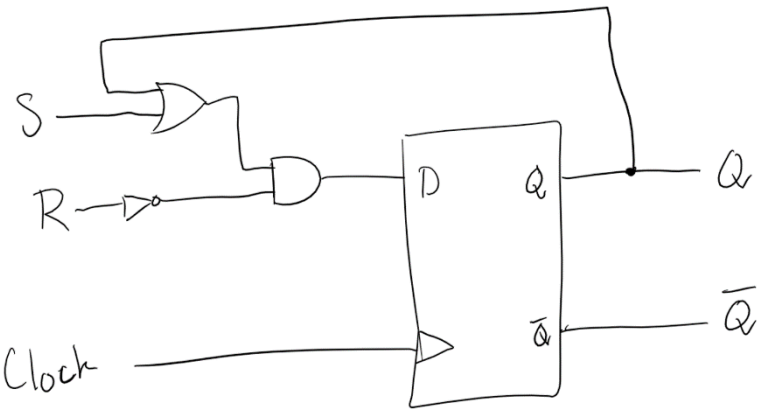
2. 7.1:



3. 7.6:



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4. 7.34:

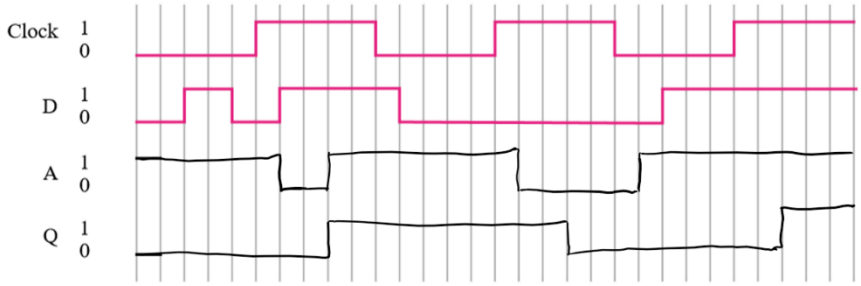


Figure P7.7 Circuit and timing diagram for Problem 7.34.

5. (a) Gated SR Latch:

States		Inputs		
Present	**Next**	**S**	**R**	**C**
0	0	X	X	0
1	1	X	X	0
0	0	0	X	1
0	1	1	0	1
1	0	0	1	1
1	1	X	0	1

From the table we get: Q* = SC + RQ + CQ

(b) Gated D Latch:

States		Inputs	
Present	**Next**	**D**	**C**
0	0	X	0
1	1	X	0
0	0	0	1
0	1	1	1
1	0	0	1
1	1	1	1

From the table we get: Q* = (~C)Q + CD

(c) D Flip-Flop:

States		Inputs
Present	**Next**	**D**
0	0	0
0	1	1
1	0	0
1	1	1

From the table we get: Q* = D

6. T Flip-Flop:

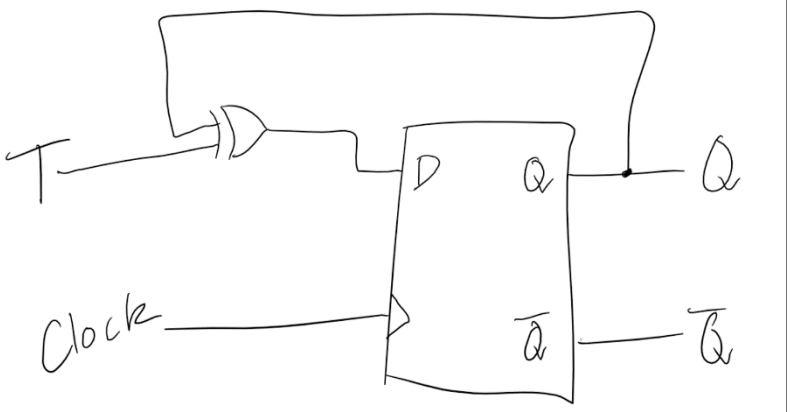
States		Inputs
Present	**Next**	**T**
0	0	0
0	1	1
1	0	1
1	1	0

Karnaugh Map:

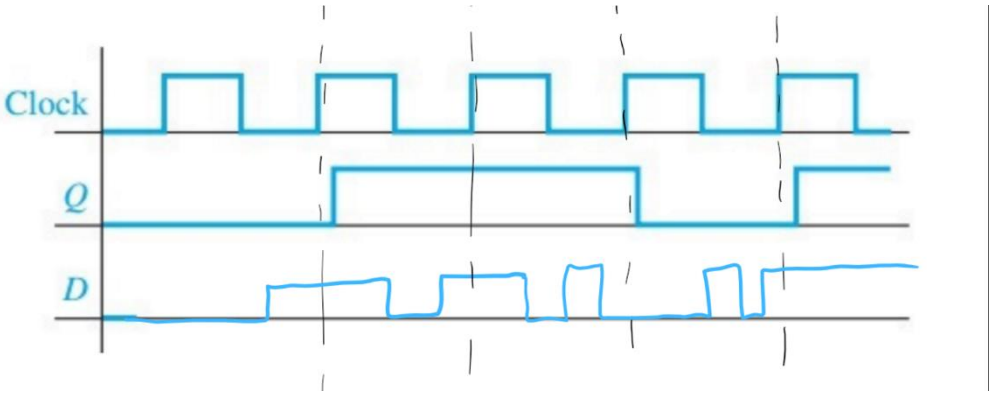
		T	
		0	**1**
Q	**0**	0	(1)
	1	(1)	0

From the Karnaugh Map we get: $Q^* = (\sim T)Q + T(\sim Q) = T \oplus Q$

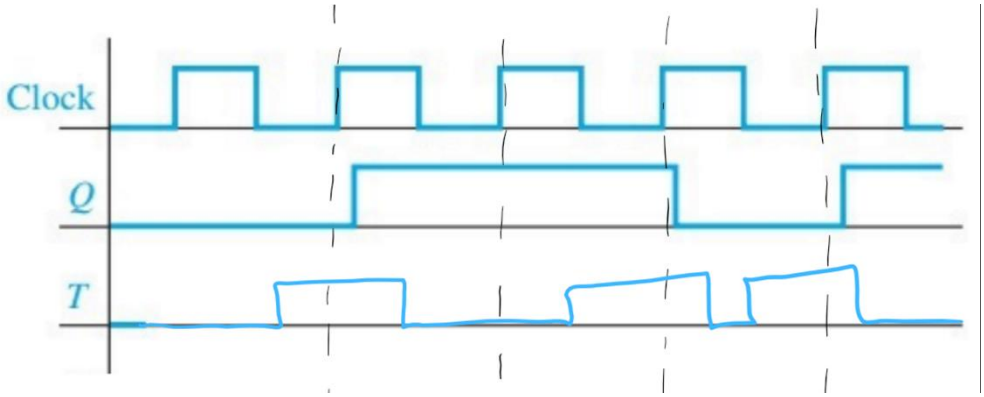
7.



8.



9.



10. **7.24:**

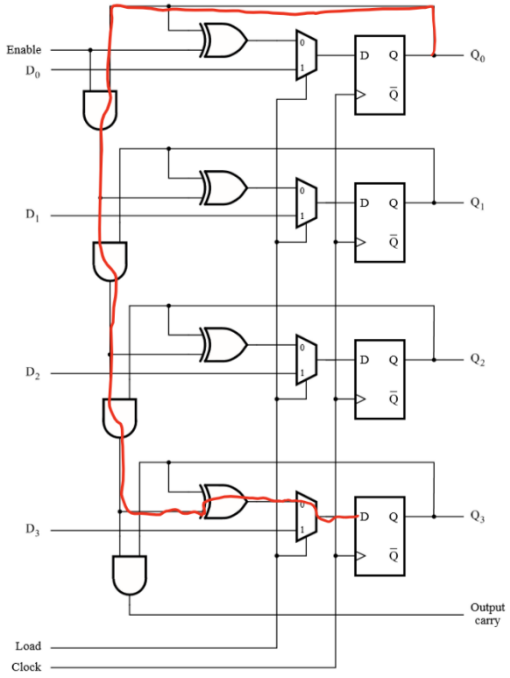


Figure 7.25 A counter with parallel-load capability.

The path shown has a delay of 5 ns thus

$$T_{min} = 5 + 3 + 1 = 9\,ns$$

$$f_{max} = \frac{1}{T_{min}} = 0.111\,Hz = 111\,MHz$$