ECE 301 Digital Electronics Counter Design Revised Fall 2013 K. Hintz & C. Lorie

OBJECTIVE

Understand the design and operation of clocked sequential circuits to implement a 3-bit counter from discrete logic.

PREPARATION

Design and construct the circuits.

PROCEDURE

Design, build, and verify the operation of a three-bit counter utilizing 74LS73 J-K FF's. Design your circuit such that it counts up when the control variable $U/\overline{D}=1$, and counts down when $U/\overline{D}=0$.

Hint: Use a logic switch to clock the flip-flops, and the LED displays to indicate the count of the system. (Or use the 74LS47 and seven segment display to display the count.) Make sure to set $\overline{Clear} = 1$ (note the inverting bubble on the CLR input of the connection diagram) and set inputs of the flip-flops high when counting. Use the clear inputs of the flip-flops to initialize the counter to zero. Check your design against the following excitation equations before assembling it.

$$\begin{split} J_0 &= K_0 = 1 \\ J_1 &= K_1 = \overline{Q_0} \bullet \overline{U} + Q_0 \bullet U \\ J_2 &= K_2 = \overline{Q_1} \bullet \overline{Q_0} \bullet \overline{U} + Q_1 \bullet Q_0 \bullet U \end{split}$$