

November 1994

54F/74F04 Hex Inverter

General Description

Features

This device contains six independent gates, each of which performs the logic INVERT function.

■ Guaranteed 4000V minimum ESD protection

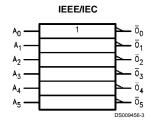
Ordering Code: See Section 0

Commercial	Military	Package	Package Description
		Number	
74F04PC		N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
	54F04DM (Note 2)	J14A	14-Lead Ceramic Dual-In-Line
74F04SC (Note 1)		M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F04SJ (Note 1)		M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F04FM (Note 2)	W14B	14-Lead Cerpack
	54F04LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

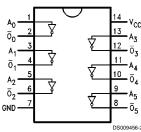
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbol

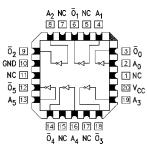


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



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Unit Loading/Fan Out See Section 0 for U.L. definitions

		54F/74F				
Pin Names	Description	U.L.	Input I _{IH} /I _{IL}			
		HIGH/LOW	Output I _{OH} /I _{OL}			
A _n	Inputs	1.0/1.0	20 μA/-0.6 mA			
\overline{O}_n	Outputs	50/33.3	–1 mA/20 mA			

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Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature -65°C to +150°C

Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias -55°C to +175°C

Plastic -55°C to +150°C

 $V_{\rm CC}$ Pin Potential to

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC} TRI-STATE® Output -0.5V to +5.5V Current Applied to Output

Recommended Operating Conditions

Free Air Ambient Temperature

Supply Voltage

Military +4.5V to +5.5V Commercial +4.5V to +5.5V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	٧ _{cc}	Conditions	
			Min	Тур	Max				
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH	54F 10% V _{CC}	2.5					I _{OH} = -1 mA	
	Voltage	74F 10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA	
		74F 5% $V_{\rm CC}$	2.7					I _{OH} = -1 mA	
V _{OL}	Output LOW	54F 10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA	
	Voltage	74F 10% V _{CC}			0.5			I _{OL} = 20 mA	
I _{IH}	Input HIGH	54F			20.0	μΑ	Max	V _{IN} = 2.7V	
	Current	74F			5.0				
I _{BVI}	Input HIGH Current	54F			100	μΑ	Max	V _{IN} = 7.0V	
	Breakdown Test	74F			7.0				
I _{CEX}	Output HIGH	54F			250	μΑ	Max	V _{OUT} = V _{CC}	
	Leakage Current	74F			50				
V _{ID}	Input Leakage	74F	4.75			V	0.0	I _{ID} = 1.9 μA	
	Test							All other pins grounded	
I _{OD}	Output Leakage	74F			3.75	μΑ	0.0	V _{IOD} = 150 mV	
	Circuit Current							All other pins grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V	
I _{os}	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V	
I _{CCH}	Power Supply Current			2.8	4.2	mA	Max	V _O = HIGH	
I _{CCL}	Power Supply Current			10.2	15.3	mA	Max	V _O = LOW	

AC Electrical Characteristics

See Section 0 for Waveforms and Load Configurations

Symbol	Parameter	74F T _A = +25°C V _{CC} = +5.0V			54F T _A , V _{CC} = Mil C _L = 50 pF		74F T _A , V _{CC} = Com C _L = 50 pF		Units	Fig. No.
		Min	C _L = 50 pl Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	++-++
t _{PHL}	A_n to \overline{O}_n	1.5	3.2	4.3	1.5	6.5	1.5	5.3		

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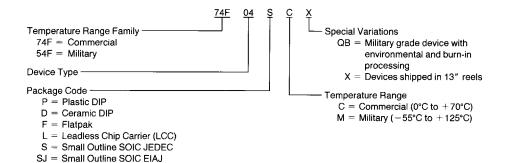
Book Extrac End

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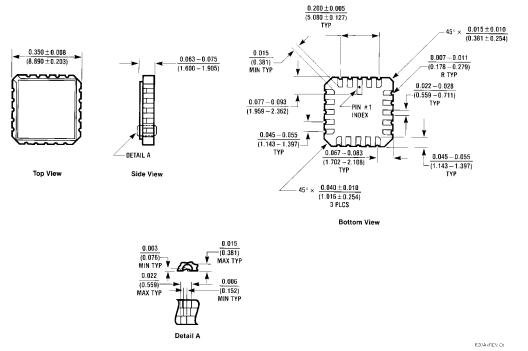
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The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters) unless otherwise noted



20-Terminal Ceramic Leadless Chip Carrier (L) NS Package Number E20A

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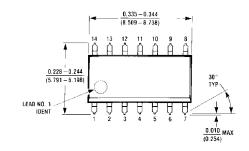
0.785 (19.939) (19.939) MAX 14 13 12 11 10 9 8 0.025 (0.635) RAD 0.220-0.310 (5.588-7.874) 1 2 3 4 5 6 7 0.005 (0.127) MIN 0.290-0.320 0.200 GLASS SEALANT (5.080) MAX 0.020-0.060 (7.366-8.128) 0.060 ±0.005 (1.524 ±0.127) 0.180 (4.572) MA (0.508-1.524)∮95° ±5° 86°94° TYP _10° MAX 0.008-0.012 0.310-0.410 (0.203-0.305) 0.018 ±0.003 0.125--0.200 0.098 (7.874-10.41) (0.457 ±0.076) (3.175-5.080)

(2.489) MAX BOTH ENDS

14-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A

0.100 ±0.010

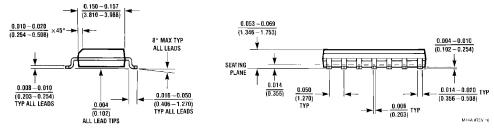
(2.540 ±0.254)



0.150

(3.81) MIN

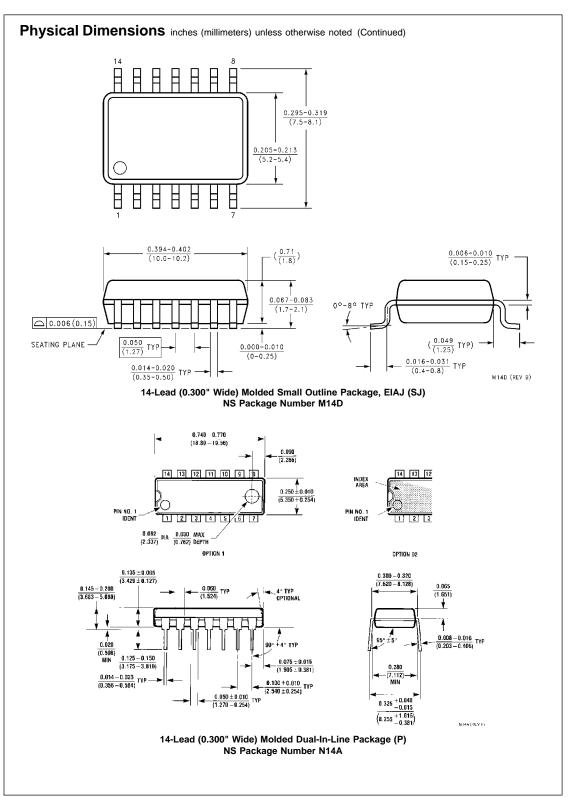
J14A (REV G)



14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S) NS Package Number M14A

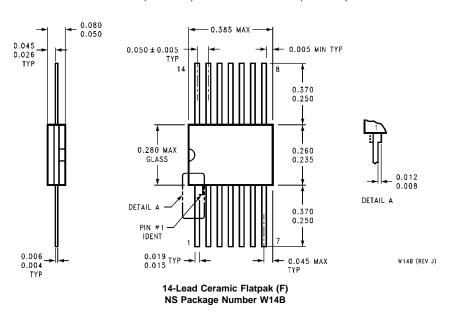
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+ No. 1 cmsery **Proof**



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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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