ECE-301-204

Lab5 Combinational Logic Circuit Design

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Objective:

To design and implement a circuit that detects all of the Fibonacci numbers between 0 and 15.

Materials and Equipment:

- ET-1000 Trainer
- Wires
- Breadboard
- 1 74xx04 (NOT gates), 1 74xx08 (AND gates), 1 74xx32 (OR gates)

Laboratory Data:

A	B	C	D	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

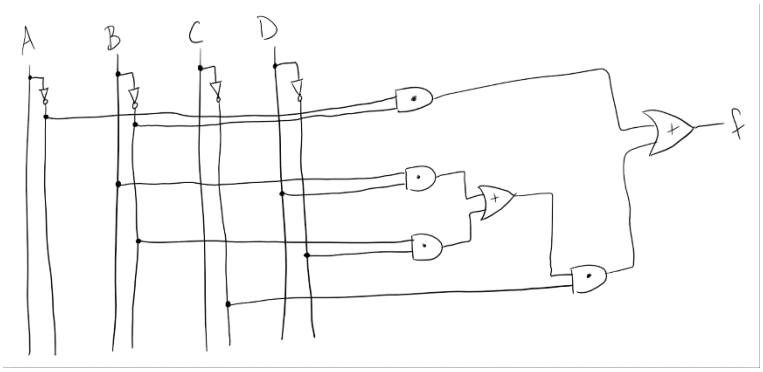
This is the truth table for the Fibonacci number from 0 to 15. The numbers that result in "1" are those of the Fibonacci series which are 0,1,2,3,5,8,13. From this we can design a Karnaugh map for the truth table.

		AB			
		00	01	11	10
CD	00	1	0	0	1
	01	1	1	1	0
	11	1	0	0	0
	10	1	0	0	0

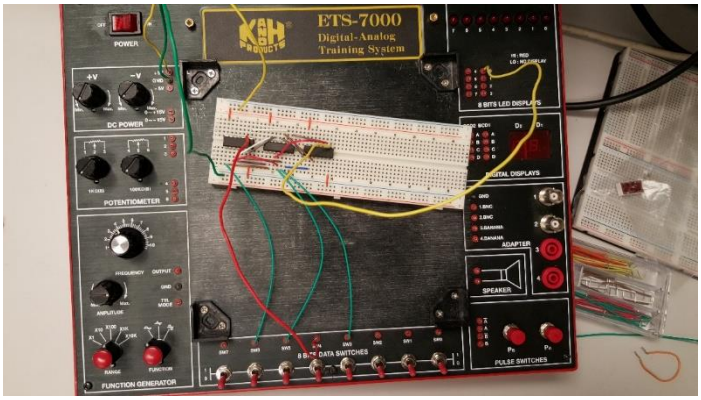
$$f = \overline{A} \cdot \overline{B} + B \cdot \overline{C} \cdot D + \overline{B} \cdot \overline{C} \cdot \overline{D}$$

$$f = \overline{A} \cdot \overline{B} + \overline{C}(B \cdot D + \overline{B} \cdot \overline{D})$$

Above is the Karnaugh map for the Fibonacci number truth table along with the SOP function that satisfies the Karnaugh map.



Above is a mapped out design for the logic circuit that will produce the Fibonacci numbers 0 to 15. Below is the physical circuit that was built from the above diagram.



Comments and Conclusions:

This lab gave us practice using 4 variable Karnaugh maps based off of a truth table that follows the rules of a common mathematical sequence. We also minimized the inputs on some of the gates from 3 to 2 using factoring on the SOP function. This allowed us to use less IC's than we would have used if we needed a 3 input gate.