Part 1. Cache Simulation with MARS

Data Collection:

Group #	Number of Blocks	Cache Block Size	Final Hit Rate	Non-Empty Blocks	Block Utilization
1	8	2	50%	4	50%
1	8	4	75%	4	50%
1	8	8	94%	4	50%
2	4	4	75%	2	50%
2	8	4	75%	4	50%
2	16	4	88%	8	50%
3	16	2	50%	8	50%
3	8	4	75%	4	50%
3	4	8	88%	2	50%
4	8	4	88%	8	100%
4	8	4	88%	8	100%
4	4	4	75%	4	100%
4	4	4	78%	4	100%
5	8	4	75%	4	50%
5	8	4	88%	8	100%
5	8	4	75%	4	50%
5	8	4	75%	4	50%
5	8	4	88%	8	100%
5	8	4	88%	8	100%

Data Observation:

Group 1:

As the cache block size increases so did the final hit rate; however, the block utilization remained the same.

Group 2:

My partner and I noticed a slight increase in the final hit rate as the number of blocks increase while the cache block sized remained static; Once again, the overall block utilization remained the same at a static 50% throughout all three trials.

Group 3:

As the number of blocks decreased and the cache block size increased so did the final hit rate. In addition, the block utilization remained static at 50% throughout all of the trials.

Group 4:

We found that, regardless of whether it was using LRU or Random, the final hit rate for a fully associative cache was approximately equivalent to one another. The block utilization remained the same regardless of method and cache block size staying at 100%.

Group 5:

For group 5, we found that the final hit rates ranged between 75% to 88%. For caches whose configurations resulted in a final hit rate of below 80% the block utilization was only 50% while those whose configurations resulted in a final hit rate of greater than 80% had 100% block utilization.

Part 2. Written Exercise for Memory

1a. Tag = 26 bits; Index = 3 bits; Offset = 3 bits;

Address	Binary pattern	Index	Tag	Hit/Miss	Replacement?
0x018	00000000000000000000000000011000	3	0	Miss	No
0x218	00000000000000000000001000011000	3	8	Miss	Yes
0x2FC	00000000000000000000001011111100	7	11	Miss	No
0x218	00000000000000000000001000011000	3	8	Hit	No
0x018	00000000000000000000000000011000	3	0	Miss	Yes
0x246	00000000000000000000001001000110	0	9	Miss	No
0x180	00000000000000000000000110000000	0	6	Miss	Yes
0x241	00000000000000000000001001000001	0	9	Miss	Yes
0x247	00000000000000000000001001000111	0	9	Hit	No
0x219	00000000000000000000001000011001	0	6	Miss	Yes

2a. Tag = 30 bits; Offset = 2 bits;

Address	Binary pattern	Tag	Hit/Miss	Replacement?	LRU order
0x018	00000000000000000000000000011000	6	Miss	No	0x018
0x218	00000000000000000000001000011000	134	Miss	No	0x218, 0x018
0x2FC	00000000000000000000001011111100	191	Miss	No	0x2FC, 0x018, 0x218
0x218	00000000000000000000001000011000	134	Miss	No	0x218, 0x2FC, 0x018
0x018	00000000000000000000000000011000	6	Hit	No	0x018, 0x218, 0x2FC
0x246	00000000000000000000001001000110	137	Miss	No	0x246, 0x018,

					0x218, 0x2FC
0x180	00000000000000000000000110000000	96	Miss	No	0x018, 0x246, 0x018, 0x218, 0x2FC
0x241	00000000000000000000001001000001	144	Miss	No	0x241, 0x018, 0x246, 0x018, 0x218, 0x2FC
0x247	00000000000000000000001001000111	145	Miss	No	0x247, 0x241, 0x018, 0x246, 0x018, 0x218, 0x2FC
0x219	00000000000000000000001000011001	134	Hit	No	0x218, 0x247, 0x241, 0x018, 0x246, 0x018, 0x2FC

3a) 1/(0.96*10^-9) = 1.041 GHz

3b) AMAT = Hit Time + (miss rate)(miss penalty)

= 0.96 + .11*(3.22+.60*80)

= 6.5942 ns

3c) CPI actual = CPI base + average mem stall per instruction

= 1.0 + .35 * (.11*.60) * 6.5942

= 1.15

4. 4KB pages = 2^12 therefore offset is 12 bits and VPN = 20 bits

Data Stream Contents:

Run	Address	Binary (Last 16 bits)	VPN	TLB Hit/Hit PT/Page Fault	PPN
1	4669	0001|0010001111 01	1	Page Fault	13
2	2227	0000|1000101100 11	0	Page Table Hit(Update TLB)	5
3	13916	0011|0110010111 00	3	TLB Hit	6
4	34587	1000|0111000110 11	8	Page Fault	14
5	48870	1011|1110111001 10	11	TLB Hit	12
6	12608	0011|0001010000 00	3	TLB Hit	6
7	49225	1100|0000010010 01	12	Page Fault	15

Page Table Initial		
Index	Valid	Physical Page or in Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4

8	**0**	**Disk**
9	**0**	**Disk**
10	**1**	**3**
11	**1**	**12**
12	**0**	**Disk**

TLB - Initial State		
Valid	**Tag**	**Physical Page Number**
1	**11**	**12**
1	**7**	**4**
1	**3**	**6**
0	**4**	**9**

Page Table – Run #1		
Index	**Valid**	**Physical Page or in Disk**
0	**1**	**5**
1	**1**	**13(Update Due to Page Fault)**
2	**0**	**Disk**
3	**1**	**6**
4	**1**	**9**
5	**1**	**11**
6	**0**	**Disk**
7	**1**	**4**

8	**0**	**Disk**
9	**0**	**Disk**
10	**1**	**3**
11	**1**	**12**
12	**0**	**Disk**

TLB – Run #1		
Valid	**Tag**	**Physical Page Number**
1	**1**	**13**
1	**11**	**12**
1	**7**	**4**
1	**3**	**6**

Page Table – Run #2		
Index	**Valid**	**Physical Page or in Disk**
0	**1**	**5**
1	**1**	**13(Update Due to Page Fault)**
2	**0**	**Disk**
3	**1**	**6**
4	**1**	**9**
5	**1**	**11**
6	**0**	**Disk**

7	**1**	**4**
8	**0**	**Disk**
9	**0**	**Disk**
10	**1**	**3**
11	**1**	**12**
12	**0**	**Disk**

TLB – Run #2		
Valid	**Tag**	**Physical Page Number**
1	**0**	**5**
1	**1**	**13**
1	**11**	**12**
1	**7**	**4**

Page Table – Run #3		
Index	**Valid**	**Physical Page or in Disk**
0	**1**	**5**
1	**1**	**13(Update Due to Page Fault)**
2	**0**	**Disk**
3	**1**	**6**
4	**1**	**9**
5	**1**	**11**
6	**0**	**Disk**

7	**1**	**4**
8	**0**	**Disk**
9	**0**	**Disk**
10	**1**	**3**
11	**1**	**12**
12	**0**	**Disk**

TLB – Run #3		
Valid	**Tag**	**Physical Page Number**
1	**3**	**6**
1	**0**	**5**
1	**11**	**12**
1	**7**	**4**

Page Table – Run #4		
Index	**Valid**	**Physical Page or in Disk**
0	**1**	**5**
1	**1**	**13(Update Due to Page Fault)**
2	**0**	**Disk**
3	**1**	**6**
4	**1**	**9**
5	**1**	**11**
6	**0**	**Disk**

7	**1**	**4**
8	**1**	**14(Update Due to Page Fault)**
9	**0**	**Disk**
10	**1**	**3**
11	**1**	**12**
12	**0**	**Disk**

TLB – Run #4		
Valid	**Tag**	**Physical Page Number**
1	**8**	**14**
1	**3**	**6**
1	**0**	**5**
1	**11**	**12**

TLB – Run #5		
Valid	**Tag**	**Physical Page Number**
1	**11**	**12**
1	**8**	**14**
1	**3**	**6**
1	**0**	**5**

TLB – Run #6		
Valid	**Tag**	**Physical Page Number**
1	**3**	**6**
1	**11**	**12**
1	**8**	**14**
1	**0**	**5**

Page Table – Run #7		
Index	**Valid**	**Physical Page or in Disk**
0	**1**	**5**
1	**1**	**13(Update Due to Page Fault)**
2	**0**	**Disk**
3	**1**	**6**
4	**1**	**9**
5	**1**	**11**
6	**0**	**Disk**
7	**1**	**4**
8	**1**	**14(Update Due to Page Fault)**
9	**0**	**Disk**
10	**1**	**3**
11	**1**	**12**
12	**1**	**15(Update Due to Page Fault)**

TLB - Final state		
Valid	**Tag**	**Physical Page Number**
1	**12**	**15**
1	**3**	**6**
1	**11**	**12**
1	**8**	**14**

Page Table Final state		
Index	**Valid**	**Physical Page or in Disk**
0	**1**	**5**
1	**1**	**13(Update Due to Page Fault)**
2	**0**	**Disk**
3	**1**	**6**
4	**1**	**9**
5	**1**	**11**
6	**0**	**Disk**
7	**1**	**4**
8	**1**	**14(Update Due to Page Fault)**
9	**0**	**Disk**
10	**1**	**3**
11	**1**	**12**
12	**1**	**15(Update Due to Page Fault)**