

ECE 301 Digital Electronics
Synchronous Finite State Machine Design and Implementation
Revised Fall 2013
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OBJECTIVE

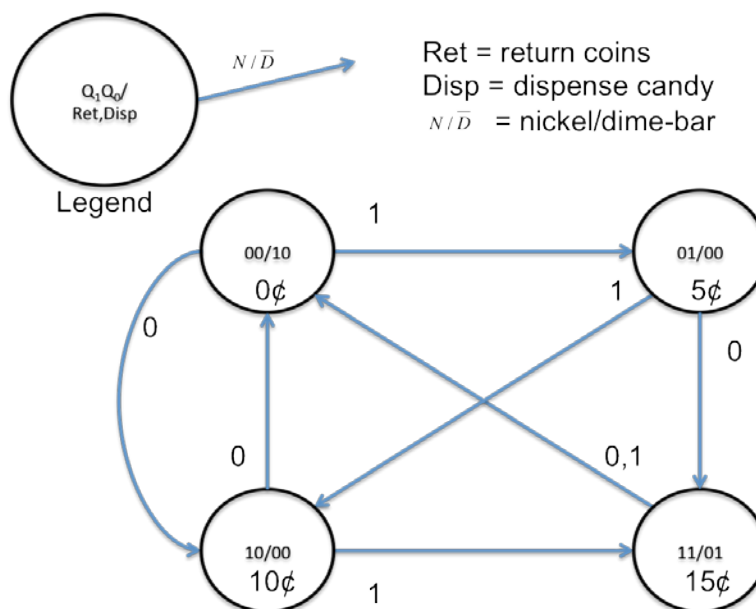
Understand the design and operation of a simple synchronous finite state machine (FSM) to dispense a produce when 15 cents has been entered in nickels and dimes.

PREPARATION

Design and construct the circuits.

PROCEDURE

- 1) Use D-FF's to design, build, and test the Moore FSM as shown in the state diagram at the bottom of the page. The FSM dispenses candy ($Disp = 1$) when 15 cents is entered in nickels and dimes. The synchronous (clocked) sequential circuit counts the value of the coins inserted. It dispenses candy when it reaches 15 cents. If too much value is entered, it resets to state 00 and refunds all the coins ($Ret = 1$).
 - The input variable is N/\bar{D} . That is when $N/\bar{D} = 0$, a dime has been put into the machine. When $N/\bar{D} = 1$, a nickel, has been put into the machine.
 - The state variables are Q_1 and Q_0 with Q_1 being the MSB and Q_0 being the LSB.
 - State 00 is the initial state.
 - When a coin is entered, the clock is (manually) cycled to cause the state to change.
- 2) How would the FSM state diagram be changed to not refund money when too much money had been inserted?
 - How would this affect the number of flip-flops required to implement the new state diagram?
 - Design, but it is not necessary to build, the circuit utilizing JK FF's.



D-Type FF implementation

minterm	Coin input	Present State		Next State		Excitation Variables		Output Variables	
		MSB	LSB	MSB	LSB			Return coins	Dispense candy
	N/D-bar	Q_1^-	Q_0^-	Q_1^+	Q_0^+	D_1	D_0	Ret	Disp
0	0	0	0						
1	0	0	1						
2	0	1	0						
3	0	1	1						
4	1	0	0						
5	1	0	1						
6	1	1	0						
7	1	1	1						

J-K- Type FF implementation

minterm	Coin input	Present State -		Next State +		Excitation Variables				Output Variables	
		MSB	LSB	MSB	LSB					Return coins	Dispense candy
	N/D-bar	Q_1^-	Q_0^-	Q_1^+	Q_0^+	j_1	k_1	j_0	k_0	Ret	Disp
0	0	0	0								
1	0	0	1								
2	0	1	0								
3	0	1	1								
4	1	0	0								
5	1	0	1								
6	1	1	0								
7	1	1	1								