ECE 301 Digital Electronics

Flip-Flops and Frequency Dividers

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OBJECTIVE

To understand the operation of D and JK Flip-flops.
To understand the usage of a flip-flops as clock signal dividers.

BACKGROUND

It is common in digital circuits to synchronize the behavior of the individual logic circuits through the use of a particular signal, generally not considered a data input, called a clock. A clock is generally a square wave, but some systems use a non-symmetric clock. It is also common to have clocks of various frequencies applied to the circuits, usually multiples (or more commonly divisors) of the base clock by 2^n. A simple way to do this is to apply the output of a D-FF back to its D-input as is done in this lab. This will divide the input clock frequency by a factor of 2. Additional divisions of the clock frequency can be done by cascading the output of one FF with the D-input of the next.

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PREPARATION

Design and construct the circuits.

PROCEDURE

1) Using a D flip-flop (74LS74), build a divide the clock frequency by 2 circuit by connecting *Q* output to the *D* input. The frequency/2 is output at the *Q* output.
   - Use the square wave signal from the trainer to provide the clock signal and display the operation of the circuit on your trainer lights, *i.e.,* connect one light to the clock signal and another to the Q output.
   - Remember to include the clear and preset inputs to the FF as part of your circuit design.

2) Repeat part 1) above using a JK flip-flop (74LS76...be careful to note the non-standard pins for *GND* and V_{cc} as shown at the top of page 2 of the datasheet).
   - For this type of flip-flop, connect a trainer light to the non-inverting output, *Q*, and another trainer light to the clock input.
   - Note that there are two possible configurations of the *J* and *K* inputs that will cause the flip-flop to divide the input clock by two. Do both configurations work correctly?