

5.1: (a) $(0111011110)_2 = (478)_{10}$

(b) $(1011100111)_2 = (743)_{10}$

(c) $(3751)_8 = (2025)_{10}$

(d) $(A25F)_{16} = (41567)_{10}$

(e) $(F0F0)_{16} = (61680)_{10}$

5.2: (a) $0111011110 = (478)_{10}$

(b) $1011100111 = (-280)_{10}$

(c) $1111111110 = (-1)_{10}$

5.3: (a) $0111011110 = (478)_{10}$

(b) $1011100111 = (-281)_{10}$

(c) $1111111110 = (-2)_{10}$

5.4: $73 =$

(a) *Signed Magnitude* = 000001001001

(b) *1's Complement* = 000001001001

(c) *2's Complement* = 000001001001

$1906 =$

(a) *Signed Magnitude* = 011101110010

(b) *1's Complement* = 011101110010

(c) *2's Complement* = 011101110010

$-95 =$

(a) *Signed Magnitude* = 100001011111

(b) *1's Complement* = 111110100000

(c) *2's Complement* = 111110100001

$$-1630 =$$

(a) *Signed Magnitude* = 111001011110

(b) *1's Complement* = 100110100001

(c) *2's Complement* = 100110100010

5.5: $00110110 + 01000101 = 01111011$

$$54 + 69 = 123$$

$$01110101 + 11011110 = [1]01010011 \quad \text{Overflow Occurs}$$

$$117 + (-34) = 83$$

$$11011111 + 10111000 = [1]10010111 \quad \text{Overflow Occurs}$$

$$(-33) + (-72) = (-105)$$

$$00110110 - 00101011 = 00001011$$

$$54 - 43 = 10$$

$$01110101 - 11010110 = [0]10011111 \quad \text{Overflow Occurs}$$

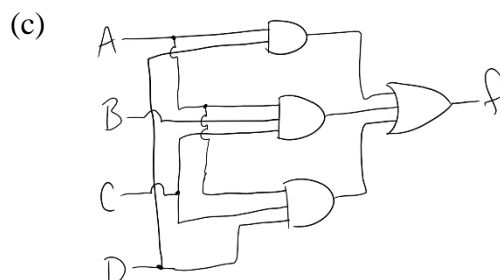
$$117 - (-42) = 159$$

$$11010011 - 11101100 = [1]11100111 \quad \text{Overflow Occurs}$$

$$(-45) - (-20) = (-25)$$

2.: (a) There are no Static-1 hazards because all of the adjacent 1's in the K-Map are covered.

(b) No product terms have to be added.



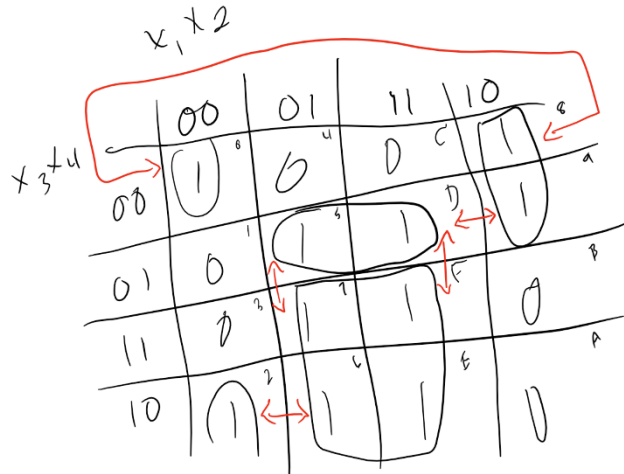
CD

	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	0	1	1
10	0	0	1	0

3.: (a) $H(x_1, x_2, x_3, x_4) = \prod M(1, 3, 4, A, B, C) = \sum m(0, 2, 5, 6, 7, 8, 9, D, E, F)$

(b) $= x_1'x_2'x_4' + x_2x_3 + x_2x_3'x_4 + x_1x_2'x_3'$

(c)



(d) *Hazard free* $= x_1'x_2'x_4' + x_2x_3 + x_2x_3'x_4 + x_1x_2'x_3' + x_2'x_3'x_4' + x_1x_3'x_4 + x_2x_4 + x_1'x_3x_4'$

4.:

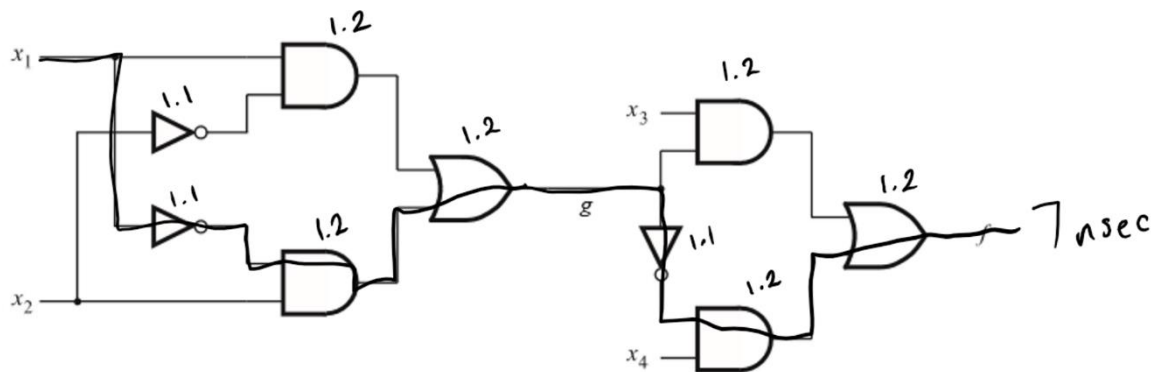
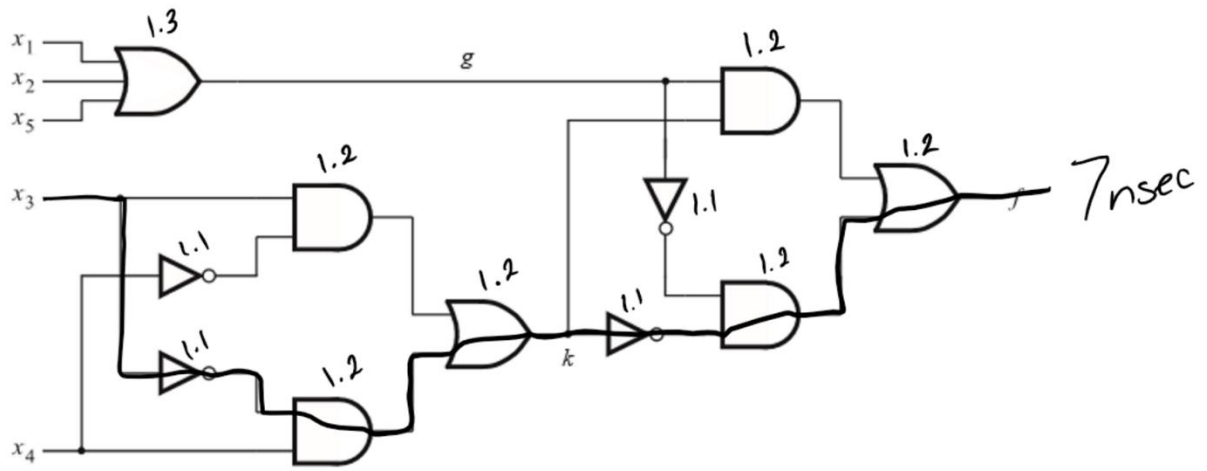


Figure 4.23 Logic circuit for Example 4.6.

Critical path delay $= 1.1nsec + 1.2nsec + 1.2nsec + 1.1nsec + 1.2nsec + 1.2nsec$

Critical path delay $= 7nsec$

5.:



(b) Circuit obtained using decomposition

Figure 4.25 Decomposition for Example 4.7.

$$\text{Critical path delay} = 1.1\text{nsec} + 1.2\text{nsec} + 1.2\text{nsec} + 1.1\text{nsec} + 1.2\text{nsec} + 1.2\text{nsec}$$

Critical path delay = 7nsec