ECE-301-204

Lab4 NAND & NOR Function Implementation

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Objective:

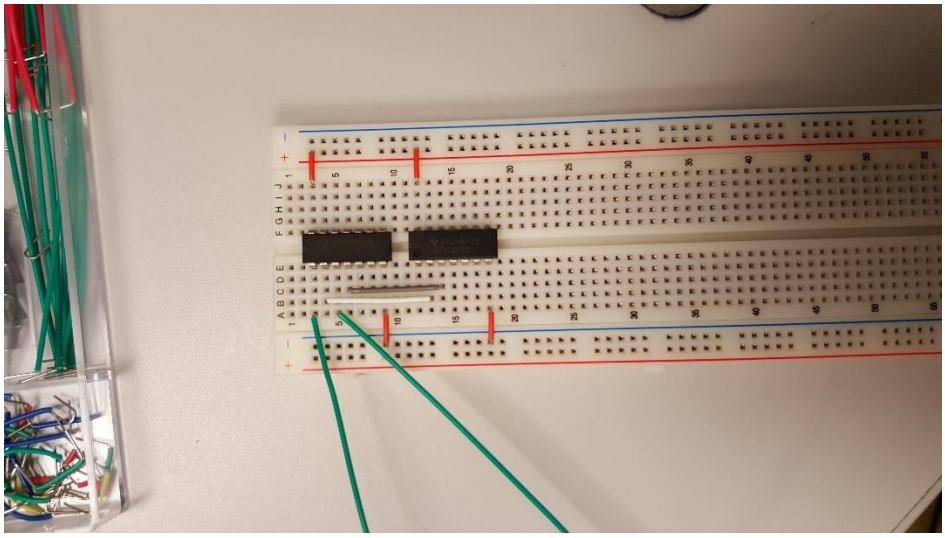
To understand the practical implications of DeMorgan's Theorem.

Understand that logic functions can be implemented utilizing only NAND and NOR gates.

Materials and Equipment:

- ET-1000 Trainer
- Wires
- 1 74xx02 (NOR gates), 1 74xx04 (NOT gates), 1 74xx00 (NAND gates)
- Breadboard

Laboratory Data:



This is the first circuit that was constructed…converting an AND gate from a NOR gate and two inverters.

$f = A \cdot B = \overline{\overline{A \cdot B}} = \overline{\overline{A} + \overline{B}}$ (DeMorgan's Law)

So in the circuit we have the two inputs being inverted and then send them through a NOR gate.

Here is the Karnaugh Map for the truth table:

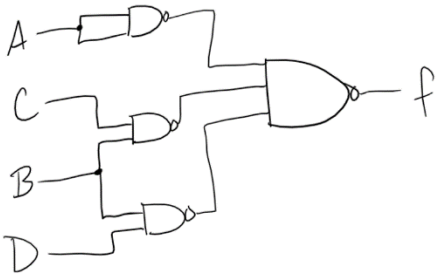
		AB			
		00	01	11	10
CD	00	0	0	1	1
	01	0	1	1	1
	11	0	1	1	1
	10	0	1	1	1

$$SOP = BC\overline{D} + BD + A = B\left(C\overline{D} + D\right) + A = B(C + D) + A = BC + BD + A = \overline{\overline{BC + BD + A}}$$

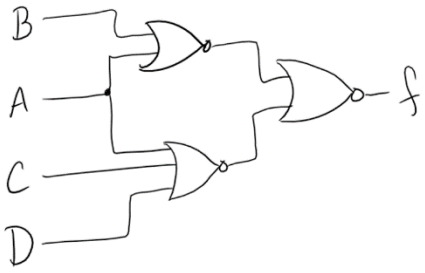
$$= \overline{(\overline{B} + \overline{C}) \cdot (\overline{B} + \overline{C}) \cdot (\overline{A})}$$

$$POS = (A + B) \cdot (A + C + D) = \overline{\overline{(A + B) \cdot (A + C + D)}} = \overline{\left(\overline{A} \cdot \overline{B}\right) + (\overline{A} \cdot \overline{C} \cdot \overline{D})}$$

SOP:



POS:



Comments and Conclusion:

In this lab we practice more DeMorgan's Laws and designing circuits around the laws. We also find that using a Karnaugh Map for big truth tables makes it really simple to either make the SOP or POS for the logic circuit. Then again we practice DeMorgan's Laws once more. Using DeMorgan's Laws to modify which gates we use could be helpful when you are restricted to only certain types of gates as well as if timing were ever an issue. Overall designing circuits with NAND or NOR only has become more fluent than it had been.