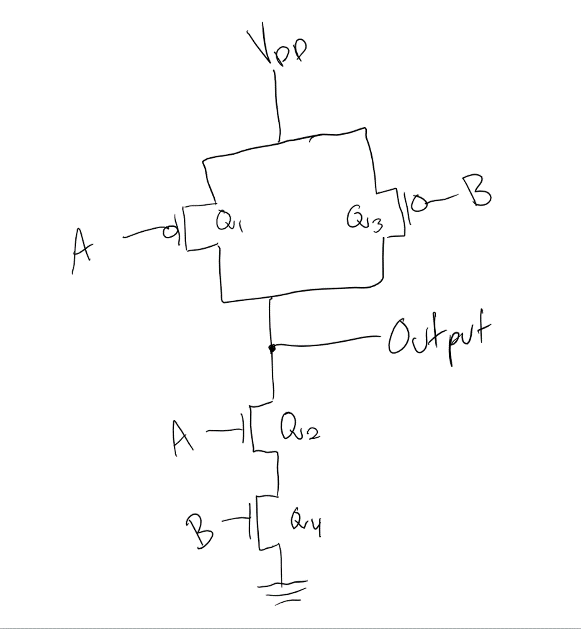
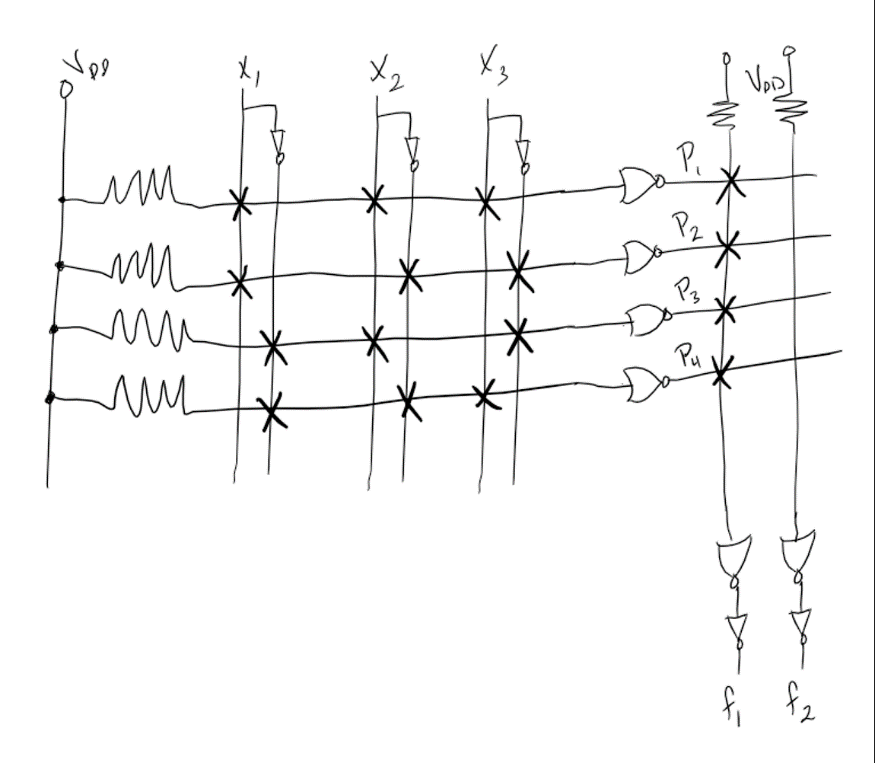
1. AND gate CMOS:

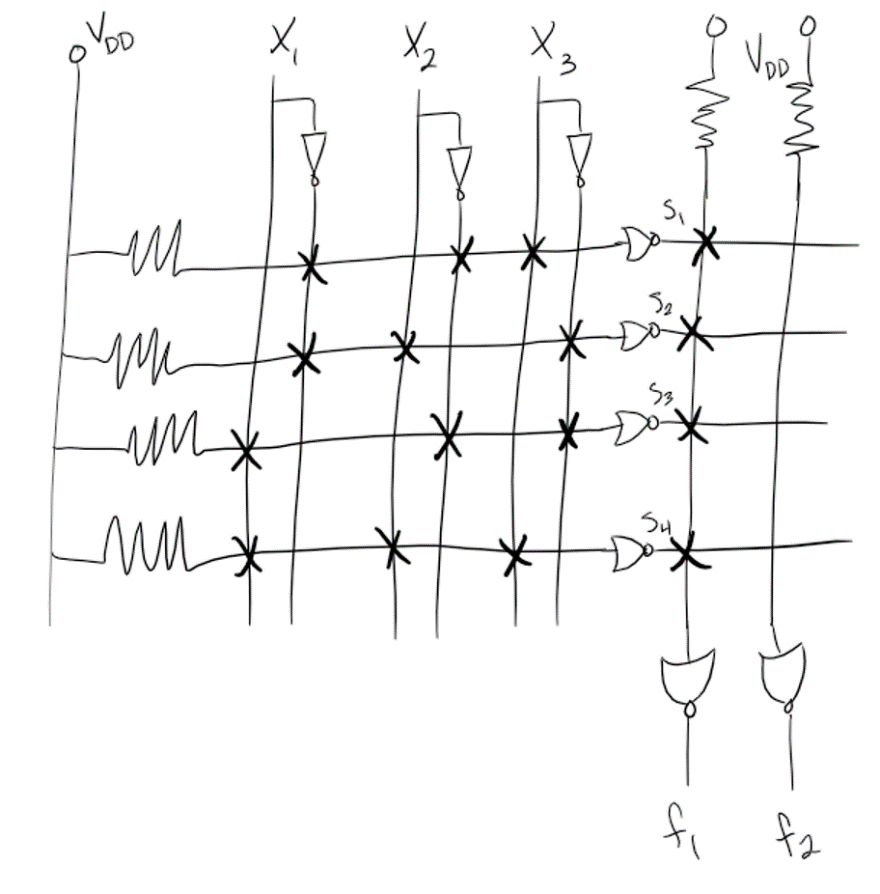
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | F |
| 0 | 0 | 0 | ON | OFF | ON | OFF | ON | OFF | 0 |
| 0 | 0 | 1 | ON | OFF | ON | OFF | OFF | ON | 0 |
| 0 | 1 | 0 | ON | OFF | OFF | ON | ON | OFF | 0 |
| 0 | 1 | 1 | ON | OFF | OFF | ON | OFF | ON | 0 |
| 1 | 0 | 0 | OFF | ON | ON | OFF | ON | OFF | 0 |
| 1 | 0 | 1 | OFF | ON | ON | OFF | OFF | ON | 0 |
| 1 | 1 | 0 | OFF | ON | OFF | ON | ON | OFF | 0 |
| 1 | 1 | 1 | OFF | ON | OFF | ON | OFF | ON | 1 |

1. Function table for the give CMOS circuit:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | Q8 | F |
| 0 | 0 | 1 | 0 | ON | OFF | ON | OFF | OFF | ON | ON | OFF | 1 |
| 0 | 1 | 0 | 0 | ON | OFF | OFF | ON | ON | OFF | ON | OFF | 0 |
| 1 | 1 | 0 | 0 | OFF | ON | OFF | ON | ON | OFF | ON | OFF | 1 |

1. Given input analyzation of the given CMOS circuit:
2. **3.37:**



1. **3.39:**