**CSC205 section 1 Spring 2015**
**Sample Test 1**

**Duration: 1 hour**

**Instructions:**
This test is open-all-resource. You may use any materials available on the internet. Cite your sources if you choose to use such materials. You are not allowed to discuss with one another or anyone outside the class, whether in person or through cellphone, live-chat, etc.

**Total possible points in this test: (score>=20?20:score) for Part A**

1. [2 pts] In what sense are hardware and software equivalent? What are the trade-offs between hardware and software?

Answer:
They are equivalent in the context of decidability of the problem. If a problem is decidable, then there is a way to solve it whether using hardware or software. If the problem is not decidable, then neither one can do it. Tradeoffs between the two implementations include speed, expandability, and development costs. Hardware implementations generally are faster, and cheaper for use once they are developed. However, the development cost of a hardware solution is usually much higher. Software solutions are slower. But debugging software solutions is much less costly, thus reducing their costs of development.

2. [2 pts] Show the steps of adding $-65_{10}$ and $-31_{10}$ in 8-bit 2's complement representation. Is there overflow? Explain why. (Note: 65 is 1000001 in binary and 31 is 11111 in binary.)

Answer:
10100000.

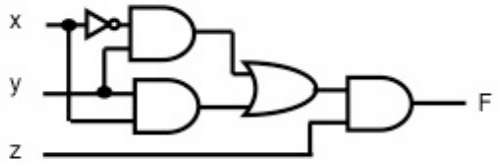
| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | -65 | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| + | -31 | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| | -96 | (1) | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

The extra left bit shown in bracket can be dropped.
There is no overflow because carry-in = carry-out.

3. [1 pt] Consider the floating point number excess-3 system with a 3-bit exponent, a 4-bit significand, with an implied binary point and an implied 1, and with reserved exponent values 000, and 111. What number does the sequence 0 110 1111 represent?

Answer:
Sign = 0, meaning positive.
Biased exponent is $110_2=6_{10}$. True exponent = $(6-3)_{10} = 3_{10}$.
Significand is 1111, representing $1.1111_2$
The decimal number represented is $+2^3 \times 1.1111_2$

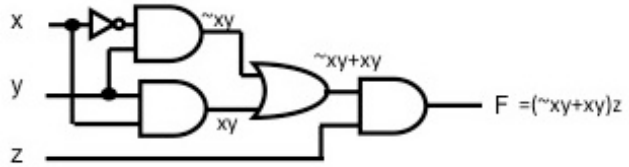
4. [3 pts] This question refers to the circuit shown below.




   a. Describe this circuit using a Boolean function, *F*, that consists of the variables *x*, *y*, and *z*, and the three Boolean operators *, +, and ~.
   b. Simplify the function *F*.
   c. Construct a truth table for the function *F*.

Answer:
a. F=(~xy+xy)z

For reference, see below for explanation. Such explanation is not required in the actual test.




b. (~xy+xy)z = ((~x+x)y)z = 1yz = yz

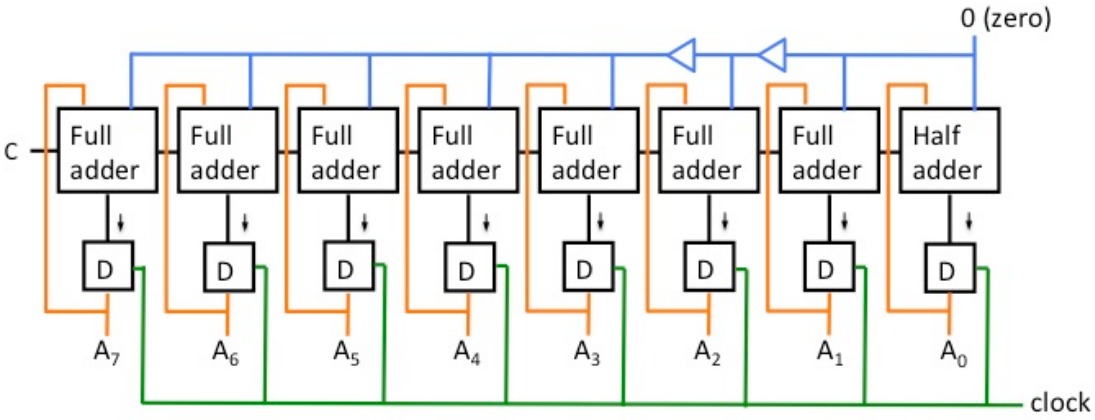
c.

| y | z | F=yz |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

5. [2 pts] Consider the 3-to-8 decoder with input of the form A=($A_2 A_1 A_0$) and output of the form B=($B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$). For each of the following cases, discuss whether it is possible for the decoder to generate such output. If yes, what is the input that gives such result? If no, explain why.
    a. B = 00010000
    b. B = 10000001

Answer:
a. Possible. Use A=100.
b. Not possible. The decoder turns on exactly one bit in the output B for all inputs A.

6. [3 pts] You are given the following circuit with one 8-bit output of the form A=($A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$). Suppose all the D flip-flops are initialized to value 0 at cycle 0.
    a. What is the binary value provided by the blue lines in the circuit?
    b. Show the value of A at cycles 1 to 10.
    c. If A is interpreted as an unsigned number, what is C?




Answer:
a. 00000100
b.

| Cycle | A |
|---|---|
| 0 | 00000000 |
| 1 | 00000100 |
| 2 | 00001000 |
| 3 | 00001100 |
| 4 | 00010000 |
| 5 | 00010100 |
| 6 | 00011000 |
| 7 | 00011100 |
| 8 | 00100000 |
| 9 | 00100100 |
| 10 | 00101000 |

c. C is the overflow.

7. [2 pts] Complete the following time sequence table describing the output Q of the JK flip-flop, at time *t+1*, with respect to its inputs, J and K, at time *t*. (Note that this table follows the convention used in the lecture notes. This is slightly different from the common convention which shows Q(t+1) instead of Q(t).)

| Time *t* | J(*t*) | K(*t*) | Q(*t*) | Reason: |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | *Initial value of Q* |
| 1 | 1 | 1 | | |
| 2 | 0 | 0 | | |
| 3 | 1 | 0 | | |
| 4 | 1 | 0 | | |
| 5 | 0 | 1 | | |
| 6 | 0 | 0 | | |
| 7 | 0 | 0 | | |

Answer:

| Time *t* | J(*t*) | K(*t*) | Q(*t*) | Reason: |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | *Initial value of Q* |
| 1 | 1 | 1 | 0 | *Toggle* |
| 2 | 0 | 0 | 1 | *Toggle* |
| 3 | 1 | 0 | 1 | *No change* |
| 4 | 1 | 0 | 1 | *Set* |
| 5 | 0 | 1 | 1 | *Set* |
| 6 | 0 | 0 | 0 | *Reset* |
| 7 | 0 | 0 | 0 | *No change* |

8. [6 pts] Consider a 256M-byte RAM board built from 16M-byte memory chips (1M=$2^{20}$).
    a. [1pt] How many address lines go into the chip?
    b. [1pt] How many data lines go into the chip?
    c. [1pt] What is the size of the decoder used on the chip to decode an address?
    d. [1pt] How many chips are needed to build the board (assuming no error check is implemented)?
    e. [1pt] What is the size of the decoder on the board?
    f. [1pt] Suppose the most significant address lines are used to refer to the chip number. What is the address of the memory location 6 of chip 3?

Answer:
a. 24 because 16M = $2^{20+4}$.
b. 8 because each addressable unit is 1 byte long.
c. 24-to-$2^{24}$.

d. 16 because 256M/16M = 16.
e. 4-to-16.
f. 0011 00000000 00000000 00000110