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HW 7A

CSC205 section 1 Spring 2015

Homework 7

How to Submit:

Please submit your solutions (parts A and B separately) through Blackboard. Remember to put your name and homework number on all the documents that you submit as attachments.

Total possible points in this homework: 3 for Part B

(You receive 1 bonus point towards Part A if you get all Part A questions correct.)

Part A

1. Let *X* be a 4-byte integer 8765432116 stored at a memory location starting at address 000016. Show how *X* is stored for each of the following architecture:
   1. Small-endian, where the atomic addressable unit is 1 byte;
   2. Small-endian, where the atomic addressable unit is 2 bytes.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| a. |  |  | b. |  |
| Address | Content |  | Address | Content |
| 0000 | 21 |  | 0000 | 4321 |
| 0001 | 43 |  | 0001 | 8765 |
| 0002 | 65 |  |  |  |
| 0003 | 87 |  |  |  |

1. A computer has an instruction format with 4 fixed fields: an opcode field; a mode field; a register address field and a memory address field. The ISA of this computer must support 4 addressing modes, 16 registers and a linear space of 220 bytes of byte-addressable memory. Assume an instruction is 32 bits long. Answer the following:
   1. How many bits must the mode field have?  
      The mode field must have 2 bits; 22 = 4
   2. How many bits must the register address field have?  
      The register address field must have 4 bits; 24 = 16
   3. How many bits must the memory address field have?  
      The memory address field must have 20 bits; 220 bytes of byte addressable memory
   4. How many bits does the opcode field have?  
      The opcode field has 6 bits; 32 – (2 + 4 + 20) = 6
   5. How many operations can be defined?  
      64 operations can be defined; 26 = 64
2. (From Textbook) Suppose we have the instruction Load 500. Given that memory and register R1 contain the values below:

Memory

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 100 | 600 |  | R1 | 200 |
| … |  |  |  |  |
| 400 | 300 |  |  |  |
| … |  |  |  |  |
| 500 | 100 |  |  |  |
| … |  |  |  |  |
| 600 | 500 |  |  |  |
| … |  |  |  |  |
| 700 | 800 |  |  |  |

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

|  |  |
| --- | --- |
| Mode | Value Loaded into AC |
| Immediate | 100 |
| Direct | 600 |
| Indirect | 500 |
| Indexed | 800 |

1. Write a program to evaluate the arithmetic statement:

*X = A \* (B+C)/D*

using instructions from:

* 1. a 0-address ISA;
  2. a 1-address ISA;
  3. a 3-address store/load ISA with many registers R1, R2…R8.

You may assume that the arithmetic operations ADD, SUBT, MULT and DIV are available in each of the ISAs.

|  |  |  |
| --- | --- | --- |
| 0-address | 1-address | 3-address store/load |
| Push A  Push B  Push C  Add  Mult  Push D  Div  Pop X | Load B  Add C  Mult A  Div D  Store X  Halt | Load R1 A  Load R2 B  Load R3 C  Load R4 D  Add R5 R2 R3  Mult R6 R1 R5  Div R7 R6 R4  Store R7 X |

1. How would you classify a GPU based on the four basic categories of processors defined in the Flynn’s Taxonomy in Chapter 9?

SIMD because it exploits multiple data streams against a single instruction stream to perform operations which may be naturally parallelized.