Marcus Domingo

HW8A

**CSC205 section 1 Spring 2015 Homework 8**

**How to Submit:**

**Please submit your solutions (parts A and B separately) through Blackboard. Remember to put your name and homework number on all the documents that you submit as attachments.**

**Total possible points in this homework: 5 for Part B**

**(You receive 1 bonus point towards Part A if you get all Part A questions correct.)**

# Part A

1. A system is designed to have a 5-stage pipeline, in which every stage is given the same amount of time. If a task at one stage is completed early, the result is stored in a register until it is fed to the next stage in the next clock cycle.

Stage 1: Fetch and decode instruction,

Stage 2: Compute operands addresses,

Stage 3: Fetch operands,

Stage 4: Execute,

Stage 5: Write operands.

The task at Stage 2 takes negligible time. The tasks at all other stages take equal amount of time. Let

*R*: Time taken to complete one single instruction without pipeline *Rp*: Time for each stage of the pipeline.

*N*: number of instructions

Suppose the pipeline is almost hazard-free. Why is the theoretical speedup of this system only 4, and not 5?

The speedup up is only 4 cause although there are 5 stages, one of the stages isn’t used. Therefore the theoretical speedup would be calculated with k-1 which is 5-1=4.