University POLITEHNICA of Bucharest

Faculty of Electronics, Telecommunications and Information Technology

Project 1

Positive Voltage Regulator

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Contents

1. Project requirements

It is required to design a positive linear voltage regulator with discrete components, with the following specifications:

- Supply voltage between 22 ÷ 25 [V];
- Programmable output voltage 15 ÷ 17 [V];
- The output current through the load between 0 ÷ 34 [mA];
- Short circuit protection of the output terminals with foldback current limiting circuit.
- Overvoltage protection of the output terminals.
- The line regulation factor $S = \frac{\Delta V_i}{\Delta V_o}\Big|_{RL} \geq 87$.
- Load resistance $Rl = \frac{Vo\_max}{Io\_max} = 500\ \Omega$.

The output impedance of the regulator $R_O \leq 3\ \Omega$.

The voltage regulator is an electronic device that is supposed to maintain a constant voltage at its output terminal. However, in practice, the voltage regulator reduces drastically the voltage ripple at its input. Therefore, the main characteristic of a voltage regulator is the *regulation factor*, which tells how much the output voltage changes with respect to the change in the input voltage $S = \frac{\Delta V_i}{\Delta V_o}\Big|_{RL}$. The focus of designing this circuit is to obtain a good enough regulation factor, higher than 100.

The presented regulator is a linear feedback regulator, that employs an active series pass transistor which is controlled by a high gain differential amplifier, which compares the output voltage with a reference voltage and adjust the control device in order to maintain a constant output voltage. It also has the capability to change its output voltage in the range of 15 to 17 V and has a maximum output current of around 34 mA.

2. The block diagram of the circuit

The block scheme of the regulator contains at least three main components: the voltage reference, the control element, and the error amplifier. These are essential for the regulator to be able to regulate the voltage. In addition, there is an overcurrent protection that prevents the accidental damage to the series pass transistor, namely the control element. There is also an overvoltage protection and a sampling circuit that provides feedback to the error amplifier, as seen in figure 1.

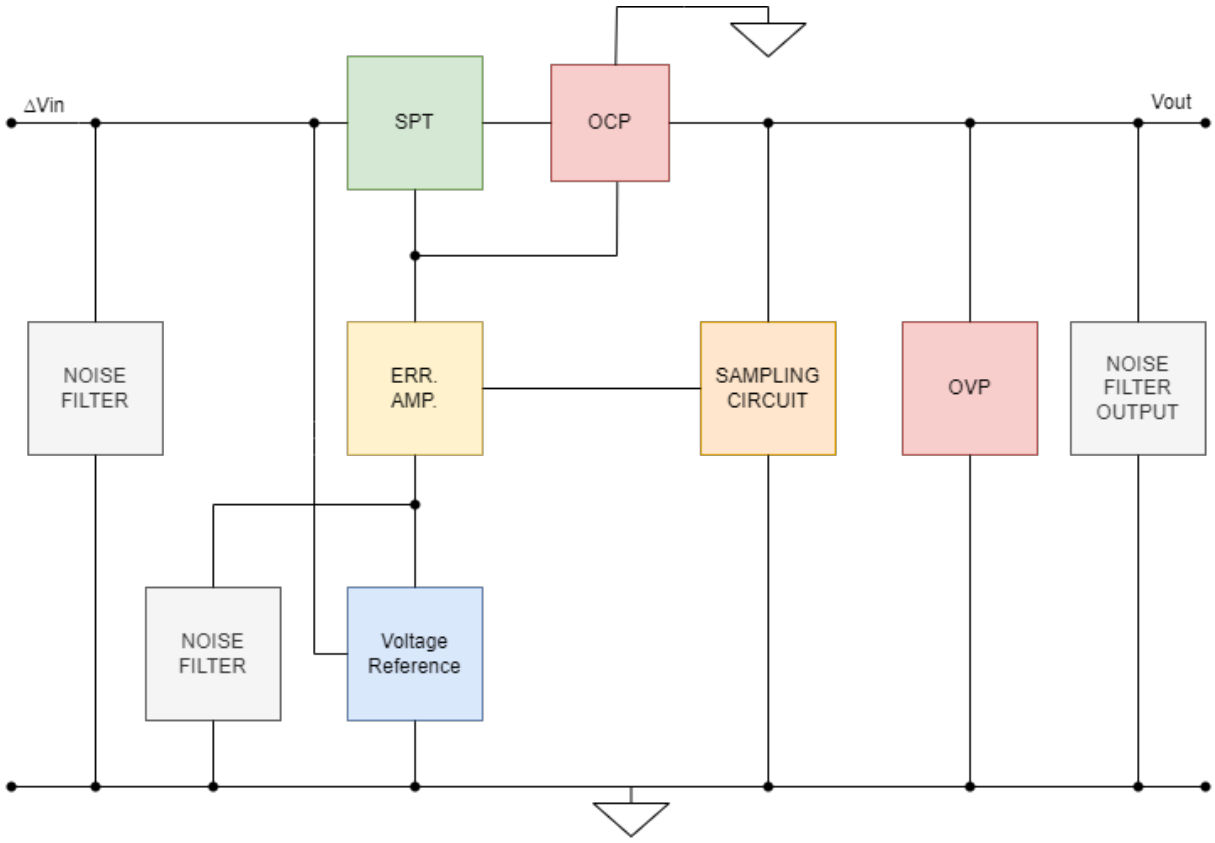


Figure 1 Block scheme of the positive voltage regulator

The full description of each block in the scheme is to be given in the following paragraph:

- **The control element (SPT)** is a series pass transistor, that is situated between the unregulated supply and the regulated output. It is controlled by the error amplifier such that to pass a specific a load current, to have the desired output voltage drop on the load.

- **The error amplifier (ERR. AMP.)** is a differential stage that controls the series pass transistor. It is also connected to the voltage reference and the sampling circuit because this part of the circuit is supposed to compare the reference, which is equal to the desired

regulated output voltage and the actual sampled output voltage, that may vary with the different resistances of the loads connected at the output of the voltage regulator.

- **The over current protection (OCP)** is a stage that is connected in between the series pass transistor and the load. It is supposed to protect the control element from a very high current that can pass through if the output terminals are accidentally short circuited. It also has a special behavior, called foldback, that maintains a lower short circuit current than the maximum current that can pass through this protection. This is an innovative way to implement such a circuit, since the series pass transistor may dissipate a high power for a very short amount of time, but after that it is advised to lower it in order to not overheat the component.

- **The over voltage protection (OVP)** is the part of the circuit that will not let the output voltage exceed the 18.4V threshold. This circuit is implemented since the purpose of the circuit is to stabilize the voltage up to 17V. It may occur in certain scenarios that the output voltage might spike higher than 17V, therefore a transistor that can sink a current parallel to the load is needed to lower the actual output voltage through the load.

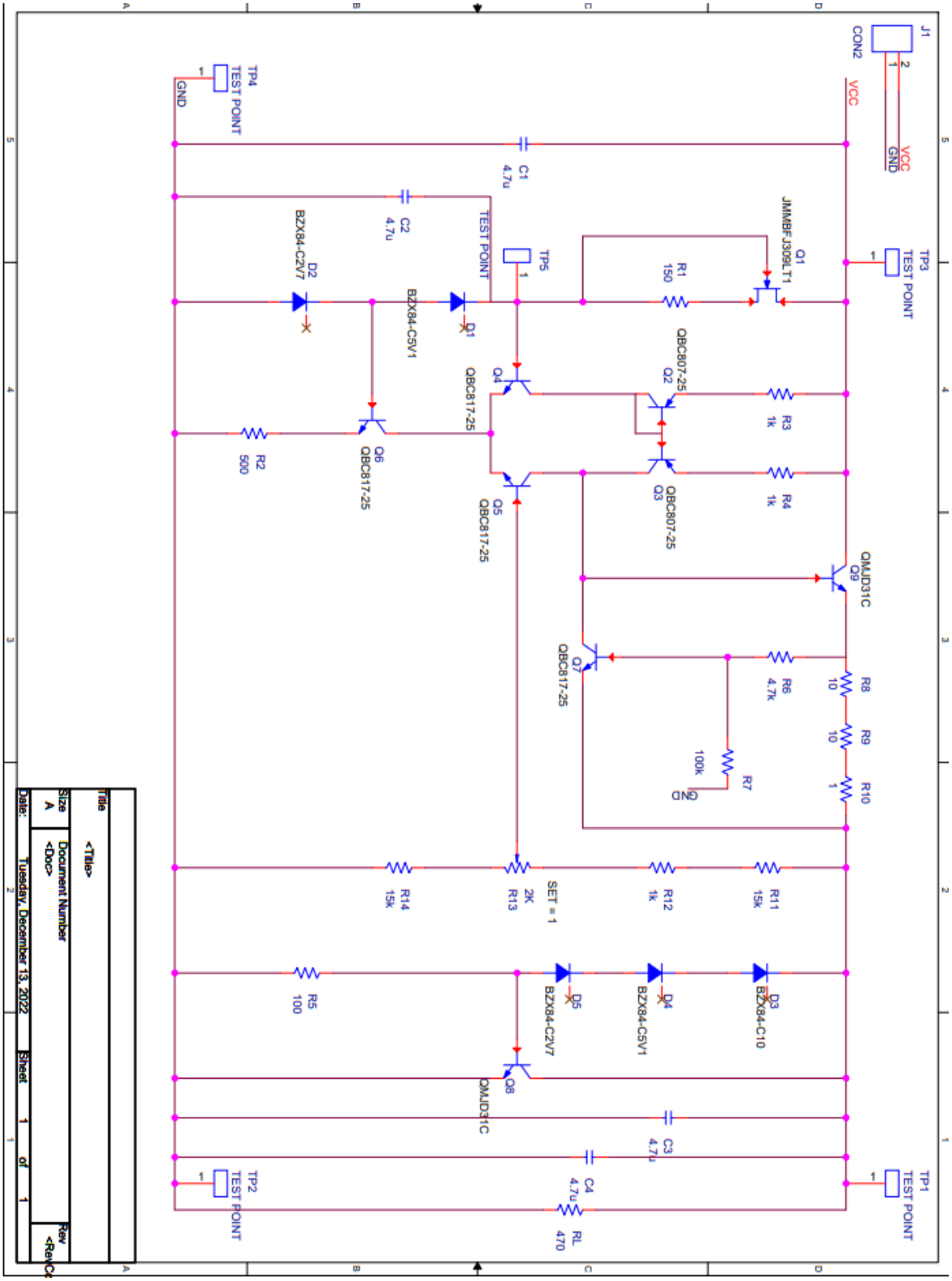
- **The sampling circuit** is a simple voltage divider that allows the user to program the output voltage by means of a potentiometer. This circuit also has the purpose to employ a negative feedback loop, that helps the overall functioning of the regulator. Because of the feedback, the regulator is able to achieve a higher resistance to noise and the ability to maintain a stable output voltage whatever the resistance of the connected load.

- **The voltage reference** is the part of the circuit that offers to the error amplifier a constant voltage to which the differential circuit compares the sampled output voltage. This is a critical part of the circuit, since the voltage drop across it must be as stable as possible, for the regulator to have a high regulating factor.

- **The noise filters** are parts of the circuit that protect that remove the noise from the input and the output of the voltage regulator. They both behave as RC filters with different cutoff frequencies.

CAUTION! Since this circuit employs an over current protection OCP, the resistance of the load must be higher than the minimum allowed resistance through which can pass the maximum allowed current by the OCP.

3. Electrical scheme



3.1 Details about each block of the circuit

- **The voltage reference** is the part of the circuit that has a stable voltage drop across at it, even if the input voltage varies. It is used as an input to the non-inverting pin of the differential voltage amplifier, as seen in figure 2.

  For this part of the circuit, the **Zener diodes D1** and **D2**, had to have around 7.8V of voltage drop across them, so the **BZX84-C5V1** with a Vz = 5.1V and **BZX84-C2V7** with a Vz = 2.7V were chosen. In order to obtain those specific Vz voltages, the Zener diodes need to have a minimum current Imin = 5mA to enter the breakdown region. The Imin current will be ensured by **Q1, a JFET transistor**, JMMBFJ309LT1 that is biased in such a way to obtain a current of 5.6 mA on the branch with the D6 and D2.

  It is critical that the current through D6 and D2 does not vary, because if the voltage drop varies on them, then the output voltage will vary too. This is why a simple resistor, on this branch of the circuit, was not acceptable in order to obtain a high regulation factor.

  The choice of having around 5.6 mA through the Zener diodes was made since it can be seen on the I-V characteristic that the voltage is more stable if a slightly higher than 5 mA current is passed through them.

- **The error amplifier** is the part of the circuit that acts as a comparator between the voltage reference and the output voltage of the regulator. It is used in order to obtain a stable output voltage. The error amplifier is composed of **a current mirror**, represented by **Q2 and Q3 PNP transistors**, BC807-25, that ensures equal currents that passing through **Q4 and Q5 NPN transistors,** BC817-25, which compose the **differential amplifier stage**. They are low power PNP and NPN transistors because the power dissipated by them does not exceed the maximum power that can be dissipated by such transistors according to the data sheet.

  The current mirror is an important part of the circuit because it guarantees the fact that the differential amplifier has a higher CMRR and higher bandwidth. The higher CMRR is especially important, because in a noisy environment, this part of the circuit is able to reject some picked up noise that might affect the reference voltage and the sampled output voltage.

  To properly equalize the currents that enter Q4 and Q5**, transistors Q2 and Q3 need to be matched.** However, due to the fact that these are discrete components, and they could have **high variations** in their process parameters, such as the **base-emitter voltage**, the **resistors R3 and R4** were added in order to neglect those variations. They are both SMD0805.

  The error amplifier has at **the non-inverting input the voltage reference** and at **the inverting input the sampled output voltage.** By solving this part of the circuit, we can

see that the sampled output voltage should be equal with the reference voltage, so this will be ensured by passing to the control element a variable current.

- **The control element Q9,** MJD31C, is a **high power NPN transistor** that is biased by the error amplifier. It ensures a proper output current so that the voltage drop across the load is a stable voltage of a particular desired value, in this case, between 15V and 17V. It is proved in the calculus provided below that the dissipated power by this transistor does not exceed its maximum power.

- **The over current protection** is a circuit made from three **sensing resistor R8, R9 and R10**, the **voltage divider composed of R6 and R7** and the Q7 **NPN transistor BC817-25**. When the current through the sensing resistors exceeds 60 mA, the Q7 transistor is going to be biased into RAN, therefore sinking the current that would have entered the base of Q9 the control element**.** This behavior makes Q9 conduct less current, therefore **ensuring a maximum allowable current through the control element** when the output terminals are short circuited. This circuit also implements **the foldback behavior**, which makes the short circuit current lower than the maximum allowable current.

Isc < Imax

- **The over voltage protection** is composed of three Zener diodes BZX84-C10, BZX84C-C5V1, BZX84-C2V7 that do not allow the output voltage to reach a higher value than 18.4V. When reaching this value, the Zener diodes will start conducting and the sense resistor R5 will have a voltage drop across it equal the base emitter voltage of the transistor Q8. If it was previously in the blocking state, the transistor will conduct the "excess" current from the load resistor, therefore stabilizing the voltage drop across it at the maximum 18.4V.

- **The sampling circuit** is the negative feedback loop for the differential amplifier. It is composed of **resistor R11, R12, R14** and the **potentiometer R13**. Their values have been calculated such that by **moving the potentiometer into its minimum value**, the output voltage will be equal to **15V** and when we move it to the **maximum value,** the output voltage will be equal to **17V**. This allows the output voltage to be programmable.

- **The noise filters at the input** are the two capacitors at the input C1 that is connected in parallel with the input of the circuit and C2 that is connected in parallel with the reference voltage. They behave as RC filters, where the cutoff frequency of the filter with C1 is dependent on the output impedance of the voltage supply source.

$$\text{f cutoff} = \frac{1}{2\pi RC}$$

where C is equal to the capacitance of C1 = 4.7 μF and R is equal to the output impedance of the voltage source

The cutoff frequency of the voltage reference filter has a higher cutoff frequency than the one at the input, since the impedance of R is the impedance of the conductor between D1 and C1.

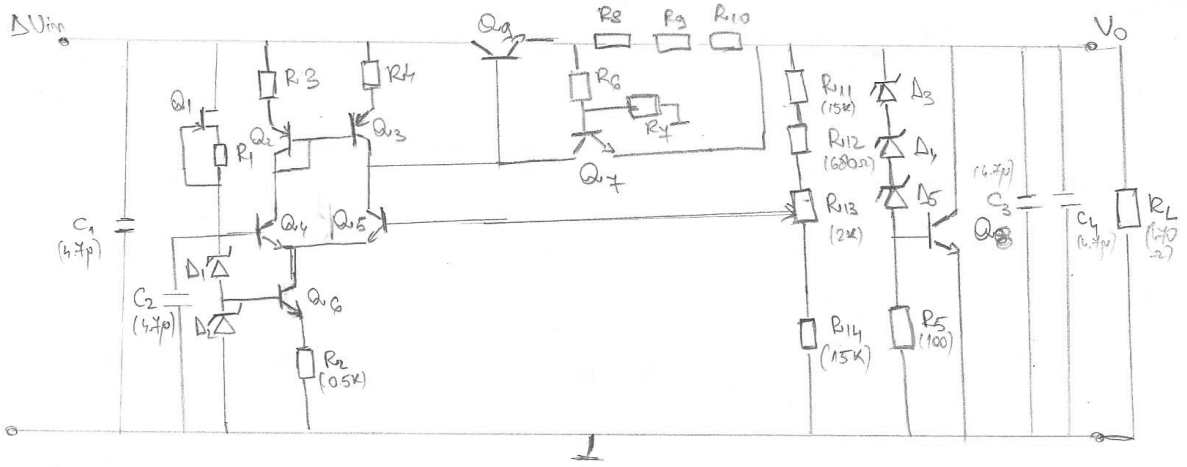
$$\text{f cutoff} = \frac{1}{2\pi RC} = 17 \text{ kHz}$$

where C is equal to the capacitance of C2 = 4.7 μF and R ≅ 1 **Ω**

- **The noise filter at the output** is composed of two parallel capacitors C3 and C4 having a capacitance equal to 9.4 μF. It acts as an RC filter having as R the output impedance of the regulator.

$$\text{f cutoff} = \frac{1}{2\pi RC} = 17 \text{ kHz}$$

3.2 Calculus of DC bias, Open-loop voltage gain, closed loop impedance, and the regulation factor



a) DC bias assumming the worst case scenario when $V_{in} = 22V$ (minimum input voltage) and $V_o = 17V$ (maximum output voltage)

KVL: $V_{GS_1} + V_{D_1} R_1 = 0$

$V_{GS_1} = -I_{D_1} R_1$

$V_{GS_1} = -21\left(1 + \frac{V_{GS_1}}{2}\right)^2 \cdot 0.15 = -3.15\left(1 + \frac{V_{GS_1}}{2}\right)^2$

$\frac{V_{GS_1}^2}{4} + 4.5\, V_{GS_1} + 3.15 = 0$

$V_{GS_1} = -0.72V$

$I_{D_1} = I_{DSS_1}\left(1 - \frac{V_{GS_1}}{V_{T_1}}\right)^2 \cdot R_1 \simeq 5.8\,mA$

C_1, C_2, C_3, C_4 are considered open circuit for all the DC bias calculus.

- PROOF THAT D1 and D2 ARE HAVING V_Z DROP ACROSS THEM

$I_{D_1} > I_{Z_6} = I_{Z_2} = 5\,mA$ From BZX84-C5V1 and BZX84-C2V7 Datasheet

$\Rightarrow V_{Z_1} = 5.1V$ and $V_{Z_2} = 2.7V$

KVL II : $V_o \cdot \frac{R_{13}+R_{14}}{R_{11}+R_{12}+R_{13}+R_{14}} = V_{BE_5} + V_{EB_4} + V_{Z_1} + V_{Z_2}$

Assumming that Q_{15} and Q_{14} are matched then $V_{BE_5} = V_{EB_4}$

$$V_o \cdot \frac{R_{11}+R_{12}}{R_{11}+R_{12}+R_{13}+R_{14}} = V_{Z_1} + V_{Z_2}$$

$\Rightarrow V_o = 14.99\ V$ the potentiometer is set to 0

KVL II(?) : $V_o \cdot \frac{R_{14}}{R_{11}+R_{12}+R_{13}+R_{14}} = V_{Z_1} + V_{Z_2}$

$\Rightarrow V_o = 16.99\ V$ the potentiometer is set to 1

$$\frac{V_o}{R_L} = I_L$$

$$I_L = 36\ mA$$

R_L was chosen initially to be equal to 500 Ω (page 3), but since this value is not available to buy, I chose a lower value that was closest to 500 Ω, such that to make sure that the circuit still works for a 500 Ω load.

KVL III $V_{Z_2} = V_{BE_6} + I_{C_6} \cdot R_2$

$$I_{C_6} = \frac{V_{Z_2} - V_{BE_6}}{R_2}$$

$\Rightarrow I_{C_6} = 4.2\ mA \simeq I_{E_6}$ considering $\beta = 200$

Q_2 and Q_3 are forming a current mirror, therefore $I_{C_2} = I_{C_3}$ because Q_{12} and Q_{13} are matched.

but $\begin{cases} I_{C_4} \simeq I_{C_4} \\ I_{C_3} \simeq I_{C_5} \end{cases} \Rightarrow I_{C_4} \simeq I_{C_5} \simeq I_{C_2} \simeq I_{C_3} = \frac{I_{C_6}}{2} = 2.1\ mA$

KVL IV : $I_{R_{11}} \simeq \frac{V_0}{R_{11}+R_{12}+R_{13}+R_{14}} = \frac{17}{33.68} \simeq 0.52\ mA$

D_3, D_4 and D_5 are in blocking since $V_0 < V_{Z_3} + V_{Z_4} + V_{Z_5} + V_{BE_6} = 18.4V$

KCL I : $I_{Eg} = I_w + I_{NFW} = 36.526\ mA$

$R_{eg} = R_8 + R_9 + R_{10} = 21\ \Omega$

KVL V : $V_{R_{eg}} = I_{Eg} \cdot R_{eg}$

$V_{R_{eg}} = 0.767\ V \Rightarrow V_{Eg} = V_0 + V_{Eg} = 17.767\ V$

$V_{CEg} = V_{IN} - V_{Eg} = 4.233\ V > V_{CEsat} \simeq 0.2\ V$

Assuming that $V_{BEg} = 0.6\ V$

$\Rightarrow Q_g$ works in the normal active region

KVL VI : $V_{IN} = V_{DS_1} + V_{Z_6} + V_{Z_2} + R_1 \cdot I_{D_1}$

$V_{DS_1} = V_{IN} - V_{Z_6} - V_{Z_2} - R_1 I_{D_1}$

$V_{DS_1} = 13.33\ V > V_{DSsat} = 3V$

Q_1 works in saturation

Q_2 is in diode connection $\Rightarrow Q_2$ works in the normal active region

KVL VII : $V_{Z_1} + V_{Z_2} = V_{BE_4} + V_{CE_5} + I_{E_6} \cdot R_2$

$V_{CE_5} = V_{Z_1} + V_{Z_2} - V_{BE_4} - I_{E_6} R_2$

$V_{CE_5} = 5.1\,V > V_{CEsat} = 0.2\,V$

Q_5 works in the normal active region

KVL VIII : $V_{IN} = I_{E_3} \cdot R_3 + V_{EC_2} + V_{CE_4} + V_{CE_5} + I_{E_6} \cdot R_2$

$V_{CE_4} = V_{IN} - I_{E_3} R_3 - V_{EC_2} - I_{E_6} R_2 - V_{CE_5}$

$V_{CE_4} = 12.1\,V > V_{CEsat} = 0.2\,V$

Q_4 works in the normal active region

KVL IX : $V_{IN} = I_{E_3} \cdot R_4 + V_{EC_3} + V_{BE_9} + V_{Reg} + V_o$

$V_{EC_3} = V_{IN} - I_{E_3} R_4 - V_{BE_9} - V_{Reg} - V_o$

$V_{EC_3} = 1.533\,V > V_{ECsat} = 0.2\,V$

Q_3 works in the normal active region

KVL X : $V_{IN} = I_{E_4} \cdot R_4 + V_{EC_3} + V_{CE_5} + V_{CE_6} + I_{C_6} \cdot R_2$

$V_{CE_5} = V_{IN} - I_{E_4} R_4 - V_{EC_3} - V_{CE_6} - I_{C_6} R_2$

$V_{CE_5} = 11.167\,V > V_{CEsat} = 0.2\,V$

Q_5 works in the normal active region

- CALCULUS OF DISSIPATED POWER BY EACH COMPONENT

$P_{Q_1} = I_{D_1} \cdot V_{DS_1} = 96\ mW < 225\ mW$ the maximum power of MMBFJ309L

$P_{R_1} = I_{D_1}^2 \cdot R_{11} = 4\ mW < 125\ mW$ the maximum power of SMD0805 – 150R – 1%

$P_{D_1} = V_{Z_1} \cdot I_{D_1} = 28.56\ mW < 300\ mW$ the maximum power of BZX84C5V1

$P_{D_2} = V_{Z_2} \cdot I_{D_2} = 15.12\ mW < 250\ mW$ the maximum power of BZX84C2V7

$P_{R_3} = P_{R_4} = I_{E_1}^2 \cdot R_3 = 4.342\ mW < 125\ mW$ the maximum power of SMD 0805 – 1K – 1%

$P_{Q_2} = V_{EC_1} \cdot I_{E_1} = 1.28\ mW < 310\ mW$ the maximum power of BC807-25

$P_{Q_3} = V_{EC_2} \cdot I_{E_2} = 19\ mW < 310\ mW$ the maximum power of BC807-25

$P_{Q_4} = V_{CE_4} \cdot I_{E_4} = 31.87\ mW < 310\ mW$ the maximum power of BC817-25

$P_{Q_5} = V_{CE_5} \cdot I_{E_5} = 21.8\ mW < 310\ mW$ the maximum power of BC817-25

$P_{Q_6} = V_{CE_6} \cdot I_{E_6} = 21.42\ mW < 310\ mW$ the maximum power of BC817-25

$P_{Q_7} = V_{CE_7} \cdot I_{E_7} = 34\ mW < 15W$ the maximum power of MJD31C

$P_{R_8} = I_{E_7}^2 \cdot R_8 = 13.51\ mW < 125\ mW$ the maximum power of SMD 0805 – 10R – 1%

$P_{R_9} = P_{R_8}$, identical resistors.

$P_{R_{10}} = 1.351\ mW < 125\ mW$ the maximum power of SMD 0805 – 1R – 1%

$P_{R11} = I_{R11}^2 \cdot R_{11} = 4.15\ mW < 125\ mW$ the maximum power of SMD 0805 – 15K – 1%

$P_{R12} = I_{R12}^2 \cdot R_{12} = 188\ \mu W < 125\ mW$ the maximum power of SMD 0805 – 620R – 1%

$P_{R13} = I_{R13}^2 \cdot R_{13} = 553\ \mu W < 250\ mW$ the maximum power of TS53YL202MR10

$P_{R14} = I_{R14}^2 \cdot R_{14} = 4\ mW < 125\ mW$ the maximum power of SMD 0805 – 15K – 1%

$P_{D3} = V_{Z5} \cdot I_{R5} = 60\ mW < 300\ mW$ the maximum power of BZX84 – C10

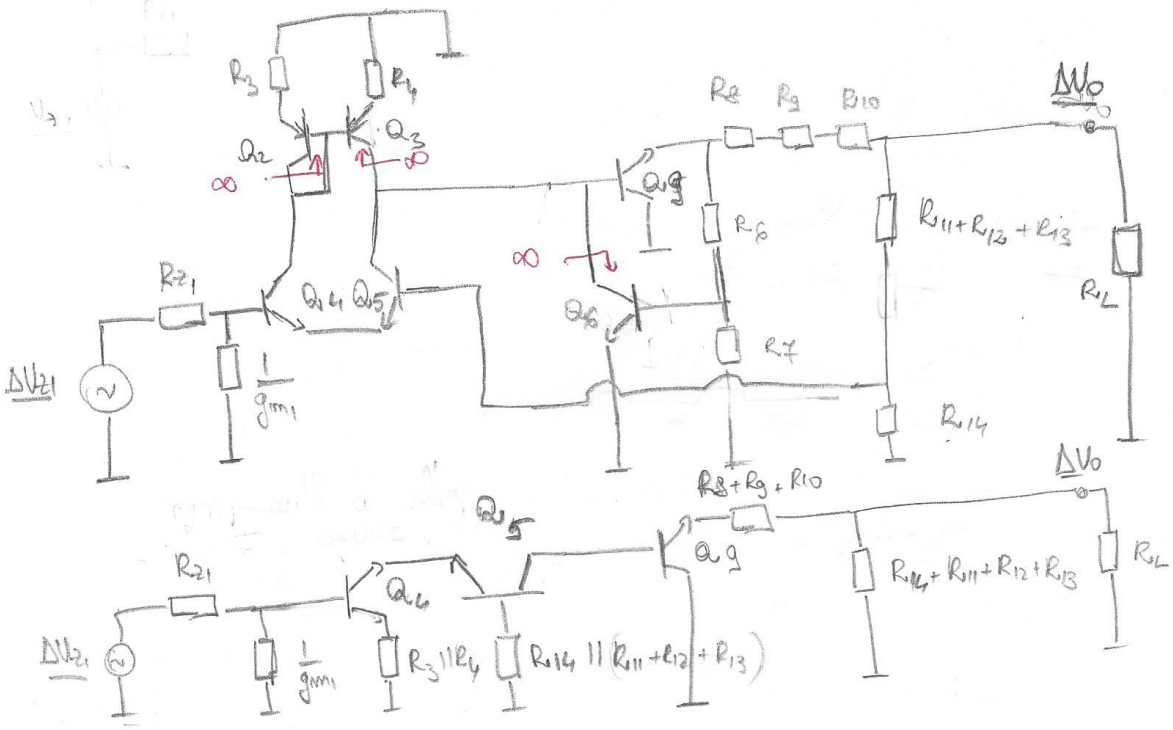
$P_{D4} = V_{Z4} \cdot I_{R5} = 30.6\ mW < 300\ mW$ the maximum power of BZX84 – C5V1

$P_{D5} = V_{Z5} \cdot I_{R5} = 16.2\ mW < 250\ mW$ the maximum power of BZX84 – C2V7

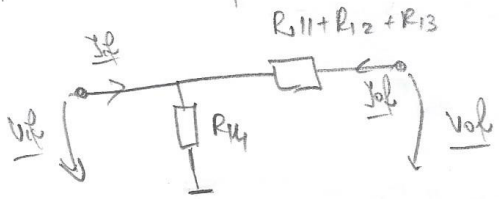
$P_{R5} = I_{R5}^2 \cdot R_5 = 3.6\ mW < 125\ mW$ the maximum pwr of SMD0805 – 100R – 1%

$P_{Q8} = V_{CE8} \cdot I_{Lmax} = 18.4 \cdot 0.06 = 1W < 15W$ the maximum power of MJD31C

OPEN LOOP VOLTAGE GAIN AMPLIFIER (a_v)



open loop amplifier

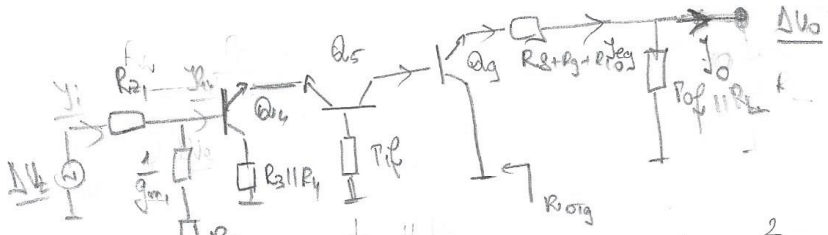


series - shunt negative feedback

$$A_f = \frac{V_{if}}{V_{of}} = \frac{R_{14}}{R_{14}+R_{13}+R_{12}+R_4} = 0.658$$

$$R_{if} = \frac{V_{if}}{I_{if}}\Big|_{V_{of}=0} = R_{14} \,||\, (R_{11}+R_{12}+R_{13})$$

$$R_{of} = \frac{V_{of}}{I_{of}}\Big|_{V_{if}=0} = R_{14} + R_{11} + R_{12} + R_{13}$$



$$g_{m1} = \frac{2}{|V_{th}|} \cdot \left(1 - \frac{V_{GS1}}{V_{t1}}\right) = 1.38\ S$$

$$\frac{1}{g_{m1}} = 0.735\ \Omega$$

$$R_{z1} \approx \frac{V_{th}}{I_{Y1}} = \frac{25\,mV}{5.8} = 4.31\ \Omega$$

$$\frac{\Delta V_o}{\Delta V_i} = \frac{Y_{i0}}{Y_{eq}} \cdot \frac{Y_{eq}}{Y_{fg}} \cdot \frac{Y_{fg}}{Y_{cs}} \cdot \frac{Y_{cs}}{Y_{es}} \cdot \frac{Y_{es}}{Y_{cu}} \cdot \frac{Y_{cu}}{Y_{fu}} \cdot \frac{Y_{fu}}{Y_i}$$

$$= \frac{r_{of} \parallel R_L}{r_{\pi g} + R_g + R_{fg} + R_{f0} + r_{of} \parallel R_L} \cdot (\beta_g + 1) \cdot \frac{\beta_5}{\beta_5 + 1} \cdot (\beta_4 + 1) \cdot \frac{\frac{1}{g_{m1}} + R_1}{\frac{1}{g_{m1}} + R_{z1} + R_1}$$

$$r_{\pi g} = \frac{\beta_g}{40\, I_{cq}}$$

0.02

$$a_v = -1331.06$$

$$T = a_v \cdot f_v = 636$$

- open-loop output impedance R_o^*

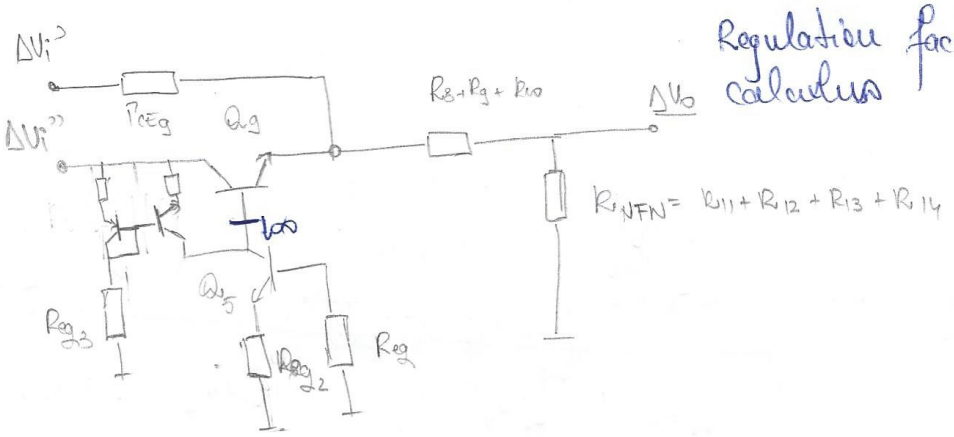
$$R_o^* = \left(R_{\pi g} \parallel R_g + R_{fg} + R_{f0}\right) \parallel r_{of} \parallel R_L \approx 512\ \Omega$$

$$\frac{1}{R_o} = \frac{1+T}{R_o^*} - \frac{1}{R_L} \Rightarrow R_o = \frac{R_o^* \cdot R_L}{R_L(1+T) - R_o^*}$$

- closed loop output impedance R_o

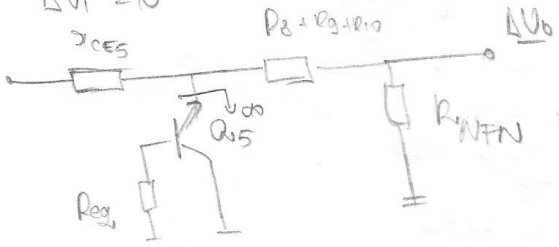
$R_o \approx 0.8\ \Omega < 3\Omega$

Regulation factor calculus



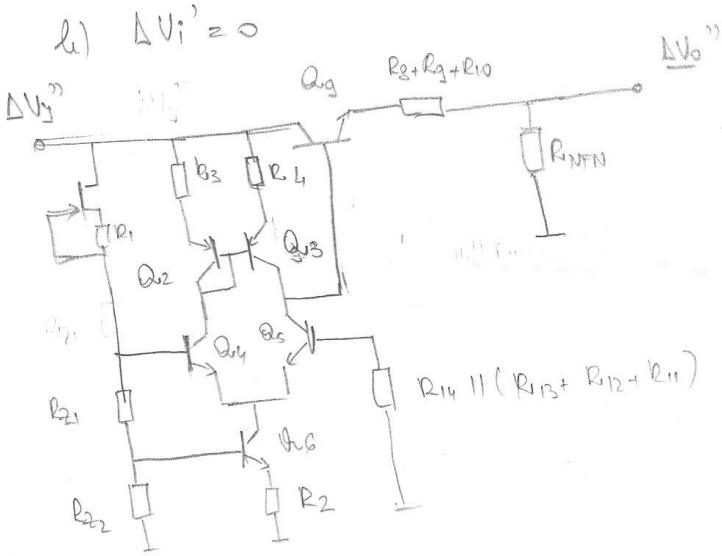
$$\frac{1}{S} = \frac{\Delta V_o'}{\Delta V_i'}\bigg|_{\Delta V_i''=0} + \frac{\Delta V_o''}{\Delta V_i''}\bigg|_{\Delta V_i'=0}$$

a) $\Delta V_i'' = 0$



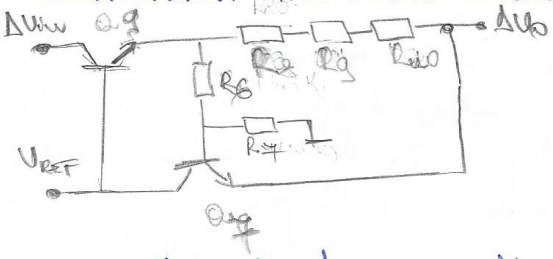
$$\frac{\Delta V_o'}{\Delta V_i'}\bigg|_{\Delta V_i''=0} = \frac{R_{iNFN}}{r_{CE5} + R_8 + R_g + R_{10} + R_{iNFN}} \approx \frac{32.68}{33.701} = 0.969$$

b) $\Delta V_i' \approx 0$



3.3 Calculus of the over current protection OCP

OVERCURRENT PROTECTION CIRCUIT



In order to design a current limiting circuit that is able to exhibit the foldback behaviour of the short circuit currents, then the voltage divider consisting of R_S and R_T is added.

First, I started by defining the parameters:

$V_{out} = 17V$; $I_R = 60\,mA$ (maximum allowable current);

$I_{sc} = 30\,mA$

$$R_{sc} = \frac{\frac{V_{out}}{I_{sc}}}{\left(1 + \frac{V_{out}}{V_{REF}}\right) - \frac{I_R}{I_{sc}}} = 20.8\,\Omega$$, my choice was to

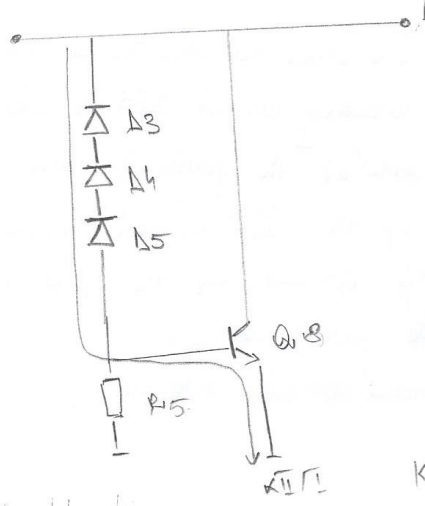
put R_{S0}, R_{S1}, 10 Ω resistors in series with R_{S2} of 1 Ω to have $R_{sc} = R_S + R_g + R_{S10} = 21\,\Omega$

$$\frac{R_T}{R_T + R_S} = \frac{V_{REF}}{I_{sc} R_{sc}} \Rightarrow R_T = 20\,R_S$$

R_S is chosen to have a large resistance of 4.7 KΩ in order to prevent current leakage through the voltage div. and R_T is chosen to be 100 kΩ standard value, instead of 94 kΩ

3.4 Calculus of the over voltage protection OVP

OVERVOLTAGE PROTECTION CIRCUIT



D3, D4 and D5 are Zener diodes. The voltage drop across them, when they are in the breakdown region, was chosen to be higher than ΔVo (Vo max)

$$V_{Z3} + V_{Z4} + V_{Z5} > V_{o\,max}$$

$V_{Z3} = 10V$; $V_{Z4} = 5.1V$; $V_{Z5} = 2.7V$

This circuit activates itself when

KII/I: $V_o = V_{Z3} + V_{Z4} + V_{Z5} + V_{BE10}$

$V_o = 18.4\,V > 17V$ (maximum programmable voltage at output)

R_{12} resistor was chosen in order to fulfill 2 constraints: → $I_{R12} \cdot R_{12} = V_{BE10} \simeq 0.6V$

↓ $I_{R12} + I_{B10} = I_{Zmin} \simeq 6\,mA$

$$\begin{cases} I_{R12} + I_{B10} = I_{Zmin} \\ I_{B10} = \dfrac{I_{c\,max}}{\beta_{min}} = \dfrac{34}{25} = 1.36\,mA \end{cases} \Rightarrow I_{R12} = 4.64\,mA$$

$R_{12} = \dfrac{V_{BE10}}{I_{R12}} = 130\,\Omega$, but my choice was to use the standard value $100\,\Omega$. In this way I am sure that the diodes will be correctly polarised.

4. SPICE simulations of the circuit

4.1 DC bias

The simulation in figure 2 is a bias point one. It is meant to show the overall functionality of the circuit. It is proved that each **bipolar junction transistor** is **working in RAN** and the **FET transistor is in saturation.** The power on each component is also shown, and proves that the maximum power is not exceeded.

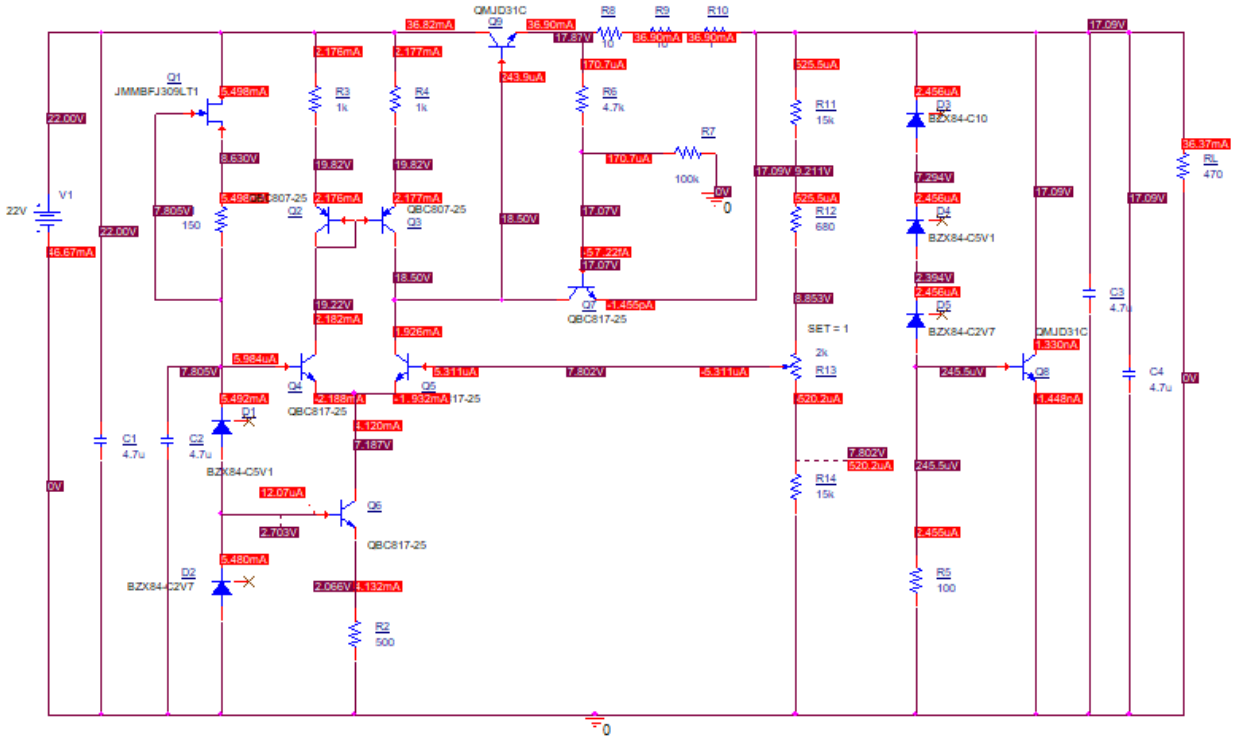


Figure 2 DC bias in the worst case scenario when Vin = 22V and Vout ≅ 17V

These two DC sweep simulations show that by setting the potentiometer at 0 respectively 1, the circuit can stabilize the voltage at 15V, respectively 17V, which are the required minimum and maximum programmable voltages.

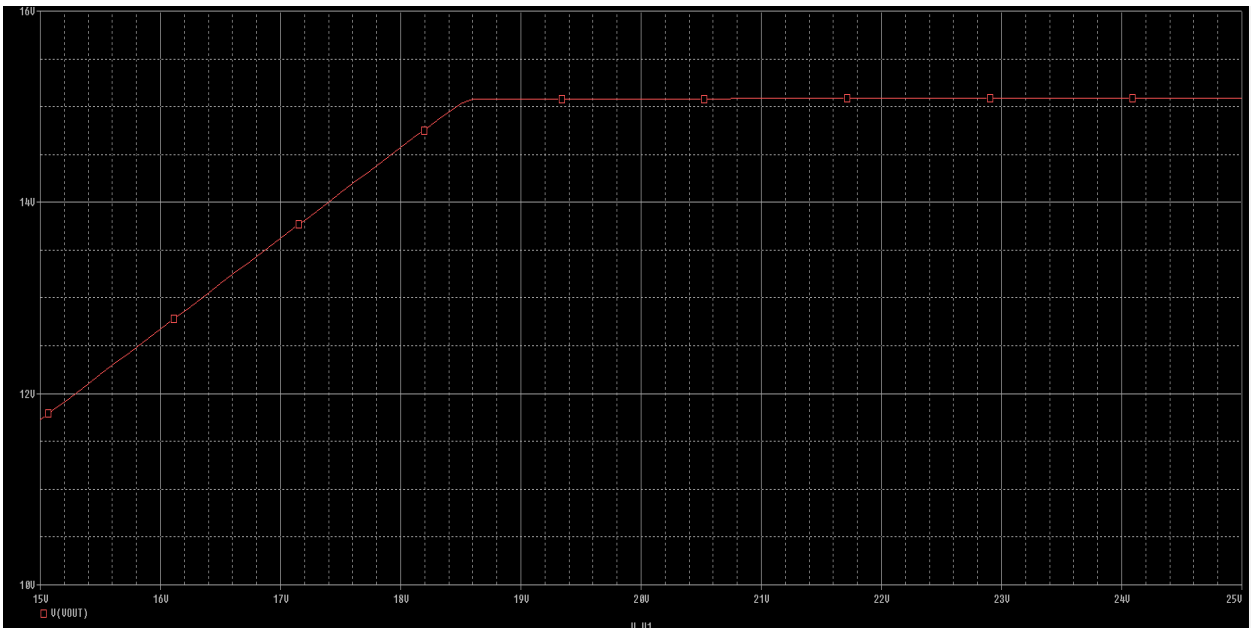


Figure 3 Minimum required programmable output voltage

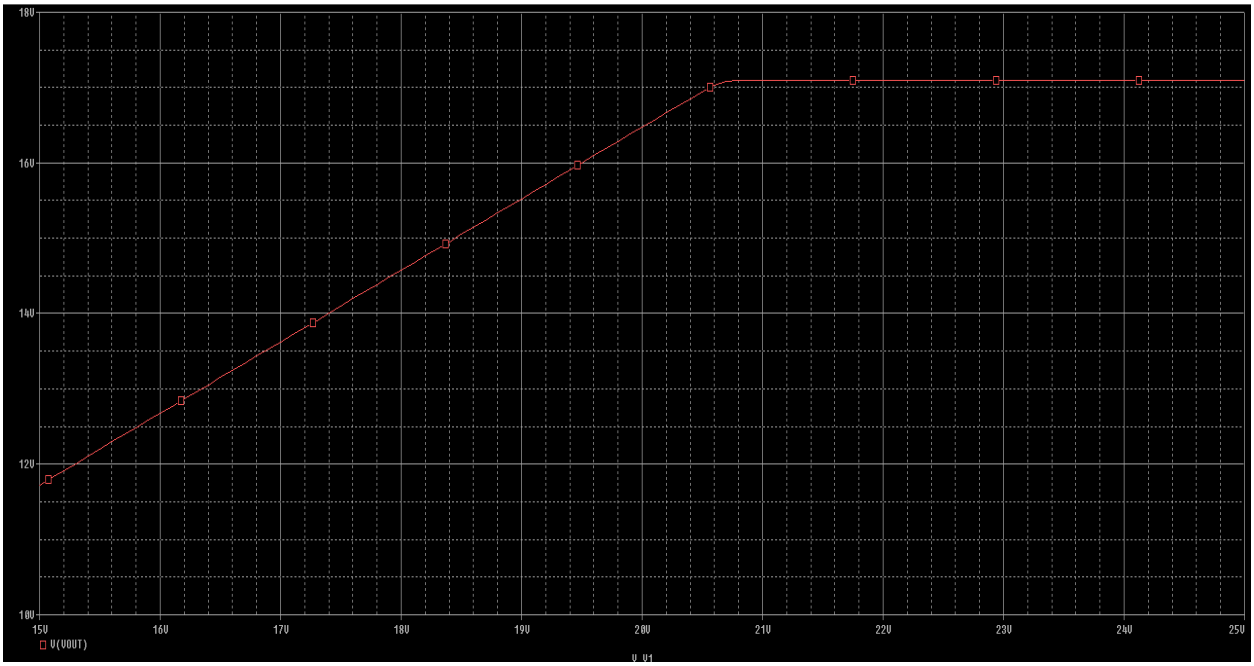


Figure 4 Maximum required programmable output voltage

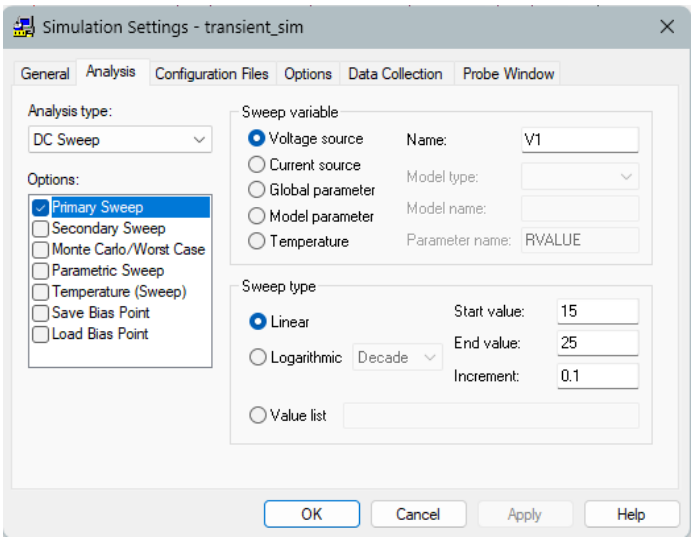


Figure 5 Maximum / minimum required programmable output voltage simulation settings

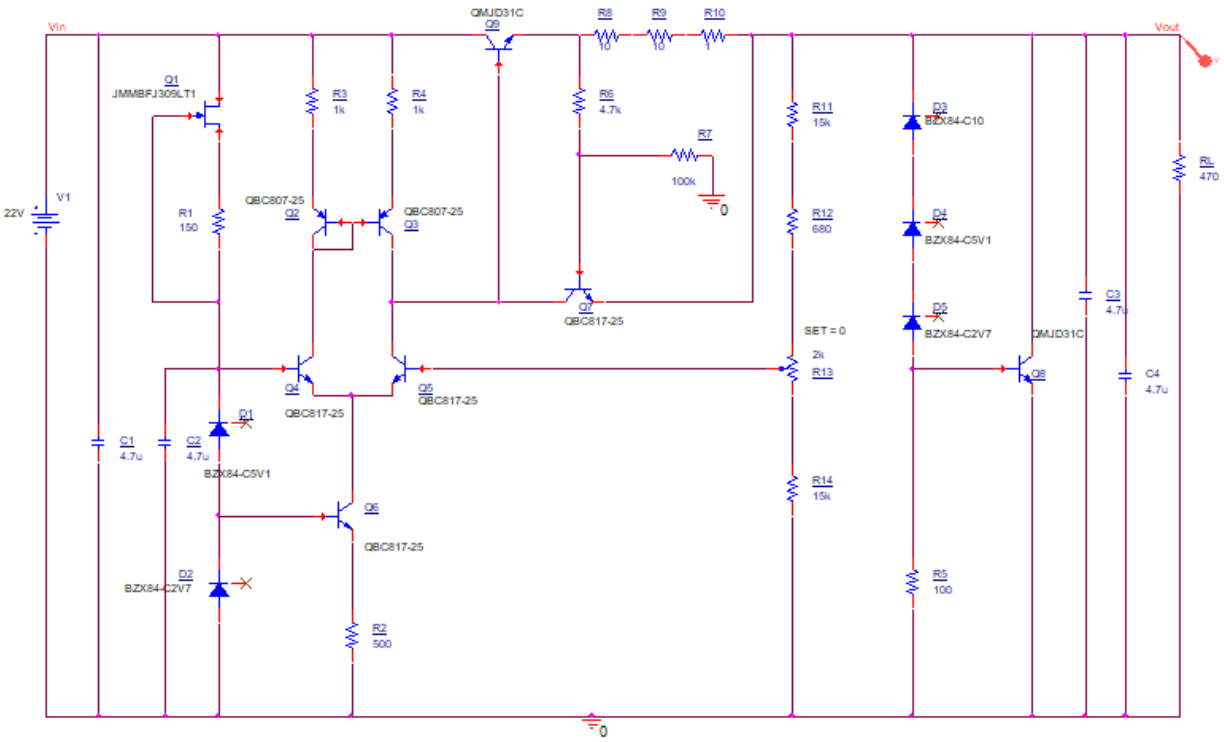


Figure 6 Maximum / minimum required programmable output voltage circuit configuration

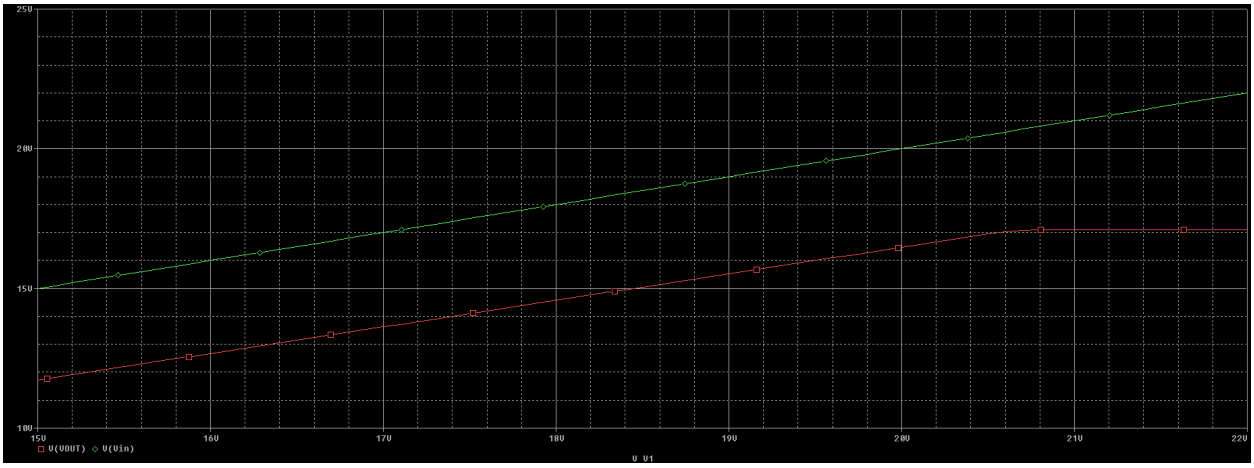


Figure 7 Worst case scenario when the input voltage is 22V and the output voltage is set to 17V

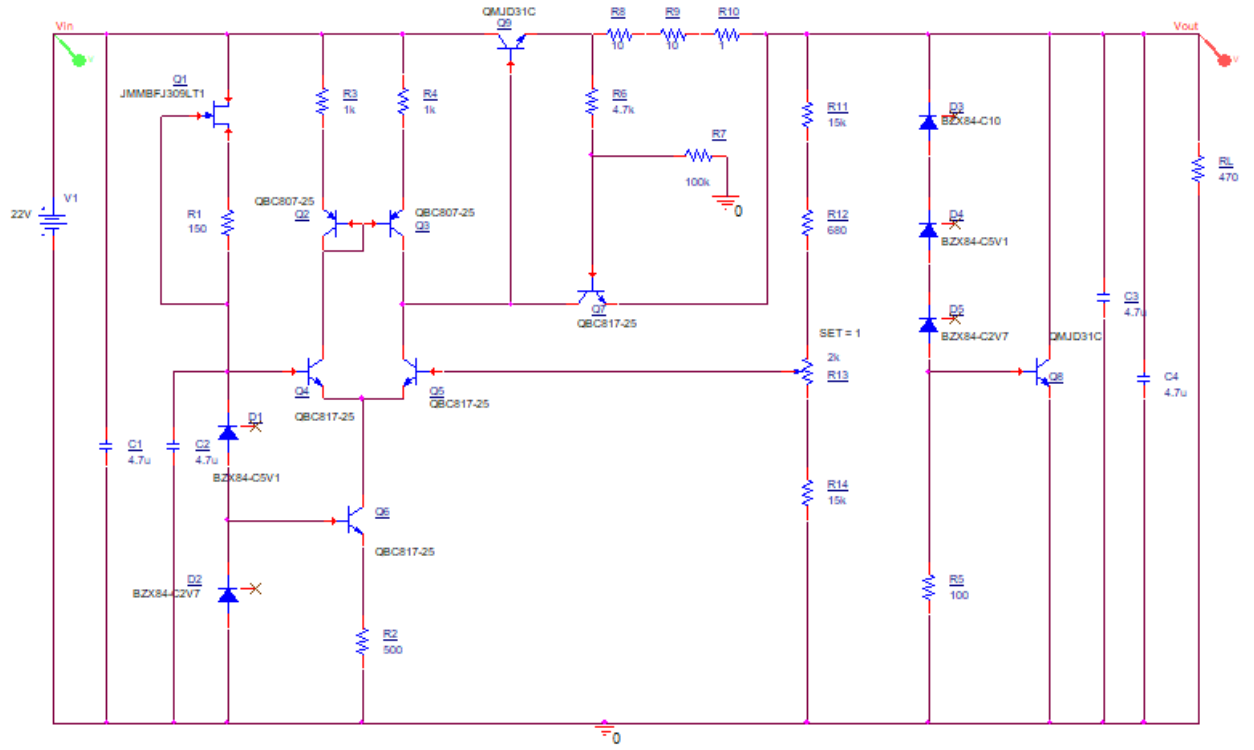


Figure 8 Circuit used in order to simulate the worst case scenario

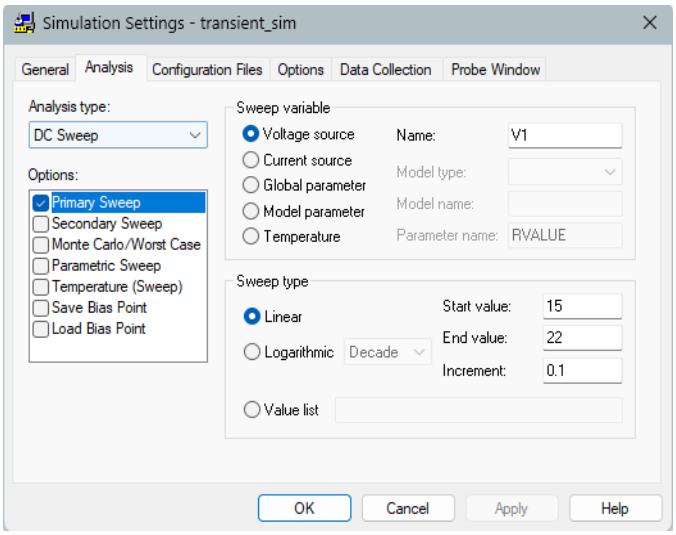


Figure 9 Simulation settings used to determine the output voltage in the worst case scenario

4.2 Stability (S)

The stability is obtained using a transient simulation on a sinusoidal generator. The obtained stability from the simulations is above 600.

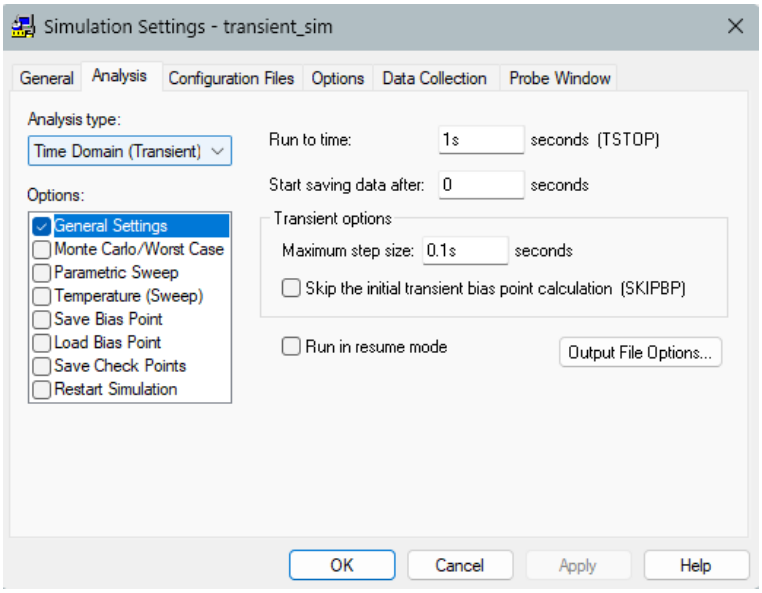


Figure 10 Settings for simulation in order to determine S

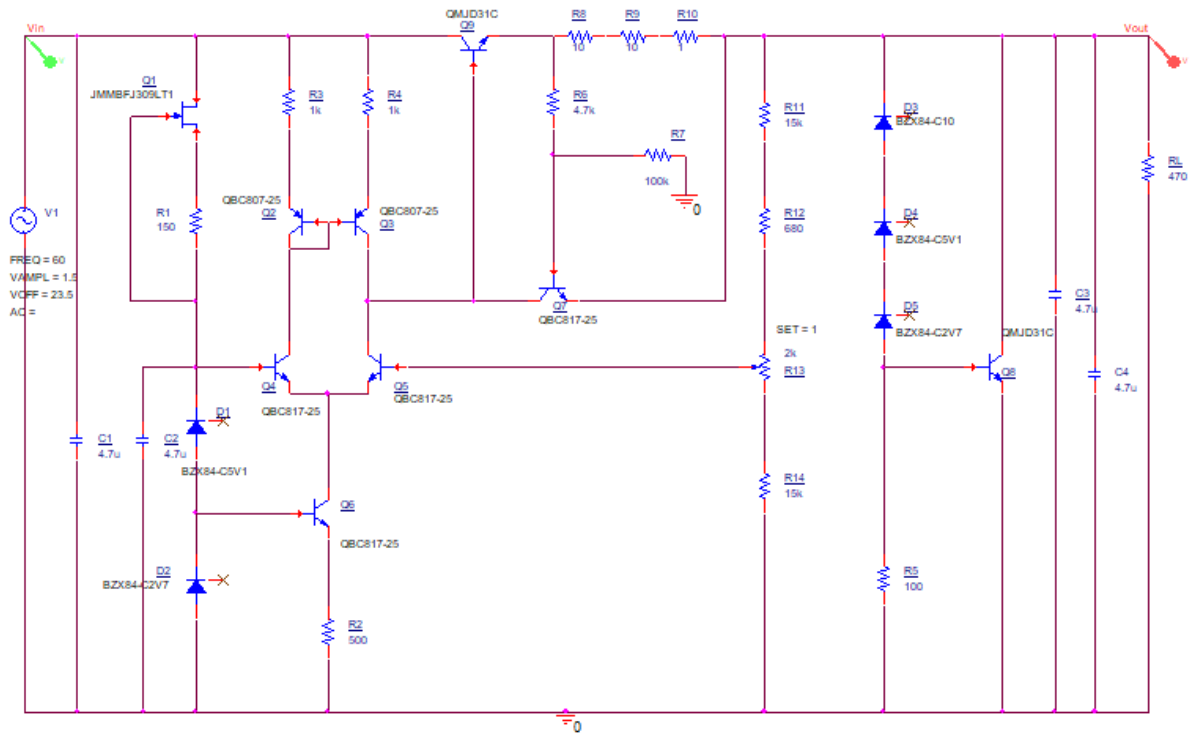


Figure 11 Circuit that was used in order to determine S

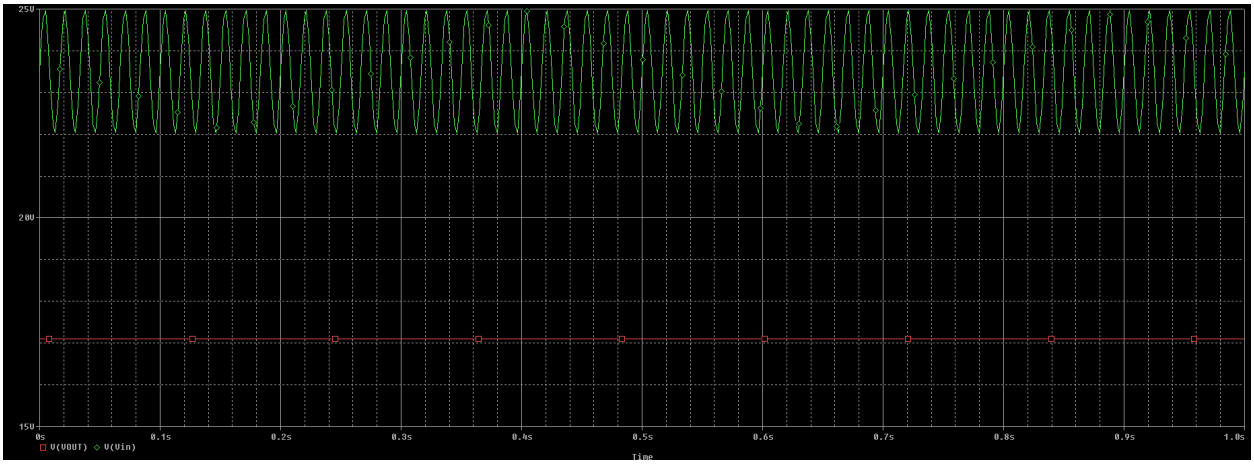


Figure 12 Variable input voltage(green) compared to the stable output voltage(red)

$$\Delta V_i = 3V$$

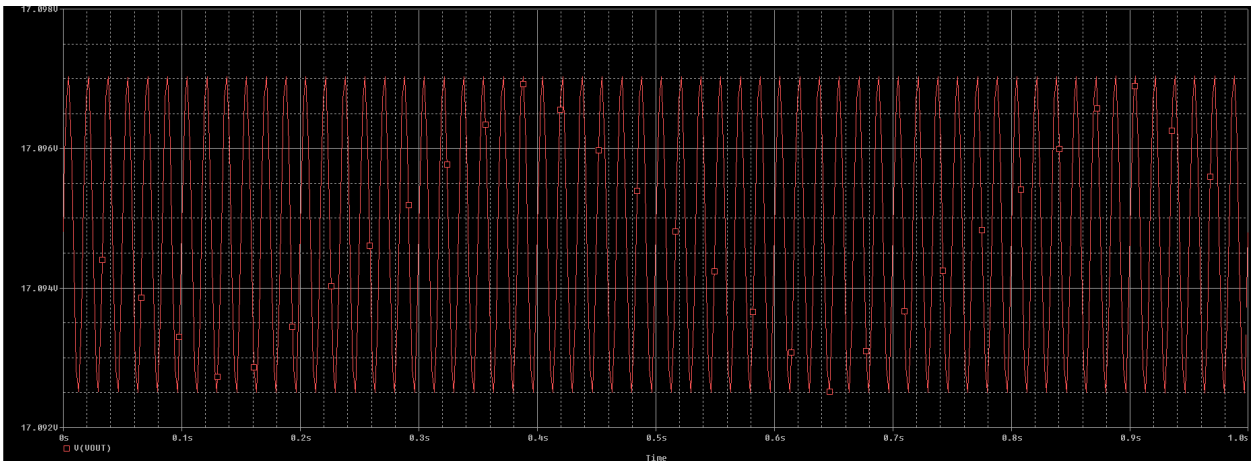


Figure 13 Actual variation of the output voltage

$$\Delta V_0 = 0.004V$$

$$S = \frac{\Delta V_i}{\Delta V_o}\Big|_{RL} = 750$$

4.3 Closed loop output impedance

The simulation of the **closed loop output impedance** is not trivial since the circuit has a negative feedback loop. The schematic was modified to be able to simulate the variation of the output voltage when the output current varies between 34mA and 28mA.

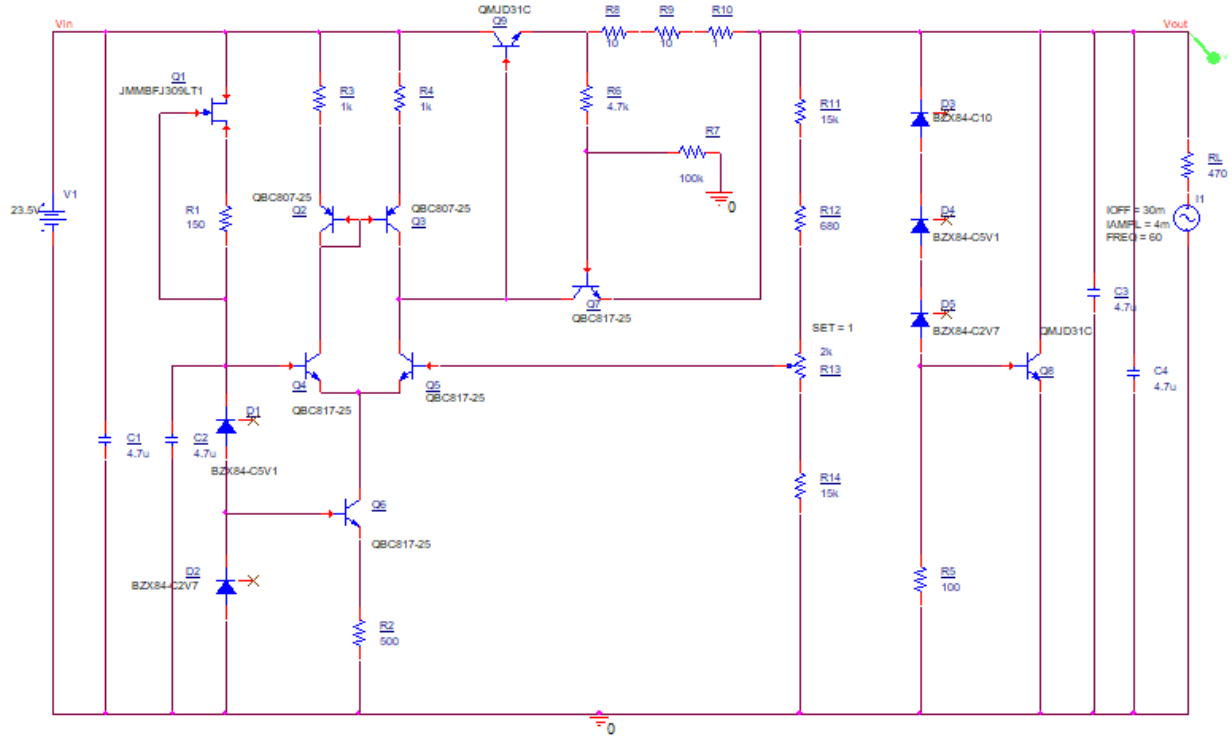


Figure 14 Circuit used in order to determine the closed loop output impedance

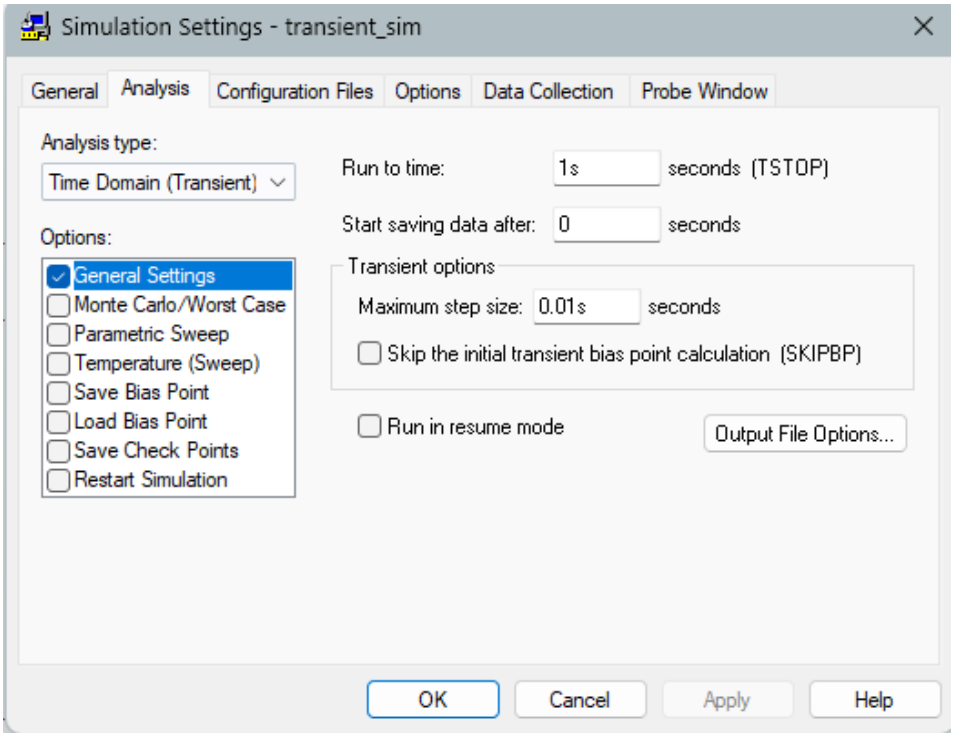


Figure 15 settings that were used in order to simulate

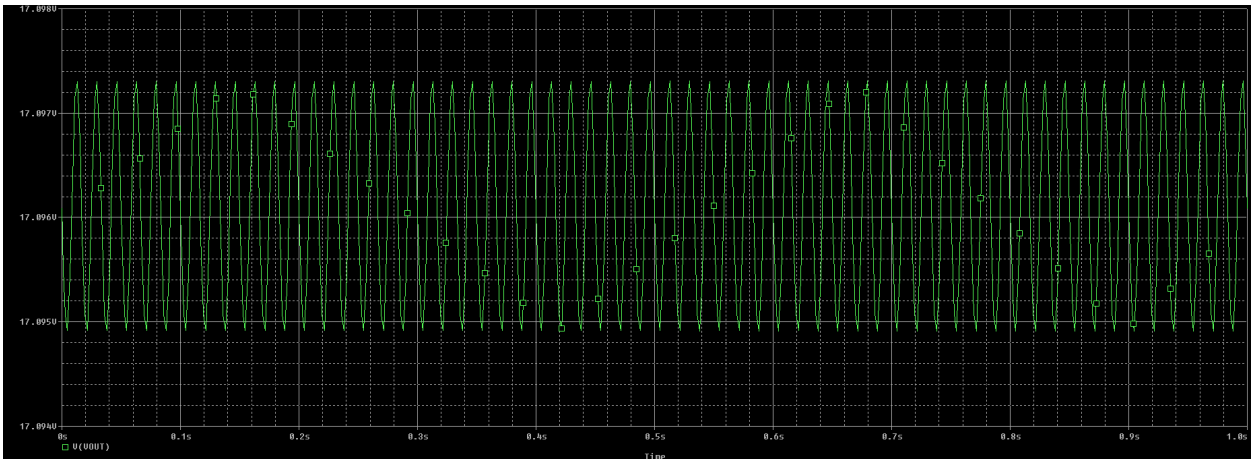


Figure 16 Variation of the output voltage

One can determine the variation of the output voltage by subtracting the maximum of the sinusoid, which is 17.097 by the minimum 17.095V and obtain a variation of 2mV.

$$\Delta V_o = 2\ mV$$

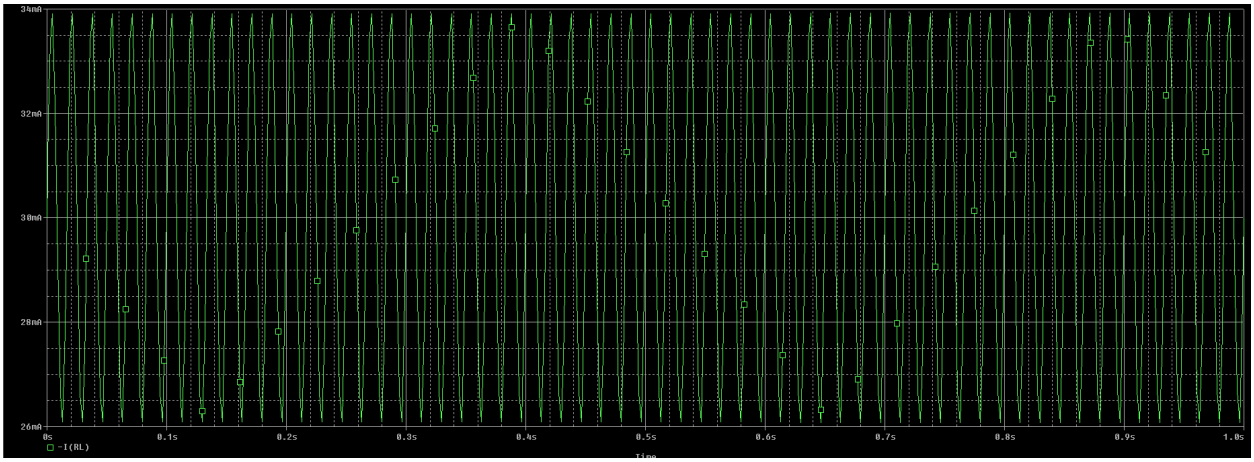


Figure 17 Variation of the output current

From the graph, one can determine that the variation of the output current is equal to 12 mA.

$$\Delta I_o = 8\ mA$$

$$Ro = \frac{\Delta V_o}{\Delta I_o} = 0.25 \text{ ohm}$$

4.4 Over current protection (OCP)

The simulation of the **over current protection** is done using a VPWL source at the output of the circuit that T1 = 20 has V1 = 17V and at T2 = 0 has V2 = 0V. This simulates a short circuit at the output of the circuit.

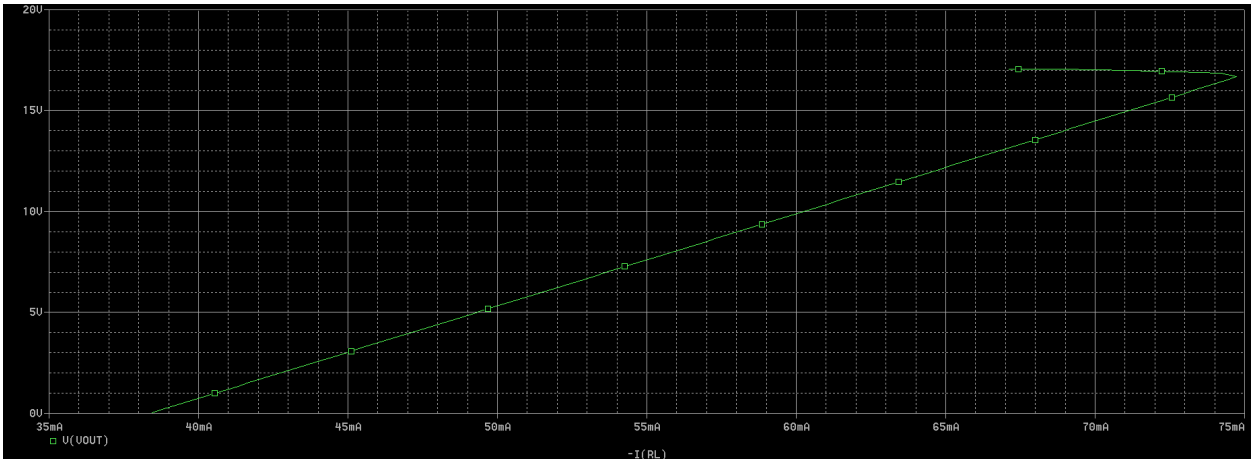


Figure 18 Overcurrent protection with foldback

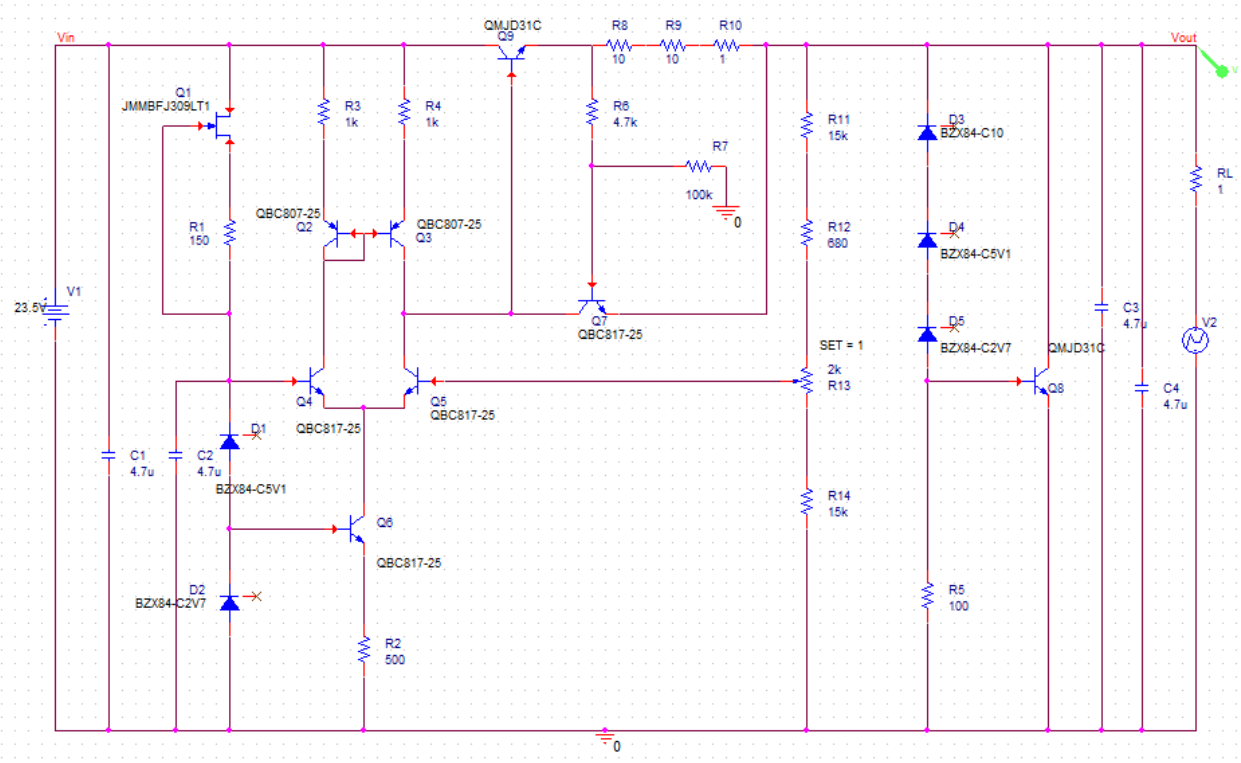


Figure 19 Circuit used in order to simulate the OCP

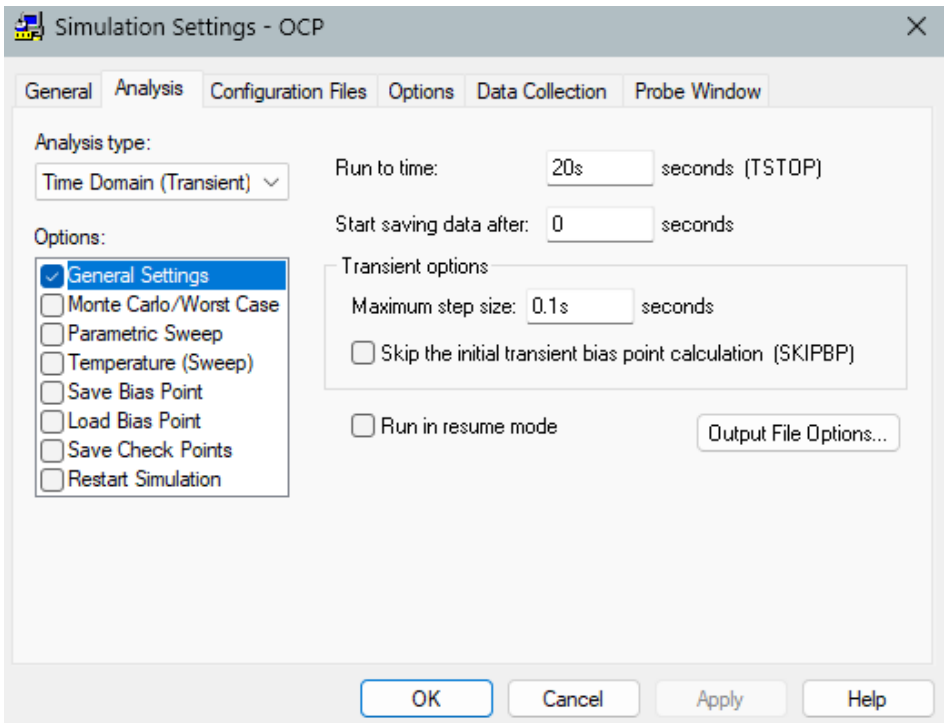


Figure 20 Settings used in order to simulate the OCP

4.5 Over voltage protection (OVP)

The simulation of the **over voltage protection** is done using a VDC source at the input and by modifying the potentiometer in such a way to have an output regulated voltage higher than 18.4V. Therefore the value of the potentiometer is changed to 5k. This is a DC sweep simulation of the input voltage source between 15V and 25V.

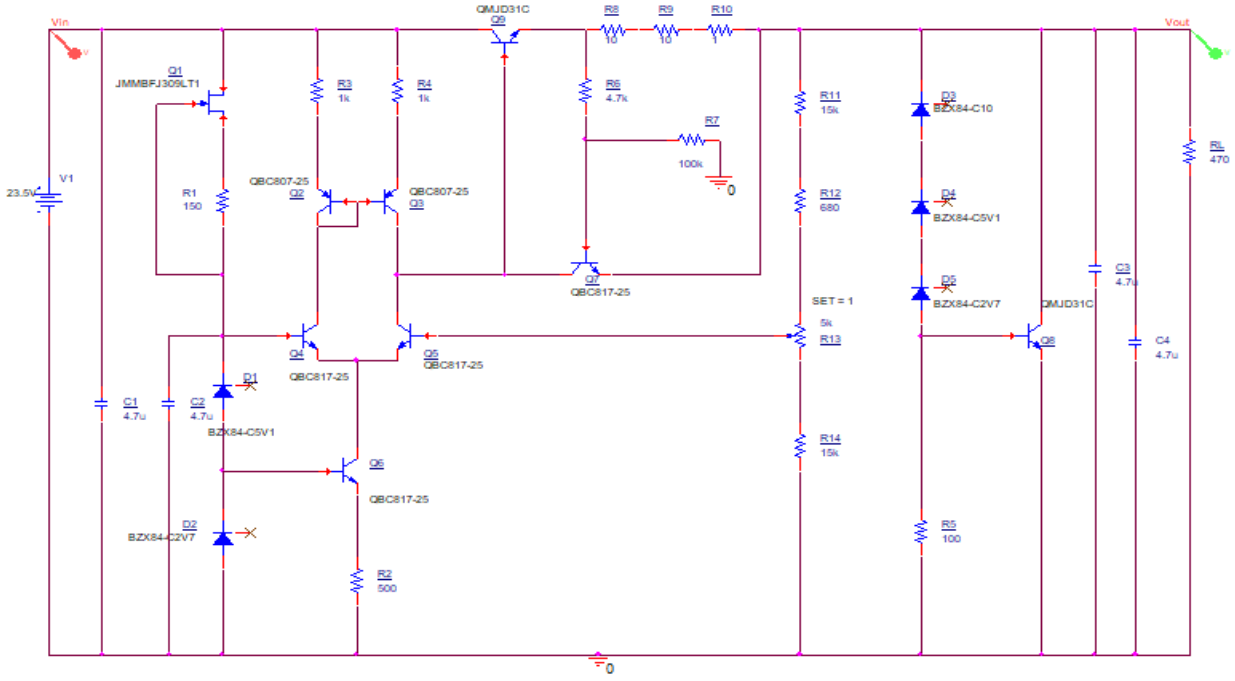


Figure 21 Circuit used in order to simulate the OVP

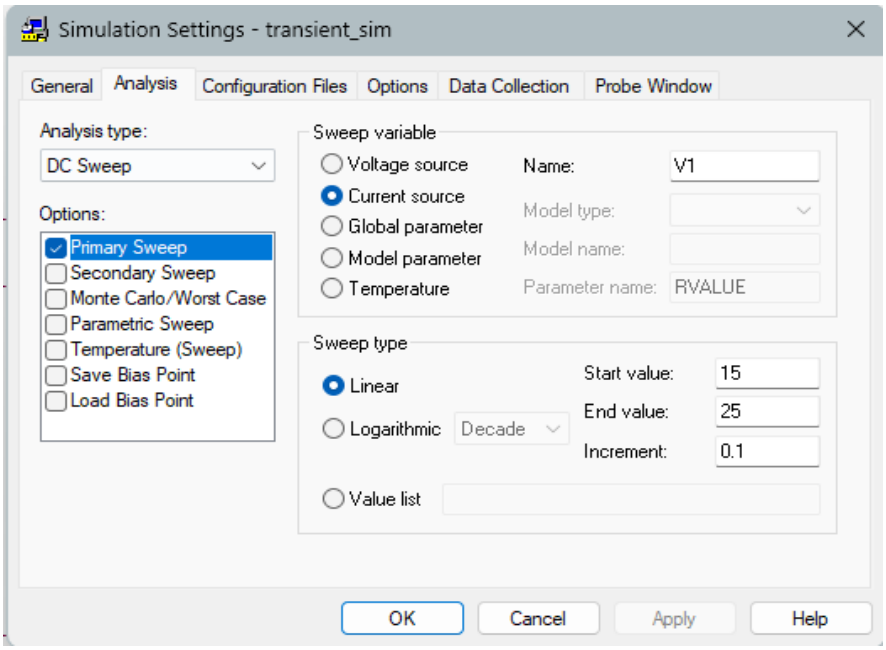


Figure 22 Settings used in order to simulate the OVP

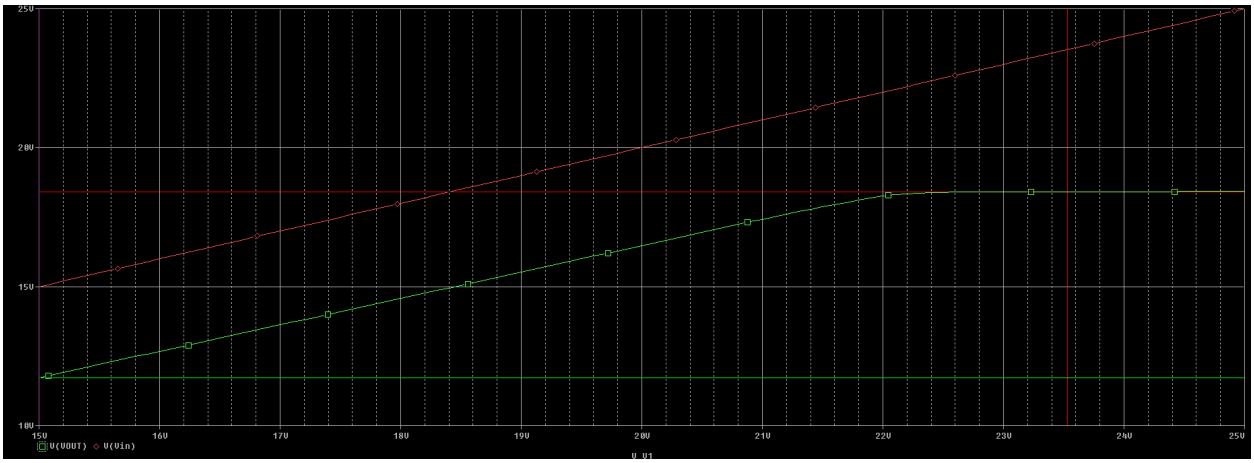


Figure 23 Output voltage(green) that is limited to 18.4V compared to the input voltage(red)

One can see that the output voltage becomes limited at the 18.4V. This is due to the fact the voltage drop across the Zener diodes in the OVP is 17.8V summed with the voltage drop across the base-emitter of the Q10 when it starts to conduct.

5. Conclusions

The purpose of the designed circuit was achieved. It was demonstrated first by means of calculus of all the parameters of the circuit and secondly by simulating them in PSpice in order to demonstrate the correctness of the calculus. Since I did not take into consideration high order effects, some of the obtained values are slightly different in the simulation.

6. Layout and mounting map

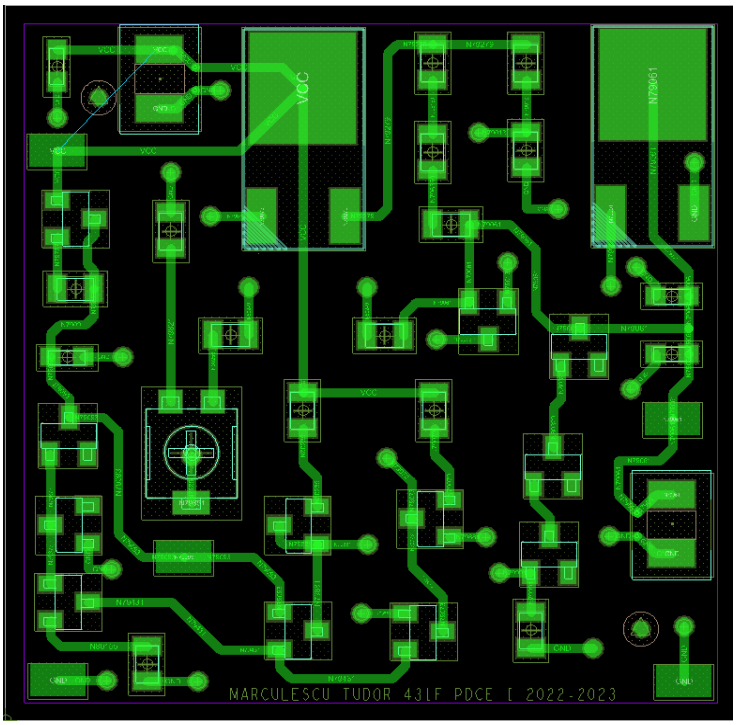


Figure 24 TOP layer view of the PCB

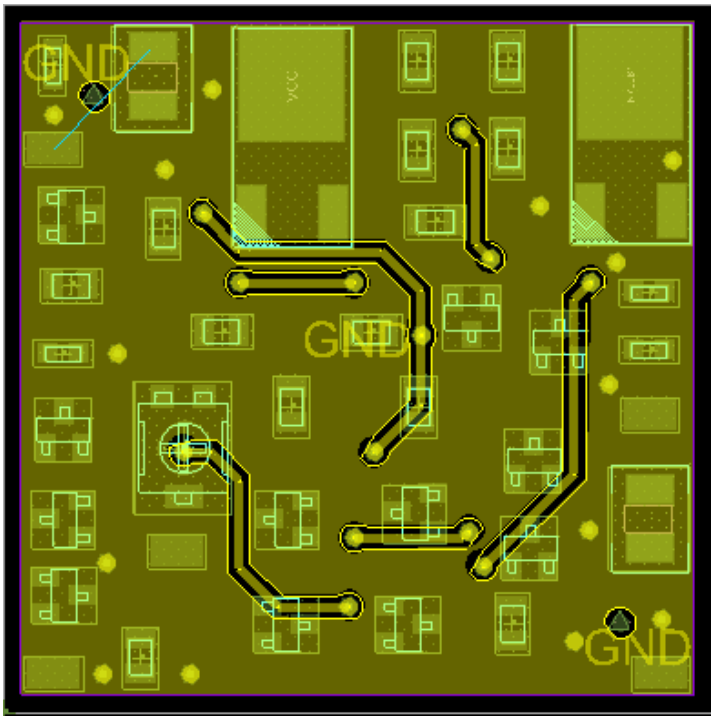


Figure 25 BOTTOM layer view of the PCB

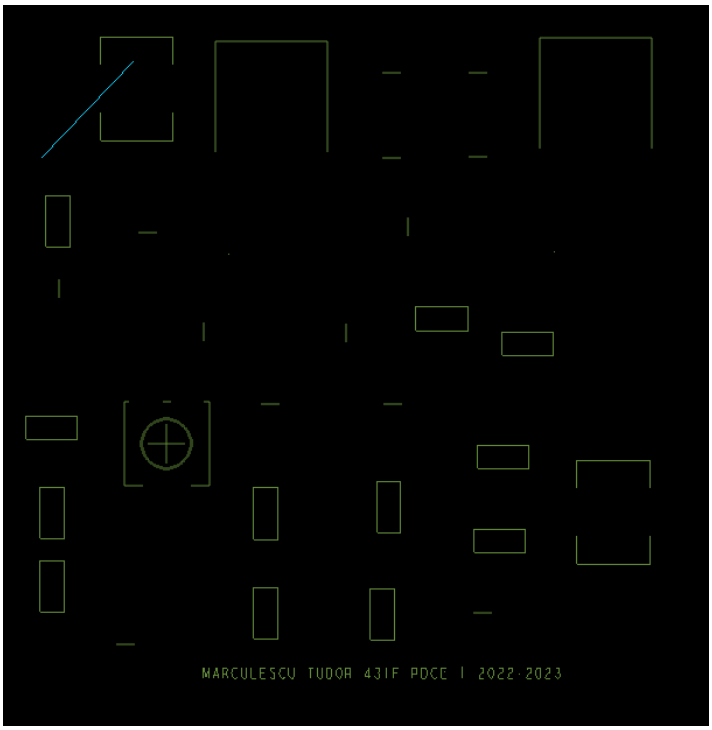


Figure 26 Silkscreen TOP layer view of the PCB

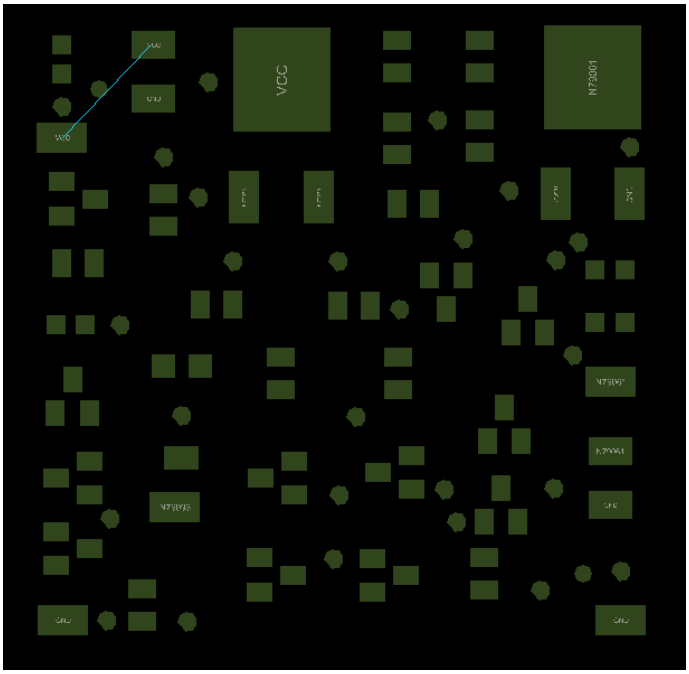


Figure 27 Soldermask TOP view of the PCB

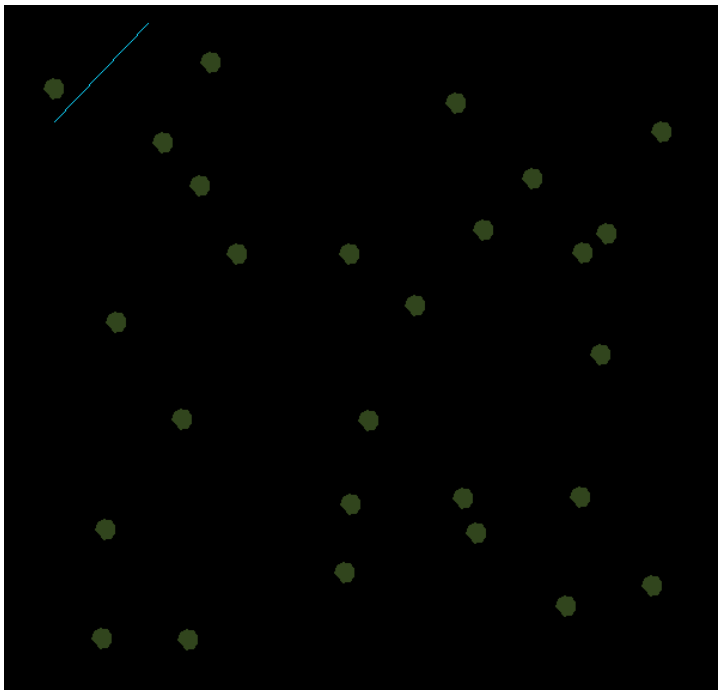


Figure 28 Soldermask BOT view of the PCB

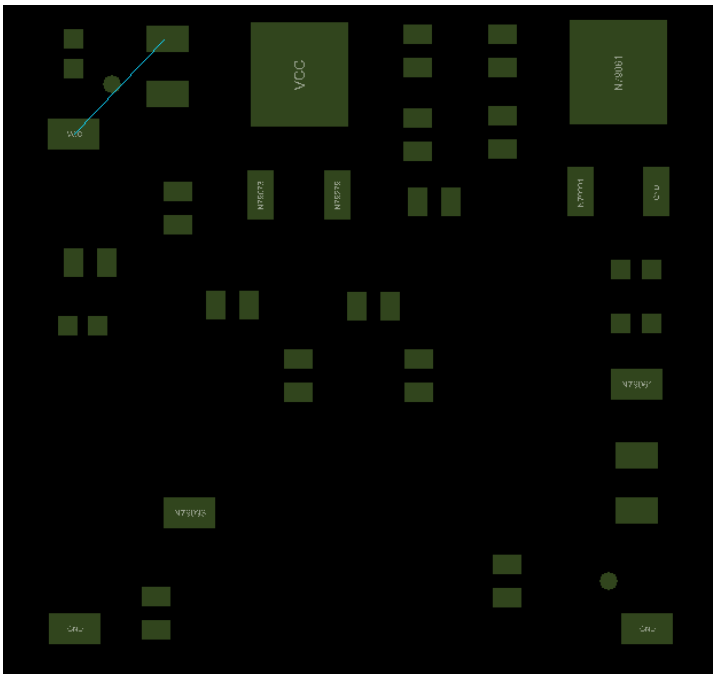


Figure 29 Soldepaste TOP view of the PCB

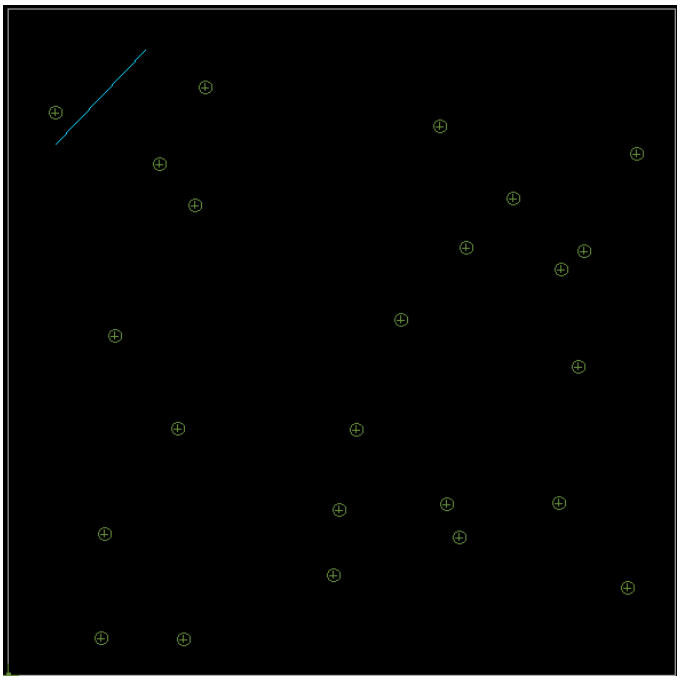


Figure 30 Mechanical layer view of the PCB

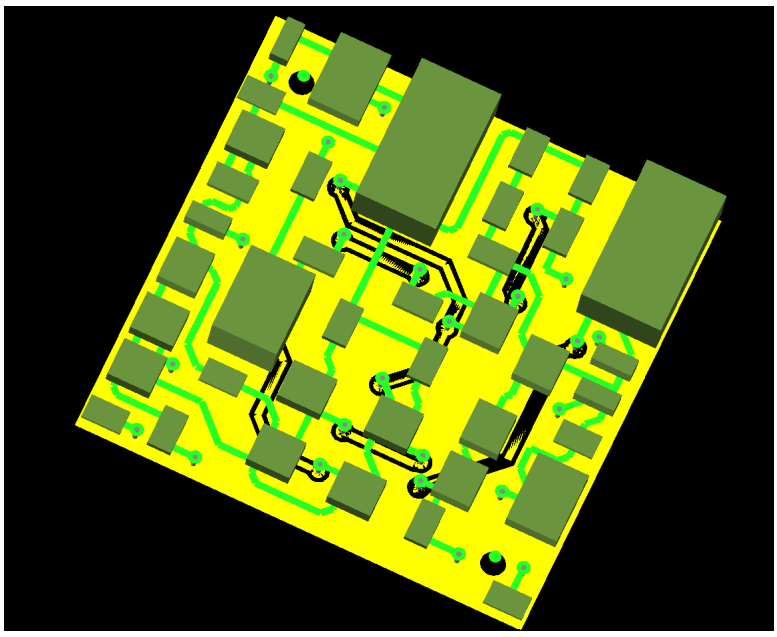


Figure 31 3D view of the whole PCB

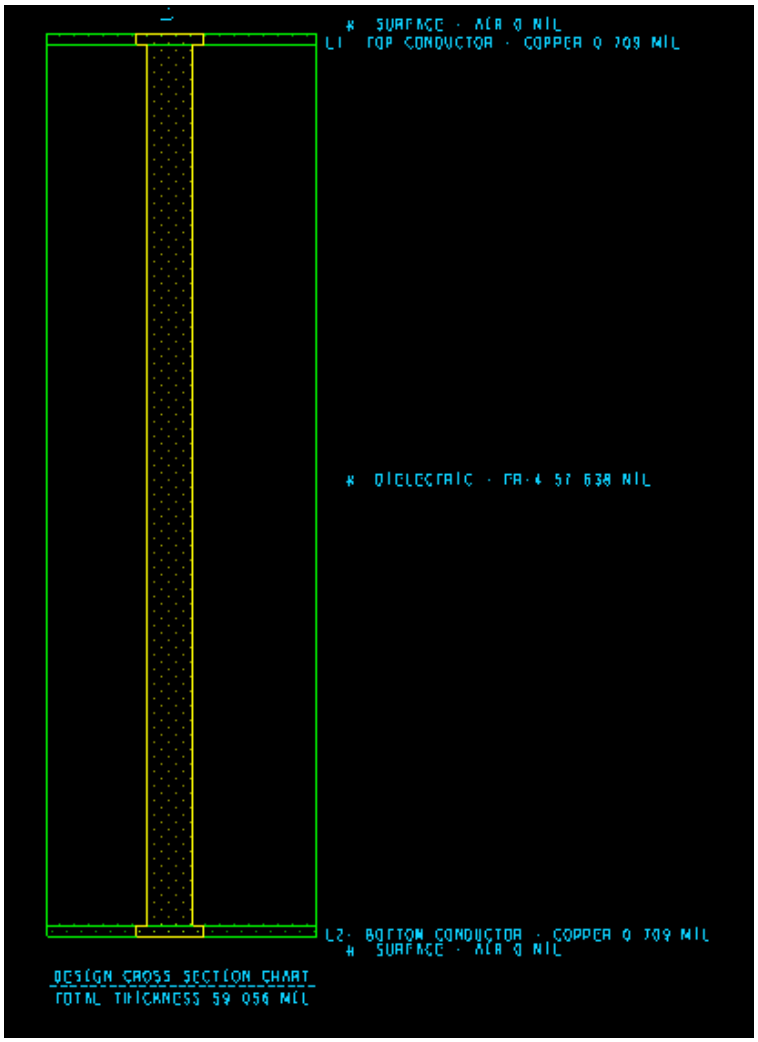


Figure 32 Cross section of the PCB

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
	15.74	PLATED	26

Figure 33 Drill chart

6.1. User manual

The voltage regulator is a good power supply for low power electronics. It stabilizes the variable input voltage in order to make sure that the circuit, to which it provides stable voltage, will work in the best conditions.

The output voltage is variable from the minimum 15V up to the maximum of 17V. It can be varied by changing the position of the potentiometer.

The maximum output current is 60 mA, however the circuit was designed to work with a load impedance of 500Ω, therefore providing a maximum current of 34 mA.

The circuit has over voltage protection at its output terminals, keeping the voltage at a maximum of 18.4V. It is also equipped with a over current protection with foldback which ensures a maximum short circuit current of around 30 mA.

A minimum input voltage of 22V should be provided to the regulator in order to ensure its best functionality.

A maximum input voltage up to 25V is allowed.

7. References

1. Motorola Inc., "LINEAR / SWITCHMODE VOLTAGE REGULATOR HANDBOOK", 1982 (https://ia800609.us.archive.org/35/items/bitsavers_motoroladaitchmodeVoltageRegulatorHandbook_23523522/1982_Linear_Switchmode_Voltage_Regulator_Handbook.pdf , last accessed 20.11.2022)
2. L. Teodorescu, http://wiki.dcae.pub.ro/images/7/79/Linear_regulator.pdf (last accessed 17.10.2022)
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5. Electronic fundamental circuits course, Linear Regulators, Faculty of Electronics, Telecommunications and Information Technology