

## Positive Voltage Regulator (431F)

It is required to design a positive linear voltage regulator with discrete components, with the following specifications:

- ◆ Supply voltage between  $(N+9) \div (N+12)$  [V];
- ◆ Programmable output voltage  $(N+2) \div (N+4)$  [V];
- ◆ The output current through the load between  $(0) \div (60-2 \cdot N)$  [mA];
- ◆ Short circuit protection of the output terminals with foldback current limiting circuit.
- ◆ Overvoltage protection of the output terminals.
- ◆  $S = \frac{\Delta V_i}{\Delta V_o} \bigg|_{RL} \geq (100-N)$ .
- ◆ The output impedance of the regulator  $R_o \leq ([N/5] + 1) \Omega$ , where  $[x]$  is the integer part of  $x$

Note: N is the index from the catalog for each student (file attached).

The circuit will be practically implemented on a PCB. There are two options:

- a. **Through Hole Technology – THT (stripboard) (maximum points = 70)**
  - b. **Surface Mount Technology – SMT (PCB) (maximum points = 100)**
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- a. **For THT (stripboard) (maximum points = 70), the following requirements should be accomplished:**

The project will be a written document (\*.pdf file) and it will contain:

    1. Cover page: title of the project, name and group of the student, the name of the project guide, project year; on the top side you can add the name of the university and the name of the faculty.
    2. The requirements page: by replacing N with your index, the project parameters will be determined and put on this page.
    3. The block diagram of the circuit with comments on it.
    4. The detailed schematic diagram with detailed explanations related to operation, identification of each subblock which was presented in the block diagram, and the calculations for each component (passive or active) that is part of that subblock.
      - *The active and the passive components will be taken from the Annex 1.*
      - *The passive components will have standard values.*
      - *The semiconductor parameters will not exceed the values from the datasheets.*
      - *The choice of a certain component will be justified by calculation.*
      - *It will prove that each component has a reliable operation (for example, for a bipolar junction transistor it will be justified that the maximum absolute values from the datasheet are not reached -  $I_{C_{MAX}}$ ,  $V_{CE_{MAX}}$ ,  $P_{d_{MAX}}$ ).*
      - *The calculus should demonstrate that the imposed specifications of the design are fulfilled.*
    5. *SPICE simulations of the designed circuit (circuit files, the waveforms, bias points, etc.).* For simulations, you may use any free or commercial SPICE simulator. A list with examples is mentioned below:
      - SPICE 3 (<https://ptolemy.berkeley.edu/projects/embedded/pubs/downloads/spice/index.htm>)
      - Spice from Microsim (<https://wiki.dcae.pub.ro/index.php/Fi%C8%99ier:Spice.rar>)
      - LTspice (<https://wiki.dcae.pub.ro/index.php/Fi%C8%99ier:Spice.rar>)
      - TINA Student version (<https://www.tina.com/tina-student-version/>)
      - Orcad 16.6 Lite (<http://www.cetti.ro/v2/orcad16.php>);  
[https://drive.google.com/drive/folders/0B7fpav7MwqmnSTJpU051amdleFU?resourcekey=0-Cm2IwCLDxFjFxrG\\_MbXWlw&usp=sharing](https://drive.google.com/drive/folders/0B7fpav7MwqmnSTJpU051amdleFU?resourcekey=0-Cm2IwCLDxFjFxrG_MbXWlw&usp=sharing))
      - Orcad 9.1 with Schematics (<https://wiki.dcae.pub.ro/index.php/Fi%C8%99ier:Pspice.rar>)The simulation print screens may be included in the project, but only accompanied by hand calculations. The total space occupied in the document by the images with the simulations must be less than 25% of the total size of the project.
    6. A short comment (less than half a page) where to summarize your personal contribution to this project, as a conclusion.

7. Bibliography. Any external document used for the project should have references in the text. For example, if you use the transistor BC337 in your project, you will mark BC337 with square brackets (e.g. BC337 [b2], where b2 is the position in the bibliography list:

b2: <https://www.onsemi.com/pub/Collateral/BC337-D.PDF>).

8. A mounting map with the placement of the components on the stripboard should be provided.

9. A bill of materials (BOM) with all THT components used in the project will be sent in .xls format to the staff. The components will be taken from Annex 1\_THT.xls provided by the faculty staff.

10. Board equipping.

11. Board testing and troubleshooting.

12. Board measurements.

13. Results presentation.

#### Important deadlines for THT implementation:

##### i. For the First Semester:

1. The project has a strict deadline. Until the end of the VII<sup>th</sup> week, requirements 1-7 should be accomplished. If not, the student will not graduate the exam. Also, the student will fail the matter on the second semester (Project 1 practical implementation and commissioning)
2. Until the end of the X<sup>th</sup> week, requirements 8-9 should be accomplished.
3. The project including the minimal content form (points 1-7 to be accomplished!) will be uploaded on Moodle until the end of the X<sup>th</sup> week (the deadline is the first working day of the week 10). The document (project) should be a \*.pdf with a size less than 10MB with the following name: *PR1\_FirstName\_LastName\_Group.pdf*. For the students who want to retake their assessments, the file name should be: *PR1\_FirstName\_LastName\_Group\_Actual\_Group.pdf*
4. The archive which contains all necessary simulation files will be also uploaded after the project upload. The file should be a .zip with a size less than 10MB with the following name: *PR1\_FirstName\_LastName\_Group.zip*. For the students who want to retake their assessments, the file name should be: *PR1\_FirstName\_LastName\_Group\_Actual\_Group.zip*

Note: if the archive is too big, you should delete some simulation files which are not necessary (e.g. \*.dat files).

##### ii. For the Second Semester:

- a. Until the end of the IV<sup>th</sup> week, requirement 10 should be accomplished.
- b. Until the end of the VI<sup>th</sup> week, requirement 11 should be accomplished.
- c. Until the end of the IX<sup>th</sup> week, requirements 12-13 should be accomplished.

#### b. For Surface Mount Technology - SMT (maximum points = 100), the following requirements should be met:

1. Requirements 1-7 of point a (THT technology)
2. A chapter which includes a short form of a user manual for the designed circuit for potential customers.
3. PCB Layout (including all layers) which include:
  - The TOP image of the designed PCB.
  - The BOTTOM image of the designed PCB.
  - The Silk Screen TOP image;
  - The Solder Mask TOP and BOTTOM images;
  - The Solder Paste TOP image;
  - The mechanical layer.
4. The Gerber files for the layout (RS-274x standard)
5. Bill of Materials (BOM) file. The components will be taken from Annex 1\_SMT.xls provided by the faculty staff.
6. Power Point presentation of the Project (max. 10 minutes) – MS Teams.
7. Board equipping.
8. Board testing and troubleshooting.
9. Board measurements.
10. Results presentation.

#### Important deadlines for SMT implementation:

##### i. For the First Semester:

1. The project has a strict deadline. Until the end of the VII<sup>th</sup> week, requirement 1(1-7 of point a THT) should be accomplished. If not, the student will not graduate the exam. Also, the student will fail the matter on the second semester (Project 1 practical implementation and commissioning).

2. Until the end of the X<sup>th</sup> week, requirements 2-5 should be accomplished.
3. **The project including the minimal content form (points 1-5 to be accomplished!) will be uploaded on Moodle until the end of the X<sup>th</sup> week (the deadline is the first working day of the week 10).** The document (project) should be a \*.pdf with a size less than 10MB with the following name: *PR1\_FirstName\_LastName\_Group.pdf*. For the students who want to retake their assessments, the file name should be: *PR1\_FirstName\_LastName\_Group\_Actual\_Group.pdf*.
4. **The archive which contains all necessary simulation files will be also uploaded after the project upload.** The file should be a .zip with a size less than 10MB with the following name: *PR1\_FirstName\_LastName\_Group.zip*. For the students who want to retake their assessments, the file name should be: *PR1\_FirstName\_LastName\_Group\_Actual\_Group.zip*

**Note:** if the archive is too big, you should delete some simulation files which are not necessary (e.g. \*.dat files).

## **ii. For the second semester:**

- a. Until the end of the IV<sup>th</sup> week, requirement 7 should be accomplished.
- b. Until the end of the VI<sup>th</sup> week, requirement 8 should be accomplished.
- c. Until the end of the IX<sup>th</sup> week, requirements 9-10 should be accomplished.

## **Information:**

1. The student should design completely the circuit (it should work properly in theory and also in simulation) until the end of the first semester.
2. The student who fails the Project 1 tasks (complete and successfully Design and Simulation) in the first semester (score less than 50 points) will fail the matter (Project 1 practical implementation and commissioning) in the second semester.
3. The student will receive all the necessary components from the faculty staff, and he will mount them on the stripboard or PCB in the second semester.
4. The student has the duty to learn the soldering techniques and how to use the measurement and test equipment (power supply, digital multimeter, oscilloscope) to built, test and measure his own Project (the board) in the second semester.
5. The student will rework, test, repair (if necessary!) and measure the board in the second semester.
6. Also, a hard copy of the Project may be provided by the student at the request of the supervisor (paper form and electronic form-on a CD - containing the written document- the Project- and the simulations).
7. **The designed board remains in the faculty property.**

The manufactured board in SMT & PCB technology will fulfil the following requests (**any further details will be provided by Dr. Mihaela Pantazică**):

- ◆ PCB dimensions: 40mm x 40mm;
- ◆ Board is double sided, FR4, thickness of the copper foil 18µm, board thickness 1.5mm;
- ◆ All components are placed on the TOP side;
- ◆ There will be used only SMD passive components in 0805 packages;
- ◆ There will be used only SMD FET, MOSFET and bipolar transistors (SOT-23, D-PAK packages);
- ◆ Round test points (maximum 5) – justified by the test plan;
- ◆ The design origin (0,0) must be placed in the bottom left corner of the PCB, all coordinates must have positive values;
- ◆ A clearance of 1mm will be kept from the edges of the board;
- ◆ The board will be provided with 2 global fiducial markers on the TOP layer, at a distance of 200mils from the edges of the board, conveniently placed; these markers will also exist on the Solder Paste Top layer (overlapping those on the TOP); they will be used when aligning the stencil with the PCB. The fiducial marker will be a circle with a minimum diameter of 1mm on the respective layer, located in a circular space with a minimum diameter double the inner circle, in which there will be nothing on any layer;
- ◆ Careful attention should be paid to the Silk Screen TOP layer; the silkscreen should not appear on the pads of the components;
- ◆ A mechanical layer will be generated. This will contain the board outline, the drill drawing, the drill chart/table, drill legend, the layer stack-up and mechanical information for PCB manufacturing.
- ◆ The dimension quotes of the PCB shouldn't appear on the TOP layer. If these quotes exist, they should appear on a non-electrical mechanical layer;

- ◆ The board will be provided with identification information about the designer (Last Name, First Name, Group, PDCE I 2022-2023).

The Gerber files (274x standard) and the Excellon file should contain the following information:

- ◆ board outline;
- ◆ electrical layer TOP;
- ◆ electrical layer BOTTOM;
- ◆ non-electrical layer Silk Screen Top;
- ◆ non-electrical layer Solder Mask Top;
- ◆ non-electrical layer Solder Mask Bottom;
- ◆ non-electrical layer Solder Paste Top;
- ◆ the aperture list and the drilling file.

The following widths and spacings are given for the routing layers:

- ◆ 1A current – 28mils;
- ◆ Few hundreds mA currents - 22mils;
- ◆ Signal - 18mils;
- ◆ Spacing - 12mils;
- ◆ The via hole diameter is 0.4mm.

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