

Project 1 Exectuion Platforms

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1 Introduction to RISC-V Instruction Set Architecture

In this section we are focusing on a decomposition of RISC-V hex instruction into the ASM instruction. The instruction format is determined based on the opcode, funct3 and funct7 fields. Table 1 depicts a detailed translation of each instruction from it's hex code to it's format fields. Some of them not used in certain instruction types, and are marked with a dash (-) in the table. The ultimate factor that determines the instruction type is the "Type" column, which indicates instruction format label R, I, S or SB.

1.1 Program Instructions Decomposition

Address	Hex Code	Opcode (6:0)	rd (11:7)	funct3 (14:12)	rs1 (19:15)	rs2 (24:20)	funct7 (31:25)	imm[11:0] (31:20)	imm[11:5] (31:25)	imm[4:0] (11:7)	Type
0x0	0x00050893	0010011	10001	000	01010	-	-	000000000000	-	-	I
0x4	0x00068513	0010011	01010	000	01101	-	-	000000000000	-	-	I
0x8	0x04088063	1100011	-	000	10001	00000	-	-	0000010	00000	SB
0xc	0x04058263	1100011	-	000	01011	00000	-	-	0000010	00100	SB
0x10	0x04060063	1100011	-	000	01100	00000	-	-	0000010	00000	SB
0x14	0x04d05063	1100011	-	101	00000	01101	-	-	0000010	00000	SB
0x18	0x00088793	0010011	01111	000	10001	-	-	000000000000	-	-	I
0x1c	0x00269713	0010011	01110	001	01101	-	-	000000000010	-	-	I
0x20	0x00e888b3	0110011	10001	000	10001	01110	0000000	-	0000000	10001	R
0x24	0x0007a703	0000011	01110	010	01111	-	-	000000000000	-	-	I
0x28	0x0005a803	0000011	10000	010	01011	-	-	000000000000	-	-	I
0x2c	0x01070733	0110011	01110	000	01110	10000	0000000	-	0000000	01110	R
0x30	0x00e62023	0100011	-	010	01100	01110	-	-	0000000	00000	S
0x34	0x00478793	0010011	01111	000	01111	-	-	000000000100	-	-	I
0x38	0x00458593	0010011	01011	000	01011	-	-	000000000100	-	-	I
0x3c	0x00460613	0010011	01100	000	01100	-	-	000000000100	-	-	I
0x40	0xff1792e3	1100011	-	001	01111	10001	-	-	1111111	00101	SB
0x44	0x00008067	1100111	00000	000	00001	-	-	000000000000	-	-	I
0x48	0xff00513	0010011	01010	000	00000	-	-	111111111111	-	-	I
0x4c	0x00008067	1100111	00000	000	00001	-	-	000000000000	-	-	I
0x50	0xff00513	0010011	01010	000	00000	-	-	111111111111	-	-	I
0x54	0x00008067	1100111	00000	000	00001	-	-	000000000000	-	-	I

Table 1: Decomposition of Hex Codes to RISC-V Instruction Format

A point to note is that the immediate fields for UJ and U type instructions are missing from Table 1. This is because the provided program is missing them. There is also an overlap between the immediates of S and SB type instructions, as they share the same positions in the instruction format. The table head includes just the immediate fields for S out of simplicity, but in the case of SB, they were calculated as depicted in the RISC-V specification from the Project 1 description [1].

Address	Hex Code	ASM Instruction (ABI)	ASM Instruction (x-registers)
0x0	0x00050893	addi a7, a0, 0	addi x17, x10, 0
0x4	0x00068513	addi a0, a3, 0	addi x10, x13, 0
0x8	0x04088063	beq a7, zero, 64	beq x17, x0, 64
0xc	0x04058263	beq a1, zero, 68	beq x11, x0, 68
0x10	0x04060063	beq a2, zero, 64	beq x12, x0, 64
0x14	0x04d05063	bge zero, a3, 64	bge x0, x13, 64
0x18	0x00088793	addi a5, a7, 0	addi x15, x17, 0
0x1c	0x00269713	slli a4, a3, 2	slli x14, x13, 2
0x20	0x00e888b3	add a7, a7, a4	add x17, x17, x14
0x24	0x0007a703	lw a4, 0(a5)	lw x14, 0(x15)
0x28	0x0005a803	lw a6, 0(a1)	lw x16, 0(x11)
0x2c	0x01070733	add a4, a4, a6	add x14, x14, x16
0x30	0x00e62023	sw a4, 0(a2)	sw x14, 0(x12)
0x34	0x00478793	addi a5, a5, 4	addi x15, x15, 4
0x38	0x00458593	addi a1, a1, 4	addi x11, x11, 4
0x3c	0x00460613	addi a2, a2, 4	addi x12, x12, 4
0x40	0xff1792e3	bne a5, a7, -28	bne x15, x17, -28
0x44	0x00008067	jalr zero, ra, 0	jalr x0, x1, 0
0x48	0xfff00513	addi a0, zero, -1	addi x10, x0, -1
0x4c	0x00008067	jalr zero, ra, 0	jalr x0, x1, 0
0x50	0xfff00513	addi a0, zero, -1	addi x10, x0, -1
0x54	0x00008067	jalr zero, ra, 0	jalr x0, x1, 0

Table 2: RISC-V Instructions with register numbers, symbolic names and addresses

In order to better understand the provided program, Table 2 is introduced to map the hex codes with their corresponding assembly instructions. As an overall view, the program is making use of

RV32I instruction set only. The registers are represented in both their symbolic names (ABI) and x-register numbers. in order to facilitate the understanding of the program.

1.2 Branch Delay Slot Concept

The branch delay slot concept is interesting when discussing pipelined processors. Essentially, when a branch instruction is taken, the instructions that were fetched after the branch instructions might become invalid. To avoid this, the branch delay slot declares that the instruction immediately following a branch instruction is always executed, regardless of whether the branch is taken or not. This helps to mitigate the performance penalty associated with branch instructions that invalidate subsequent instructions in the pipeline. As explained in [2]: "The idea of the branch shadow or delay slot is to recover a part of the clocks. If you declare that the instruction after a branch is always executed then when a branch is taken, then the instruction in the decode slot also gets executed, while the instruction in the fetch slot is discarded. Therefore one has a hole of time not two."

In terms of advantages and disadvantages, there are several points to consider. For disadvantages:

- Branch delay slots may create complications in code debugging, since the instruction in the delay slot might have side effects, it may lead to an unexpected state of the registers and memory.
- It adds to the waiting time when trying to execute interruptions, since they will be deferred until the delay slot instruction is executed. This is a problem in the case of real time systems.
- Software compatibility requirements dictate that an architecture may not change the number of delay slots from one generation to the next. This inevitably requires that newer hardware implementations contain extra hardware to ensure that the architectural behaviour is followed despite no longer being relevant.

Advantages of using branch delay slots include:

- Improved performance in pipelined architectures, since it helps to reduce the number of pipeline stalls caused by branch instructions.

plus branch delay slots was initially a good idea then a bad idea

1.3 Branch Instructions Analysis

In order to understand better the provided program, it is useful to check the branch instructions and where they lead to.

Table 3: RISC-V Instructions with Addresses

Address	Conditional branch	Branch to
0x08	beq a7, zero, 64	0x48: addi a0, zero, -1
0x0c	beq a1, zero, 68	0x50: addi a0, zero, -1
0x10	beq a2, zero, 64	0x50: addi a0, zero, -1
0x14	bge zero, a3, 148	0x54: jalr zero, ra, 0
0x40	bne a5, a7, -28	0x24: lw a4, 0(a5)

From the table above we can see that there are 4 first conditional branches, that being the addresses 0x08, 0x0c, 0x10 and 0x14, which resemble input value checks. Considering the calling

convention for RISC-V, the registers a0-a7 are used for passing function arguments from the caller to the callee. In this case, the supposition of input value checks is valid. The first three jump to a return -1 in case the input values are 0, while the fourth one jumps to a return with the number of elements to be processed, which would be less than or equal to 0.

The last conditional branch at address 0x40 is part of a loop. It checks whether the address stored in register a5, used as a counter, is equal to the last address to be processed, which is stored in register a7. If they are not equal, the program branches back to address 0x24 to continue processing the next elements. If they are equal, the program continues to the return instruction.

1.4 Program Functionality

The program can be divided into three main parts: input validation, processing loop, and return value. The input validation part checks if any of the first three caller arguments are 0. The arguments are passed are actually pointers to the input and output arrays, so they are checked if they are null, which would indicate an invalid memory access, therefore leading to a jump to the section of the program corresponding to return -1. The fourth argument is the number of elements to be processed, which is checked in the register a3 to see if it is less than or equal to 0. In case it is, the program jumps to the section corresponding to return. In this case, it will return to the callee the value stored in a0, which is actually a3, the number of elements to be processed.

The processing loop starts at address 0x18 and continues until the branch instruction at address 0x40. It consists of an initial setup for the loop counter in register a5 and for the final value of the counter, which is stored in register a7. Register a7 will store the address of the last element to be processed from one of the input arrays, calculated as the base address plus the number of elements multiplied by 4, the size of each element. Because the elements are 4 bytes long, it can be extrapolated that the arrays are made of 32-bit integers. The loop itself consists of loading the elements from both input arrays, by using registers a5 and a1, which store the current addresses of the elements. Afterwards, the elements are summed and stored in register a4, which is then stored in the output array location pointed by register a2. Finally, the addresses in registers a5, a1 and a2 are incremented by 4 to point to the next elements to be processed. The loop continues until the address in register a5 is equal to the address in register a7. This is ensured by the branch if not equal instruction at address 0x40.

Finally, the return part is reached at address 0x44, where the program jumps back to the callee, using the address stored in register ra. The return value is stored in register a0, which is equal to the number of elements to be processed.

2 RISC-V Tool Chain

2.1 Reimagined C Code

The above explanation of the program's functionality allows us to reimagine the C code that could have generated the assembly instructions that were previously described. An example of such C code is provided in the listing below:

```
1 int addv(int *in1 , int *in2 , int *out , int n)
2 {
3     if (in1 == NULL)
4         return -1;
5     if (in2 == NULL)
```

```

6      return -1;
7      if (out == NULL)
8          return -1;
9      if (n <= 0)
10         return n;
11
12     for (int i = 0; i < n; i++) {
13         out[i] = in1[i] + in2[i];
14     }
15
16     return n;
17 }

```

2.2 Compiling the C Code to RISC-V Assembly

By using the RISC-V GCC toolchain, one can compile the above C code into RISC-V object code and then disassemble it to obtain the assembly instructions. The following command was used in order to produce the object file from the C source code:

```
riscv64-linux-gnu-gcc -g -O0 -mmodel=medlow -mabi=ilp32 -march=rv32im -Wall -c -o
se201-prog.o se201-prog.c
```

A fair mention is that in order to have a compiled program, one needs to provide a main function as an entry point. What is shown below is the dummy main function in which the `addv` function is called:

```

1 int main() {
2     int a[] = {1, 2, 3, 4, 5};
3     int b[] = {10, 20, 30, 40, 50};
4     int n = 5;
5     int result[5];
6
7     int res = addv(a, b, result, n);
8     return 0;
9 }

```

2.3 Comparison between the generated and the previous instructions

After successfully compiling the C code, one can disassemble it to obtain the assembly instructions. The following command is used to do so:

```
riscv64-linux-gnu-objdump -d ./se201-prog.o
```

Then, because the `addv` function is the one of interest, we can navigate to the corresponding part of the output, containing the label `addv`. Below is a snippet of the generated assembly instructions for the `addv` function:

Generated Assembly Instructions:

```

00000000 <adv>:
    0:  fd010113      addi    sp,sp,-48
    4:  02812623      sw       s0,44(sp)
    8:  03010413      addi    s0,sp,48
   c:  fca42e23      sw       a0,-36(s0)
  10:  fcb42c23      sw       a1,-40(s0)
  14:  fcc42a23      sw       a2,-44(s0)
  18:  fcd42823      sw       a3,-48(s0)
 1c:  fdc42783      lw       a5,-36(s0)
 20:  00079663      bnez    a5,2c <.L2>
 24:  fff00793      li      a5,-1
 28:  0980006f      j       c0 <.L3>

0000002c <.L2>:
   2c:  fd842783      lw       a5,-40(s0)
  30:  00079663      bnez    a5,3c <.L4>
  34:  fff00793      li      a5,-1
  38:  0880006f      j       c0 <.L3>

0000003c <.L4>:
   3c:  fd442783      lw       a5,-44(s0)
  40:  00079663      bnez    a5,4c <.L5>
  44:  fff00793      li      a5,-1
  48:  0780006f      j       c0 <.L3>

0000004c <.L5>:
   4c:  fd042783      lw       a5,-48(s0)
  50:  00f04663      bgtz    a5,5c <.L6>
  54:  fd042783      lw       a5,-48(s0)
  58:  0680006f      j       c0 <.L3>

0000005c <.L6>:
   5c:  fe042623      sw       zero,-20(s0)
  60:  0500006f      j       b0 <.L7>

00000064 <.L8>:
   64:  fec42783      lw       a5,-20(s0)
   68:  00279793      slli    a5,a5,0x2
   6c:  fdc42703      lw       a4,-36(s0)
   70:  00f707b3      add     a5,a4,a5
   74:  0007a683      lw       a3,0(a5)
   78:  fec42783      lw       a5,-20(s0)
   7c:  00279793      slli    a5,a5,0x2
   80:  fd842703      lw       a4,-40(s0)
   84:  00f707b3      add     a5,a4,a5
   88:  0007a703      lw       a4,0(a5)
   8c:  fec42783      lw       a5,-20(s0)

```

```

90:    00279793          slli    a5 , a5 , 0x2
94:    fd442603          lw      a2 , -44(s0)
98:    00f607b3          add     a5 , a2 , a5
9c:    00e68733          add     a4 , a3 , a4
a0:    00e7a023          sw      a4 , 0(a5)
a4:    fec42783          lw      a5 , -20(s0)
a8:    00178793          addi    a5 , a5 , 1
ac:    fef42623          sw      a5 , -20(s0)

000000b0 <.L7>:
b0:    fec42703          lw      a4 , -20(s0)
b4:    fd042783          lw      a5 , -48(s0)
b8:    faf746e3          blt     a4 , a5 , 64 <.L8>

000000bc <.LBE2>:
bc:    fd042783          lw      a5 , -48(s0)

000000c0 <.L3>:
c0:    00078513          mv      a0 , a5
c4:    02c12403          lw      s0 , 44(sp)
c8:    03010113          addi    sp , sp , 48
cc:    00008067          ret

```

By comparing the generated assembly with the one provided in the first section, one can observe that several differences exist. Firstly, in this generated assembly, only the stack is used for passing arguments from the caller to the callee, while in the provided assembly, the registers were used to pass the arguments.

Secondly, the check for null pointers, which can be observed in the section .L2, .L4 and .L5 is done using the bnez instruction and instead of jumping to a common return -1, each check contains its own jump to the return -1 section. This leads to a larger code size and is also less efficient due to the fact that the positive case needs an extra jump, which normally, flushes the pipeline.

Thirdly, the loop structure is different, as it can be seen in .L8 and .L7 sections.

2.4 Changing the Optimization Level

By switching the optimization level from -O0 to -O1, the generated assembly code changes significantly. It is observed that the code size is reduced, and the loop starts to resemble more the code provided in the first section. Below is a snippet of the generated assembly instructions:

```

00000000 <adv>:
0:    00050813          mv      a6 , a0
4:    00068513          mv      a0 , a3

00000008 <.LVL1>:
8:    04080063          beqz    a6 , 48 <.L4>
c:    04058263          beqz    a1 , 50 <.L5>
10:   04060463          beqz    a2 , 58 <.L6>
14:   04d05463          blez    a3 , 5c <.L2>
18:   00080793          mv      a5 , a6

```

```

1c:    00269713      slli    a4,a3,0x2
20:    00e80833      add     a6,a6,a4

00000024 <.L3>:
24:    0007a703      lw      a4,0(a5)
28:    0005a883      lw      a7,0(a1)
2c:    01170733      add     a4,a4,a7
30:    00e62023      sw      a4,0(a2)
34:    00478793      addi    a5,a5,4
38:    00458593      addi    a1,a1,4
3c:    00460613      addi    a2,a2,4
40:    ff0792e3      bne     a5,a6,24 <.L3>
44:    00008067      ret

00000048 <.L4>:
48:    fff00513      li      a0,-1
4c:    00008067      ret

00000050 <.L5>:
50:    fff00513      li      a0,-1

00000054 <.LVL5>:
54:    00008067      ret

00000058 <.L6>:
58:    fff00513      li      a0,-1

0000005c <.L2>:
5c:    00008067      ret

```

Changes in code size occur as well when switching to higher optimization levels, such as -O3.

```

00000000 <adv>:
0:    00050793      mv      a5,a0
4:    04050063      beqz    a0,44 <.L8>
8:    02058e63      beqz    a1,44 <.L8>
c:    02060c63      beqz    a2,44 <.L8>
10:   00269893      slli    a7,a3,0x2
14:   011508b3      add     a7,a0,a7
18:   02d05263      blez    a3,3c <.L5>

0000001c <.L4>:
1c:    0007a703      lw      a4,0(a5)
20:    0005a803      lw      a6,0(a1)
24:    00478793      addi    a5,a5,4
28:    00458593      addi    a1,a1,4
2c:    01070733      add     a4,a4,a6
30:    00e62023      sw      a4,0(a2)
34:    00460613      addi    a2,a2,4

```



```

    38:    ff1792e3                bne    a5,a7,1c <.L4>
0000003c <.L5>:
    3c:    00068513                mv     a0,a3
00000040 <.LVL2>:
    40:    00008067                ret
00000044 <.L8>:
    44:    fff00513                li     a0,-1
00000048 <.LVL4>:
    48:    00008067                ret

```

3 RISC-V Architecture

References

- [1] *PR1-SE201-21*, 2021. Unpublished internal document.
- [2] James. What is a branch delay slot and why is it used?, 2020. Accessed: June 10, 2024.