

USING THE Si3402-B PoE PD CONTROLLER IN ISOLATED AND NON-ISOLATED DESIGNS

1. Introduction

Power over Ethernet (PoE) is an IEEE standard (IEEE 802.3-2012) for delivering power through Ethernet cables. The first PoE standard (IEEE802.3af) was ratified in 2003. This standard defined power classes 0-3 with maximum cable current of 350 mA and 15 W power delivery capability. This was extended to 30 W (class 4) by the IEEE802.3at standard in 2009. According to the revised standard, the maximum cable current is 600 mA. The PoE devices were divided in to two types:

- Type 1 devices which are compatible with the 802.3af standard.
- Type 2 devices which are compatible with the newly-defined Class 4 power class. These devices are also called PoE+.

The 802.3at standard is backward compatible with the 802.3af version, and the latest published IEEE802.3-2012 standard contains the 802.3at specification.

Two configurations of connection of PSEs to PDs are shown in Figures 1 and 2. The option shown in Figure 1 must be used for “midspan equipment”, which injects power on the Ethernet connection of an existing Ethernet link. Endpoint equipment, such as an Ethernet switch, can use either option.

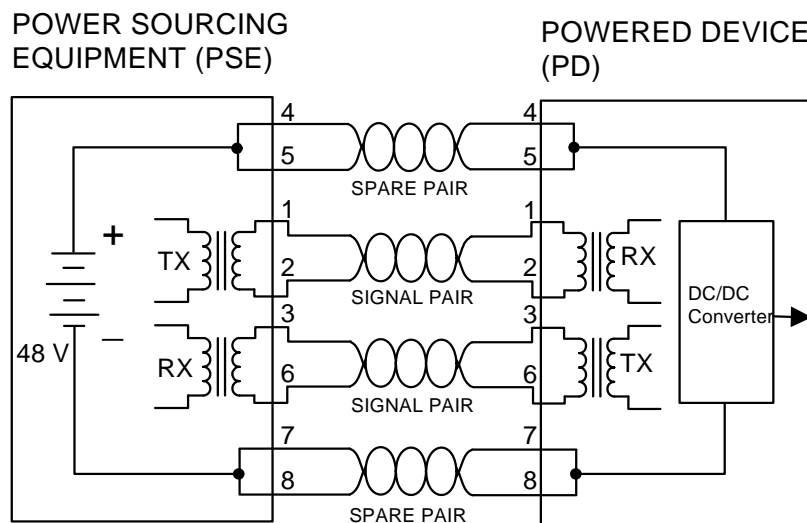


Figure 1. Power Delivered over Spare Pair (Midspan)

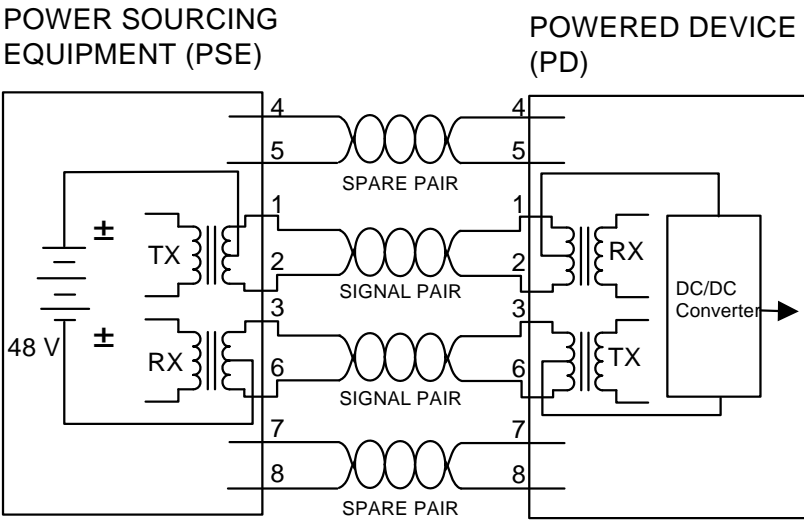


Figure 2. Power Delivered over Signal Pair

The IEEE802.3-2012 Type 1 compatible Power Sourcing Equipment (PSE) supplies 44 to 57 VDC and must be isolated from earth ground. The powered device (PD) must not consume more than 12.95 W (PD input power for class 3), which translates to no more than 350 mA (Type 1) of steady state input current, allowing for 20 Ω of cabling resistance between the PSE and PD. This means that with practical conversion efficiencies, approximately 10 W of regulated power is available to PD applications, making PoE a preferred alternative for powering devices, such as VoIP phones, wireless routers, and security devices, because it eliminates the need for a local power source, greatly simplifies installation, and allows easy power backup through an uninterruptible power source (UPS) on the PSE end. The advantages of IEEE 802.3-2012-compliant equipment include:

- This standard provides a standard way for the PSE to recognize that the PD side is PoE-enabled and not supply power unless a valid signature is detected, thus eliminating the possibility of damaging equipment that is not PoE-enabled.
- This standard provides a method of allowing the 802.3af PD device to supply classification information to the PSE so that the PSE can determine the load requirements of the multiple pieces of PD equipment it is powering.
- This standard ensures interoperability of PSE and PD devices from different manufacturers.

The Si3402-B device is a highly-integrated, efficient IC with both a Power over Ethernet PD interface and PWM dc-dc converter. It is fully-compatible with IEEE 802.3-2012 Type 1 specification, and has a two-step inrush current-limiting feature to allow PD designs that are compatible with pre-standard PSE equipment. It supports PD designs that require isolation between the Ethernet cables and powered equipment as well as the lower-cost option without isolation for fully-enclosed devices.

This application note covers the basic operation of the Si3402-B as well as design equations and selection criteria for signature resistors and capacitors, dc-dc converter power train, input filter, output filter, feedback and compensation, soft-start, duty cycle limits, and switcher current limit. The Si3402-B also feature integrated surge protection.

2. Typical Application Schematics

Figures 3 and 4 show the basic application circuits for the Si3402-B evaluation board.

Notes:

1. The external diode bridge (D8–D15), built from Schottky type diodes, is recommended for high power levels (Class 3 operation). For lower power levels, such as Class 1 and Class 2, the diodes can be removed.
2. When the Si3402-B is used in external diode bridge configuration, it requires that at least one pair of the CTx and SPx pins be connected to the PoE voltage input terminals (to the input of the external bridge).

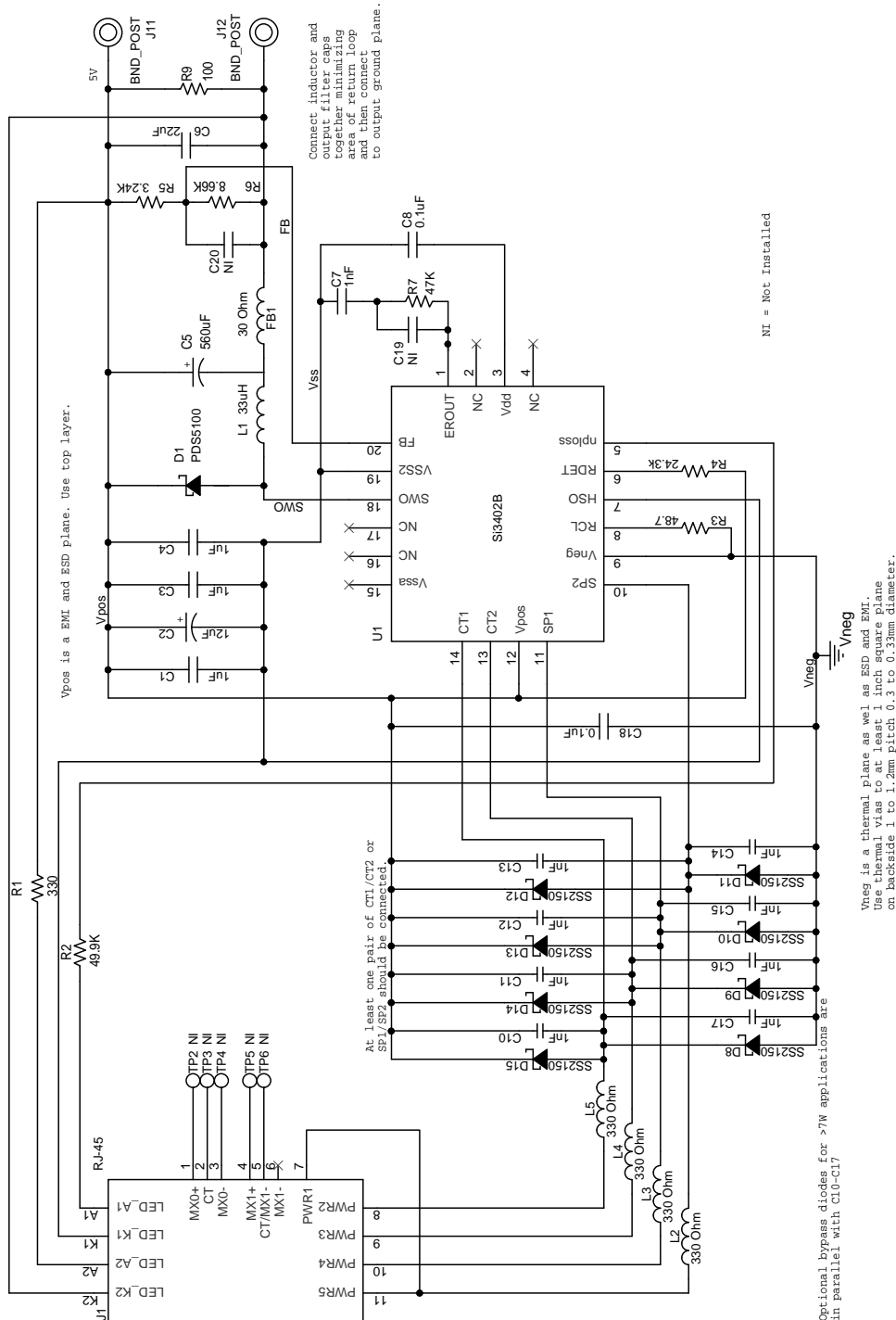
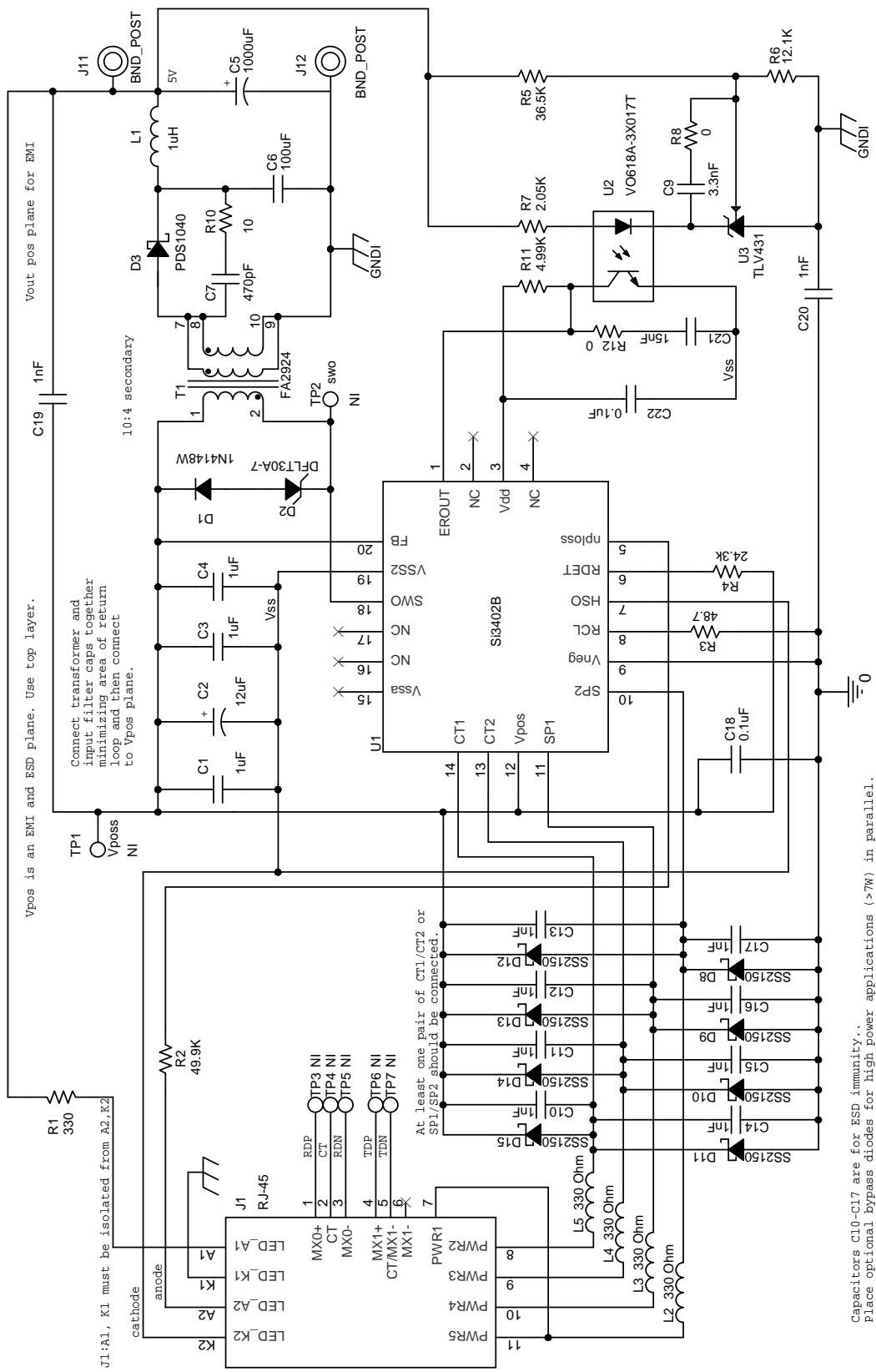


Figure 3. Non-Isolated Buck Configuration for Si3402-B-EVB (5 V Output)



400 W Cesar Chavez St., Austin, TX
78701, United States

Figure 4. Isolated Flyback Configuration for Si3402-B-ISO-EVB (5 V Output)

3. Basic Detection, Classification, and Power Sequencing

The circuit configurations in Figures 3 and 4 have the same operation during detection, classification, and power sequencing. A full power cycle is shown in Figure 5.

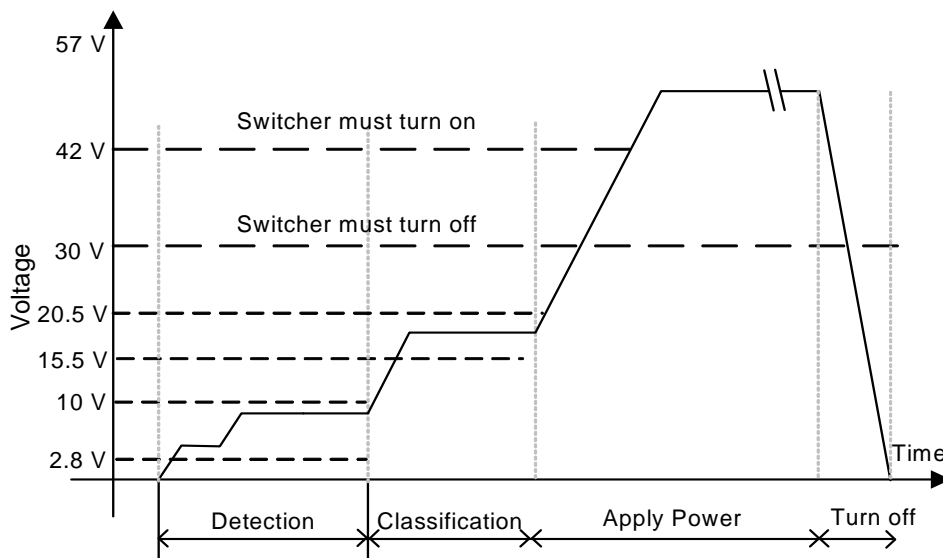


Figure 5. Full Power Cycle

As will be described in more detail below, a low voltage is used to detect a valid PD; a higher voltage is used to classify the power level of the PD, and full power operation starts at a voltage of 42 to 57 V.

3.1. Detection

During the detection phase, the PSE applies two voltages between 2.8 and 10 V dc and measures the current (with a current limit of 5 mA). The slope of the I-V characteristic of the PD must be between 23.75 and 26.25 k Ω . This slope is set by the resistor, RDET (R4 in Figures 3 and 4). 24.3 k Ω 1% resistor ensures valid detection in all conditions. Additionally, the input capacitance must be between 50 and 120 nF, which is set by the capacitor, CDET (C18 in Figures 3 and 4).

The low voltage and current applied in the detect phase as well as the requirement for specific values of resistance and capacitance makes it unlikely that non-PoE enabled equipment will be recognized if plugged into PSE equipment that supports PoE.

3.2. Classification

During the classification phase, the PSE applies a voltage between 15.5 and 20.5 V, current-limited to 100 mA, and determines the maximum output power requirement: PD requested Class, based on the current consumed by the PD.

Class	Power Level that the PSE Must Support
0	15.4 W
1	4.0 W
2	7 W
3	15.4 W

Over the range of 14.5 to 20.5 V, the PD current during the classification stage must be as shown in Table 1.

Table 1. Classification Stage PD Current

Class	Minimum Current	Maximum Current	Units
0	0	4	mA
1	9	12	mA
2	17	20	mA
3	26	30	mA

The classification current for the Si3402-B is set by the resistor, R_{class} ($R3$ in Figures 3 and 4).

3.3. PoE Power Clarification

Per the IEEE standard for type 1 configuration, the maximum allowed cable resistance is $R_{max} = 20\ \Omega$ between the PSE and PD. Additionally, the standard defines the following magnitudes: PSE maximum output current (I_{out_max} PSE), PSE minimum output voltage ($V_{PSE_out_min}$), and PSE output power (P_{PSE_out}).

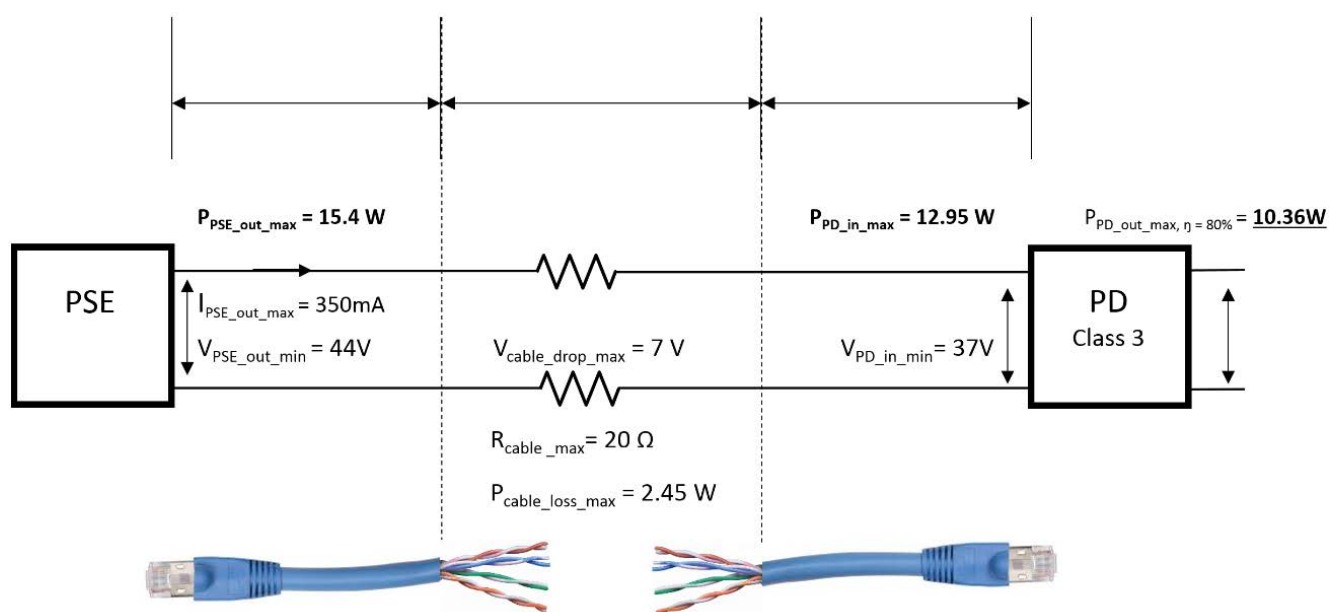


Figure 6. Power Clarification in Class 3 Example

Figure 6 represents an example for type 1, class 3 option. Due to the resistance of the Ethernet cable, by increasing the PSE output current, a significant power loss can occur in the cable. In worst case ($20\ \Omega$ cable resistance + maximum PSE output current $I=350\text{ mA}$ for class 3), it means almost 2.5 W of cable losses. By reducing the cable length this loss can be decreased, but it is strongly recommended to include [the reduction](#) into the calculations. Table 1 includes a brief summary of power magnitudes required and allowed by the IEEE standard.

Table 2. Power Magnitudes by PoE Classes with Maximum Allowed Cable Resistance

Class	PSE Pout Max [W]	Rcable Max [Ω]	PSE Vout Min [V]	PSE Iout Max [mA]	Max Cable Loss [W]	PD Pinmax [W]	PD Pout max η = 80% [W]	Type
0	15.40	20	44	350.00	2.45	12.95	10.36	1
1	3.84	20	44	87.27	0.15	3.69	2.95	1
2	6.49	20	44	147.50	0.44	6.05	4.84	1
3	15.40	20	44	350.00	2.45	12.95	10.36	1
4	30.00	12.5	50	600.00	4.50	25.50	20.40	2

3.4. Powerup

During detection and classification, the PD must isolate the switcher input filter and not apply power to the load. After completion of this phase, the PSE ramps up to between 44 and 57 V, and PD turns on by closing the internal hot swap switch.

The PD must turn on at an input voltage of 42 V. After turning on, this voltage can drop to 37 V due to cabling resistance.

The Si3402-B hot swap switch has a two-step current limit. The input filter capacitor is first charged to within about 1.3 V of its final value at a typical current of 150 mA. When the filter input capacitor is nearly charged, the current limit is increased to over 400 mA, and the switcher is allowed to turn on. The hot swap switch operates at the higher current limit as long as the input filter is charged to about 30 V to allow for any switcher startup transients.

The Si3402-B is designed so that the hot swap switch current limit is generally not the limitation in terms of the amount of power the PD can draw. This limit is intended to be set by the switching regulator and load or by the power sourcing equipment.

However, to limit inrush current as the switcher turns on, the switcher design supports integrated dynamic soft-start operation, which is further described in the detailed switcher descriptions of this application note.

Figure 7 shows the input current and output voltage vs. time when 48 VDC is suddenly applied to the PD circuit. The initial current spike is due to the charging of the 0.1 μ F input capacitor. For this particular device, the filter capacitor charges up with a current limit of 141 mA in 5 msec. At this point, the current limit increases, and the capacitor is allowed to fully charge the last 1.3 V.

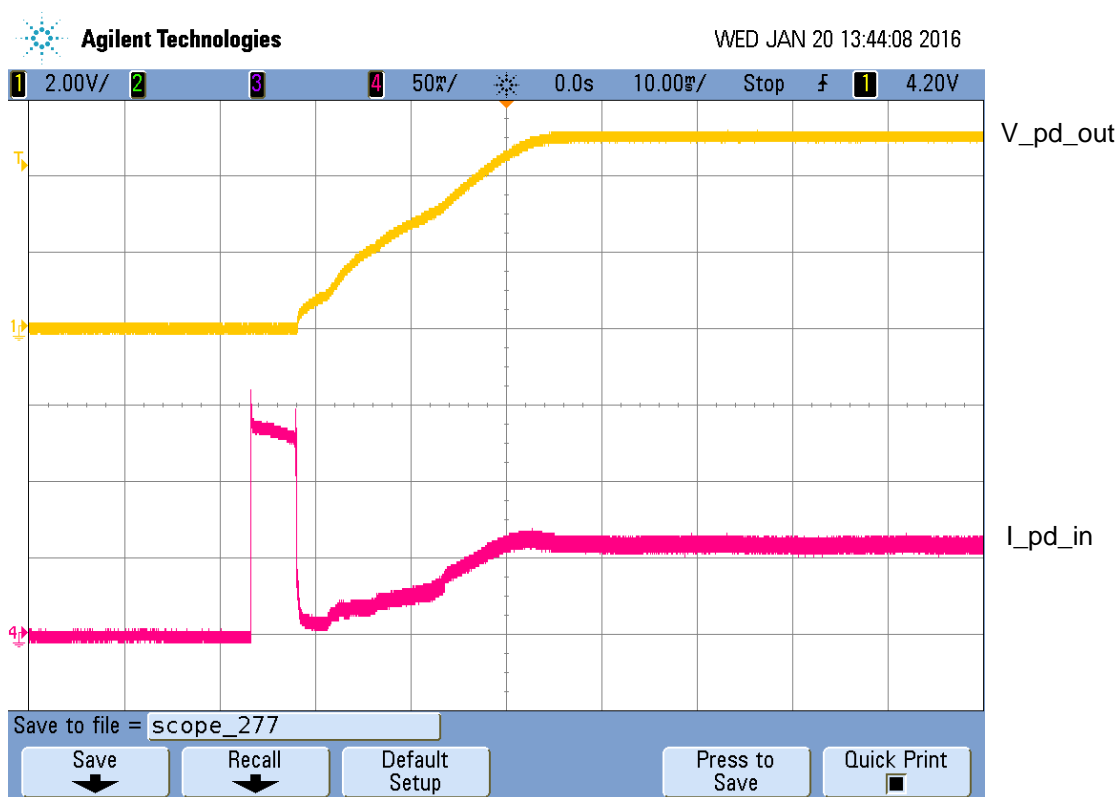


Figure 7. Typical Startup Waveform with 2.5 Ω Load

3.5. Maintain Power Signature (MPS)

The PSE detects the dc current to the PD by either looking for the low ac impedance of the input filter or making sure that it is drawing current.

For this reason, the input filter capacitor must be $>5 \mu\text{F}$, and the load must be such that the input current is $>10 \text{ mA}$. Since the Si3402-B is designed to be very efficient and dissipate very little power, there is a minimal load current requirement of 250 mW (50 mA at 5 V output) so as to draw $>10 \text{ mA}$ from the input supply. It has also been observed that if the switcher is operated with no load, the switcher tends to pulse on and off, which may be undesirable. For this reason, it is recommended that a 250 mW load always be present.

3.6. Turn Off

The minimum input voltage level at which the PD is required to turn off is 30 V.

The Si3402-B has approximately 4 V of hysteresis between turn-on and turn-off with respect to the voltage across the switcher input filter capacitor so that inrush current at startup will not cause the part to turn off.

Additionally, the Si3402-B has an early power loss feature where the voltage on the cable side of the diode bridge is sensed. If V_{pos} becomes 1.5 V higher than V_{ct} or V_{sp} , the power loss signal ($\overline{\text{PLOSS}}$) is asserted. This allows for early detection of power removal while the switcher input capacitor is still charged.

3.7. Signature Resistors and Capacitors and Component Selection Criteria

The Si3402-B is designed to meet IEEE 802.3 signature requirements with RDET (connected to pin RDET) = 24.3 k Ω , $\pm 1\%$.

Recommended resistor values for RCLASS (connected to pin RCL) are listed in Table 3.

Table 3. RCLASS Recommended Resistor Values

Class	Requested PSE Power Level	RCLASS $\pm 1\%$
0	15.4 W	Open circuit
1	4.0 W	140 Ω
2	7 W	75 Ω
3	15.4 W	48.7 Ω

The voltage across these resistors is limited so that 0603 or larger surface mount resistors may be used.

C18 should be a 100 V X7R type surface mount with tolerance of $\pm 10\%$. While this type of capacitor exhibits a strong voltage and temperature dependence, the 50–120 nF requirement of IEEE 802.3 will be met.

3.8. Input Filter

IEEE 802.3 requires that the input filter capacitor be greater than 5 μF . Additionally, the ripple at the RJ-45 input at the switching frequency of approximately 350 kHz must be less than 150 mV. To reduce the chance of conducted or radiated emissions due to induced common-mode voltage on the Ethernet cable pairs, it may be desirable to further reduce the input ripple.

To maintain the $>5 \mu\text{F}$ input capacitance, an aluminum electrolytic capacitor, such as a Sanyo 100ME12AX or Panasonic EEUFC120, is used. This capacitor has an ESR of up to 0.4 Ω and results in excessive input ripple because of the ripple current from the switcher, which can be as much as 3 A. To keep input ripple down, it is recommended that additional X7R surface mount capacitors be used in parallel (for example, a 1 μF , 100 V, X7R 1210 capacitor with an ESR of less than 0.6 Ω is available from several vendors).

The input filter capacitor also helps absorb surge current. If the input capacitor is too large, the reaction time of the hot swap switch current limit function increases. An input filter capacitor of 15 μF total has been found to be a good compromise.

4. DC-DC Converter Operation

There are two basic configurations for the dc-dc converter: buck and flyback. Additionally, the converter may be designed so that its power output is electrically isolated from the power input. Isolation is required per IEEE 802.3 when the PD does not provide the isolation.

In the non-isolated case, the buck topology is generally used, and, in the isolated case, the flyback topology is generally used. It is possible to use the flyback topology in the non-isolated case, although this is not described in detail in this application note.

The equations used for determining all of the components surrounding the switching converter are briefly described below.

4.1. Non-Isolated Buck Design

Under most conditions, the current through the inductor ($L1$ in Figure 3) is continuous, and the voltage across the inductor switches from positive to negative as shown in Figure 8.

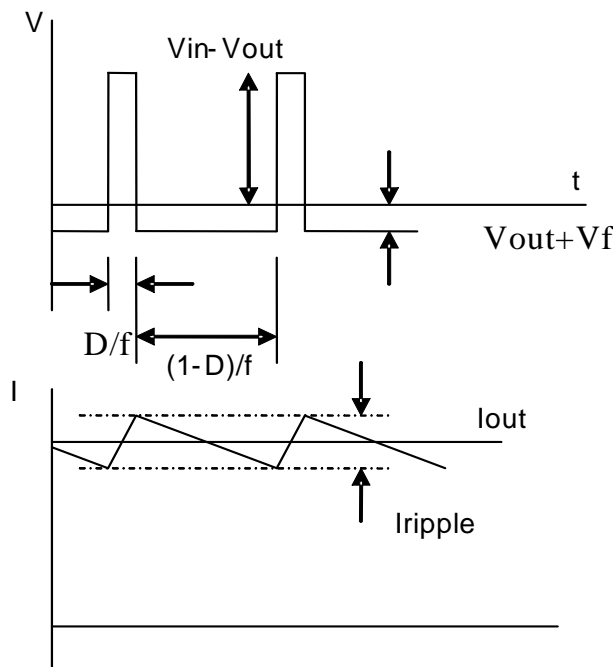


Figure 8. Voltage Polarity

The average voltage across the inductor must be zero; so, the duty cycle is:

$$D \times (V_{in} - V_{out}) = (1 - D) \times (V_{out} + V_f)$$

Where V_{out} is the desired output voltage; V_f is the forward drop of the diode ($D1$ in Figure 3), and V_{in} varies with the PD input voltage, which is generally 42–55 V. Solving:

$$D = \frac{(V_{out} + V_f)}{(V_{in} + V_f)}$$

The ripple current that has to be supported in the output filter is:

$$I_{ripple} = \frac{(V_{in} - V_{out}) \times (V_{out} + V_f)}{((V_{in} + V_f) \times L \times F)}$$

Where L is the inductance.

$L = 33 \mu\text{H}$, $V_{\text{out}} = 5 \text{ V}$, $V_{\text{in}} = 53 \text{ V}$, $V_f = 0.7 \text{ V}$

F is the internally-set switch frequency of approximately 350 kHz.

$I_{\text{ripple}} = 441 \text{ mA}$

This is the ripple current into the output filter. The peak-to-peak ripple current that must be handled by the input filter is equal to the average current delivered to the output plus half of the ripple current in the inductor.

The rectifier diode in the non-isolated design must be rated for at least the input voltage. Generally, a 100 V diode is chosen for margin. A Schottky diode is preferred to avoid the large voltage drop and excess power associated with stored charge. Typical part numbers are PDS5100 from Diodes Incorporated or the equivalent UPS5100 from Microsemi. Note that these 100 V diodes have a larger forward drop than the lower voltage diodes used for the non-isolated design below.

Overall efficiency is determined by dividing the output power by the input power including conduction losses in the inductor, rectifier, switching FET, input bridge, and hot swap switch, as well as bias and switching losses.

4.1.1. Output Voltage—Non-Isolated Design

The output voltage in the isolated case is determined by R5 and R6 according to the following equation:

$$V_{\text{out}} = 1.35 \times \left(1 + \frac{R6}{R5}\right)$$

For example, for a 5 V output, values of 8.66 k Ω for R6 and 3.24 k Ω for R5 are recommended.

The supported minimum output voltage in non-isolated buck topology is 3.3 V.

4.1.2. Output Filter and Loop Stability—Non-Isolated Design

Generally, the current in the output inductor is continuous (does not return to zero). The current becomes discontinuous for very light loads, but the continuous mode of operation is most difficult to stabilize due to the LC filter resonance that occurs in this case.

The output filter section has a resonant frequency described by the following equation:

$$\frac{1}{2 \times \pi \times \sqrt{LC}}$$

The circuit will be critically damped with a resistance of:

$$2 \times \sqrt{\frac{L}{C}}$$

For a typical 33 μH inductor and 560 μF filter cap, the resonant frequency is 1170 Hz, and the resistance for critical damping is 0.48 Ω .

The damping resistance is a combination of capacitor ESR, inductor series resistance, and switch and diode resistance. It has been found that the combination of switcher FET resistance and Schottky diode effective series resistance results in an effective 0.5–1 Ω in series with the inductance for the recommended applications circuit. This damps the output resonance and allows for the use of low ESR filter capacitors without stability concerns.

The network of Rc and Cc stabilizes the feedback loop by introducing a zero in the feedback loop. It has been found that values of 1 nF (C7 in Figure 3) and 47 k Ω (R7 in Figure 3) work well. This translates to a zero at 3.3 kHz.

For designs that must operate below 0 $^{\circ}\text{C}$, it has been found that a low ESR 560 μF capacitor such as the Panasonic EEU-FM0J561 gives better results with the same stability network.

4.1.3. Soft Start Non-Isolated Case

Si3402-B has an internal dynamic soft-start circuitry, which further reduces BOM costs. The dynamic soft-start function adapts the rise time to the load attached to the output at start-up. At light load conditions, the rise time is very short, typically 5-10 ms. With heavy load conditions at start-up, the rise-up time is much longer to ensure safe power-up and no overshoot voltage on the output.

A typical startup waveform on the buck-based EVB board with a $2.5\ \Omega$ load is shown in the figure below.

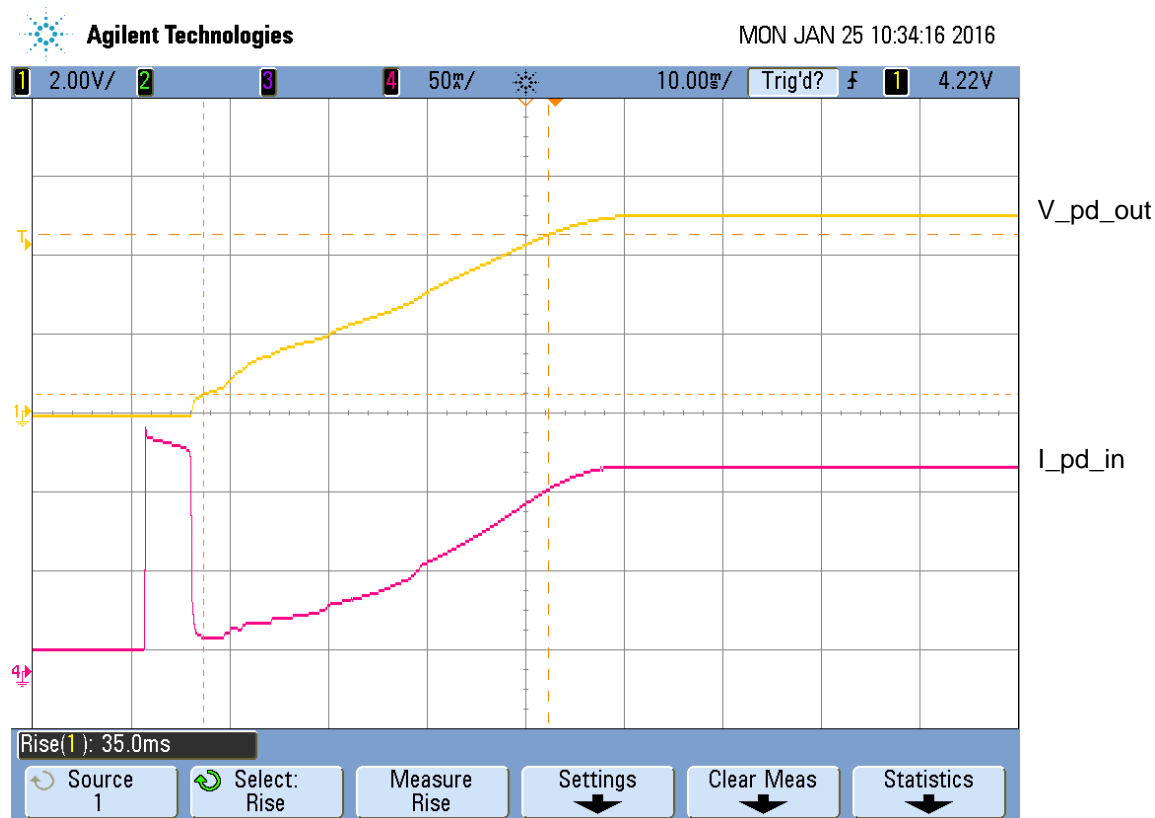


Figure 9. Typical Startup Waveform on the Buck-based EVB Board with a 10 W Load, Rise Time: 35 ms

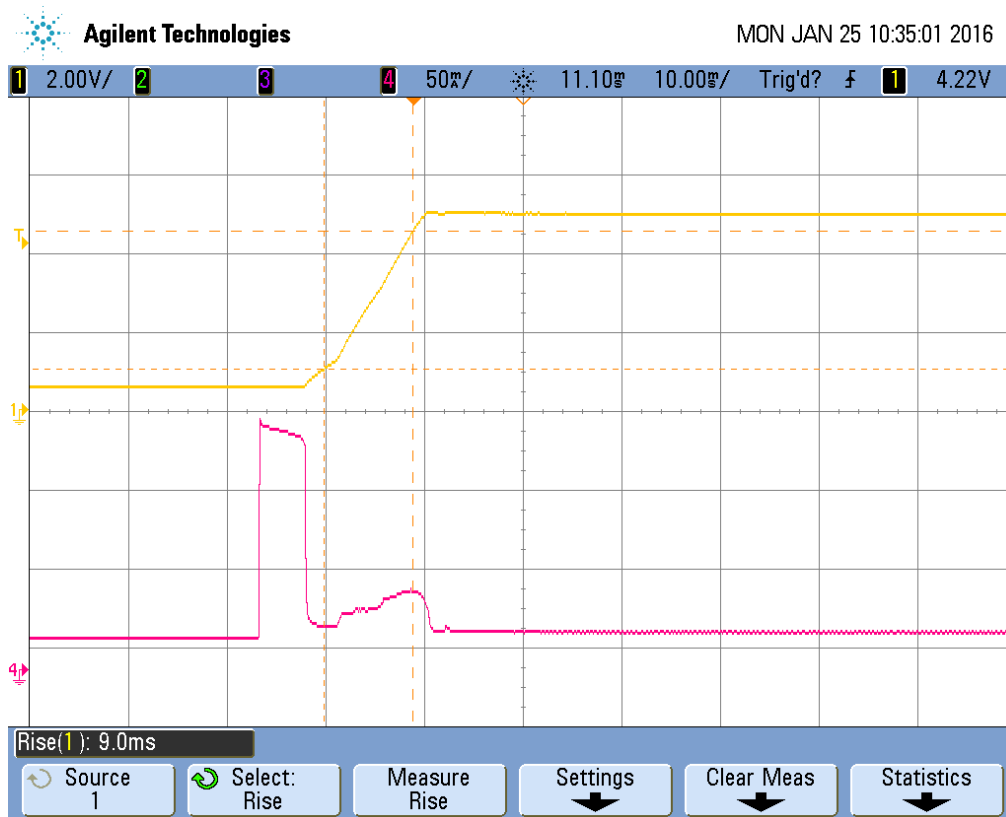


Figure 10. Typical Startup Waveform on the Buck-based EVB Board without Load-Rise Time = 9 ms

4.2. Isolated Flyback Design

For the isolated design, a flyback transformer approach is used. In a flyback transformer, the primary inductance is "charged" when the main switcher FET turns on, and the energy stored in this inductance is delivered to the secondary when the switcher FET turns off. This type of circuit may be designed to operate in either the continuous or discontinuous mode. In the continuous mode, current always flows in either the transformer primary or secondary. In the discontinuous mode, the secondary current drops to zero before the next cycle of primary current. Typical waveforms are shown in Figure 11.

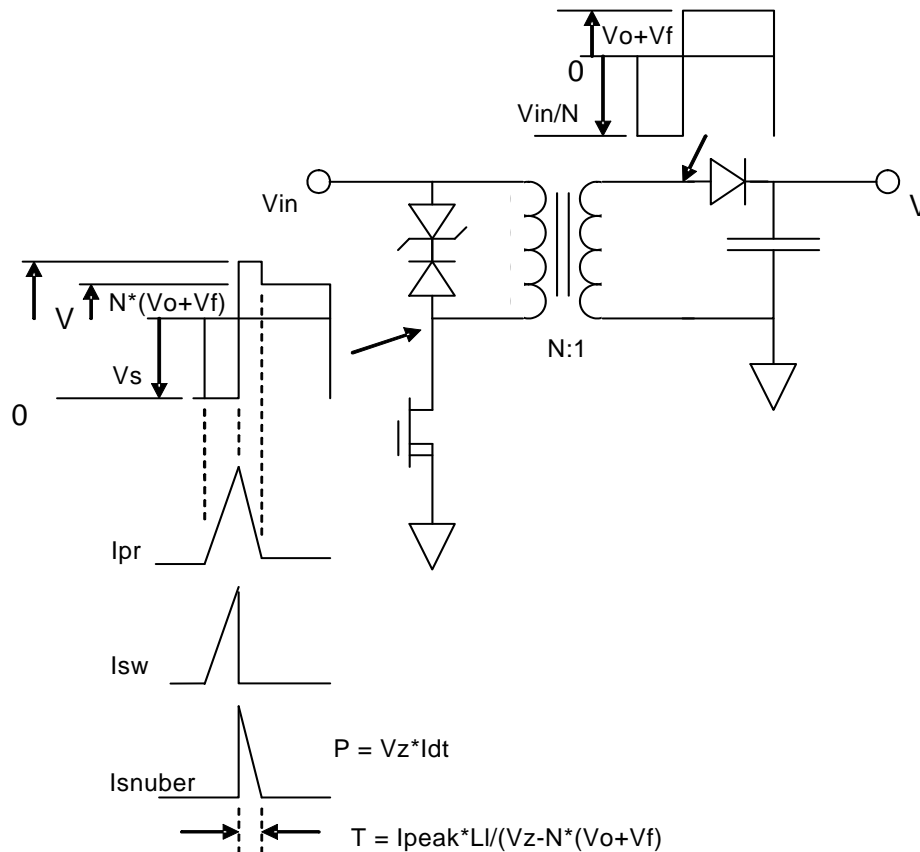


Figure 11. Typical Waveforms

A transformer with a turns ratio of N:1 is used to help reduce peak currents.

In the discontinuous mode, the output power, $I_0 \times V_0$, must be supplied by the $\frac{1}{2} \times LI^2$ energy stored in the transformer with some margin for switching losses. If ε is the margin for switching losses (typically 90%), then:

$$P_0 = I_0 \times V_0 = \frac{1}{2} \times I_p^2 \times L_m \times f \times \varepsilon$$

Where P_0 , I_0 , and V_0 are output power, current and voltage, and I_p , L_m , and f are transformer primary peak current, magnetizing inductance, and operating frequency.

The portion of the switching waveform where the FET is on d_1 is:

$$d_1 = I_p \times L_m \times \frac{f}{V_p}$$

Where V_p is the input voltage.

The time, d_2 , where current flows in the secondary is:

$$d_2 = V_p \times \frac{d_1}{(N \times (V_0 + V_f))}$$

Where V_0 is the output voltage (plus diode drop), and N is the transformer turns ratio.

Solving with the constraint that $d_1 + d_2 = 1$ gives the following:

$$I_0 = \left[\varepsilon \times \frac{V_0 + V_f}{(2 \times f \times L_m)} \right] \times \left[\frac{N}{\left(1 + N \times \frac{(V_0 + V_f)}{V_p} \right)} \right]^2$$

For a given power transformer magnetizing inductance, turns ratio, output voltage, frequency, and input voltage, this gives the output current at which the current becomes continuous and always flows in either the transformer primary or secondary.

$L_m = 40 \mu\text{H}$ gives a good compromise between transformer size (larger L_m gives a larger transformer) and peak current (larger L_m gives smaller peak current at the input and output).

Plugging in $V_0 + V_f = 5.7 \text{ V}$, $V_p = 48 \text{ V}$, $N = 3$, $L_m = 40 \mu\text{H}$, $\varepsilon = 0.9$, and $f = 350 \text{ kHz}$ gives:

$$I_0 = 0.85 \text{ A}$$

Above this current, the transformer current becomes continuous in that there is always current flow in either the transformer primary or secondary.

For larger output current, the duty cycle stays fairly constant at

$$D = N \times \frac{(V_o + V_f)}{(V_p + N(V_o + V_f))}$$

In the continuous mode, the average current while the switcher FET is on is determined by setting the average input power after an efficiency, ε , to equal the average output power:

$$I_{\text{avg}} \times V_p \times \varepsilon \times D = I_O \times (V_o + V_f)$$

In this mode of operation, there is a change in primary current while the FET is on

$$\Delta I = \frac{V_p \times D}{(L_m \times f)}$$

The peak current that the transformer must handle is

$$I_{\text{peak}} = I_{\text{avg}} + \frac{\Delta I}{2}$$

For the same transformer above with $I_O = 3 \text{ A}$, the peak transformer current is 1.85 A.

Increasing the turns ratio decreases peak current, particularly on the primary side. However, the secondary voltage is reflected back to the primary, and the increased turns ratio also increases the voltage on the switcher FET. Additionally, transformer leakage inductance causes an additional spike of voltage on the switcher FET, which must be clamped by a snubber.

The FET maximum drain voltage is 120 V, and the maximum voltage at V_{pos} is about 57 V; so, the snubber must clamp to 63 V.

A Zener diode and fast recovery diode are recommended to clamp the output at less than 40 V above V_{POS} to have around 20 V margin.

Increasing the turns ratio will increase snubber power. Therefore, there is an optimal turns ratio that compromises between high peak current at a low turns ratio and high snubber power at a high turns ratio.

Silicon Laboratories, Inc. has partnered with Coilcraft to develop flyback transformers that are optimized for Si3402-B at 3.3, 5, and 12 V output. The recommended part numbers are:

- FA2924-AL for 3.3 V and 5 V output voltages (40 μ H and 1:0.3 turns ratio)
- FA2805-CL for 12 V output voltages (40 μ H and 1:0.4 turns ratio).

Note: For Si3402-B, follow the recommendation from this document, not from the Coilcraft data sheet. FA2805-CL can be used for 5 V output as it was recommended for the obsolete Si3402-A. For new designs with Si3402-B, Silicon Laboratories, Inc. recommends FA2924-AL for 5 V output for better efficiency and FA2805-CL for 12 V output voltages. Contact Silicon Labs for other output supply configurations and recommendations.

The rectifier for 3.3 or 5 V output does not need as high a voltage rating because the transformer turns ratio limits the reverse voltage to $((1/N) \times V_{in}) + V_{out}$. The PDS1040 from diodes incorporated or the equivalent UPS1040 from Microsemi can be used, and these parts have much lower forward drop and overall loss due to their lower voltage rating of 40 V. For 9 V and 12 V output voltages, the PS5100 is recommended.

4.2.1. Output Voltage—Isolated Design

In the isolated design, a TLV431 (U3 in Figure 4) is used as an isolated reference voltage. The TLV431 is available from many suppliers and regulates at a reference voltage of 1.24 V; so, the output voltage is:

$$V_{out} = 1.24 \times (1 + R5/R6)$$

An opto-isolator, such as VO618A (U2 in Figure 4), which is also available from many suppliers, is used to couple the error signal back to the Si3402-B.

4.2.2. Output Filter and Loop Stability—Isolated Design

In the flyback design, even if the transformer current always flows in the transformer primary or secondary (i.e. is continuous), the secondary current does not flow during the time that primary current flows; thus, there is always a large ripple current in the output that must be filtered. For the isolated design, it is recommended that a pi-section filter be used with a 1.0 μ H inductor, such as Coilcraft D01608-102ML.

The feedback compensation for the isolated case was chosen to be type 2 for improved load transient response.

A typical Bode plot is shown in Figure 12 5 V output at the worst case (minimum V_{in} and max I_{load}) conditions. Typical Bode plots are shown in Figure 12 for the continuous case operation.

By setting $C21 = 15$ nF, $R12 = 0$ Ω , and $C9 = 3.3$ nF, $R8 = 0$ Ω a high dc gain has been achieved with unity gain frequency at around 3.3 kHz. 60° of phase margin and ~17 dB of gain margin results stable output voltage with good transient response. Figures 12 and 14 show the transient response of the converter, where the output starts with light load (discontinuous case) and ends with a heavy load (continuous case). Further optimization of this result is possible with larger or lower ESR output filter capacitors.

4.2.3. Soft Start Isolated Case

Si3402-B employs a dynamic soft-start described under section “4.1.3. Soft Start Non-Isolated Case”.

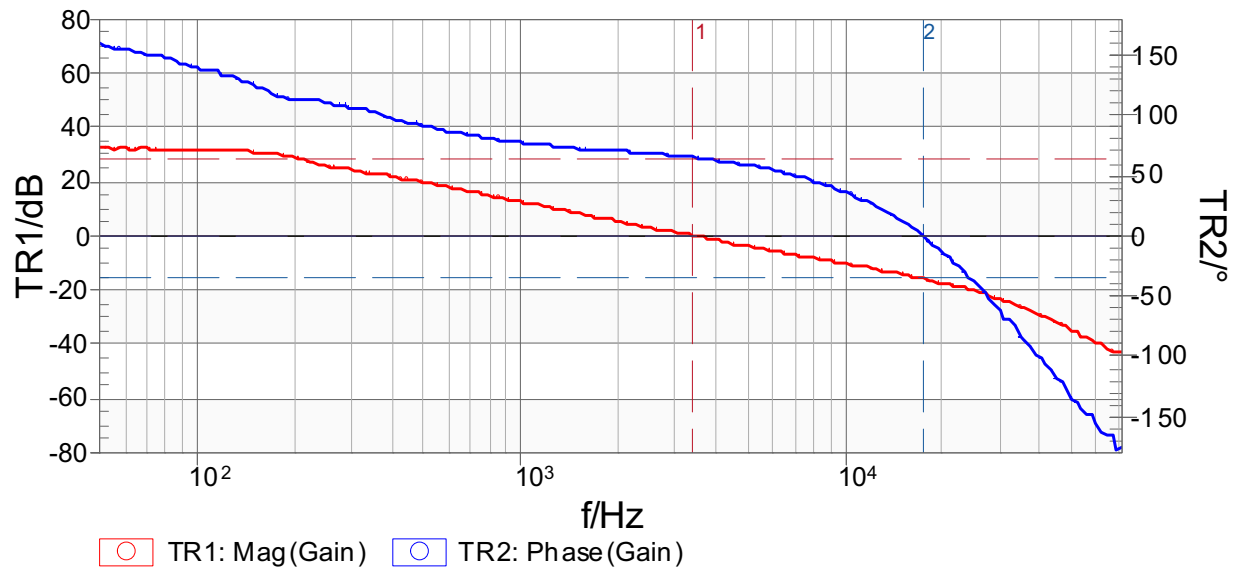


Figure 12. Bode Plots for Minimum Input Voltage, and Maximum Output Current; (Blue – Phase, Red – Gain)

Notice that measurement by breaking the loop with the injection signal will give the phase margin directly, without having to measure it from -180 °. That is because the measurement test setup includes an extra inversion that was not part of Bode's original theory for loop gains.

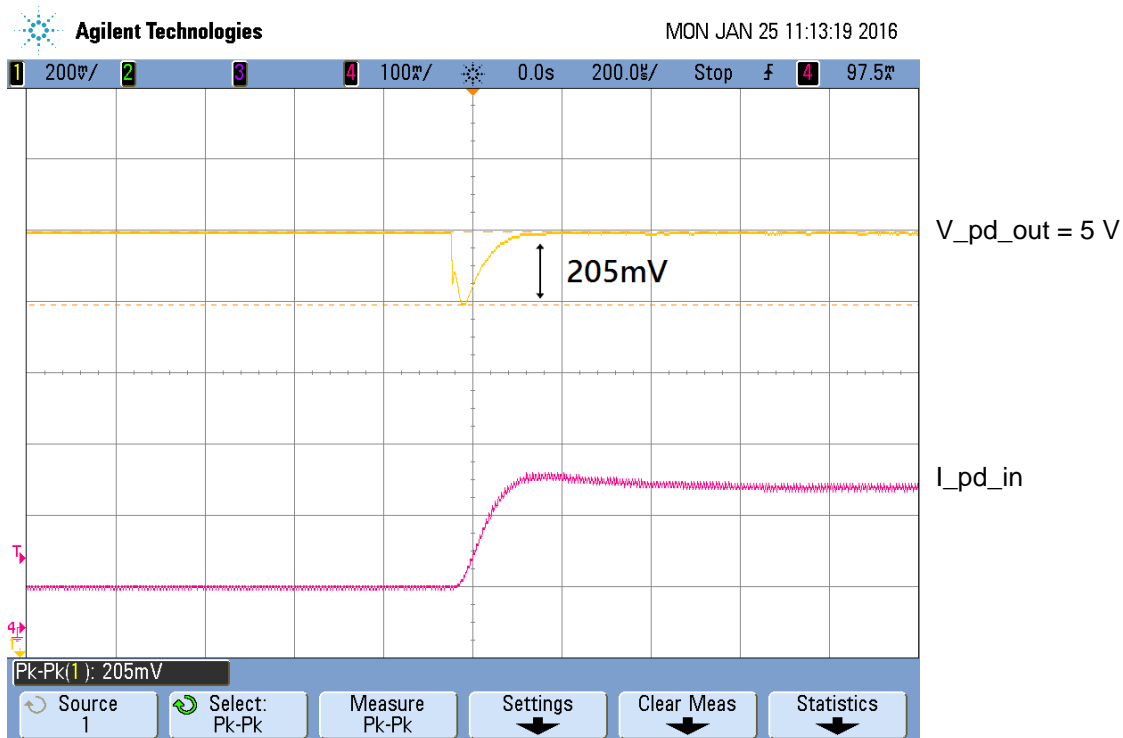


Figure 13. Step Load Transient from 2.5 W to 10 W

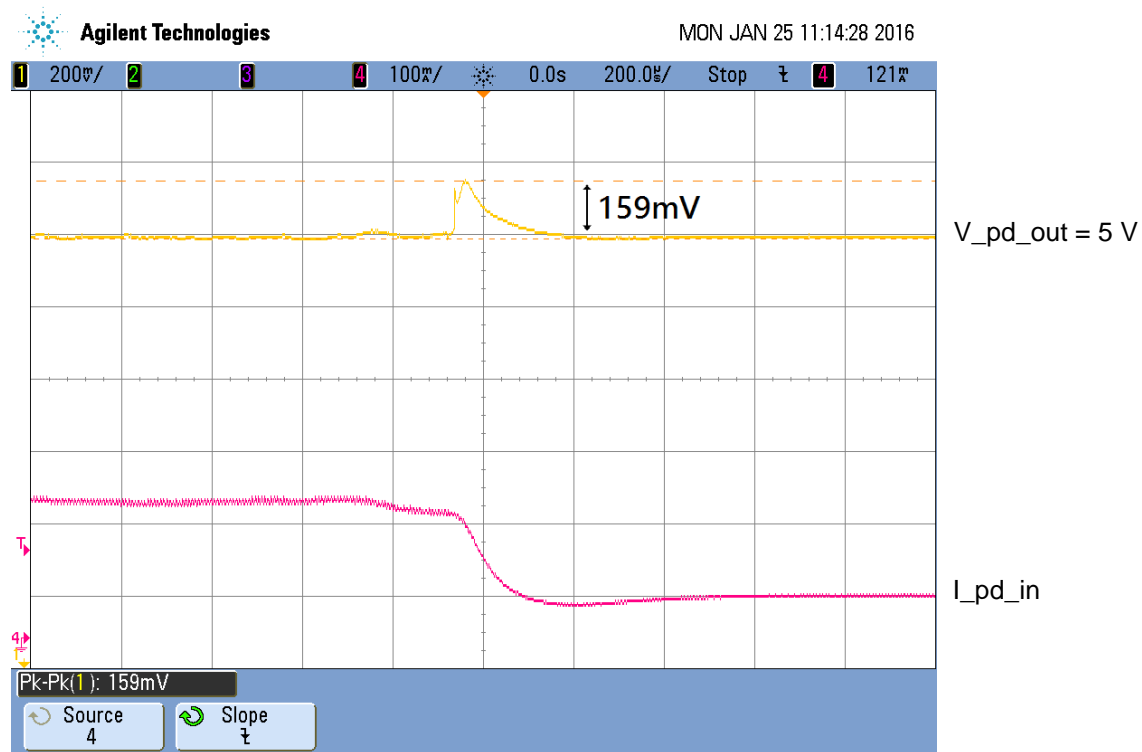


Figure 14. Step Load Transient from 10 W to 2.5 W

5. General Guidelines for Selecting Output Filter Capacitor

5.1. Non-Isolated Case Output Capacitor Selection

In the non-isolated case, the peak-to-peak ripple current is generally low enough that a single electrolytic capacitor can be used for the output filter with reasonable output ripple voltage.

Generally, the main selection factor for the output filter is load transient response.

The change in output voltage for a load step of ΔI is:

$$\Delta V = \Delta I \times \left(\text{ESR} + \frac{K}{C_{\text{out}} \times B} \right)$$

Where ESR is the output capacitor ESR; C_{out} is the output capacitor value, and B is the loop bandwidth and experimentally, $K \sim 0.3$.

Higher values of C_{out} and lower values of ESR generally result in lower loop bandwidth. As discussed in "4.1.2. Output Filter and Loop Stability—Non-Isolated Design" on page 12, it has been found that, due to the stabilizing effects of the switch and rectifier resistance, even ultra-low ESR capacitors do not give a large peaking in the feedback loop. For this reason, lower ESR capacitors and higher values of capacitance always give better load transient response despite the reduced bandwidth.

Standard designs from Silicon Laboratories, Inc. have been optimized for a load transient response of about $\pm 5\%$ for 10% to full load or full load to 10% load. For optimal load transient response, the low ESR designs are recommended.

In general, it can be expected that, for low ESR designs, the load transient response is dominated by:

$$\Delta V = \Delta I \times \left(\frac{K}{C_{\text{out}} \times B} \right)$$

and the bandwidth is decreased as the square root of capacitance; so:

$$\Delta V = \Delta I \times \frac{1}{\sqrt{C_{\text{out}}}}$$

When varying the output capacitor, it is important to optimize and verify the loop stability.

5.2. Isolated Case Output Capacitor Selection

For the isolated case, the output ripple current is much larger and a pi section filter is used.

The first capacitor is used to reduce most of the ripple. Generally, very low ESR ceramic capacitors are used in the first section of the filter because of their small size and excellent ripple handling capability. Two 0805 capacitors in parallel are generally adequate.

A small inductor of about 1 μH is used in the pi filter to avoid saturation and also to avoid inductive resonance with the output filter capacitor.

The final capacitor for the pi filter is chosen based on load transient response.

As with the non-isolated case, the change in output voltage for a load step of ΔI is:

$$\Delta V = \Delta I \times \left(\text{ESR} + \frac{K}{C_{\text{out}} \times B} \right)$$

Where ESR is the output capacitor ESR; C_{out} is the final output capacitor value; B is the loop bandwidth, and, experimentally, $K \sim 0.3$. Higher values of C_{out} and lower values of ESR generally result in lower loop bandwidth.

Standard designs from Silicon Laboratories, Inc. have been optimized for a load transient response of about $\pm 5\%$ for 10% to full load or full load to 10% load. For optimal load transient response, the low ESR designs are recommended.

In general, it can be expected that, for low ESR designs, the load transient response is dominated by:

$$\Delta V = \Delta I \times \left(\frac{K}{C_{out} \times B} \right)$$

and the bandwidth is decreased as the square root of capacitance; so:

$$\Delta V = \Delta I \times \frac{1}{\sqrt{C_{out}}}$$

When varying the output capacitor, it is important to optimize and verify the loop stability.

5.3. Steady State Failure Rate

The MTBF (Mean Time Between Failure) value is a quantitative measure of component reliability. The output capacitor determines overall loop stability, output voltage ripple, and, more importantly, load transient response.

The life of aluminum electrolytic capacitors is very dependent on environmental and electrical factors. Environmental factors include temperature, humidity, atmospheric pressure, and vibration. Electrical factors include operating voltage, ripple current, and charge-discharge duty cycle. Among these factors, temperature (ambient temperature and internal heating due to ripple current) is the most critical to the life of aluminum electrolytic capacitors, whereas conditions, such as vibration, shock, and humidity, have little affect on the actual life of the capacitor. The electrolytic capacitors are evaluated by accelerated life tests. The acceleration tests contain three factors: temperature, voltage, and ripple current, which are shown by following equation:

$$L_B = L_A \times A_T \times A_V \times A_R$$

Where:

L_B = Lifetime under a certain condition, "B"

L_A = Lifetime under a certain condition, "A"

A_T = Temperature acceleration factor

A_V = Voltage acceleration factor

A_R = Ripple current acceleration factor

In case of Si3402-B based flyback designs, the output filter stage typically consists of a two-stage LC filter or a simple Pi filter. In both these cases, the capacitor close to the output rectifier diode should have the lowest ESR and be able to absorb most of the ac current ripple. The second-stage capacitor is meant to have high capacitance in order to give good transient response; therefore, ESR does not become a critical factor. The location of the second-stage capacitor is also not critical and can be moved away from heat dissipating components. In most of the designs, the first-stage capacitor is a ceramic capacitor with very low ESR, and the second stage capacitor is aluminum electrolytic with high capacitance. Generally, the temperature acceleration factor (A_T) is between 1.7 ~ 2.3.

Voltage within the allowed operating range has little effect on the actual life expectancy of a capacitor. However, in certain applications or misapplications, the applied voltage can be detrimental to the life of an aluminum electrolytic capacitor. When capacitors are used at or below their rated voltage, the acceleration factor (A_V) is equal to 1.

Finally, compared with other types of capacitors, aluminum electrolytic capacitors have a higher dissipation factor Tan Delta and, therefore, are subject to greater internal heat generation when ripple currents exist. To assure the capacitor's life, the maximum permissible ripple current of the product is specified.

When ripple current flows through the capacitor, heat is generated by the power dissipated in the capacitor accompanied by a temperature increase. Internal heating produced by ripple currents can be represented by:

$$W = I_R^2 \times R_{ESR} + V \times I_L \dots\dots\dots(1)$$

Where:

W = Internal power loss

I_R = Ripple current

R_{ESR} = Internal resistance (Equivalent Series Resistance)

V = Applied voltage

I_L = Leakage current

The ripple current multiplier (A_R) dependency on the frequency is attached here.

Table 4. Typical Values for Working Voltage ≤ 100

Nominal Capacitance (μF)	Frequency (Hz)					
	50/60	100/120	300	1K	10K	50K
4.7 or below	0.65	1.00	1.35	1.75	2.30	2.50
10 to 47	0.75	1.00	1.25	1.50	1.75	1.80
100 to 1,000	0.80	1.00	1.15	1.30	1.40	1.50

For Si3402-B based designs, the aluminum electrolytic capacitor is normally operated at a voltage much lower than its rated voltage, and it does not absorb much of the ripple current.

The output filter capacitor value for a given output voltage and the converter configuration must be close to the value specified in the Si3402-B-EVB and Si3402-B-ISO-EVB users guide available on the Silicon Laboratories, Inc. web site:

<http://www.silabs.com/products/power/poe/Pages/PoweredDevices.aspx>

For users who would like to use the Si3402-B dc-dc converter as an add-in module to a system that has its own input capacitance, the total output capacitance of the Si3402-B dc-dc converter including the input capacitance of the system should not exceed the specified value.

6. Surge

The Si3402-B has an input clamp that will protect it against surges as spelled out in IEEE 802.3.

IEEE 802.3 specifies a 1000 V surge with 0.3 μ sec rise time and 50 μ sec fall time applied to each conductor through a series resistance of 402 Ω . Because this pulse is generally applied to all conductors, the differential current at the input is generally very limited.

The Si3402-B is designed to handle a 50 μ sec, 5 A pulse that would result from applying the surge to either both Tx or Rx pairs and grounding the other pair. This is accomplished by turning on the hot swap switch while disabling the switcher if current flows in the input clamp. During the 50 μ s transient, a large portion of the input energy is redirected to the switcher input capacitor. For this reason, a 15 μ F minimum input capacitor is recommended.

The Si3402-B is also required to survive the application of telephony ringing voltage. IEEE 802.3 specifies 56 V dc + 175 V peak ringing applied through 400 Ω source impedance at a frequency of 20 to 60 Hz. In this case, when the voltage reaches 100 V, the telephony switch turns ON, protecting the controller.

Continuous application of such a large ringing signal will damage the Si3402-B (although it will not cause a safety hazard). However, such a large ringing signal should also cause a "ring trip" or apparent off-hook indication at the central office within 200 msec. It has been found that the Si3402-B can withstand application of telephony ringing for over one second before damage occurs; so, in general, telephony ringing will not cause damage.

In some applications, up to 16 kV of system-level ESD immunity is required. The standard Si3402-B EVB designs meet this requirement when the input is not powered. However, when the input is powered and the Si3402-B is producing an output through the dc-dc converter, damage may occur to the input diode bridges for ESD events above 4 kV when applied to the output terminals if C10 to C17 are not used. Capacitors C10 to C17 allow passing system-level ESD events in excess of 16 kV.

For isolated applications that require a high level of system-level ESD immunity, the capacitors are recommended. For non-isolated applications, it is generally not possible for an ESD event (at the output supply) to occur because the output terminals of the dc-dc converter are generally not accessible while input power is applied. However, even for non-isolated designs, there is a possibility for large ESD events may reach the power supply terminals, in which case these capacitors (C10 to C17) are also recommended.

7. Use with an Auxiliary Power Supply

In some applications, it is desirable to be able to use either the power from the RJ45 Power over Ethernet or from a low-cost auxiliary power supply. This is very easy to do with the Si3402-B, and a 48 V auxiliary supply is shown in Figure 15.

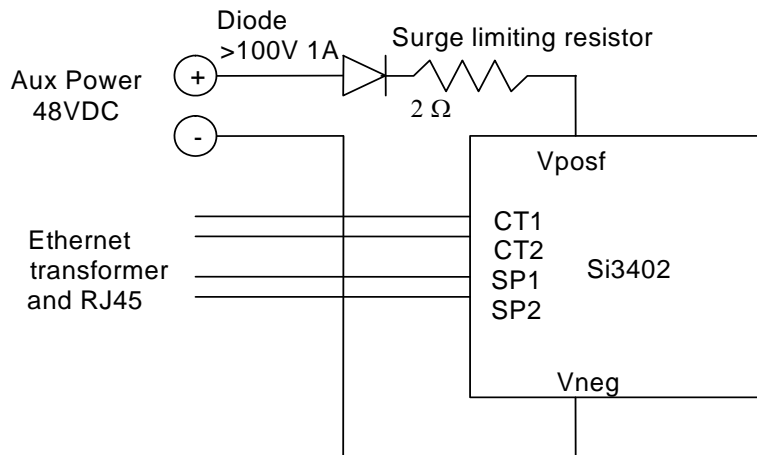


Figure 15. 48 V Auxiliary Supply

The auxiliary power source must supply between 41 and 56 V and at least 15 W for class 0 or 3 equipment (less if the equipment is class 1 or 2). It must also have output that is isolated from earth ground. To prevent damage from hot insertion suddenly charging the 0.1 μ F input capacitor, a 2 Ω surge limiting resistor in series with the auxiliary power supply is recommended.

This provides a very simple and inexpensive means of providing auxiliary power. The diode bridges in the Si3402-B ensure that no power is fed back to the PSE.

The auxiliary power source always provides the power if it is plugged in first because the PSE will not successfully complete the detection and classification cycle. If the PSE is plugged in first, the auxiliary power or the auxiliary power source could provide the power, whichever has the greater output voltage. If the auxiliary power source provides the power, the PSE will generally sense a disconnect.

The Si3402-B PLOSS signal indicates whether power is being provided from the auxiliary power source.

It is also possible to use a lower-voltage auxiliary power source, such as 12 V by diode OR at the output of the switching converter, as shown in Figure 16.

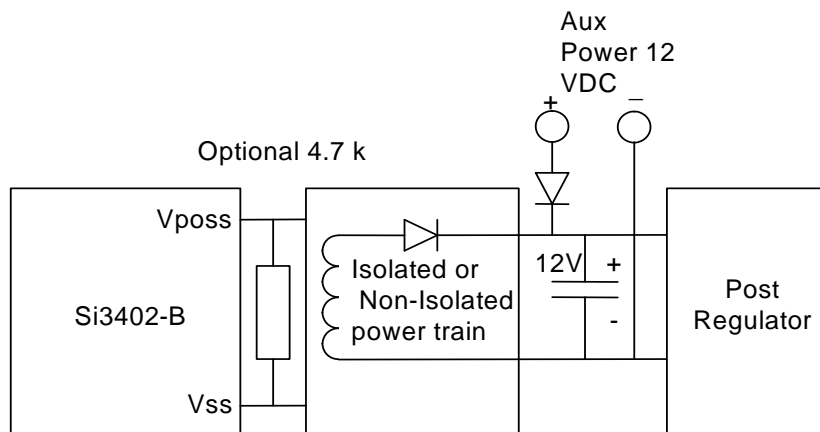


Figure 16. 12 V Auxiliary Supply

This option may be preferable when a post regulator is required for generation of very low voltages, such as 1.8 V, or when the post regulator is required for low noise.

With the post regulator option, the larger output voltage will again supply the power. In this case, the Si3402-B will attempt to go through the detection and classification cycle, but if the AUX supply is providing the power, the Si3402-B will not draw enough dc current, and the PSE may disconnect and cycle continuously. To prevent this, it is possible to add a 4.7 k Ω , 1 W resistor from VPOSF to VSS of the Si3402-B to ensure >10 mA power drain from the PSE. If this resistor is added, the PSE will always have >10 mA power drain and will stay connected even if the auxiliary power source is providing the load current.

In this option, the PLOSS indicator will not be active when the auxiliary power source is providing the power and the PSE is not present.

8. Layout, EMI, and EMC Considerations

Refer to the files located at www.silabs.com/PoE under the documentation page for examples of recommended PCB layouts in the evaluation board user's guides. Silicon Labs strongly recommends adhering to the layouts shown in these designs to avoid potential performance issues. In general, four-layer PCB designs yield the most robust design, as shown in the evaluation board user's guides. Two-layer PCB designs must be carefully considered. Silicon Labs strongly recommends all two-layer PCB designs be reviewed before fabrication.

Submit PCB schematics and layout files to PoEinfo@silabs.com for feedback and recommendations on these designs.

8.1. Thermal Considerations

The thermal pad of the Si3402-B must be connected to a heat spreader. Generally, a 2 in² bottom plane connected to the thermal pad of the Si3402-B and electrically connected to Vneg is recommended. While the heat spreader generally is not a circuit ground, it is a good reference plane for the Si3402-B and is also useful as a shield layer for EMI reduction.

With the 2 in² thermal plane on an outer layer, the thermal impedance of the Si3402-B was measured at 44 °C/W. As an added data point, 54 °C/W was measured with a 1 in² plane on an inner layer.

Due to heating of the ambient air from the Schottky diode etc., the effective thermal impedance can be considerably higher than this. It is not unusual for the Si3402-B junction temperature to rise 70 °C. The Si3402-B is rated up to a junction temperature of 140 °C, with thermal shutdown to 160 °C typical. If such a high junction temperature is a concern, it can be reduced by bypassing the on-chip diode bridges. Diode bridge bypass for full-power applications should also be considered in a two-layer design where it is difficult to include such a large thermal plane.

8.2. Voltage Considerations

Since the Si3402-B is not exposed to dc voltages over 60 V dc, it is generally considered to be a safety-extra-low-voltage (SELV) circuit, and there are no particular spacing requirements other than those of high-yield board manufacture.

8.3. Current Considerations

Pins CT1, CT2, SP1, SP2, HSO, and V_{POSF} carry up to 325 mA dc. 12 mil traces have been found to be adequate. Pins SWO and V_{SS} carry current spikes of up to several amps, although the dc current is no more than 325 mA, and 25 mil traces are used for these pins. Output current can be up to 3 A depending on output voltage, and 50 mil traces are recommended in the output section.

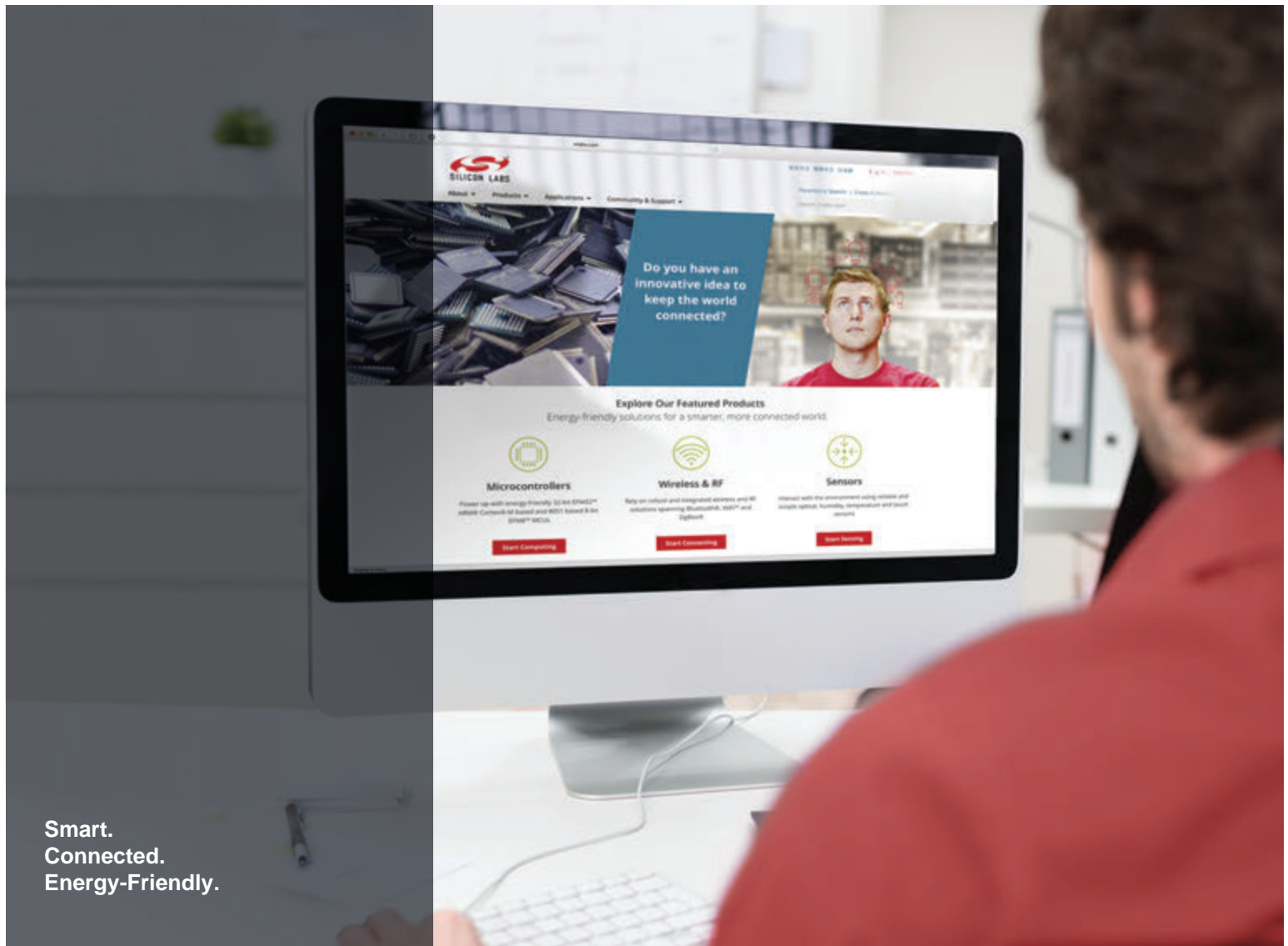
8.4. Minimum Load Considerations

To ensure the switcher does not pulse on and off when no load is on the output, Silicon Labs recommends a ≥250 mW load be present. See "3.5. Maintain Power Signature (MPS)" on page 9 for more information.

9. Conclusion

This application note has covered the basic operation and design equations for the Si3402-B, allowing the design of highly-integrated and efficient PDs for PoE applications.

As mentioned earlier, reference designs are also available at www.silabs.com/PoE to assist in the easy design-in process for the Si3402-B. The evaluation boards and reference designs are documented separately and include example layouts and BOM lists.



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