QCA9531 v2.0 802.11n 2x2 2.4 GHz Premium SOC for WLAN Platforms

Data Sheet

80-Y7991-1 Rev. C

October 2014

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Revision history

Revision	Date	Description
A	May 2014	Initial Version
B	June 2014	Added Reliability, Section 10
C	October 2014	■ Section 3.7.1, DDR Configurations. Remove link from Table 3-6. ■ Section 9.2, Recommended Operating Conditions: Updated Table 9-2. ■ Section 9.5.2, DDR Timing: Updated section Table 9-8, added Table 9-9. Renamed Figure 9-3.

Contents

1 General Description

The Qualcomm® XSPAN™ QCA9531 is a highly integrated and feature-rich IEEE 802.11n 2x2 2.4 GHz System-on-a-Chip (SoC) for advanced WLAN platforms.

It includes a MIPS 24Kc processor, one PCI Express 1.1 Root Complex interface, five port IEEE 802.3 Fast Ethernet Switch with MAC/PHY, one USB 2.0 MAC/PHY, and external memory interface for serial Flash, DDR1 or DDR2, UART, and GPIOs that can be used for LED controls or other general purpose interface configurations.

The QCA9531 PCIE root complex interface can be used to connect to an endpoint such as the Qualcomm Atheros single-chip MAC/BB/radio for dual concurrent WLAN applications. The QCA9531 supports 802.11n operations up to 144 Mbps for 20 MHz and 300 Mbps for 40 MHz, and 802.11b/g data rates. Additional features include Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC) and Maximal Ratio Combining (MRC).

The QCA9531 supports booting from NOR flash.

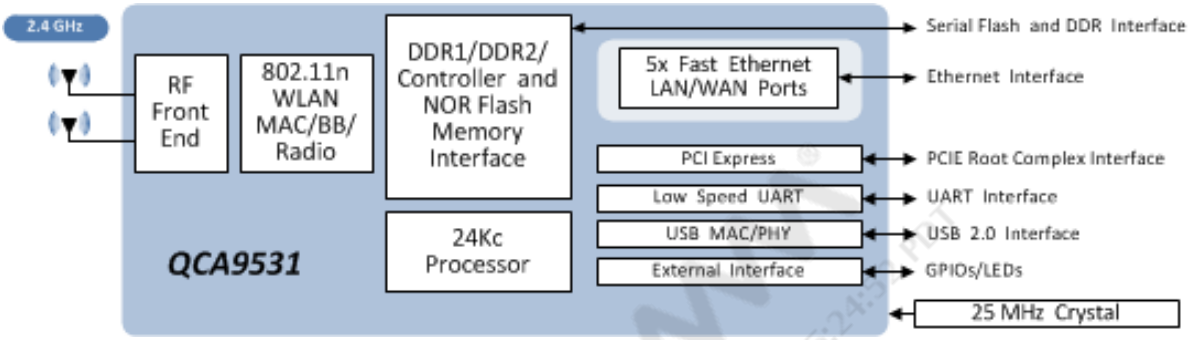
1.1 Features

- 24Kc MIPS processor with 64 KB I-Cache and 32 KB D-Cache, operating at up to 650 MHz
- External 16-bit DDR1, operating at up to 200 MHz, DDR2 operating at up to 300 MHz (600M transfers/sec)

  NOTE For DDR2 designs, Qualcomm Atheros recommends using a 4-layer baord. See *80-Y6755-1_A_Using_DDR2_on_QCA953X_Designs.pdf* for a more detailed explanation.

- SPI NOR Flash memory support
- 10/100 Ethernet Switch with four IEEE 802.3 Ethernet LAN ports and one WAN port
- PCI Express 1.1 Root Complex interface
- One USB 2.0 controller with built-in MAC/ PHY supports Host mode
- One low-speed UART (115 Kbps) and multiple GPIO pins for general purpose I/O
- Fully integrated RF Front-End including PAs and LNAs
- Optional external LNA/PA
- 25 MHz reference clock input
- 1.2 V switching regulator
- Advanced power management with dynamic clock switching for ultra-low power modes
- 156-pin 12 mm x 12 mm DRQFN package

1.2 QCA9531 System Block Diagram



2 Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
OD	An open-drain digital output signal
O	A digital output signal
P	A power or ground signal

Figure 2-1 shows the QCA9531 pinout.

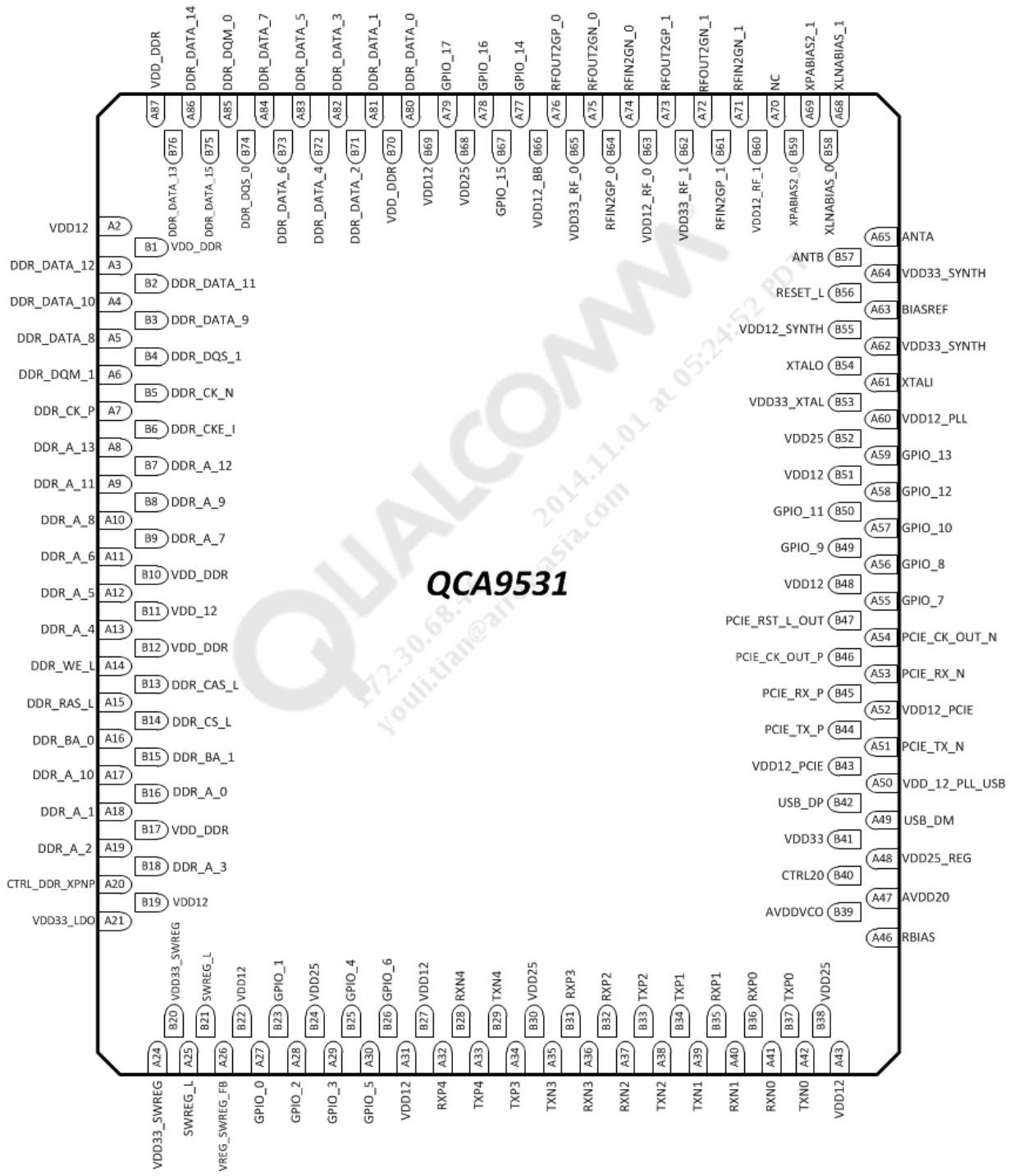


Figure 2-1 Package Pinout (See-Through Top View)

Table 2-1 provides the signal-to-pin relationship information for the QCA9531.

Table 2-1 Signal to Pin Relationships and Descriptions

Signal Name	Pins	Type	Description
General			
RESET_L	B56	IH	External power on reset with weak pull up. This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.
XTALI	A61	I	25 MHz crystal When using an external clock (TCXO), the XTALI pin is grounded and the XTALO pin should be driven with a square wave clock. AC coupling is recommended for the clock signal to the XTALO pin. The internal circuit provides the DC bias of approximately 0.6 V. The peak-to-peak swing of the external clock can be between 0.3 V and 1.2 V. In general, larger swings and sharper edges reduce jitter, but introduce the potential of high frequency spurious tones. The phase noise of the oscillator should be lower than -145 dBc/Hz at 100 KHz carrier offset.
XTALO	B54	I/O	
Radio			
RFIN2GN_0	A74	IA	Differential RF inputs for 2.4 GHz chain 0; Use one side for single-ended input
RFIN2GP_0	B64	IA	
RFOUT2GN_0	A75	OA	Differential RF outputs for 2.4 GHz chain 0
RFOUT2GP_0	A76	OA	
RFIN2GN_1	A71	IA	Differential RF inputs for 2.4 GHz chain 1; Use one side for single-ended input
RFIN2GP_1	B61	IA	
RFOUT2GN_1	A72	OA	Differential RF outputs for 2.4 GHz chain 1
RFOUT2GP_1	A73	OA	
Analog Interface			
BIASREF	A63	BIASREF voltage is 310 mV; must connect a 6.19 KΩ ± 1% resistor to ground	
RBIAS	A46	BIAS for Ethernet	
XPABIAS2_0	B59	Optional external power amplifier bias	
XPABIAS2_1	A69		
XLNABIAS_0	B58	Optional external LNA bias	
XLNABIAS_1	A68		
External Switch Control			
ANTA	A65	O	External RF switch control These output pins are in the V_{dd33} voltage domain.
ANTB	B57	O	

Table 2-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pins	Type	Description
Ethernet Switch			
RXN0	A41	IA	Ethernet port 0 receive pair, can be grounded if not used
RXP0	B36	IA	
RXN1	A40	IA	Ethernet port 1 receive pair, can be grounded if not used
RXP1	B35	IA	
RXN2	A37	IA	Ethernet port 2 receive pair, can be grounded if not used
RXP2	B32	IA	
RXN3	A36	IA	Ethernet port 3 receive pair, can be grounded if not used
RXP3	B31	IA	
RXN4	B28	IA	Ethernet port 4 receive pair, can be grounded if not used
RXP4	A32	IA	
TXN0	A42	OA	Ethernet port 0 transmit pair, can be left open if not used
TXP0	B37	OA	
TXN1	A39	OA	Ethernet port 1 transmit pair, can be left open if not used
TXP1	B34	OA	
TXN2	A38	OA	Ethernet port 2 transmit pair, can be left open if not used
TXP2	B33	OA	
TXN3	A35	OA	Ethernet port 3 transmit pair, can be left open if not used
TXP3	A34	OA	
TXN4	B29	OA	Ethernet port 4 transmit pair, can be left open if not used
TXP4	A33	OA	
External Memory Interface			
DDR_A_0	B16	O	14-bit external memory address bus
DDR_A_1	A18	O	
DDR_A_2	A19	O	
DDR_A_3	B18	O	
DDR_A_4	A13	O	
DDR_A_5	A12	O	
DDR_A_6	A11	O	
DDR_A_7	B9	O	
DDR_A_8	A10	O	
DDR_A_9	B8	O	
DDR_A_10	A17	O	
DDR_A_11	A9	O	
DDR_A_12	B7	O	
DDR_A_13	A8	O	

Table 2-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pins	Type	Description
DDR_BA_0	A16	O	2-bit bank address to indicate which bank the chip is accessing
DDR_BA_1	B15	O	
DDR_CKE_L	B6	O	Deactivates the external memory clock when the signal is high
DDR_CK_N	B5	O	DDR_CK_P and DDR_CK_N are differential clock outputs. All address and control signals timing are related to the crossing of the positive edge of DDR_CK_P and the negative edge of DDR_CK_N.
DDR_CK_P	A7	O	
DDR_CS_L	B14	O	External memory chip select signal, active low
DDR_CAS_L	B13	O	When this signal is asserted, it indicates the address is a column address. Active when the signal is low.
DDR_RAS_L	A15	O	When this signal is asserted, it indicates the address is a row address. Active when the signal is low.
DDR_DQM_0	A85	O	DDR data mask for data byte 0 and 1
DDR_DQM_1	A6	O	
DDR_DQS_0	B74	I/O	DDR data strobe for data byte 0 and 1
DDR_DQS_1	B4	I/O	
DDR_WE_L	A14	O	When this signal is asserted, it indicates that the following transaction is write. Active when the signal is low.
DDR_DATA_0	A80	I/O	16-bit external memory data bus
DDR_DATA_1	A81	I/O	
DDR_DATA_2	B71	I/O	
DDR_DATA_3	A82	I/O	
DDR_DATA_4	B72	I/O	
DDR_DATA_5	A83	I/O	
DDR_DATA_6	B73	I/O	
DDR_DATA_7	A84	I/O	
DDR_DATA_8	A5	I/O	
DDR_DATA_9	B3	I/O	
DDR_DATA_10	A4	I/O	
DDR_DATA_11	B2	I/O	
DDR_DATA_12	A3	I/O	
DDR_DATA_13	B76	I/O	
DDR_DATA_14	A86	I/O	
DDR_DATA_15	B75	I/O	

Table 2-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pins	Type	Description
GPIO			
GPIO0	A27	I/O	General purpose I/O, programmable, can be used as JTAG, SPI, UARTs, LED control. Default input pins can be grounded, and default output pins can be left open if not used. Please note that GPIO17 is an open-drain GPIO. When used as outputs, these pins should be pulled up to V_{dd25}. or V_{dd33} depends on the supply voltage of the external pin that is being driven.
GPIO1	B23	I/O	
GPIO2	A28	I/O	
GPIO3	A29	I/O	
GPIO4	B25	I/O	
GPIO5	A30	I/O	
GPIO6	B26	I/O	
GPIO7	A55	I/O	
GPIO8	A56	I/O	
GPIO9	B49	I/O	
GPIO10	A57	I/O	
GPIO11	B50	I/O	
GPIO12	A58	I/O	
GPIO13	A59	I/O	
GPIO14	A77	I/O	
GPIO15	B67	I/O	
GPIO16	A78	I/O	
GPIO17	A79	I/O	
USB			
USB_DM	A49	IA/OA	USB D- signal; carries USB data to and from the USB 2.0 PHY
USB_DP	B42	IA/OA	USB D+ signal; carries USB data to and from the USB 2.0 PHY
PCI Express Root Complex			
PCIE_TX_N	A51	OA	Differential transmit, can be left open if not used
PCIE_TX_P	B44	OA	
PCIE_RX_N	A53	IA	Differential receive, can be left open if not used
PCIE_RX_P	B45	IA	
PCIE_CK_OUT_P	B46	OA	Differential reference clock (100 MHz), can be left open if not used
PCIE_CK_OUT_N	A54	OA	
PCIE_RST_L_OUT	B47	OD	PCI Express reset, open drain, should be pulled up to Vdd33 through 1 KΩ resistor, can be left open if not used.

Symbol	Pin	Description	
Regulator Control			
CTRL_DDR_XPNP	A20	OA	External PNP Control. Connect to the base of an external PNP: collector to VDD_DDR and emitter to VDD33.
CTRL20	B40	OA	External PNP control. Connect to the base of an external PNP: collector to AVDD20 and emitter to VDD33.
Internal Voltage Regulator			
SWREG_L	A25, B21	1.2 V switching regulator output	
VDD33_SWREG	A24, B20	3.3 V input to the internal switching regulator	
VREG_SWREG_FB	A26	Feedback to the internal switching regulator	
Power			
AVDD20	A47	2.0 V switching regulator output;	
AVDDVCO	B39	1.2 V output from the internal switching regulator	
VDD12	A2, B11, B19, B22, A31, B27, A43, B48, B51, B69	Digital 1.2 V supply	
VDD12_PCIE	B43, A52	Analog 1.2 V supply	
VDD12_PLL_USB	A50		
VDD12_PLL	A60		
VDD12_SYNTH	B55		
VDD12_RF_0	B63		
VDD12_RF_1	B60		
VDD12_BB	B66		
VDD_DDR	B1, B10, B12, B17, B70, A87	DDR1/DDR2 supply 2.6 V and 1.8 V typical	
VDD25	B24, B30, B38, B52, B68,	I/O 2.62 V Supply	
VDD33	B41	Analog I/O, LDO reg SWREG 3.3 V supplies	
VDD33_LDO	A21		
VDD33_SYNTH	A62, A64		
VDD33_XTAL	B53		
VDD33_RF_0	B65		
VDD33_RF_1	B62		
NC	A70	No connect	
Ground Pad			
Exposed Ground Pad	—	Tied to GND; see “Package Dimensions” on page 375	

3 Functional Description

3.1 Functional Block Diagram

Figure 3-1 illustrates the QCA9531 functional block diagram.

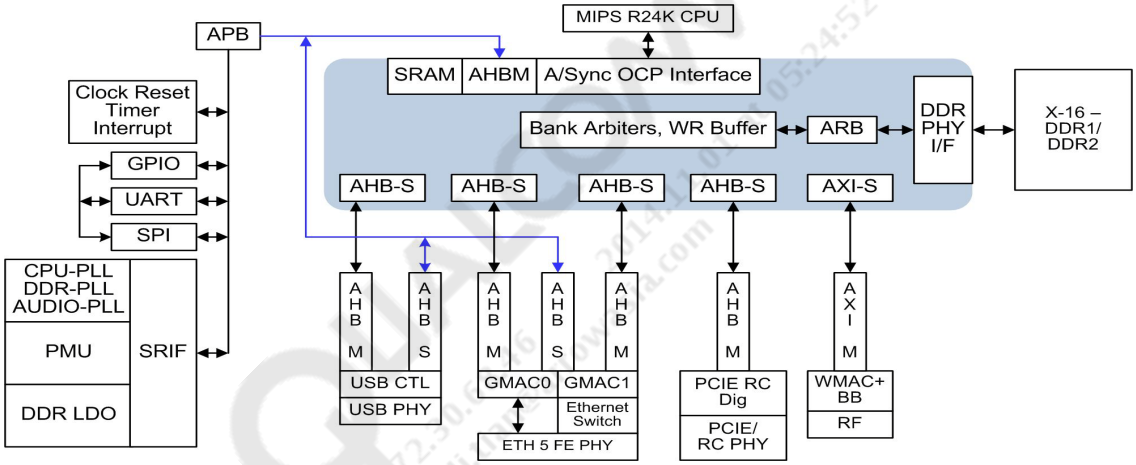


Figure 3-1 Functional Block Diagram

The QCA9531 is comprised of several internal functional blocks, as summarized in Table 3-1.

Table 3-1 Functional Blocks

Block	Description
CPU Core and Memory Controller	The MIPS R24 K supports 64 KByte I-Cache and 32 KByte D-Cache, targeted to operate at up to 650 MHz. ■ The memory controller is targeted to run at a frequency of 300 MHz (600 M transfers/sec) ■ Supports DDR self refresh mode for low power consumption ■ Synchronous mode is also supported where the memory controller and CPU operate with a single phase align clock ■ Clock dithering for DDR/CPU clocks to reduce EMI interference ■ DDR Clock dithering effected immediately after refresh cycle
Clocking	Three internal PLLs: CPU, DDR and the WLAN PHY layer generate various internal clocks. The PLLs support a 25-MHz reference clock input. See PLL and Clock Control.
DDR Memory	■ DDR1 x16, DDR2 x16 See DDR Memory Controller.
PCI Express Interface	PCIE 1.1 interface Root Complex interface. See PCIE RC.
USB	USB 2.0 controller with built-in MAC/ PHY supports Host mode. See USB 2.0 Interface.

Table 3-1 Functional Blocks (cont.)

Block	Description
Gigabit Ethernet MAC	Independent IEEE 802.3 complaint Gigabit (GB) Ethernet MAC. ■ Internal 10/100 Ethernet switch with 4 LAN ports and one WAN port ■ The QCA9531 integrates two GB Ethernet MACs (GMAC0 and GMAC1). GMAC0 is connected to the Ethernet switch, while GMAC1 is connected to the FE PHY ports (port 0 or 4) of the switch. Please see Ethernet Subsystem, page 8-353 for more details. ■ GMAC1 Connects to the internal Ethernet switch Can be configured to run at 1000 Mbps speed or in 100 Mbps speed. This interface supports flow control between the CPU port and the switch.
WLAN	2 chain / 2 stream (2x2) IEEE 802.11n WLAN MAC, PHY, and internal radio that operates in 2.4 GHz
UART	Normal speed UART (16550 equivalent) at speeds up to 115.2 Kbps. See Low-Speed UART Interface.
GPIO	Contains 17 highly configurable GPIO pins; any multiplexed signal can be routed to any GPIO as output, and any multiplexed input can be routed from any GPIO pin to the internal logic. See GPIO.
Voltage Regulator and LDOs	Efficient 1.2 V switching regualtor for providing analog and digital core voltage of 1.2 V. LDOs are also provided to generate power to DDR1 (2.6 V), DDR2 (1.8 V) that can supply power to external memories and HB Pads. External memories are assumes to directly get the power from external 3.3 V. GPIOs are powered by 2.62 V LDO.
Bootstrap Options	Several features of the QCA9531 can be configured or selected based on bootstrap pins whose state on power-on reset selects a given choice or configuration, for example boot from internal ROM or external flash. See Bootstrap Options.

3.2 Bootstrap Options

Table 3-2 details the QCA9531 bootstrap options. The GPIO pins have internal pull-downs and the DDR pins have internal pull-ups.

Table 3-2 Bootstrap Options

Bit	Name	Pin	Description	
15:13	RES	Reserved	Reserved (Reset 0x0)	
12	SOFTWARE_OPTION_2	GPIO12	Can be used by software for any purpose	
11	SOFTWARE_OPTION_1	GPIO14	Can be used by software for any purpose	
10	RES	GPIO6	Reserved (Reset 0x0). No pull down capable.	
9	RES	Reserved	Reserved (Reset 0x0)	
8	RES	GPIO4	Reserved (Reset 0x0) Do not pull up.	
7	USB_MODE	GPIO13	0	Host mode
			1	Reserved
6	RES2	Reserved	Reserved (Reset 0x0)	
5	JTAG_MODE	GPIO16	0	JTAG (Default)
			1	EJTAG
4	REF_CLK	GPIO15	0	CLK25 (Default)
			1	Reserved
3:2	RES	Reserved	Reserved (Reset 0x0)	
1	RES	GPIO7	Reserved (Reset 0x0)	
0	DDR_SELECT	GPIO10	0	Selects DDR 2 (Default)
			1	Selects DDR 1

3.3 Reset

Figure 3-2 shows the QCA9531 reset.

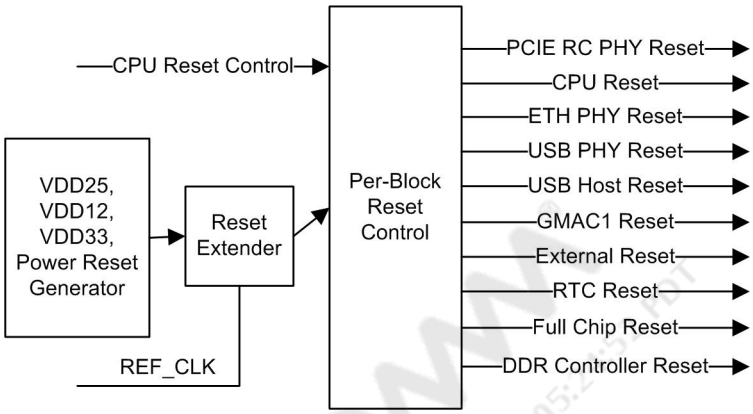


Figure 3-2 Reset

Each of the per- block resets can be issued by software by writing to the RST_RESET register. See Reset (RST_RESET) for the bit definitions for each per block reset.

3.4 PLL and Clock Control

3.4.1 Full Chip Clocking Structure

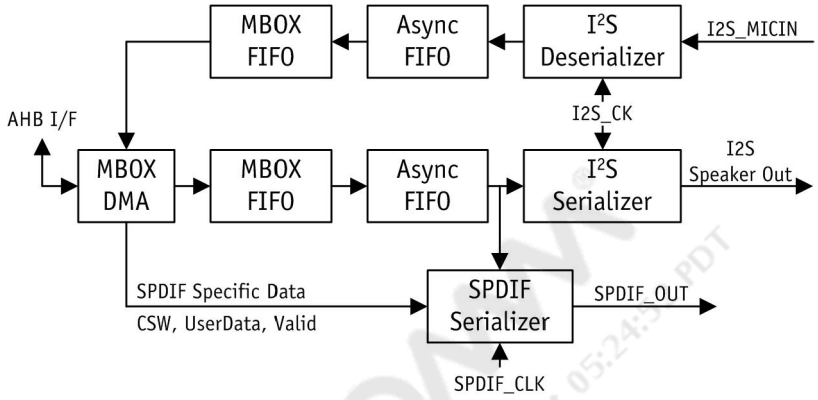


Figure 3-3 Full Chip Clocking Structure

The QCA9531 includes the BB, CPU, DDR,as well as the Ethernet PLLs. See Table 3-3.

Table 3-3 QCA9531 PLLs

PLL	Description
BB PLL	By default, this PLL generates clocks for the radio, baseband, and WMAC.
PLL	By default the source clock for the CPU_CLK, although it can also be derived from the DDR PLL.
DDR PLL	By default the source clock for DDR_CLK and AHB_CLK, though both can also be derived from the CPU PLL.
PCIE PLL	Generates the 100 MHz reference clock for the PCIE RC. The final output frequency of the PCIE PLL is similarly configurable, like the CPU and DDR PLLs, although a fixed 100 MHz clock is required. OUTDIV should be set to 3, and N=14 for 100 MHz.
Ethernet PLL	Generates the clock for all Ethernet interfaces, MAC
USB PLL	Generates the USB 30 MHz/480 MHz clock for USB controller.

3.4.2 PLL

The CPU PLL is configured by the bit CPU_PLL_CONFIG in the registers CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG) and CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL). The clock can vary slightly by changing the divider's FRAC. The dithering is controlled through the CPU PLL Dither Parameter (CPU_PLL_DITHER) register. Note that if DDR_CLK is derived from the CPU PLL, it is better to turn off dithering.

The clock switcher and dynamic clock divider guarantee any change in inputs to this module is glitch-free; thus input to this block can change. Make sure when modifying the select to the clock switcher module that both clock inputs are present as switching from one clock to another depends on both clocks. Figure 3-4 details the derivation of the CPU_CLK that clocks the MIPS processor.

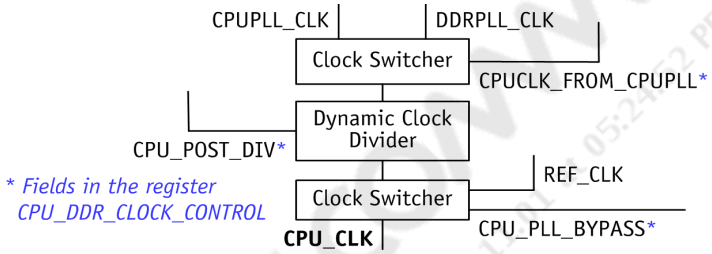


Figure 3-4 24Kc Processor CPU Clock

3.4.3 DDR PLL

The DDR PLL is configured with the registers DDR PLL Configuration (DDR_PLL_CONFIG) and CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL). The DDR PLL clock is dithered by DDR PLL Configuration (DDR_PLL_CONFIG); it is done immediately after issuing an auto refresh command to the DDR. Figure 3-5 shows the DDR_CLK and AHB_CLK select signal change to clock switching logic, which should be made only if both clock inputs are preset.

The FRAC part of the PLL is dynamic, but the INT part of the divider requires the PWD to go high and then low. Thus, changing the PLL clocks dynamically would be possible only by:

1. Asserting the PLL_BYPASS mode bit.
2. Asserting the PWD for that PLL.
3. Reconfiguring divider INT/FRAC values.
4. Deasserting the PWD for the PLL
5. Waiting for the clock to become stable by polling the UPDATE bit.
6. Removing the PLL_BYPASS bit for this PLL.

The CPU can do this procedure any time for CPU_CLK/AHB_CLK, which is useful to enter low power states leading to minimal chip power consumption. Another way to change the CPU/AHB/DDR_POST_DIV is to shift down to lower clock for these clocks. An optimal DDR and CPU frequency can be dynamically chosen, and the PLL reprogrammed for optimal power. However, make sure no DDR transaction is pending or in progress before changing DDR_CLK frequency.

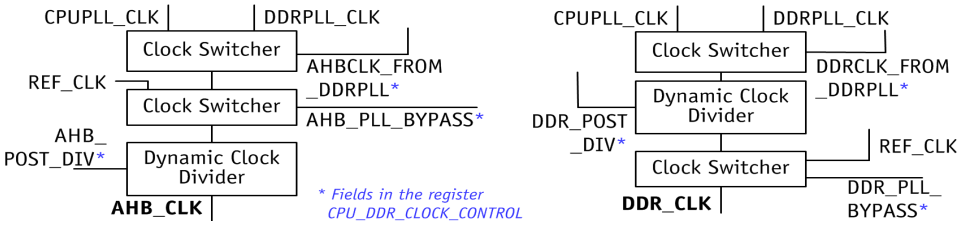


Figure 3-5 DDR_CLK and AHB_CLK

3.4.4 Ethernet PLL

The Ethernet PLL is controlled by the register Switch Clock Source Control (SWITCH_CLOCK_SPARE).

3.5 MIPS Processor

The QCA9531 integrates an embedded MIPS 24Kc processor.

Table 3-4 summarizes the configuration settings used by the QCA9531. Upon reset, the CPU puts out an address of 0xBFC00000 which is mapped to the flash address space. The QCA9531 processor supports a clock frequency of up to 500 MHz.

Table 3-4 Core Processor Configuration Settings

Setting	Description
Cache Size	The QCA9531 implements 64 KB 4-way set associative instruction cache and 32 KB four-way set associative data cache. It supports single cycle multiply-accumulate, MIPS32 and MIPS16 instruction sets, and non-blocking cached reads.
Endian	The QCA9531 implements big Endian addressing.
Block Addressing	The QCA9531 implements sequential ordering.

3.6 Address Map

Figure 3-6 shows the address space allocation.

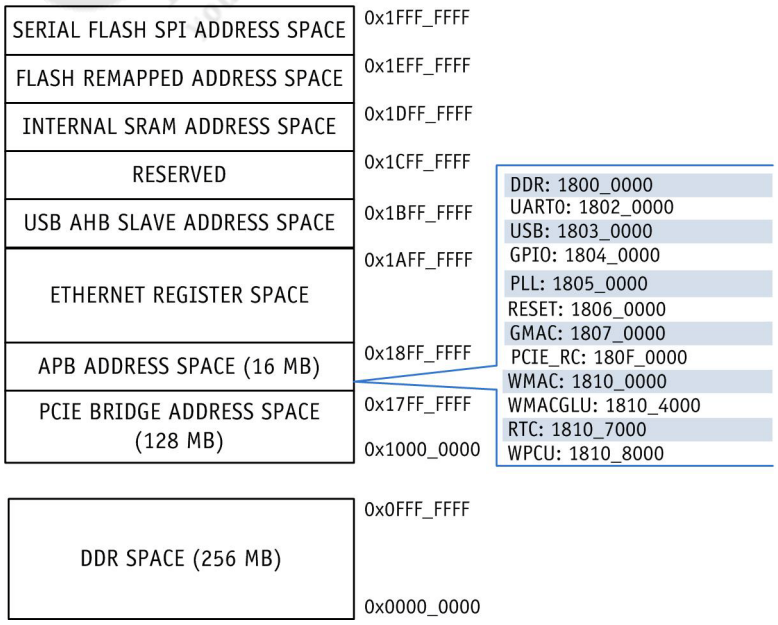


Figure 3-6 Address Space Allocation

3.7 DDR Memory Controller

The QCA9531 allows an external memory interface supporting 16-bit DDR1, or DDR2. The memory controller can enter DDR self refresh for low power modes. The DDR1 and DDR2 modes have small differences in read/write transactions. For a write transaction, DDR2 memory expects write data after a latency depending on CAS latency. DDR1 memory expects the first data immediately after the clock in which the write command is issued.

The controller uses the configurable parameter DDR2_TWL in the DDR2 Configuration (DDR_DDR2_CONFIG) register. The parameter is applicable for DDR1 and DDR2 modes: it should be set to one for DDR1 mode, and to (CAS – 1) * 2 – 1 for DDR2 mode.

Enabling DDR2 Mode

Set the bit MODE_EN in DDR Controller Configuration (DDR_CTL_CONFIG) to zero, and the bit ENABLE_DDR2 in the DDR2 Configuration (DDR_DDR2_CONFIG) register to one.

- If HALF_WIDTH is set, x16 mode is selected and requires the VEC field in the register DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE) to be set to 0xFFFF.
- Set the bit SEL_18 in the register DDR2 Configuration (DDR_DDR2_CONFIG) to one.

3.7.1 DDR Configurations

Table 3-5 and Table 3-6 show the DDR configurations. See the reference design for details.

Table 3-5 DDR Configurations when DDR_CONFIG2_SWAP_A26_A27 = 0

Device on Board	Total Memory	Mode	DDR1	DDR2	Notes
512 Mbits x 16	64 MBytes	16 Bit	Yes	Yes	For both DDR1 and DDR2, CPU address A26, A27 unused
512 Mbits x 8 512 Mbits x 8	128 MBytes	16 Bit	Yes	Yes	In DDR1, CPU address A26 is A11 of COL, A27 used In DDR2, A27 unused

Table 3-6 DDR Configurations when DDR_CONFIG2_SWAP_A26_A27 = 1

Device on Board	Total Memory	Mode	DDR1	DDR2	Notes
512 Mbits x 16	64 MBytes	16 Bit	Yes	Yes	For both DDR1 and DDR2, CPU address A26, A27 unused
1 Gbit x 16	128 MBytes	16 Bit	No	Yes	—

3.7.2 DDR Initialization Sequences

3.7.2.1 DDR1 Controller Initialization

NOTE It is extremely important to leave the reset values of many register fields untouched. Therefore software should always read a register and then modify only the required fields unless otherwise mentioned.

- Burst length (BL) should always be 8.
- Read Latency (RL) = Additive Latency (AL) + CAS Latency (CL)
- Write Latency (WL) = RL – 1
- tCK = CK_P CLK period

1. Program the register DDR Controller Configuration (DDR_CTL_CONFIG):

Bit	Bit Name	Setting	
1	HALF_WIDTH	0	Reserved
		1	For x16

This step must to be done before memory initialization; the other steps do not have this dependency.

2. Set a value in DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE):
   - 0xFFFF for x16
3. If $F_{DDR\_CLK} < 2 * F_{AHB\_CLK}$ (frequency of DDR_CLK and AHB_CLK), program the DDR FSM wait control with 0x00000A24.
4. Set the timing parameters in DDR DRAM Configuration (DDR_CONFIG). These numbers typically use the values from the specification, but greater values can also be used. Numbers are in terms of the number of controller clocks.

Bit	Bit Name	Description
26:23	TMRD	Load mode register command cycle time.
22:17	TRFC	Auto-refresh command period
16:13	TRRD	Active bank a to active bank delay
12:9	TRP	Precharge command period
8:5	TRCD	Active to read or write delay
4:0	TRAS	Active to precharge time = max(tRAS_min, tRCD + CL). A greater value can be programmed if tRTP is not satisfied.

5. Set timing parameters in DDR Controller Configuration (DDR_CTL_CONFIG). Bits [25:8] show minimum values; a greater value can also be programmed. Numbers are in terms of controller clock numbers.

Bit	Bit Name	Setting
29:26	GATE_OPEN_LATENCY	2 * CAS_LATENCY
25:21	TWTR	Write-to-read Command delay [1+BL/2 + tWTR/tCK] * 2 For example: tWTR=2 tCK; BL=8 TWTR=2 * [1+4+2]= 14
20:17	TRTP	Read-to-precharge command delay BL/2 + max(tRTP,2)-2
16:12	TRTW	Read-to-write command delay (CL + BL/2) * 2 For example: CL=3; BL=8; TRTW=7 * 2= 14
11:8	TWR	Write recovery time [BL/2+tWR/tCK] * 2 – 1 For example: BL=8; tWR= 15 ns; tCK=(1/200 MHz)= 5 ns TWR=[4+3] * 2-1= 13

6. Initialize DDR memory as shown in DDR Memory Initialization.
7. Set the register DDR Refresh Control and Configuration (DDR_REFRESH).
   E.g., for TREFI = 7.8 µs, set DDR_REFRESH[13:0] to 195 (REFCLK = 25 MHz).
8. Set the ENABLE bit.

3.7.2.2 DDR2 Controller Initialization

NOTE It is extremely important to leave the reset values of many register fields untouched. Therefore software should always read a register and then modify only the required fields unless otherwise mentioned.

- Burst length (BL) should always be 8.
- Read Latency (RL) = Additive Latency (AL) + CAS Latency (CL)
- Write Latency (WL) = RL – 1
- tCK = CK_P CLK period

1. Program the register DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER):

Bit	Bit Name	Setting	
1	HALF_WIDTH	0	Reserved
		1	For x16

This step must to be done before memory initialization; the other steps do not have this dependency.

2. Set a value in DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE):
   - 0xFFFF for x16
3. If $F_{DDR\_CLK} < 2 * F_{AHB\_CLK}$ (frequency of DDR_CLK and AHB_CLK), program the DDR FSM wait control with 0x00000A24.
4. Set the timing parameters in DDR DRAM Configuration (DDR_CONFIG). These numbers typically use the values from the specification, but greater values can also be used. Numbers are in terms of the number of controller clocks.

Bit	Bit Name	Description
26:23	TMRD	Load mode register command cycle time.
22:17	TRFC	Auto-refresh command period
16:13	TRRD	Active bank a to active bank delay
12:9	TRP	Precharge command period
8:5	TRCD	Active to read or write delay
4:0	TRAS	Active to precharge time = max(tRAS_min, tRCD + CL). A greater value can be programmed if tRTP is not satisfied.

5. Set timing parameters in DDR DRAM Configuration 2 (DDR_CONFIG2). Bits [25:8] show minimum values; a greater value can also be programmed. Numbers are in terms of controller clock numbers.

Bit	Bit Name	Setting
29:26	GATE_OPEN_LATENCY	2 * CAS_LATENCY

25:21	TWTR	[WL+BL/2 + max(2, tWTR/tCK)] * 2
		For example:
		tWTR = 7.5 ns;
		tCK = (1/200 MHz) = 5 ns;
		BL = 8; CL = 4; AL = 0
		WL = AL+CL-1 = 0+4-1 = 3
		TWTR = [3+4+max(2, 7.5/5)] * 2 = [3+4+2] * 2 = 18

20:17	TRTP	16-bit | [(AL+BL+max(tRTP/tCK,2))-2] * 2
		For example:
		tRTP = 7.5 ns;
		tCK= (1/200 MHz) = 5 ns;
		BL=8; AL=0
		TRTP = [(0+8+2)-2] * 2=16

16:12	TRTW	(RL+BL/2+1-WL) * 2 For example: CL = 4; BL = 8; AL = 0; WL=3; TRTW = [4+4+1-3]*2 = 12
11:8	TWR	(BL/2+tWR/tCK) * 2-1 For example: BL = 8; TWR = 15 ns; TCK = (1/200 MHz) = 5 ns TWR = [4+3] * 2-1 = 13

6. Initialize DDR memory as shown in DDR Memory Initialization.
7. Set the register DDR Refresh Control and Configuration (DDR_REFRESH)
   a. Store a refresh PERIOD value of 300 (REFCLK = 25 MHz).
   b. Set the ENABLE bit.

3.7.3 DDR Memory Initialization

These steps are performed as step 6 under DDR1 Controller Initialization, and as step 7 under DDR2 Controller Initialization.

1. To initialize DDR memory, when:
   - CKE is set low
   - Clocks are stable

   Allow a 200 µs delay then send an NOP/DESELECT command.
2. Set the CKE bit of the register DDR DRAM Configuration 2 (DDR_CONFIG2).
3. Issue a precharge all commands by setting the PREA bit of the register DDR DRAM Configuration (DDR_CONFIG) twice with a interval of 200 clock cycles between them.
4. Write to the register DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER) to enable the DLL. Refer to the DDR memory device datasheet for bit-definitions of this register.
5. Issue an EMRS command to DDR by setting the EMRS bit in the register DDR DRAM Configuration (DDR_CONFIG) to enable the DLL.
6. Write to the register DDR Mode Value (DDR_MODE_REGISTER) with the value 0x1*N*3 (the reset value) to reset the DLL, where *N* indicates to set the four fields appropriately per the CAS value. Refer to the DDR memory device datasheet for bit-definitions of this register.
7. Issue an MRS command to DDR by setting the MRS bit of the register DDR DRAM Configuration (DDR_CONFIG).
8. Re-issue two precharge all commands again by redoing step 3.
9. After a 200 CLK second delay, issue two refresh commands by setting REF (bit [2]) of the register DDR DRAM Configuration (DDR_CONFIG) twice with a interval of 200 clock cycles between them.
10. Write to the register DDR Mode Value (DDR_MODE_REGISTER) with the value 0x0*N*3 to bring DLL out of reset, where *N* indicates to set the four fields appropriately per the CAS.
11. Issue an MRS command to DDR by setting the MRS bit of the register DDR DRAM Configuration (DDR_CONFIG).

3.7.4 CPU DDR Address Mapping

Table 3-7 shows the correspondence of the internal CPU address, the DDR interface address, and the physical memory address.

Table 3-7 CPU Address: DDR Interface Address Mapping

DDR Interface Address	Column Address	Row Address[1]	Bank Address
DDR_A_0	0	CPU_ADDR[11]	—
DDR_A_1	CPU_ADDR[2]	CPU_ADDR[12]	—
DDR_A_2	CPU_ADDR[3]	CPU_ADDR[13]	—
DDR_A_3	CPU_ADDR[4]	CPU_ADDR[14]	—
DDR_A_4	CPU_ADDR[5]	CPU_ADDR[15]	—
DDR_A_5	CPU_ADDR[6]	CPU_ADDR[16]	—
DDR_A_6	CPU_ADDR[7]	CPU_ADDR[17]	—
DDR_A_7	CPU_ADDR[8]	CPU_ADDR[18]	—
DDR_A_8	CPU_ADDR[23]	CPU_ADDR[19]	—
DDR_A_9	CPU_ADDR[25]	CPU_ADDR[20]	—
DDR_A_10	0	CPU_ADDR[21]	—
DDR_A_11	CPU_ADDR[26]	CPU_ADDR[22]	—
DDR_A_12	CPU_ADDR[27]	CPU_ADDR[24]	—
DDR_A_13 / DDR_BA_2	—	CPU_ADDR[26][2 3]	CPU_ADDR[26][4]
DDR_BA_0	—	—	CPU_ADDR[9]
DDR_BA_1	—	—	CPU_ADDR[10]

1. Row address: DDR_A_0 through DDR_A_12, when the row is accessed.
2. CPU_ADDR[26] is DDR_A_13 in DDR1 1 GBit
3. CPU_ADDR[26] is DDR_BA_2 in DDR2 1 GBit
4. CPU_ADDR[26] and CPU_ADDR[27] can be swapped during column addressing, to support these on-board configurations: 2 x (DDR1 1 GBit x8), 2 x (DDR1/2 1 GBit x16)

3.7.5 Refresh

DDR memory must refresh periodically. The DDR controller has an automatic refresh command generation module that clocks with REF_CLK. Because DDR_CLK is dynamic, the auto REFRESH_PERIOD works on the fixed REF_CLK.

3.7.6 Self Refresh

The QCA9531 DDR controller supports a self refresh (SF) sequence; that is, it has hardware support to issue commands to place DDR memory into and to exit SF mode. The register Self Refresh Timer (SF_TIMER) controls basic SF behavior.

If EN_SELF_REFRESH is set and no valid DDR transactions are in progress, the DDR controller initiates an SF enter sequence. If DDR clients have transactions in progress, the controller waits until no DDR activity is occurring.

If EN_AUTO_SF_EXIT is set, the controller initiates an exit SF sequence upon detecting a DDR request from any DDR client. If this bit is not set, DDR is in SF, a DDR new request is seen, the controller generates a miscellaneous DDR_ACTIVITY_IN_SF interrupt (see the register

Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)). Software can alternatively force the controller to exit SF by setting EN_SELF_REFRESH to 0.

The controller can also generate an interrupt to the CPU while entering SF, exiting SF, and while in SF if DDR activity is detected. Immediately after exiting SF, read commands should not be issued until TXSR is met and non-read commands should not be issued until TXSNR is met. These timing parameters can be programmed via the TXSNR and TXSR fields of the DDR_SF_CTL registers. Note that these are in terms of DDR_CLK and not REF_CLK.

While in SF, DDR_CK_P and DDR_CK_N clocks can be gated, optionally using the EN_SF_CLK_GATING bit.

3.8 PCIE RC

The QCA9531 has a PCIE root complex (RC) supporting a single-lane PCIE link at 2.5 Gbps. The RC core implements the PCIE protocol layers: transaction, data link, and physical.

The PCIE PHY module resides outside of the RC core, interfacing through the PIPE, which is the standard interface between the PHY and the RC core. The PHY is split across the PIPE so MAC functionality is in the RC core and PHY functionality is implemented in the PIPE-compliant PHY external to the RC.

It has a sideband interface referred to as data bus interface (DBI) controlled by the CPU via APB, which programs the RC core configuration space. The DBI delivers a read/write request from application logic to the internal registers of the core. The RC core configuration space contains these register maps:

- PCI 3.0 compatible configuration space header
- PCI capabilities structures (starts at offset 0x40)
- PCIE extended configuration space (starts at offset 0x100)
- Port logic (vendor-specific registers) (starts at offset 0x700)

The configuration and memory accesses to the two PCIE RC interfaces are mapped to the CPU AHB address space:

	Memory Slave	Configuration Slave
PCIE RC0	0x1000_0000 to 0x11FF_FFFF	0x1400_0000 to 0x5FF_FFFF

See Figure 3-7.

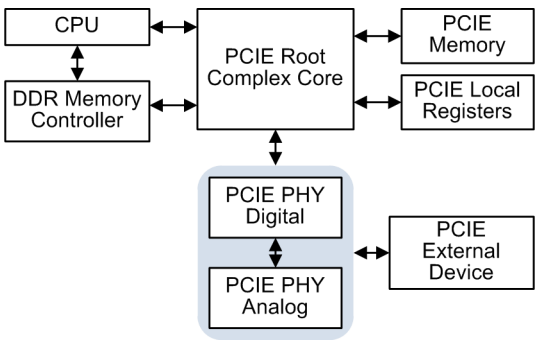


Figure 3-7 PCIE RC

3.8.1 Power Management

The PCIE RC supports L0s and L1 active state power management space. L0s is the low power standby state with lower entry/exit latencies. L1 saves more power, but with increased entry and exit latencies.

The PCIE RC includes the capacity to shut off the reference clocks going to the endpoint and powering down the RC PCIE PLL in L1 mode.

3.8.2 Interrupts

PCIE RC supports legacy INTx interrupts generated through PCIE message transactions. The application monitors the assertion and de-assertion messages for inbound INTx legacy interrupts (from the downstream component). It also supports MSI-based interrupt signalling through posted memory write transfers (only one of INTx or MSI can be enabled at any time).

3.8.3 Error Reporting Capability and Status Checking

PCIE RC support advanced error reporting (AER) and has the ability to capture correctable and uncorrectable (fatal and non-fatal) errors in transmit and receive. The provision to capture these error messages as interrupts also exists.

3.8.4 Byte-Swap Option

The PCIE RC AHB interface is configured as big-Endian. Depending on whether data is to be sent to the endpoint in little- or big-Endian format, PCIE RC software can add a byte-swap in slave data going into the PCIE core.

3.8.5 Request Sizes and Payloads

The PCIE RC supports:

- The maximum number of outstanding incoming non-posted requests is 32
- The maximum payload size is 128
- The maximum read the request size (AHB Master) is 128 bytes
- The burst size for master requests is 64 bytes (INCR)

3.9 GPIO

The GPIO module is structured in such a way that any signal listed in GPIO Output Select Values (Table 3-9) and GPIO Input Select Values (Table 3-10) can be available through any GPIO pin, except for the JTAG signals, which cannot be programmed on any other GPIO pins.

GPIO pins can be configured as input/output by programming the appropriate bits in the GPIO function registers. On reset, GPIO[17:0] are configured with certain default signals, as shown in Table 3-8. Some of these GPIOs will get configured based on the Boot selection in the Boot ROM Mode.

NOTE JTAG pins must use GPIO[3:0]. Apart from JTAG, all signals can use any GPIO and can use GPIO[3:0] by setting the DISABLE_JTAG bit to 1 in the GPIO_OUT_FUNCTIONx register.

Table 3-8 Default GPIO Signals

GPIO	Signal	Direction	During Reset	After Reset	Description
GPIO0	TCK	Input	Input	Input	JTAG Clock
GPIO1	TDI	Input	Input	Input	JTAG data input
GPIO2	TDO	Output	0	0	JTAG data output
GPIO3	TMS	Input	Input	Input	JTAG test mode
GPIO4	CPU_CLK/4	Output	Input	Output	Clock Observation
GPIO5	SPI_CS	Output	Input	1	SPI chip select (Default = 1)
GPIO6	SPI_CLK	Output	Input	0	SPI clock (Default = 0)
GPIO7	SPI_MOSI	Output	Input	0	SPI data output (Default = 0)
GPIO8	SPI_MISO	Input	Input	Input	SPI data input
GPIO9	Software Configured	Input	Input	Input	Software configurable
GPIO10	Software Configured	Input	Input	Input	Software configurable
GPIO11	Software Configured	Input	Input	Input	Software configurable
GPIO12	Software Configured	Input	Input	Input	Software configurable
GPIO13	Software Configured	Input	Input	Input	Software configurable
GPIO14	Software Configured	Input	Input	Input	Software configurable
GPIO15	Software Configured	Input	Input	Input	Software configurable
GPIO16	Software Configured	Input	Input	Input	Software configurable
GPIO17	SYS_RST_L	Output	Output	Output	Software configurable

3.9.1 GPIO Output

GPIO is structured to output one of 128 signal through any GPIO pin. See Figure 3-8.

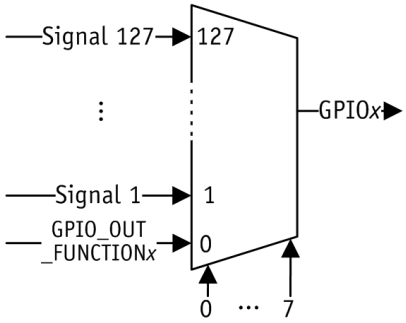


Figure 3-8 GPIO is Structured to Output 1 of 128 Signal Through Any GPIO

Each GPIO output is structured as 128:1 MUX. The MUX select is an 8-bit register that can be programmed with the values 0-127 to allow that particular input signal through the GPIO pin, as shown in Table 3-9. The signal gets the source from the GPIO_OUT_FUNCTIONx registers. Each 32-bit register has select values for four GPIO pins (8 bits each).

Register	Selects values for these GPIO pins
GPIO Function 0 (GPIO_OUT_FUNCTION0)	GPIO pins 0, 1, 2, 3
GPIO Function 1 (GPIO_OUT_FUNCTION1)	GPIO pins 4, 5, 6, 7
GPIO Function 2 (GPIO_OUT_FUNCTION2)	GPIO pins 8, 9, 10, 11
GPIO Function 3 (GPIO_OUT_FUNCTION3)	GPIO pins 12, 13, 14, 15
GPIO Function 4 (GPIO_OUT_FUNCTION4)	GPIO pins 16, 17

If set to zero, the CPU directly controls the GPIO through the GPIO Per Bit Set (GPIO_SET)/GPIO Per Bit Clear (GPIO_CLEAR) registers, or observes via the GPIO Input Value (GPIO_IN) register.

To output the signal through the GPIO pin, use this register programming:

1. If using a non-JTAG signal on GPIO[3:0], write the bit DISABLE_JTAG of the GPIO_OUT_FUNCTIONx register to 1.
2. Set the corresponding GPIO bit in GPIO Output Enable (GPIO_OE) to 0.
3. Write the particular GPIO field in GPIO_OUT_FUNCTIONx with the corresponding output signal value from Table 3-9.

For example, to drive the SPI_CLK signal through the GPIO4 pin:

1. Set bit[4] of GPIO Output Enable (GPIO_OE) register to 0.
2. Set the 8-bit field ENABLE_GPIO4 (bits [7:0]) of the GPIO Function 1 (GPIO_OUT_FUNCTION1) register to 10.

Table 3-9 GPIO Output Select Values

MUX Select Value	Signal Name	Description
1	SYS_RST_L	SYS_RST_L
2:7	RES	Reserved
8	SPI_CLK	SPI Clock
9	SPI_CS_0	SPI Chip Select 0
10	SPI_CS_1	SPI Chip Select 1
11	SPI_CS_2	SPI Chip Select 2
12	SPI_MOSI	SPI data output
21:13	RES	Reserved
22	UART0_SOUT	Low-speed UART0 serial data out
23	SRIF_OUT	SRIF data output
25:24	RES	Reserved
30:26	LED_ACTN_0	5-port Ethernet switch activity LEDs
35:31	LED_COLN_0	5-port Ethernet switch collision detect LEDs
40:36	LED_DUPLEXN_0	5-port Ethernet switch full-duplex/half-duplex LEDs
45:41	LED_LINK	5-port Ethernet switch indicator LEDs
47:46	RES	Reserved
49:48	SMART_ANT_CTL [3:2]	Smart antenna control bits [3:2]
50	ATT_LED	External LNA control for chain 0
51	PWR_LED	External LNA control for chain 1
52	TX_FRAME	MAC Tx Frame (indicates the MAC is transmitting)
53	RX_CLEAR_INTERNAL	WLAN Active
54	LED_NETWORK_EN	MAC network enable
55	LED_POWER_EN	MAC power LED
77:56	RES	Reserved
78	RX_CLEAR_EXTENSION	Medium clear for Rx
85:79	RES	Reserved
86	USB_SUSPEND	USB suspend
87	RES	Reserved
88	DDR_DQ_OE	DDR data output enable
89	CLKREQ_N_RC	Clock request root complex
90	CLK_OBS0	GE0 MII CLKC25
91	CLK_OBS1	PCIE_RC_CLK
92	CLK_OBS2	CLK125
93	CLK_OBS3	CPU_CLK/4
94	CLK_OBS4	AHB_CLK/2
95	CLK_OBS5	USB_CLK
96	CLK_OBS6	WMAC_CLK
127:97	RES	Reserved

3.9.2 GPIO Input

GPIO inputs are structured so that any signal listed in Table 3-10 can source from any GPIO pin. See Figure 3-9.

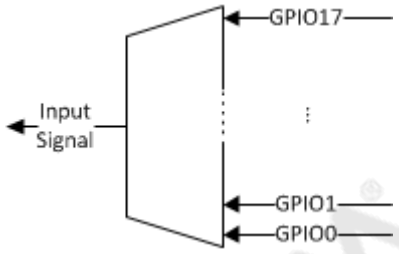


Figure 3-9 Any Signal Can Receive Input From Any GPIO

Each signal can receive its input from GPIO[17:0]. Each signal has an 8-bit register that can be programmed with the GPIO values 0-17; the signal gets its input for the corresponding GPIO pin programmed in the GPIO_IN_ENABLEx registers (GPIO In Signals 0 (GPIO_IN_ENABLE0). See Table 3-10.

To route the GPIO input to a particular signal, use this register programming:

1. If using a non-JTAG signal on GPIO[3:0], write the bit DISABLE_JTAG of the GPIO Function (GPIO_FUNCTION) register to 1.
2. Set the corresponding GPIO bit in the GPIO Output Enable (GPIO_OE) register to 1.
3. Write the particular 8-bit GPIO field in the register GPIO In Signals 0 (GPIO_IN_ENABLE0) with the corresponding output signal value from Table 3-9.

   If a value greater than 17 is written, this signal is assigned a default value of 0.

For example, to route the UART0_SIN signal through the GPIO9 signal:

1. Set bit [9] of the GPIO Output Enable (GPIO_OE) register to 1.
2. Set the UART0_SIN field (bits[15:8]) in the GPIO In Signals 0 (GPIO_IN_ENABLE0) register to 0x9.

Table 3-10 shows the GPIO input select values.

Table 3-10 GPIO Input Select Values

Signal Name	Description
UART_SIN	Low speed UART0 serial data in
SPI_MISO	SPI data input

3.10 Serial Flash SPI/ROM

The SPI controller supports two ways of programming the SPI device:

- The bit blasting method by which data, CLK, and the CS are programmed directly by CPU bit in the controller register SPI_IO_CNTRL_ADDR, which is shifted on to the interface signals.
- Direct programming of the data and the number of bits to shift. The controller takes care of shifting the specified number of bits.

The SPI controller has a dedicated chip select available to an external flash for booting, as well as two more configurable chip selects.

3.10.1 SPI Operations

Before performing any SPI operation, the FUNCTION_SELECT and REMAP_DISABLE bits of the register SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR) are set to 1. Any page program or erase operations on the SPI device must enable the write enable latch (WEL).

3.10.2 Write Enable

1. Program the register SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR) with the WREN CMD value.
2. Program SPI_SHIFT_CNT_ADDR:

SHIFT_CNT	8	Number of WREN command bits
TENATE	1	After shifting 8-bit deassert chip select
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

3.10.3 Page Program

- Send a **write enable** command before any page program or erase operations.
- Use the **send** command:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the PP CMD value.
  b. Program SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	8	Number of command bits
TENATE	0	Do not deassert CS; CMD is followed by address/data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Send the address:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the address to be programmed.
  b. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR):

SHIFT_CNT	24	Number of address command bits
TENATE	0	Do not deassert CS; CMD is followed by address/data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Send the data:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the data to be programmed.
  b. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR):

SHIFT_CNT	32	Number of data bits
TENATE	1	Deassert chip select after programming the data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

The command and address can be programmed together in SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) in the order: {8'CMD, 24'ADDR}. The SHIFT_CNT field in SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) is set to 32.

3.10.4 Page Read

- Send command and address:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the **read** command and address.
  b. Program SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	32	Number of command and address bits
TERMINATE	0	Keep chip select asserted until the data is read
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Read the data by programming SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	32	Number of bits to be read
TERMINATE	1	Deassert the chip select after the data is read
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

3.11 Low-Speed UART Interface

The QCA9531 contains a 16550 equivalent UART controller/port for debug/console monitoring. The UART pins are multiplexed with GPIO pins. GPIO Output describes the multiplexed GPIO options. The UART controller can be programmed through a set of control registers. The UART supports programmable baud rates and can support up to 115.2 Kbps. This UART does not support hardware flow control.

3.12 USB 2.0 Interface

The USB controller supports a standard USB 2.0 host. In USB host mode, the QCA9531 can support the full number of devices/endpoints allowed in the USB 2.0 specification. It can be connected, either directly or through one or more hubs, at high-speed (480 Mbps) or full-speed (12 Mbps). The QCA9531 implements four bulk downstream endpoints, one bulk upstream endpoint, and one interrupt upstream endpoint. The USB core acts as a master on the internal AHB bus, maximizing data transfer speeds with the system DDR memory. The USB supports low power suspend mode wherein the total power consumed is less than 10 mW. See Figure 3-10.

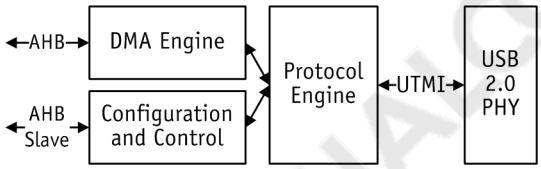


Figure 3-10 USB Interface

Table 3-11 describes the USB interface elements.

Table 3-11 USB Interface Elements

Name	Description
System Interface	The USB controller provides a AHB master interface for DMA transfer of descriptors and endpoint data between the System memory and the USB serial interface. QCA9531 CPU can control the USB controller operation through an AHB Slave interface. In Host Mode, the controller registers and data structures are compliant to Intel EHCI specifications. QCA9531 software must set the operation by writing into the CM bits of the USBMODE register.
Host Data Structure	The host data structures are used to communicate control, status, data and between software and the USB host controller. The data structure is compliant with EHCI specifications. A periodic frame list which is an array of pointers to a transfer list is used. There are asynchronous transfer lists for bulk and control data transfers and Isochronous Transfer list for Isochronous data transfers.
XCVR Interface	The USB Controller interfaces with an on-chip USB 2.0 PHY through the UTMI standard interface.

Table 3-12 shows the USB interface signals.

Table 3-12 USB Interface Elements

Name	Type	Description
USB_DP	IA/OA	USB D+ Signal
USB_DM	IA/OA	USB D– Signal

The QCA9531 has an exclusive USB 2.0 compliant host, that supports High-speed (480 Mbps), full speed (12Mbps) or Low speed (1.5 Mbps) clients. The USB core acts as a master on the internal AHB bus, thus maximizing data transfer speeds with the system DDR memory. The USB Host only interface supports all features of a compliant USB 2.0 host.

4 WLAN Medium Access Control (MAC)

The WLAN MAC consists of the following major functional blocks: 10 queue control units (QCUs), 10 distributed coordination function (DCF) control units (DCUs), a single DMA Rx unit (DRU), and a single protocol control unit (PCU). See Figure 4-1.

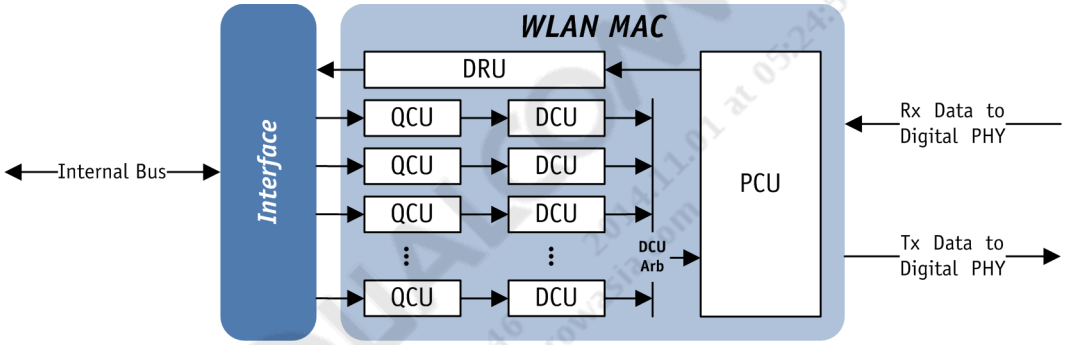


Figure 4-1 WLAN MAC Block Diagram

4.1 Overview

The WLAN MAC block supports full bus-mastering descriptor-based scatter/gather DMA. Frame transmission begins with the QCUs. QCUs manage the DMA of frame data from the host through the PCIE interface, and determines when a frame is available for transmission.

Each QCU targets exactly one DCU. Ready frames are passed from a QCU to its targeted DCU. The DCU manages the enhanced distributed coordination function (EDCF) channel access procedure on behalf of the QCUs associated with it.

Functionality of the WLAN MAC block includes:

- Tx frame data transfer from the DDR
- Rx frame data transfer the DDR
- Interrupt generation and reporting
- Sleep-mode sequencing
- Miscellaneous error and status reporting functions

Once the DCU gains access to the channel, it passes the frame to the PCU, which encrypts the frame and sends it to the baseband logic. The PCU handles both processing responses to the transmitted frame, and reporting the transmission attempt results to the DCU.

Frame reception begins in the PCU, which receives the incoming frame bitstream from the digital PHY. The PCU decrypts the frame and passes it to the DRU, which manages Rx descriptors and writes the incoming frame data and status.

4.2 Descriptor

The WLAN MAC is responsible for transferring frames between the DDR and the digital PHY. For all normal frame transmit/receive activity, the CPU provides a series of descriptors to the WLAN MAC, and the WLAN MAC then parses the descriptors and performs the required set of data transfers.

4.3 Descriptor Format

The transmit (Tx) descriptor format contains twenty-three 32-bit words and the receive (Rx) descriptor contains twelve 32-bit words.

A descriptor must be aligned on a 32-bit boundary in host memory, although best performance is achieved if the descriptor is aligned on a cache-line boundary. The MAC uses the final nine words of the Tx descriptor and the twelve words of the Rx descriptor to report status information back to the host.

See these tables for more information:

Table	Words	Description
Table 4-1	0–14	Tx descriptor format
Table 4-4	15–22	Tx descriptor format
Table 4-5	0–8	Tx descriptor status format
Table 4-6	0–11	Rx descriptor format

The Tx descriptor format is described in Table 4-1. With certain exceptions as noted, all Tx descriptor fields must be valid in the first descriptor of a non-aggregate frame. The fields for all following descriptors are ignored. For aggregate frames only the first descriptor of the first frame of the aggregate is valid. The fields for all following descriptors are ignored.

Table 4-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
0	31:16	ATHEROS_ID	The unique Qualcomm Atheros identifier of 0x168C is used to visually identify the start of the descriptor.
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.
	14	DESC_CTRL _STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 1 indicating control descriptor.
	13:12	RES	Reserved
	11:8	TX_QCU_NUM	Tx QCU number Indicates which QCU this descriptor is part of.
	7:0	DESC_ LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x17 (23 Dwords).

Table 4-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
1	31:0	LINK_PTR	Link pointer address Contains the 32-bit next descriptor pointer. Must be 32-bit aligned (bits [1:0] must be 0). A null value: (link_ptr= 0x0) is only allowed at the end of a non-aggregate or non-RIFS packet. If the packet is part of an aggregate or RIFS burst, a null is only allowed on the last descriptor of the last packet. A legal null value causes the QCU to stop. Must be valid for all descriptors.
2	31:0	BUF_PTR0	Data buffer pointer 0 Contains the 32-bits address of the first data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Must not be null (buf_ptr0 = 0x0) for all descriptors.
3	31:28	RES	Reserved

	27:16	BUF_LEN0	Data buffer length associated with data buffer pointer 0. Specifies the length, in bytes, of the data buffer associated with buf_ptr0. buf_len0 must not be 0. Note: This field must be valid for all descriptors.
			`case (header_length, qos packet) {`
			`  24, no : pad_length = 0;`
			`  24, yes: pad_length = 2;`
			`  30, no : pad_length = 2;`
			`  30, yes: pad_length = 0;`
			`}`
			`case (encrypt_type) {`
			`  wep  : icv_length = 4;`
			`  tkip nomic : icv_length = 4;`
			`  aes  : icv_length = 8;`
			`  tkip : icv_length = 12;`
			`  wapi : icv_length = 16;`
			`}`
			`fcs_length = 4;`
			`frame_length = buf_len0 + buf_len1 + buf_len2 + buf_len3 +`
			`  icv_length + fcs_length - pad_length`

	15:0	RES	Reserved
4	31:0	BUF_PTR1	Data buffer pointer 1 Contains the 32-bits address of the second data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Only valid if buf_ptr0 is not null.
5	31:28	RES	Reserved
	27:16	BUF_LEN1	Data buffer length associated with data buffer pointer 1. buf_len1 can only be 0 if and only if buf_ptr1 is null. See buf_len0 for details.
	15:0	RES	Reserved
6	31:0	BUF_PTR2	Data buffer pointer 2 Contains the 32-bits address of the third data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Only valid if buf_ptr0 and buf_ptr1 are not null.
7	31:28	RES	Reserved
	27:16	BUF_LEN2	Data buffer length associated with data buffer pointer 2. buf_len2 can only be 0 if and only if buf_ptr2 is null. See buf_len0 for details.
	15:0	RES	Reserved

Table 4-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
8	31:0	BUF_PTR3	Data buffer pointer 3 Contains the 32-bits address of the third data buffer associated with this descriptor. A Tx data buffer may begin at any byte address. Only valid if buf_ptr0, buf_ptr1, and buf_ptr2 are not null.
9	31:28	RES	Reserved
	27:16	BUF_LEN3	Data buffer length associated with data buffer pointer 2. buf_len2 can only be 0 if and only if buf_ptr3 is null. See buf_len0 for details.
	15:0	RES	Reserved
10	31:16	TX_DESC_ID	Tx descriptor sequence number Software will select a unique sequence number associated with this descriptor. This value is copied to the tx_desc_id in the transmit status.

	15:0	PTR_ CHECKSUM	Memory pointer checksum
			Verifies the integrity of the memory pointers/addresses in this descriptor. The equation looks like this:
			`checksum[31:0] = TXC[0]+TXC[1]+TXC[2]+TXC[3]+TXC[4]+`
			`TXC[5]+TXC[6]+TXC[7]+TXC[8]+TXC[9];`
			`ptr_checksum[15:0] = checksum[31:16] + checksum[15:0];`
			
			The carry bits above the MSB of the checksum or ptr_checksum will disappear.

11	31	CTS_ENABLE	Self-CTS enable Precedes the frame with CTS flag. If set, the PCU first sends a CTS before sending the frame described by the descriptor; used mainly for 802.11g frames to quiet legacy stations before sending a frame the legacy stations cannot interpret, even at the PHY level. At most only one of the rts_enable and cts_enable bits may be set; it is illegal to set both.
	30	DEST_INDEX _VALID	Destination index valid flag Specifies whether the contents of the DestIdx field are valid.
	29	INT_REQ	Interrupt request flag Set to one by the driver to request that the DMA engine generate an interrupt upon completion of the frame to which this descriptor belongs. Note: This field must be valid and identical for all descriptors of the frame. That is, all descriptors for the frame must have this flag set, or all descriptors for the frame must have this flag clear.
	28:25	RES	Reserved
	24	CLEAR_DEST _MASK	Clear destination mask bit flag If set, instructs the DCU to clear the destination mask bit at the index specified by the dest_index field.
	23	VEOL	Virtual end-of-list flag When set, indicates that the QCU should act (mostly) as if this descriptor had a null link_ptr, even though its link_ptr field may be non-null. Note: This field must be valid in the final descriptor of a frame and must be clear for all other descriptors of the frame.
	22	RTS_ENABLE	RTS enable If set, the PCU transmits the frame using the RTS/CTS protocol. If clear, the PCU transmits the frame without transmitting a RTS. At most only one of the rts_enable and cts_enable bits may be set; it is illegal to set both.
	21:16	TPC_0	TPC for Tx series 0. These bits pass unchanged to the baseband, where they control Tx power for the frame.
	15	CLEAR_ RETRY	Setting this bit disables the retry bit from being set in the Tx header on a frame retry; applies to both aggregate and non-aggregate frames.

Table 4-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
11 (cont.)	14	LOW_RX_ CHAIN	When set to 1, indicates that switches the Rx chain mask to low power mode after transmitted this frame.
	13	FAST_ANT _MODE	Fast antenna mode If set to 0, this means that this Tx frame to use the omni antenna mechanism. if set to 1, then the opposite omni antenna should be used.
	12	VMF	Virtual more fragment If this bit is set, bursting is enabled for this frame. If there is no burst in progress, it will initiate a CTS protected burst if cts_enable is set. If there is a previous burst in progress, it ignores the cts_enable bit assuming that this burst is protected.
	11:0	FRAME_ LENGTH	Frame length Specifies the length, in bytes, of the entire MAC frame, including the FCS, IC, and ICV fields.

Table 4-1 Tx Descriptor Format: Words 0–14

<table>
<tr><th>Word</th><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="15">12</td><td>31</td><td>MORE_RIFS</td><td>More RIFS burst flag; When set, indicates that the current packet is not the last packet of an aggregate. All descriptors for all packets of a RIFS burst except the descriptors of the last packet must have this bit set. All descriptors of the last packet of a RIFS burst must have this bit clear.</td></tr>
<tr><td>30</td><td>IS_AGG</td><td>This packet is part of an aggregate flag. All descriptors of the all packets in an aggregate must have this bit set.</td></tr>
<tr><td>29</td><td>MORE_AGG</td><td>More aggregate flag; When set, indicates that the current packet is not the last packet of an aggregate. All descriptors for all packets of an aggregate except the descriptors of the last packet must have this bit set. All descriptors of the last packet of an aggregate must have this bit clear.</td></tr>
<tr><td>28</td><td>EXT_AND_ CTL</td><td>Extension and control channel enable
Only four combinations are allowed; otherwise desc_config_error asserts. When neither ext_only nor ext_and_ctl are set, the RTS/CTS and data frame is sent based on the bandwidth: HT20 when 20_40 is set to 0 and HT40 shared when 20_40 is set to 1 (RTS/CTS frames are sent at in HT40 duplicate mode if 20_40 is set to 1). When ext_and_ctl is set the RTS/CTS and data frame is sent at HT40 duplicate. When ext_only is set the RTS/CTS and data frame is sent out in HT20 extension channel mode.
<table>
<tr><th>ETX_AND_CTL</th><th>20_40</th><th>DATA</th><th>RTS/CTS</th></tr>
<tr><td>0</td><td>0</td><td>HT20 Control</td><td>HT20 Control</td></tr>
<tr><td>0</td><td>1</td><td>HT40 Shared</td><td>HT40 Duplicate</td></tr>
<tr><td>1</td><td>1</td><td>HT40 Duplicate</td><td>HT40 Duplicate</td></tr>
</table></td></tr>
<tr><td>27</td><td>RES</td><td>Reserved</td></tr>
<tr><td>26</td><td>CORRUPT_ FCS</td><td>Corrupt packet FCS; When set, the FCS of the packet will be inverted to guarantee the transmitted FCS is incorrect.</td></tr>
<tr><td>25</td><td>RES</td><td>Reserved</td></tr>
<tr><td>24</td><td>NO_ACK</td><td>No ACK flag; When set, indicates to the PCU that it should not expect to receive (and should not wait for) an ACK for the frame. Must be set for any frame that has the 802.11 NoACK bit set in the QoS field. Also must be set for all other frame types (such as beacons and other broadcast/multicast frames) that do not receive ACKs.</td></tr>
<tr><td>23:20</td><td>FRAME_TYPE</td><td>Frame type indication; indicates what type of frame is being sent:
<table>
<tr><td>15:5</td><td>Reserved</td></tr>
<tr><td>4</td><td>Probe response</td></tr>
<tr><td>3</td><td>Beacon</td></tr>
<tr><td>2</td><td>PS-Poll</td></tr>
<tr><td>1</td><td>ATIM</td></tr>
<tr><td>0</td><td>Frame type, other than the types listed in [15:1]</td></tr>
</table></td></tr>
<tr><td>19:13</td><td>DEST_INDEX</td><td>Destination table index
Specifies an index into an on-chip table of per-destination information. The PCU fetches the encryption key from the specified index in this table and uses this key to encrypt the frame. The DMA logic uses the index to maintain per-destination transmit filtering status and other related information.</td></tr>
<tr><td>12</td><td>MORE</td><td>More descriptors in this frame flag
Set to one by the driver to indicate that there are additional descriptors (that is, DMA fragments) in the current frame. The last descriptor of a packet must have this bit set to 0. Note: This field must be valid for all descriptors.</td></tr>
<tr><td>11:9</td><td>PA</td><td>Pre-distortion chain mask</td></tr>
<tr><td>8:0</td><td>RES</td><td>Reserved</td></tr>
</table>

Table 4-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
13	31:28	TX_TRIES3	Number of frame data exchange attempts permitted for Tx series 3. A value of zero means skip this transmission series.
	27:24	TX_TRIES2	Number of frame data exchange attempts permitted for Tx series 2. A value of zero means skip this transmission series.
	23:20	TX_TRIES1	Number of frame data exchange attempts permitted for Tx series 1. A value of zero means skip this transmission series.
	19:16	TX_TRIES0	Number of frame data exchange attempts permitted for Tx series 0. A frame data exchange attempt means a transmission attempt in which the actual frame is sent on the air (in contrast to the case in which the frame has RTS enabled and the RTS fails to receive a CTS. In this case, the actual frame is not sent on the air, so this does not count as a frame data exchange attempt. Unlike TX_TRIES1...3, a value of zero is illegal for TX_TRIES0 field.
	15	DUR_ UPDATE_EN	Frame duration update control. If set, the MAC updates (overwrites) the duration field in the frame based on the current transmit rate. If clear, the MAC does not alter the contents of the frame duration field.
	14:0	BURST _DURATION	Burst duration value in usec. If this frame is not part of a burst or the last frame in a burst, this value should be zero. In a burst, this value is the amount of time to be reserved (via NAV) after the completion of the current transmit packet sequence (after the ACK if applicable).
14	31:24	TX_RATE3	Tx rate for transmission series 3; see Table 4-2 and Table 4-3
	23:16	TX_RATE2	Tx rate for transmission series 2; see Table 4-2 and Table 4-3
	15:8	TX_RATE1	Tx rate for transmission series 1; see Table 4-2 and Table 4-3
	7:0	TX_RATE0	Tx rate for transmission series 0; see Table 4-2 and Table 4-3

Table 4-2 MAC Rate Encodings

MAC Rate Encoding	Protocol
0x01	Reserved
0x02	
0x03	
0x06	
0x07	
0x8	OFDM_48Mb
0x9	OFDM_24Mb
0xA	OFDM_12Mb
0xB	OFDM_6Mb
0xC	OFDM_54Mb
0xD	OFDM_36Mb
0xE	OFDM_18Mb
0xF	OFDM_9Mb
0x18	CCK_11Mb_L
0x19	CCK_5_5Mb_L
0x1A	CCK_2Mb_L
0x1B	CCK_1Mb_L
0x1C	CCK_11Mb_S
0x1D	CCK_5_5Mb_S
0x1E	CCK_2Mb_S

Table 4-3 Tx Rates[1]

Rate	Desc	Stream	HT20; GI= 0 Mbps	HT20; GI = 1 Mbps	HT40; GI= 0 Mbps	HT40; GI= 1 Mbps
0x80	MCS 0	1	6.5	7.2	13.5	15
0x81	MCS 1	1	13	14.4	27	30
0x82	MCS 2	1	19.5	21.7	40.5	45
0x83	MCS 3	1	26	28.9	54	60
0x84	MCS 4	1	39	43.3	81	90
0x85	MCS 5	1	52	57.8	108	120
0x86	MCS 6	1	58.5	65.0	121.5	135
0x87	MCS 7	1	65	72.2	135	150
0x88	MCS 8	2	13	14.4	27	30
0x89	MCS 9	2	26	28.9	54	60
0x8A	MCS 10	2	39	43.3	81	90
0x8B	MCS 11	2	52	57.8	108	120
0x8C	MCS 12	2	78	86.7	162	180
0x8D	MCS 13	2	104	115.6	216	240
0x8E	MCS 14	2	117	130.0	243	270
0x8F	MCS 15	2	130	144.4	270	300

1. All rates not listed are reserved. Note that for short guard interval (GI=1), HT20 mode is allowed.

The Tx descriptor format for words 15 through 22 is described in Table 4-4.

Table 4-4 DMA Tx Descriptor Format for Words 15–22

Word	Bits	Name	Description	
15	31	RTS_CTS _QUAL1	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 1	
			1	Default behavior with respect to rts_enable and cts_enable
	30:16	PACKET _DURATION1	Packet duration 1 (in µs); Duration of the actual Tx frame associated with TXRate1. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	RTS_CTS _QUAL0	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 0	
			1	Default behavior with respect to rts_enable and cts_enable
	14:0	PACKET _DURATION0	Packet duration 0 (in µs); Duration of the actual Tx frame associated with TXRate0. This time does not include RTS, CTS, ACK, or any associated SIFS.	

Table 4-4 DMA Tx Descriptor Format for Words 15–22 (cont.)

Word	Bits	Name	Description	
16	31	RTS_CTS _QUAL3	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 3	
			1	Default behavior with respect to rts_enable and cts_enable
	30:16	PACKET _DURATION3	Packet duration 3 (in µs); Duration of the actual Tx frame associated with TXRate3. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	RTS_CTS _QUAL2	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 2	
			1	Default behavior with respect to rts_enable and cts_enable
	14:0	PACKET _DURATION2	Packet duration 2 (in µs); Duration of the actual Tx frame associated with TXRate2. This time does not include RTS, CTS, ACK, or any associated SIFS.	
17	31	RES	Reserved	
	30	CALIBRATING	Calibrating indication; causes the BB to apply the correct MCSD PPDU, which is used for radio calibration.	
	29	DC_AP _STA_SEL	Select for remaining the TBTT between TSF and TSF2, where 0 is from TSF and 1 is from TSF2. Should be used only when both ap_sta_enable and txop_tbtt_ limit_enable are enabled.	
	28:26	ENCRYPT_TYPE	Encryption type; DMA engine must add the number of necessary extra Dwords at the end of a packet to account for the encryption ICV generated by hardware. The encrypt type fields must be valid for all descriptors.	
			0	None; 0 pad bytes
			1	WEP or TKIP (no MIC); 4 pad bytes
			2	AES; 8 pad bytes
			3	TKIP; 12 pad bytes
			4	WAPI; 16 pad bytes
			7:5	Reserved
	25:18	PAD_DELIM	Pad delimiters; Between each packet of an A-MPDU aggregate the hardware will insert a start delimiter which includes the length of the next frame. Sometimes hardware on the transmitter or receiver requires some extra time between packets which can be satisfied by inserting zero length delimiters. This field indicates the number of extra zero length delimiters to add.	
	17:16	RES	Reserved	

	15:0	AGG_LENGTH	Aggregate (A-MPDU) length; the aggregate length is the number of bytes of the entire aggregate. This length should be computed as:
			`delimiters = start_delim + pad_delim;`
			`frame_pad = (frame_length % 4) ? (4 - (frame_ length % 4)) : 0`
			`agg_length = sum_of_all (frame_length + frame_pad + 4 * delimiters)`
			
			For the last packet of an aggregate the FRAME_PAD = 0 and delimiter= 0, frame_pad aligns to the next delimiter to be Dword aligned. Each delimiter is 4 bytes long. PAD_DELIM is the number of zero-length delimiters used to introduce an extra time gap between packets. START_DELIM is always 1 and includes the length of the next packet in the aggregate.	

Table 4-4 DMA Tx Descriptor Format for Words 15–22 (cont.)

Word	Bits	Name	Description	
18	31:28	STBC	STBC settings for all four series. If bit [0] is set, STBC is enabled for Tx series 0...3. Only supported for single stream rates, so only the lower bit is set.	
	27:20	RTS_CTS_RATE	RTS or self-CTS rate selection. Specifies the rate the RTS sends at if rts_enable is set, or self CTS sends at if cts_enable is set; see Table 4-3.	
	19:17	CHAIN_SEL_3	Chain select for Tx series 3. 1 and 3 are the only valid values.	
	16	GI_3	Guard interval control for Tx series 3	
			0	Normal guard interval
			1	Short guard interval
	15	20_40_3	20_40 control for Tx series 3	
			0	HT20 Tx packet
			1	HT40 Tx packet
	14:12	CHAIN_SEL_2	Chain select for Tx series 2. 1 and 3 are the only valid values.	
	11	GI_2	Guard interval control for Tx series 2	
	10	20_40_2	20_40 control for Tx series 2	
	9:7	CHAIN_SEL_1	Chain select for Tx series 1. 1 and 3 are the only valid values.	
	6	GI_1	Guard interval control for Tx series 1	
	5	20_40_1	20_40 control for Tx series 1	
	4:2	CHAIN_SEL_0	Chain select for Tx series 0. 1 and 3 are the only valid values.	
	1	GI_0	Guard interval control for Tx series 0	
	0	20_40_0	20_40 control for Tx series 0	

Table 4-4 DMA Tx Descriptor Format for Words 15–22 (cont.)

Word	Bits	Name	Description	
19	31:30	NESS_0	Number of Extension Spatial Streams (NESS) field of HT-SIG for Tx series 0. This setting is valid when the Tx rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29	NOT _SOUNDING	Not sounding HT-SIG field; sends sounding PPDU in explicit feedback as BF. If rts_enable is set to 1, this field affects RTS only, not the next data frame.	
			0	The PPDU is a sounding PPDU
			1	The PPDU is not a sounding PPDU
	28	RTS_HTC_TRQ	Sounding request of RTS frame; available when rts_enable is set to 1.	
			0	The responder is not requested to transmit a sounding PPDU
			1	Request the responder to transmit a sounding PPDU
	27	RTS_HTC_MRQ	MCS request of RTS frame; available when rts_enable is set to 1	
			0	No MCS feedback is requested
			1	MCS feedback is requested
	26:24	RTS_HTC_MSI	MCS Request Sequence Identifier (MSI) of RTS frame	
			0	Reserved
			1	Contains a sequence number (0–6) to identify the specific request
	23:0	ANTENNA_0	Antenna switch for Tx series 0	
20	31:30	NESS_1	NESS field of HT-SIG for Tx series 1. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_1	TPC for Tx series 1. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_1	Antenna switch for Tx series 1	
21	31:30	NESS_2	NESS field of HT-SIG for Tx series 2. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_2	TPC for Tx series 2. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_2	Antenna switch for Tx series 2	
22	31:30	NESS_3	NESS field of HT-SIG for Tx series 3. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_3	TPC for Tx series 3. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_3	Antenna switch for Tx series 3	

The Tx descriptor status format for words 0 through 8 is described in Table 4-5.

The words status is only considered valid when the done bit is set.

Table 4-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
0	31:16	ATHEROS_ID	The unique Qualcomm Atheros identifier of 0x168C is used to visually identify the start of the descriptor.
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.
	14	DESC_CTRL _STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 0 indicating status descriptor.
	13:12	RES	Reserved
	11:8	TX_QCU_NUM	Tx QCU number Indicates which QCU this descriptor is part of.
	7:0	DESC_LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x9 (9 Dwords).
1	31:16	TX_DESC_ID	Tx descriptor sequence number Software will select a unique sequence number associated with this descriptor. This value is copied to the tx_desc_id in the Tx status.
	15:0	RES	Reserved
2	31	RES	Reserved
	30	BA_STATUS	Block ACK status If set, this bit indicates that the BA_BITMAP values are valid.
	29:16	RES	Reserved
	15:8	ACK_RSSI_ ANT01	Rx ACK signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	7:0	ACK_RSSI_ ANT00	Rx ACK signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.

Table 4-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
3	31:20	RES	Reserved
	19	TX_TIMER _EXPIRED	Tx timer expired. This bit is set when the Tx frame is taking longer to send to the baseband than is allowed based on the TX_TIMER register. Some regulatory domains require that Tx packets may not exceed a certain amount of transmit time.
	18	RES	Reserved
	17	TX_DATA_ UNDERRUN_ERR	Tx data underrun error These error conditions occur on aggregate frames when the underrun condition happens while the MAC is sending the data portion of the frame or delimiters.
	16	TX_DELMTR _UNDERRUN_ ERR	Tx delimiter underrun error These error conditions occur on aggregate frames when the underrun conditions happens while the MAC is sending delimiters.
	15:12	VIRTUAL_ RETRY_CNT	Virtual collision count Reports the number of virtual collisions that occurred before transmission of the frame ended. The counter value saturates at 0xF. A virtual collision refers to the case, as described in the 802.11e QoS specification, in which two or more output queues are contending for a TXOP simultaneously. In such cases, all lower-priority output queues experience a virtual collision in which the frame is treated as if it had been sent on the air but failed to receive an ACK.
	11:8	DATA_FAIL_CNT	Data failure count Reports the number of times the actual frame (as opposed to the RTS) was sent but no ACK was received for the final transmission series (see the final_tx_index field).
	7:4	RTS_FAIL_CNT	RTS failure count Reports the number of times an RTS was sent but no CTS was received for the final transmission series (see the final_tx_index field). For frames that have the rts_enable bit clear, this count always will be zero. Note that this count is incremented only when the RTS/CTS exchange fails. In particular, this count is not incremented if the RTS/CTS exchange succeeds but the frame itself fails because no ACK was received.
	3	FILTERED	Frame transmission filter indication If set, indicates that the frame was not transmitted because the corresponding destination mask bit was set when the frame reached the PCU or if the frame violated TXOP on the first packet of a burst. Valid only if frm_xmit_ok is clear.
	2	FIFO_UNDERRUN	Tx FIFO underrun flag If set, transmission of the frame failed because the DMA engine was not able to supply the PCU with data as quickly as the baseband was requesting transmit data. Only valid for non-aggregate or non-RIFS underrun conditions unless the underrun occurred on the first packet of the aggregate or RIFS burst. See also the description for tx_delmtr_underrun_err and tx_data_underrun_err. Valid only if frm_xmit_ok is clear.
	1	EXCESSIVE _RETRIES	Excessive tries flag If set, transmission of the frame failed because the try limit was reached before the frame transmitted. Valid only if frm_xmit_ok is clear.
	0	frm_xmit_ok	Frame transmission success flag If set, the frame was transmitted successfully. If clear, no ACK or BA was received successfully.

Table 4-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
4	31:0	SEND _TIMESTAMP	Timestamp at start of transmit A snapshot of the lower 32 bits of the PCU timestamp (TSF value). This field can be used to aid the software driver in implementing requirements associated with the aMaxTransmitMSDULifetime MAC attribute. The transmit timestamp is sampled on the rising of tx_frame signal which goes from the MAC to the baseband. This value corresponds to the last attempt at packet transmission not the first attempt.
5	31:0	BA_BITMAP_0-31	Block ACK bitmap 0 to 31 These bits are the values from the block ACK received after the successful transmission of an aggregate frame. If set, bit [0] represents the successful reception of the packet with the sequence number matching the seq_num value.
6	31:0	BA_BITMAP_32-63	Block ACK bitmap 32 to 63 These bits are the values from the block ACK received after the successful transmission of an aggregate frame. If set, bit [32] represents the successful reception of the packet with the sequence number matching the seq_num value + 32.
7	31:24	ACK_RSSI _COMBINED	Rx ACK signal strength indicator of combination of all active chains on the control and extension channels. The value of 0x80 (–128) is used to indicate an invalid number.
	23:16	RES	Reserved
	15:8	ACK_RSSI_ANT11	Rx ACK signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	7:0	ACK_RSSI_ ANT10	Rx ACK signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.
8	31:28	TID	Traffic Identifier (TID) of block ACK Indicates the TID of the response block ACK. This field is only valid on the last descriptor of the last packet of an aggregate.
	27:26	RES	Reserved
	25	PWR_MGMT	Power management state Indicates the value of the PwrMgt bit in the frame control field of the response ACK frame.
	24:23	RES	Reserved
	22:21	final_tx_index	Final transmission attempt series index Specifies the number of the Tx series that caused frame transmission to terminate.
	20:18	RES	Reserved
	17	TXOP_ EXCEEDED	TXOP has been exceeded Indicates that this transmit frame had to be filtered because the amount of time to transmit this packet sequence would exceeded the TXOP limit. This should only occur when software programs the TXOP limit improperly.
	16:13	RES	Reserved

Table 4-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
8 (Cont.)	12:1	seq_num	The starting sequence number is the value of the Block ACK Starting Sequence Control field in the response Block ACK. Only consulted if the Tx frame was an aggregate.
	0	DONE	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid only for the final descriptor of a non-aggregate frame, regardless of the state of the FrTxOK flag. For an aggregate frame it is valid for only the final descriptor of the final packet of an aggregate. The driver is responsible for tracking what descriptors are associated with a frame. When the DMA engine sets the done flag in the final descriptor of a frame, the driver must be able to determine what other descriptors belong to the same frame and thus also have been consumed.

The DMA Rx logic (the DRU block) manages Rx descriptors and transfers the incoming frame data and status to the host through the PCIE Interface.

Words 0, and 2 are valid for all descriptors. Words 0, 2, and 11 is valid for the last descriptor of each packets. Words 0–11 are valid for the last descriptor of an aggregate or last descriptor of a stand-alone packet. Additional validity qualifiers are described individually. See Table 4-6.

Table 4-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description	
0	31:16	ATHEROS_ID	The unique Atheros identifier of 0x168C is used to visually identify the start of the descriptor.	
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.	
	14	DESC_CTRL_ STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 1 indicating status descriptor.	
	13:9	RES	Reserved	
	8	RX_PRIORITY	0	Low priority queue
			1	High priority queue
	7:0	DESC_LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x9 (9 Dwords).	
1	31:24	RX_RATE	Rx rate indication Indicates the rate at which this frame was transmitted from the source. Encodings match those used for the tx_rate*' field in word 5 of the Tx descriptor. Valid only if the frame_rx_ok flag is set or if the frame_rx_ok flag is clear and the phy_error flag is clear.	
	23:16	RES	Reserved	
	15:8	RSSI_ANT01	Received signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.	
	7:0	RSSI_ANT00	Received signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.	

Table 4-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description
2	31:23	RES	Reserved
	22	HW_UPLOAD _DATA	The upload data is valid only when the field hw_upload_data_valid at RXS 4 bit [7] is set. See RXS 11 bit [26:25] hw_upload_data_type to know which data type is uploaded. Valid for all descriptors.
	21:14	NUM_DELIM	Number of zero length pad delimiters after current packet This field does not include the start delimiter which is required between each packet in an aggregate. This field is only valid for aggregate packets except for the last packet of an aggregate.
	13	RES	Reserved
	12	MORE	More descriptors in this frame flag If set, then this is not the final descriptor of the frame. If clear, then this descriptor is the final one of the frame. Valid for all descriptors.
	11:0	DATA_LEN	Received data length Specifies the length, in bytes, of the data actually received into the data buffer associated with this descriptor. The actual received data length will be between zero and the total size of the data buffer, as specified originally in this field (see the description for the buf_len field). Valid for all descriptors. See “Data Buffer Length (DATABUF)” on page 149.
3	31:0	RCV _TIMESTAMP	A snapshot of the PCU timestamp (TSF value), expressed in µs (that is, bits [31:0] of the PCU 64-bit TSF). Intended for packet logging and packet sniffing. The timestamp is sampled on the rising edge of rx_clear, which goes from the baseband to the MAC.
4	31:8	RES	Reserved
	7	HW_UPLOAD _DATA_VALID	Specifies whether the contents of the hardware upload data are valid
	6:5	NESS	Receive packet NESS field Shows the number of Rx extension spatial steams.
	4	NOT _SOUNDING	Rx packet not sounding flag If this value is clear, then the Rx frame is a sounding PPDU. If this value is set, the receive frame is not a sounding PPDU.
	3	STBC	Rx packet STBC indicator If this value is set then the baseband has received an STBC frames as indicated in the HT_PLCP.
	2	DUPLICATE	Rx packet duplicate indicator If this value is set, the baseband has determined that this packet is a duplicate packet.
	1	20_40	Rx packet 20 or 40 MHz bandwidth indicator If this value is clear, then the receive frame was a HT20 packet (20 MHz bandwidth). If this value is set, then the receive frame was a HT40 packet (40 MHz bandwidth).
	0	GI	Rx packet guard interval If this value is clear, then the Rx frame used a long guard interval. If this value is set, the Rx frame used a short guard interval.

Table 4-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description
5	31:24	RX_COMBINED	Receive signal strength indicator of combination of all active chains on the control and extension channels. The value of 0x80 (–128) is used to indicate an invalid number.
	23:16	RES	Reserved
	15:8	RSSI_ANT11	Received signal strength indicator of extension channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	7:0	RSSI_ANT10	Received signal strength indicator of extension channel chain 0 A value of 0x80 (–128) indicates an invalid number.
6	31:0	EVM0	Rx packet error vector magnitude 0

Bits Mode	HT20 Mode	HT40 Mode	Diagnostic
evm0[31:24]	pilot1_str0	pilot1_str0	legacy_plcp_byte_1
evm0[23:16]	RES	RES	legacy_plcp_byte_2
evm0[15:8]	pilot0_str1	pilot0_str1	legacy_plcp_byte_3
evm0[7:0]	pilot0_str0	pilot0_str0	service_byte_1

7	31:0	EVM1	Rx packet error vector magnitude 1

Bits Mode	HT20 Mode	HT40 Mode	Diagnostic
evm1[31:24]	pilot2_str1	pilot2_str1	service_byte_2
evm1[23:16]	pilot2_str0	pilot2_str0	ht_plcp_byte_1
evm1[15:8]	RES	RES	ht_plcp_byte_2
evm1[7:0]	pilot1_str1	pilot1_str1	ht_plcp_byte_3

8	31:0	EVM2	Rx packet error vector magnitude 2

Bits Mode	HT20 Mode	HT40 Mode	Diagnostic
evm2[31:24]	RES	RES	service_byte_4
evm2[23:16]	pilot3_str1	pilot3_str1	ht_plcp_byte_5
evm2[15:8]	pilot3_str0	pilot3_str0	ht_plcp_byte_6
evm2[7:0]	RES	RES	0x0

9	31:0	EVM3	Rx packet error vector magnitude 3

Bits Mode	HT20 Mode	HT40 Mode	Diagnostic
evm3[31:24]	0x80	pilot5_str0	0x0
evm3[23:16]	0x80	RES	0x0
evm3[15:8]	0x80	pilot4_str1	0x0
evm3[7:0]	0x80	pilot4_str0	0x0

10	31:16	RES	Reserved
	15:0	EVM4	Rx packet error vector magnitude 4

Bits Mode	HT20 Mode	HT40 Mode	Diagnostic
evm4[15:8]	0x80	RES	0x0
evm4[7:0]	0x80	pilot4_str1	0x0

Table 4-6 DMA Rx Descriptor Format for Words 0–11

<table>
<tr><th>Word</th><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="13">11</td><td>31</td><td>KEY_MISS</td><td>Key cache miss indication
When set, indicates that the PCU could not locate a valid decryption key for the frame. Valid only if the frame_rx_ok flag is clear.</td></tr>
<tr><td>30</td><td>RES</td><td>Reserved</td></tr>
<tr><td>29</td><td>FIRST_AGG</td><td>First packet of aggregate
If set, indicates that this packet is the first packet of an aggregate.</td></tr>
<tr><td>28</td><td>HI_RX_CHAIN</td><td>If set indicates that the Rx chain control in high power mode.</td></tr>
<tr><td>27</td><td>RES</td><td>Reserved</td></tr>
<tr><td>26:25</td><td>HW_UPLOAD_
DATA_TYPE</td><td>Indicates the hardware upload data (H, V, or CV). The upload data is valid only when the field hw_upload_data_valid at RXS 4 bit [7] is set:
01 Upload is H
10 Upload is V
11 Upload is CV
Request report:
<table>
<tr><th>regs_config</th><th>Request CSI</th><th>Request V/CV</th></tr>
<tr><td>{0,0,x}</td><td>HW upload H</td><td>HW upload V/CV</td></tr>
<tr><td>{0,1,x}</td><td>HW upload H</td><td>HW upload H</td></tr>
</table>
If regs_config is {1,x,0}, it means hardware supports immediate response even if it does not need to respond to ACK. Hardware will upload H only when the request report is CSI.
If regs_config is {1,0,1}, it means HW support immediate response but hardware will upload H/V/CV base on request report for delay response if hardware does not need to respond to ACK.
Request Report:
<table>
<tr><th>regs_config</th><th>Request CSI</th><th>Request V/CV</th></tr>
<tr><td>{0,0,x}</td><td>HW upload H</td><td>HW upload V/CV</td></tr>
<tr><td>{0,1,x}</td><td>HW upload H</td><td>HW upload H</td></tr>
</table>
If regs_config is {1,1,1}, the hardware supports immediate response but hardware will only uploads H for a delay response if it does not need to respond to ACK.
For RTS, hardware only supports a delay response and will upload H, V, or CV to software.</td></tr>
<tr><td>24:19</td><td>RES</td><td>Reserved</td></tr>
<tr><td>18</td><td>POST_DELIM
_CRC_ERR</td><td>Delimiter CRC error is detected after this current frame
Only occurs when the start delimiter of the last frame in an aggregate is bad.</td></tr>
<tr><td>17</td><td>AGGREGATE</td><td>Aggregate flag
If set, indicates that this packet is part of an aggregate.</td></tr>
<tr><td>16</td><td>MORE_AGG</td><td>More aggregate flag
Set to 1 in all packets of an aggregate that have another packet of the current aggregate to follow. If clear, indicates that this packet is the last one of an aggregate.</td></tr>
</table>

Table 4-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description
11 (Cont.)	15:9	key_idx	If the FrRxOK bit is set, then this field contains the decryption key table index. If KEY_IDX_VALID is set, then this field specifies the index at which the PCU located the frame's destination address in its on-chip decryption key table. If key_idx_VALID is clear, the value of this field is undefined. If the FrRxOK bit is clear and the PHYErr bit is set, then this field contains bits [7:1] of the PHY error code.
	8	KEY_IDX_VALID	If frame_rx_ok is set, this field contains the decryption key table index valid flag. If set, indicates that the PCU successfully located the frame's source address in its on-chip key table and that the key_idx field reflects the table index at which the destination address was found. If clear, indicates that PCU failed to locate the destination address in the key table and that the contents of key_idx field are undefined. If the frame_rx_ok bit is clear and the phy_error bit is set, then this field contains bit [0] of the PHY error code.
	7	ASPD_TRIG	Received APSD trigger frame The received frame matched the profile of an APSD trigger frame.
	6	PRE_DELIM_CRC_ERR	Delimiter CRC error detected before this current frame. May indicate that an entire packet may have been lost.
	5	MIC_ERROR	Michael integrity check error flag If set, then the frame TKIP Michael integrity check value did not verify correctly. Valid only when all of the following are true: ■ frame_rx_ok bit is set ■ The frame was decrypted using TKIP key type ■ The frame is not a fragment
	4	PHY_ERROR	PHY error flag If set, then reception of the frame failed because the PHY encountered an error. In this case, bits [15:8] of this word indicate the specific type of PHY error; see the baseband specification for details. Valid only if the frame_rx_ok flag is clear.
	3	DECRYPT_CRC_ERR	Decryption CRC failure flag If set, reception of the frame failed because the frame was marked as encrypted but the PCU was unable to decrypt the frame properly because the CRC check failed after the decryption process completed. Valid only if the frame_rx_ok flag is clear.
	2	CRC_ERROR	CRC error flag If set, reception of the frame failed because the PCU detected an incorrect CRC value. Valid only if the frame_rx_ok flag is clear.
	1	FRAME_RX_OK	Frame reception success flag. If set, the frame was received successfully. If clear, an error occurred during frame reception.
	0	DONE	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid for all descriptors.

4.4 Queue Control Unit (QCU)

The queue control unit performs two tasks:

- Managing the Tx descriptor chain processing for frames pushed to the QCU from the CPU by traversing the linked list of Tx descriptors and transferring frame data from the host to the targeted DCU.
- Managing the queue transmission policy to determine when the frame at the head of the queue should be marked as available for transmission.

The MAC contains ten QCUs. Each QCU contains all the logic and state registers needed to manage a single queue (linked list) of Tx descriptors. A QCU is associated with exactly one DCU. When a QCU prepares a new frame, it signals ready to the DCU. When the DCU accepts the frame, the QCU responds by getting the frame data and passing it to the DCU for eventual transmission to the PCU and on to the air.

The host controls how the QCU performs these tasks by writing to various QCU configuration registers.

4.5 DCF Control Unit (DCU)

Collectively, the ten DCUs implement the EDCF channel access arbitration mechanism defined in the Task Group E (TGe) QoS extension to the 802.11 specification. Each DCU is associated with one of the eight EDCF priority levels and arbitrates with the other DCUs on behalf of all QCUs associated with it. A central DCU arbiter monitors the state of all DCUs and grants one the next access to the PCU (that is, access to the channel).

Because the EDCF standard defines eight priority levels, the first eight DCUs (DCUs 0–7) map directly to the eight EDCF priority levels. The two additional DCUs handle beacons and beacon-gated frames for a total of ten DCUs.

The mapping of physical DCUs to absolute channel access priorities is fixed and cannot be altered by software:

The highest-priority DCU is DCU 9. Typically, this DCU is the one associated with beacons.

The next highest priority DCU is DCU 8. Typically, this DCU is the one associated with beacon-gated frames.

The remaining eight DCUs priority levels are filled with DCUs 7 through 0. Among these 8 DCUs, DCU 7 has highest priority, DCU 6 the next highest priority, and so on through DCU 0, which has the lowest priority. Typically, these DCUs are associated with EDCF priorities seven through zero, respectively.

4.6 Protocol Control Unit (PCU)

The PCU is responsible for the details of sending a frame to the baseband logic for transmission, for receiving frames from the baseband logic and passing the frame data to the DRU, including:

- Buffering Tx and Rx frames
- Encrypting and decrypting
- Generating ACK, RTS, and CTS frames
- Maintaining the timing synchronization function (TSF)
- Forming aggregate

- Maintaining sequence state and generating Block ACK
- Inserting and verifying FCS
- Generating virtual clear channel assessment (CCA)
- Updating and parsing beacons
- The PCU is primarily responsible for buffering outgoing and incoming frames and conducting medium access compatible with the IEEE 802.11 DCF protocol

Figure 4-1 shows the PCU functional block diagram.

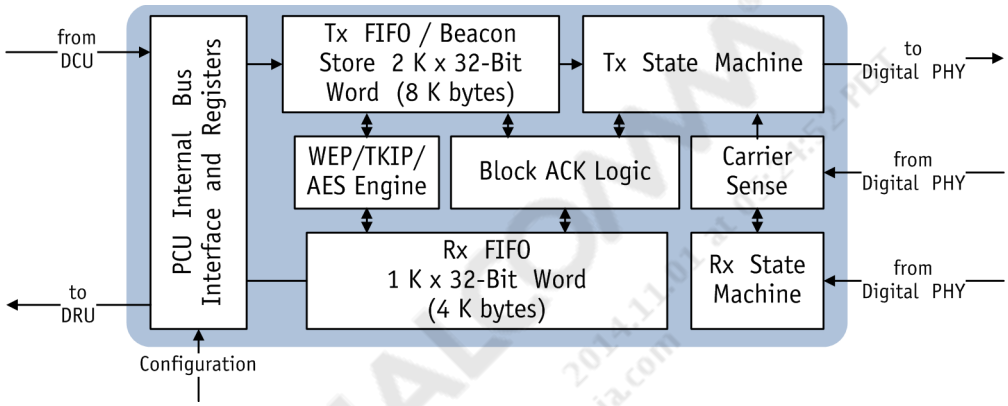


Figure 4-2 PCU Functional Block Diagram

4.7 Register Programming Details for Observing WMAC Interrupts

To configure the WMAC glue registers for observing WMAC interrupts:

1. Set bit [1] of these registers to observe MAC interrupts:
   - Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)
   - Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_SYNC_CAUSE)
   - Interface Timeout (WMAC_GLUE_INTF_TIMEOUT)
   - Asynchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_ ASYNC_ENABLE)
2. Write 0xFFFF_FFFF to the Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_ SYNC_CAUSE) register to clear any pending interrupts.
3. Set bit [0] of the Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS) register to enable MAC interrupts.
4. Enable primary MAC interrupts in the Primary Interrupt Mask (IMR_P) register (for example: bit [6] (TXOK), bit [1] (RXOK(LP)), and bit [0] (RXOK(HP)).
5. Enable secondary interrupts by writing to the IMR_S* registers: Secondary Interrupt Mask 0 (IMR_S0) through Secondary Interrupt Mask 5 (IMR_S5).
6. Read bits [3:0] of the register PCIE WMAC Interrupt Status (RST_PCIE _WMAC_ INTERRUPT_STATUS):

- Bit [0] = 1: Indicates a WMAC interrupt
- Bit [0] = 1, bit [1] = 1: Indicates a WMAC Tx interrupt
- Bit [0] = 1, bit [2] = 1: Indicates a WMAC Rx LP interrupt
- Bit [0] = 1, bit [3] = 1: Indicates a WMAC Rx HP interrupt

7. Read the Primary Interrupt Status (ISR_P) register to find the exact interrupt. Clear the interrupt by writing 1 to corresponding bit.

5 Digital PHY Block

The digital physical layer (PHY) block is described in 802.11n mode and 802.11 b/g legacy mode. Transmit and receive paths are provided and shown as block diagrams for 802.11n mode.

5.1 Overview

The digital PHY block is a half-duplex, OFDM, CCK, DSSS baseband processor compatible with IEEE 802.11n and 802.11b/g. The QCA9531 supports both 20- and 40-MHz channel modes and data rates up to 300 Mbps defined by the IEEE 802.11b/g/n standards. Modulation schemes include BPSK, QPSK, 16-QAM, 64-QAM and forward error correction coding with rates of 1/2, 2/3, 3/4, 5/6.

Two 802.11n advanced features, Space Time Block Code (STBC) and Low-Density Parity Check (LDPC) are supported in the QCA9531 chip. In addition, many new performance enhancing features are included, such as maximum likelihood (ML) MIMO receiver, and maximum ratio combining (MRC) for OFDM and 802.11b packet detection.

5.2 802.11n (MIMO) Mode

Frames beginning with training symbols are used for signal detection, automatic gain control, frequency offset estimation, symbol timing, and channel estimation. This process uses 56 sub-carriers for 20-MHz HT mode: 52 for data transmission and 4 for pilots. It uses 114 sub-carriers for 40-MHz HT mode: 108 for data transmission and 6 for pilots.

5.2.1 Transmitter (Tx)

Figure 5-1 shows the Tx path digital PHY 802.11n (MIMO mode) block diagram.

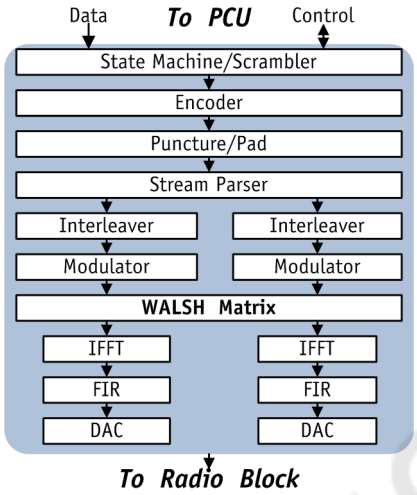


Figure 5-1 Digital PHY 802.11n Tx

The PCU block initiates transmission. The digital PHY powers on the digital to analog converter (DAC) and transmit the training symbol. The training symbols are a fixed waveform and are generated within the digital PHY in parallel with the PCU sending the Tx header (frame length, data rate, etc.). The PCU must send transmitted data quickly enough to prevent buffers in the digital PHY from becoming empty. The PCU is prevented from sending data too quickly by pauses generated within the digital PHY.

Figure 5-1 shows a 2x2 MIMO system with three spatial data streams. The spatial parser splits the coded data into multiple data streams by allocating the proper number of bits to each data stream so that the number of data symbols resulted in each stream is the same. Then it interleaves coded bits across different data subcarriers followed by the modulation. To achieve the maximum spatial diversity for one-stream and two-stream transmission, the Walsh matrix orthogonally spreads the modulated stream(s) into three Tx antennas before undergoing IFFT processing to produce time domain signals.

5.2.2 Receiver (Rx)

Figure 5-2 shows the Rx path digital PHY 802.11n (MIMO mode) block diagram.

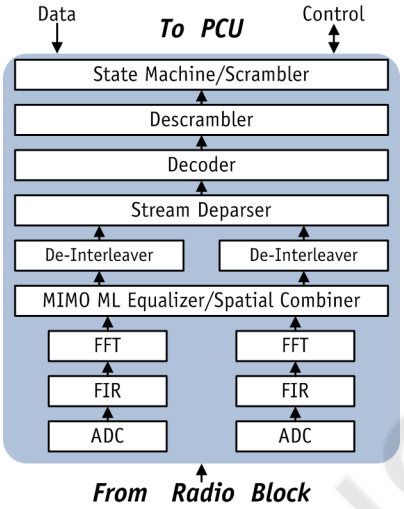


Figure 5-2 Digital PHY 802.11n Rx

The receiver inverts the transmitter's steps, performing a fast Fourier transform (FFT), extracting bits from received constellations, de-interleaving, accounting for puncturing, decoding, and descrambling. The Rx block shows 2x2 MIMO configuration. Figure 5-2 shows a frequency-domain Maximum Likelihood (ML) equalizer handling degradation due to multi-path.

5.3 802.11 b/g Legacy Mode

5.3.1 Transmitter

The QCA9531 digital PHY incorporates an OFDM and DSSS transceiver that supports all data rates defined by IEEE 802.11b/g. Legacy mode is detected on per-frame basis. PLCP frames are detected for legacy network information. The transmitter switches dynamically to generate legacy signals (802.11 b/g in 2.4 GHz).

5.3.2 Receiver

The receiver is capable of dynamically detecting legacy, HT 20 MHz or 40 MHz frames and will demodulate the frame according to the detected frame type. Maximum ratio combining (MRC) is used for OFDM and 802.11b packet detection.

6 Radio Block

The transceiver of the QCA9531 solution consists of these major functional blocks:

- 2 x Receive chain

  Each chain = Radio + BB programmable gain filter
- 2 x Transmit chain

  Each chain = Radio + BB programmable gain filter
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)

See Figure 6-1.

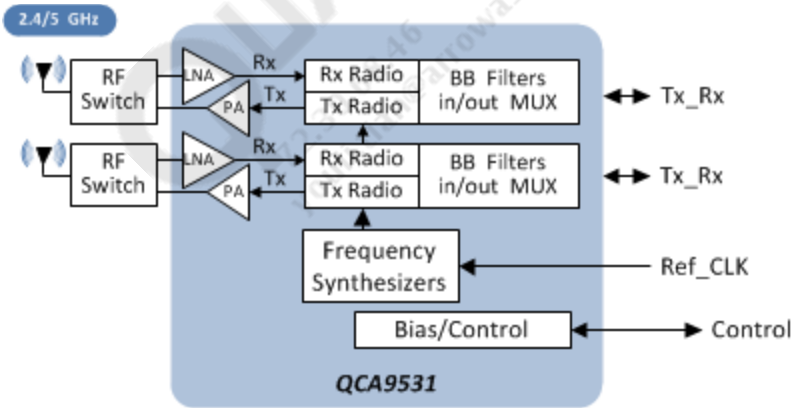


Figure 6-1 Radio Functional Block Diagram

6.1 Receiver (Rx) Block

The receiver converts an RF signal (with a 20 MHz or 40 MHz band) to baseband I and Q outputs. The dual band receiver operates in the 2.4 GHz band to support CCK and OFDM signals for 802.11b, 802.11g, and 802.11n.

The 2.4 GHz receiver implements a direct-conversion architecture and consists of a low noise amplifier (LNA), a pair of quadrature radio frequency (RF) mixers, and in-phase (I) and quadrature (Q) baseband programmable gain filter/amplifiers (PGA). The mixers convert the output of the on-chip LNA to baseband I and Q signals. The I and Q signals are low-pass filtered and amplified by a baseband programmable gain filter controlled by digital logic. The baseband signals are sent to the ADC within the MAC/Baseband processor.

The DC offset of the receive chain is reduced using multiple DACs controlled by the MAC/ Baseband processor. Additionally, the receive chain can be digitally powered down to conserve power.

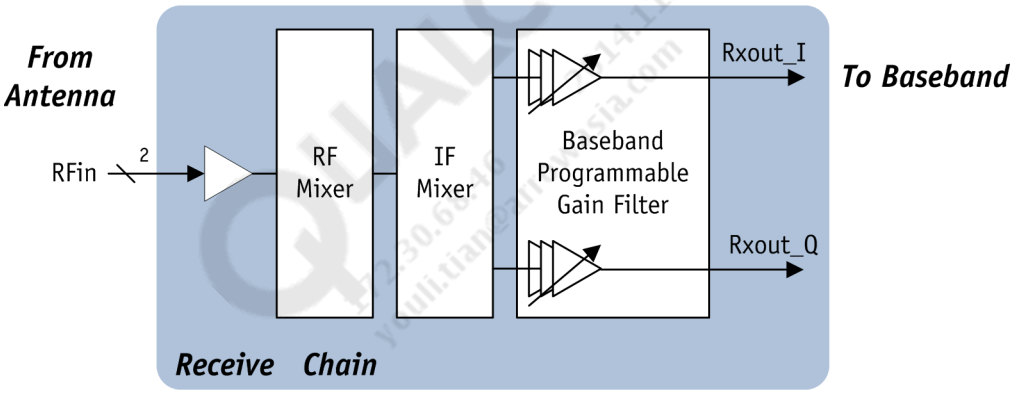


Figure 6-2 Radio Receive Chain Block Diagram

6.2 Transmitter (Tx) Block

The transmitter converts baseband I and Q inputs to 2.4 GHz RF outputs as shown in Figure 6-3. The inputs to the transmitter are current outputs of the I and Q DAC within the MAC/Baseband processor. These currents are low-pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise.

The I and Q signals are converted to RF signals using an integrated up-conversion architecture.

For 2.4 GHz transmitter, the baseband I and Q signals are up-converted directly to RF using a pair of quadrature mixers. The up-converted RF signals are driven off-chip through a power amplifier.

The transmit chain can be digitally powered down to conserve power. To ensure that the FCC limits are observed and the output power stays close to the maximum allowed, the transmit output power is adjusted by a digitally programmed control loop at the start of each packet. The QCA9531 provides an open loop power control based on an on-chip temperature sensor.

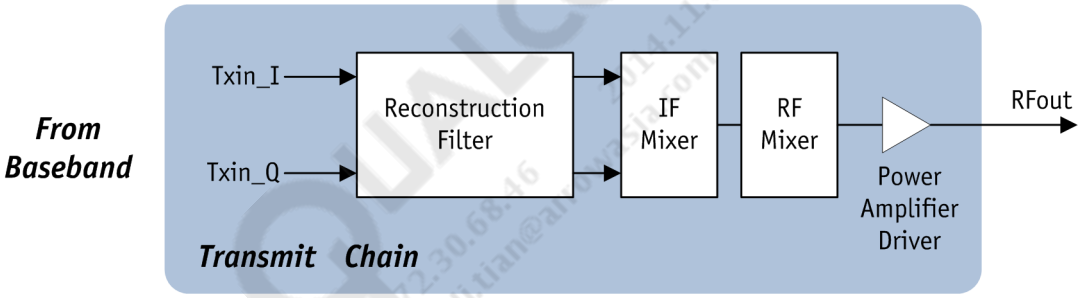


Figure 6-3 Radio Transmit Chain Block Diagram

6.3 Synthesizer (SYNTH) Block

The radio supports an on-chip synthesizer to generate local oscillator (LO) frequencies for the receiver and transmitter mixers. The synthesizer has the topology shown in Figure 6-4. The QCA9531 generates the reference input from a 40 MHz crystal for the synthesizer. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase locked loop.

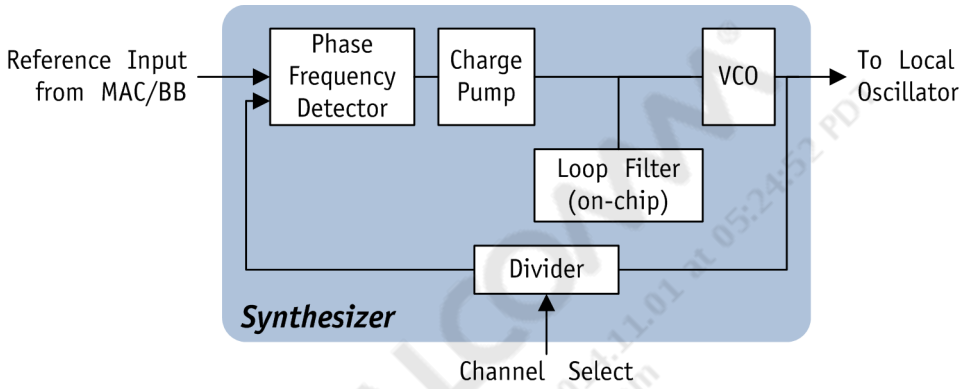


Figure 6-4 Radio Synthesizer Block Diagram

6.4 Bias/Control (BIAS) Block

The bias/control block provides the reference voltages and currents for all other circuit blocks (see Figure 6-5). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 KΩ ±1% resistor.

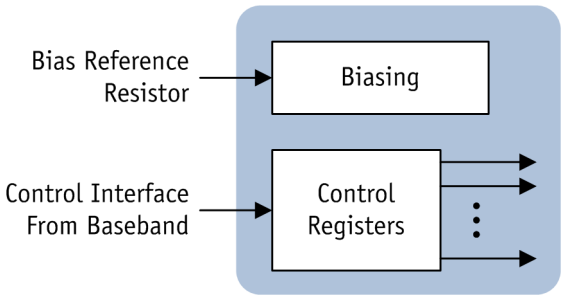


Figure 6-5 Bias/Control Block Diagram

7 Register Descriptions

These sections describe the internal registers for the various QCA9531 blocks.

Table 7-1 summarizes the CPU mapped registers for the QCA9531.

Table 7-1 CPU Mapped Registers Summary

Address	Description	Page
0x18000000–0x18000128	DDR Registers	page 82
0x18020000–0x18020018	UART0 (Low-Speed) Registers	page 96
0x18030000–0x1803000C	USB Registers	page 105
0x18040000–0x1804006C	GPIO Registers	page 106
0x18050000–0x18050048	PLL Control Registers	page 113
0x18060000–0x180600AC	Reset Control Registers	page 121
0x18070000	GMAC Interface Registers	page 130
0x180F0000 - 0x180F005C	PCIE RC Control Registers	page 131
0x18100008–0x1810012C	WDMA Registers	page 143
0x18100800–0x18100A44	WQCU Registers	page 162
0x18101000–0x18101F04	WLAN DCU Registers	page 169
0x18104000–0x181040F0	WMAC Glue Registers	page 178
0x18107000–0x18107058	RTC Registers	page 186
0x18108000–0x18108800	WPCU Registers	page 196
0x18116C40-0x18116C44	PMU Registers	page 301
0x18116180-0x181161C8	PLL SRIF Registers	page 237
0x19000000–0x190002E8	GMAC0/GMAC1 Registers	page 252
0x1F000000–0x1F000018	Serial Flash SPI Registers	page 298
Ethernet Switch Registers:		
0x0000-0x00B8	Global Control Registers	page 302
0x00-0x1E	PHY Control Registers	page 332
0x0B-0x3C	Debug Port Registers	page 345
0x00-0x16	MMD3 PCS Registers	page 349
0x00-0x8000	MMD7 Auto-Negotiation Registers	page 351

7.1 DDR Registers

Table 7-1 summarizes the DDR registers for the QCA9531.

NOTE The memory controller core clock is twice the frequency of the DDR_CK_P clock.

Table 7-2 DDR Registers Summary

Address	Name	Description	Page
0x18000000	DDR_CONFIG	DDR DRAM Configuration	page 83
0x18000004	DDR_CONFIG2	DDR DRAM Configuration 2	page 84
0x18000008	DDR_MODE	DDR Mode Value	page 85
0x1800000C	DDR_EXTENDED_MODE_REGISTER	DDR Extended Mode Value	page 85
0x18000010	DDR_CONTROL	DDR Control	page 85
0x18000014	DDR_REFRESH	DDR Refresh Control and Configuration	page 86
0x18000018	DDR_RD_DATA_THIS_CYCLE	DDR Read Data Capture Bit Mask	page 86
0x1800001C	TAP_CONTROL_0	DQS Delay Tap Control for Byte 0	page 86
0x18000020	TAP_CONTROL_1	DQS Delay Tap Control for Byte 1	page 87
0x1800009C	DDR_WB_FLUSH_GE0	GE0 Interface Write Buffer Flush	page 87
0x180000A0	DDR_WB_FLUSH_GE1	GE1 Interface Write Buffer Flush	page 87
0x180000A4	DDR_WB_FLUSH_USB	USB Interface Write Buffer Flush	page 88
0x180000A8	DDR_WB_FLUSH_PCIE	PCIE Interface Write Buffer Flush	page 88
0x180000AC	DDR_WB_FLUSH_WMAC	WMAC Interface Write Buffer Flush	page 88
0x180000B8	DDR_DDR2_CONFIG	DDR2 Configuration	page 89
0x180000BC	DDR_EMR2	DDR Extended Mode 2 Value	page 89
0x180000C0	DDR_EMR3	DDR Extended Mode 3 Value	page 89
0x180000C4	DDR_BURST	DDR bank arbiter per client burst size 1	page 90
0x180000C8	DDR_BURST2	DDR bank arbiter per client burst size 2	page 90
0x180000CC	AHB_MASTER_TIMEOUT_MAX	AHB Master Timeout Control	page 91
0x180000D0	AHB_MASTER_TIMEOUT_CURNT	AHB Timeout Current Count	page 91
0x180000D4	AHB_MASTER_TIMEOUT_SLAVE_ADDR	Timeout Slave Address	page 91
0x18000108	DDR_CTL_CONFIG	DDR Control Configuration	page 92
0x18000110	DDR_SF_CTL	DDR Self Refresh	page 93
0x18000114	SF_TIMER	DDR Self Refresh Timer	page 94
0x18000128	WMAC_FLUSH	WMAC Flush	page 94
0x1800015C	DDR3_CONFIG	DDR3 Configuration	page 95

7.1.1 DDR DRAM Configuration (DDR_CONFIG)

Address: 0x18000000
Access: Read/Write
Reset: See field description

This register is used to configure the DDR DRAM parameters.

Bit	Bit Name	Reset	Description
31	CAS_LATENCY_MSB	0x0	DRAM CAS latency parameter MSB rounded up in memory core clock cycles
30	RES	0x1	Reserved
29:27	CAS_LATENCY	0x6	DRAM CAS latency parameter (first 3 bits) rounded up in memory core clock cycles. CAS_LATENCY is used by the hardware to estimate the internal DDR clock latency of a read. It should be greater than or equal to GATE_OPEN_ LATENCY as specified in the DDR_CONFIG2 register. The value of this register should be memory cas_latency * 2 or cas_latency * 2+1/2/3.
26:23	TMRD	0xF	DRAM tMRD parameter rounded up in memory core clock cycles
22:17	TRFC	0x1F	DRAM tRFC parameter rounded up in memory core clock cycles
16:13	TRRD	0x4	DRAM tRRD parameter rounded up in memory core clock cycles
12:9	TRP	0x6	DRAM tRP parameter rounded up in memory core clock cycles
8:5	TRCD	0x6	DRAM tRCD parameter rounded up in memory core clock cycles
4:0	TRAS	0x10	DRAM tRAS parameter rounded up in memory core clock cycles

7.1.2 DDR DRAM Configuration 2 (DDR_CONFIG2)

Address: 0x18000004
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31	HALF_WIDTH_LOW	—	This bit controls which part of the 32 bit DDR DQ bus is populated with DRAM in a 16 bit wide memory system.	
			0	31:16
			1	15:0
30	SWAP_A26_A27	0x0	This bit gives a choice to drive CPU address A26 and A27 on different column lines. This is needed to support different combinations of devices on board.	
			0	Drives CPU_ADDR[26] on A11 of COL if DDR_CONFIG_HALF_WIDTH==1 or on A9 of COL if DDR_CONFIG_HALF_WIDTH==0. In this case, CPU_ADDR[27] will be driven on A12 of COL if DDR_CONFIG_HALF_WIDTH==1 and A11 of COL if DDR_CONFIG_HALF_WIDTH==0.
			1	Drives CPU_ADDR[27] on A11 of COL if DDR_CONFIG_HALF_WIDTH==1 or on A9 of COL if DDR_CONFIG_HALF_WIDTH==0. In this case, CPU_ADDR[26] will be driven on A12 of COL if DDR_CONFIG_HALF_WIDTH==1 and A11 of COL if DDR_CONFIG_HALF_WIDTH==0.
29:26	GATE_OPEN_LATENCY	0x6	DRAM gate open latency parameter rounded up in memory core clock cycles	
25:21	TWTR	0xE	DRAM tWTR parameter rounded up in memory core clock cycles	
20:17	TRTP	0x8	DRAM read to precharge parameter rounded up in memory core clock cycles. The normal value is two clock cycles.	
16:12	TRTW	0x10	DRAM tRTW parameter rounded up in memory core clock cycles. The value should be calculated as CAS LATENCY + BURST LENGTH + BUS TURN AROUND TIME.	
11:8	TWR	0x6	DRAM tWR parameter rounded up in memory core clock cycles	
7	CKE	0x1	DRAM CKE bit	
6	PHASE_SELECT	0x0	Selects the output phase	
5	CNTL_OE_EN	0x1	Control bit to allow the memory controller to tri-state the address/control outputs	
4	BURST_TYPE	0x0	DRAM burst type	
			0	Sequential
			1	Interleaved
3:0	BURST_LENGTH	0x8	DRAM burst length setting. Only 8 is supported.	

7.1.3 DDR Mode Value (DDR_MODE_REGISTER)

Address: 0x18000008
Access: Read/Write
Reset: See field description

This register is used to set the DDR mode register value.

Bit	Bit Name	Reset	Description
31:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	0x133	Mode register value. Reset to CAS 3, BL=8, sequential, DLL reset off.

7.1.4 DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER)

Address: 0x1800000C
Access: Read/Write
Reset: See field description

This register is used to set the extended DDR mode register value.

Bit	Bit Name	Reset	Description
31:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	0x2	Extended mode register value. Reset to weak driver, DLL on.

7.1.5 DDR Control (DDR_CONTROL)

Address: 0x18000010
Access: Read/Write
Reset: 0x0

This register is used to force update cycles in the DDR control.

Bit	Bit Name	Description
31:6	RES	Reserved
5	EMR3S	Forces an EMR3 update cycle
4	EMR2S	Forces an EMR2 update cycle
3	PREA	Forces a PRECHARGE ALL cycle
2	REF	Forces an AUTO REFRESH cycle
1	EMRS	Forces an EMRS update cycle
0	MRS	Forces an MRS update cycle

7.1.6 DDR Refresh Control and Configuration (DDR_REFRESH)

Address: 0x18000014
Access: Read/Write
Reset: See field description

This register is used to configure the settings to refresh the DDR.

Bit	Bit Name	Reset	Description
31:15	RES	0x0	Reserved
14	ENABLE	0x0	Setting this bit to one will enable a DDR refresh
13:0	PERIOD	0x12C	Sets the refresh period intervals with respect to the ref clock (25 MHz)

7.1.7 DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE)

Address: 0x18000018
Access: Read/Write
Reset: See field description

This register is used to set the parameters to read the DDR and capture bit masks.

Bit	Bit Name	Reset	Description
31:0	VEC	0xFF	DDR read and capture bit mask. Each bit represents a cycle of valid data. Set to 0xFFFF for 16-bit DDR memory systems.

7.1.8 DQS Delay Tap Control for Byte 0 (TAP_CONTROL_0)

Address: 0x1800001C
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 0, DQ[7:0], DQS_0.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this lane. There are a total of 64 taps available, which may be set using these six bits.

7.1.9 DQS Delay Tap Control for Byte 1 (TAP_CONTROL_1)

Address: 0x18000020
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 1, DQ[15:8], DQS_1.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this lane. There are a total of 64 taps available, which may be set using these six bits.

7.1.10 GE0 Interface Write Buffer Flush (DDR_WB_FLUSH_GE0)

Address: 0x1800009C
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the GE0 interface.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	Set this bit to 1 to flush the write buffer for the GE0 interface. This bit will reset to 0 when the flush is complete.

7.1.11 GE1 Interface Write Buffer Flush (DDR_WB_FLUSH_GE1)

Address: 0x180000A0
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the GE1 interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the GE1 interface. This bit will reset to 0 when the flush is complete.

7.1.12 USB Interface Write Buffer Flush (DDR_WB_FLUSH_USB)

Address: 0x180000A4
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the USB interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the USB interface. This bit will reset to 0 when the flush is complete.

7.1.13 PCIE Interface Write Buffer Flush (DDR_WB_FLUSH_PCIE)

Address: 0x180000A8
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the USB interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the PCIE interface. This bit will reset to 0 when the flush is complete.

7.1.14 WMAC Interface Write Buffer Flush (DDR_WB_FLUSH_WMAC)

Address: 0x180000AC
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the WMAC interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the WMAC interface. This bit will reset to 0 when the flush is complete.

7.1.15 DDR2 Configuration (DDR_DDR2_CONFIG)

Address: 0x180000B8
Access: Read/Write
Reset: 0x0858

Bit	Bit Name	Type	RW	Description	
31:14	RES	RO	0x0	Reserved	
13:10	DDR2_TWL	RW	0x1	Delays driving the data signals for writing commands with respect to command issue by TWL DDR clocks	
9	DDR2_ODT	RW	0x1	This DDR2 setting enables a High output n the ODT signal	
8	RES	RO	0x0	Reserved	
7:2	DDR2_TFAW	RW	0x16	tFAW parameter in core DDR_CLK cycles	
1	RES	RW	0x0	Reserved	
0	ENABLE_DDR2	RW	0x0	0	DDR1
				1	DDR2

7.1.16 DDR EMR2 (DDR_EMR2)

Address: 0x180000BC
Access: Read/Write
Reset: 0x0

This register is used set the extended mode register 2 value.

Bit	Bit Name	Type	Reset	Description
31:14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	RW	0x0	Extended mode register 2 value, reset to weak driver, DLL on

7.1.17 DDR EMR3 (DDR_EMR3)

Address: 0x180000C0
Access: Read/Write
Reset: 0x0

This register is used set the extended mode register 3 value.

Bit	Bit Name	Type	Reset	Description
31:14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	RW	0x0	Extended mode register 3 value, reset to weak driver, DLL on

7.1.18 DDR Bank Arbiter Per Client Burst Size (DDR_BURST)

Address: 0x180000C4
Access: Read/Write
Reset: See field description

NOTE Changes to this register is not recommended.

Bit	Bit Name	Reset	Description
31	CPU_PRIORITY	0x0	Setting this bit causes the bank arbiters to break current burst and grant CPU
30	CPU_PRIORITY_BE	0x1	Setting this bit causes the bank arbiters to break only at current burst completion and grant CPU
29:28	ENABLE_RWP_MASK	0x3	Enables the Read/Write mask and the Precharge Mask
27:24	MAX_WRITE_BURST	0x0	Max Write Burst size. Reads are masked in the BANK_ARB.
23:20	MAX_READ_BURST	0x4	Max Read Burst size. Writes are masked in the BANK_ARB.
19:16	CPU_MAX_BL	0x0	CPU burst size
15:12	USB_MAX_BL	0x1	USB burst size
11:8	PCIE_MAX_BL	0x3	PCIE burst size
7:4	GE1_MAX_BL	0x4	GE1 burst size
3:0	GE0_MAX_BL	0x4	Ethernet burst size

7.1.19 DDR Bank Arbiter Per Client Burst Size 2 (DDR_BURST2)

Address: 0x180000C8
Access: Read/Write
Reset: See field description

NOTE Changes to this register is not recommended.

Bit	Bit Name	Reset	Description
31:4	RES	0x0	Reserved
3:0	WMAC_MAX_BL	0x2	WNAC burst size

7.1.20 DDR AHB Master Timeout Control (DDR_AHB_MASTER_TIMEOUT_MAX)

Address: 0x180000CC
Access: Read/Write
Reset: 0x0

This register specifies the maximum timeout value of the AHB master control.

Bit	Bit Name	Type	Reset	Description
31:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19:0	VALUE	RW	0x8000	Maximum time out value

7.1.21 DDR AHB Timeout Current Count (DDR_AHB_MASTER_TIMEOUT_CURNT)

Address: 0x180000D0
Access: Read/Write
Reset: 0x0

This register specifies the current AHB timeout value.

Bit	Bit Name	Type	Reset	Description
31:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19:0	VALUE	RO	0x0	Current time out value

7.1.22 Timeout Slave Address (AHB_MASTER_TIMEOUT_SLV_ADDR)

Address: 0x180000D4
Access: Read/Write
Reset: 0x0

This register specifies the maximum timeout value to access the slave address space.

Bit	Bit Name	Type	Reset	Description
31:0	ADDR	RO	0x0	Maximum time out value

7.1.23 DDR Controller Configuration (DDR_CTL_CONFIG)

Address: 0x18000108
Access: Read/Write
Reset: 0x0

This register specifies the control bits for the DDR.

Bit	Bit Name	Type	Reset	Description
31:30	SRAM_TSEL	RW	0x1	Determines the TSEL value of the SRAM memory
29:21	CLIENT_ACTIVITY	RO	0x0	Indicates if there is currently any activity in each of the AHB/AXI/OCP clients connected to the DDR
20	GE0_SRAM_SYNC	RW	0x1	This bit is used to make sure that GE0 launches a SRAM write request only if all pending DDR write requests of GE0 have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before GE0 updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.
				0 Disabled
				1 Enabled
19	GE1_SRAM_SYNC	RW	0x1	This bit is used to make sure that GE1 launches a SRAM write request only if all pending DDR write requests of GE1 have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before GE1 updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.
				0 Disabled
				1 Enabled
18	USB_SRAM_SYNC	RW	0x1	This bit is used to make sure that USB launches a SRAM write request only if all pending DDR write requests of USB have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before GE1 updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.
				0 Disabled
				1 Enabled
17	PCIE_SRAM_SYNC	RW	0x1	This bit is used to make sure that PCIE launches a SRAM write request only if all pending DDR write requests of PCIE have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before PCIE updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.
				0 Disabled
				1 Enabled

16	WMAC_SRAM_ SYNC	RW	0x1	This bit is used to make sure that WMAC launches a SRAM write request only if all pending DDR write requests of WMAC have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before WMAC updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.	
				0	Disabled
				1	Enabled
15:14	RES	R	0x0	Reserved	
6	PAD_DDR2_SEL	RW	0x0	Controls the SEL_18 of the DDR_PADS.	
				0	DDR1 mode
				1	DDR2 mode
5	RES	R	0x0	Reserved	
4	GATE_SRAM_CLK	RW	0x0	SRAM gating enable	
				0	SRAM not gated
				1	SRAM gated
3	SRAM_REQ_ACK	RW	0x0	This bit is needed to make sure that two back-to-back requests from a AHB/AXI adapter are recognized as two requests in the CPU domain when the CPU is running at a slower clock compared to AHB_CLK. The synchronized request in CPU domain has to become 0 and get checked by the logic in AHB/AXI if it has become 0. Only then the adapter can launch the second request. Set this bit to 1 if the CPU_ CLK is slower than the AHB_CLK. Otherwise, there is no issue of back-to-back req synchronization.	
2	CPU_DDR_SYNC	RW	0x0	Set to 1 if the CPU and DDR clocks are needed to operate synchronously. By default, CPU and DDR clocks are asynchronous to each other.	
1	HALF_WIDTH	RW	0x1	Set to one for x16 DDR configurations	
0	RES	R	0x0	Reserved	

7.1.24 DDR Self Refresh Control (DDR_SF_CTL)

Address: 0x18000110
Access: Read/Write
Reset: 0x0

This register specifies the settings for the DDR self refresh mode.

Bit	Bit Name	Type	Reset	Description
31	EN_SELF_REFRESH	RW	0x0	Setting this bit will initiate entering self refresh mode. This bit can be cleared by S/W or H/W if the auto exit is enabled
30	EN_AUTO_SF_EXIT	RW	0x0	Setting this bit will initiate exiting self refresh mode upon request from any AHB/AXI master
29	CUR_SR_STATE	RO	0x0	Indicates if the DDR is currently in self refresh mode
28	CUR_CKE_STATE	RO	0x0	Indicates if the DDR CKE is high or low

27	EN_SF_CLK_ GATING	RW	0x0	Setting this bit gates CK_P and CK_N during self refresh mode
26:25	CKE_GATE_DLY_ SEL	RW	0x0	Determines the delay of the CKE assertion from CK_P and stops gating when exiting self refresh mode
24:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:18	NO_ACTIVITY_ CNTR	RO	0x0	Indicates the duration on no activity in the AHB/AXI clients of the DDR in terms of the DDR refresh period
17:8	TXSRD	RW	0x1C2	Indicates XSND parameter of the memory in the number of DDR_ CLKs
7:0	TXSNR	RW	0x3C	Indicates XSNR parameter of the memory in the number of DDR_ CLKs

7.1.25 Self Refresh Timer (SF_TIMER)

Address: 0x18000114
Access: Read/Write
Reset: 0x0

This register specifies the DDR refresh periods for self refresh mode.

Bit	Bit Name	Type	Reset	Description
31:16	RF_OUT_DPR_ COUNT	RO	0x0	Indicates the number of DDR_REFRESH_PERIODs for which HW remained out of the self refresh mode
15:0	IN_RF_DPR_ COUNT	RO	0x0	Indicates the number of DDR_REFRESH_PERIODs for which HW remained in self refresh mode

7.1.26 WMAC Flush (WMAC_FLUSH)

Address: 0x18000128
Access: Read/Write
Reset: 0x0

This register specifies the settings for the WMAC Flush.

Bit	Bit Name	Type	Reset	Description
31:10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
9	DONE	RW	0x0	Set to 1 by HW after the flush is completed and the adapter is ready. SW clears it back to 0.
8:1	DDR_CLK_ CNTR	RW	0x28	Number of DDR clocks to count down after the last grant, ensuring all I/O reads are completed.
0	FORCE	RW	0x0	Set to 1 by software to start the AXI FLUSH. Hardware clears this field to 0.

7.1.27 DDR3 Configuration Register (DDR3_CONFIG)

Address: 0x1800015C
Access: Read/Write
Reset: 0x0

This register holds the configuration parameters for DDR timing.

Bit	Bit Name	Reset	Description
31:4	SPARE	0x0	Spare bits
3	TWR_MSB	0x0	MSB of TWR timing parameters expressed as an internal DDR clock
2	TRAS_MSB	0x0	MSB of TRAS timing parameters expressed as an internal DDR clock
1:0	TRFC_LSB	0x0	TRFC timing parameter. LSB two bits; in terms of the internal DDR clock.

7.2 UART0 (Low-Speed) Registers

Table 7-3 summarizes the UART0 registers for the QCA9531.

Table 7-3 UART0 (Low-Speed) Registers Summary

Address	Name	Description	Page
0x18020000	RBR	Receive Buffer	page 96
0x18020000	THR	Transmit Holding	page 97
0x18020000	DLL	Divisor Latch Low	page 97
0x18020004	DLH	Divisor Latch High	page 98
0x18020004	IER	Interrupt Enable	page 98
0x18020008	IIR	Interrupt Identity	page 99
0x18020008	FCR	FIFO Control	page 100
0x1802000C	LCR	Line Control	page 101
0x18020010	MCR	Modem Control	page 102
0x18020014	LSR	Line Status	page 103
0x18020018	MSR	Modem Status	page 104

7.2.1 Receive Buffer (RBR)

Address: 0x18020000
Access: Read-Only
Reset: 0x0

This read-only register contains the data byte received on the serial input port (SIN). The data in this register is only valid if the Data Ready (DR) bit in the Line Status Register (LSR) is set. In the non-FIFO mode (FIFO_MODE = 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. In FIFO mode (FIFO_MODE = 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already residing in the FIFO is full and this register will be preserved but any incoming data will be lost. An overrun error will also occur

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	RBR	The receive buffer register value

7.2.2 Transmit Holding (THR)

Address: 0x18020004
Access: Write-Only
Reset: 0x0

This write-only register contains data to be transmitted on the serial port (s_{OUT}). Data can be written to the THR any time the THR Empty (THRE) bit of the Line Status Register is set. If FIFOs are not enabled and the THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled and the THRE is set, up to sixteen characters of data may be written to the THR before the FIFO is full. Attempting to write data when the FIFO is full results in the write data being lost.

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	THR	The transmit buffer value

7.2.3 Divisor Latch Low (DLL)

Address: 0x18020008
Access: Read/Write
Reset: 0x0

This register, in conjunction with the Divisor Latch High (DLH), page 7-98 register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART0. It is accessed by first setting the DLAB bit (bit [7]) in the Line Control (LCR), page 7-101 register. The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLL	RW	0x0	Divisor latch low

7.2.4 Divisor Latch High (DLH)

Address: 0x1802000C
Access: Read/Write
Reset: 0x0

This register, in conjunction with the Divisor Latch Low (DLL), page 7-97 register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART0. It is accessed by first setting the DLAB bit (bit [7]) in the Line Control (LCR), page 7-101 register. The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLH	Divisor latch high

7.2.5 Interrupt Enable (IER)

Address: 0x18020010
Access: Read/Write
Reset: 0x0

This register contains four bits that enable the generation of interrupts.

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	EDDSI	Enable modem status interrupt
2	ELSI	Enable receiver line status interrupt
1	ETBEI	Enable register empty interrupt
0	ERBFI	Enable received data available interrupt

7.2.6 Interrupt Identity (IIR)

Address: 0x18020014
Access: Read-Only
Reset: 0x0

This register identifies the source of an interrupt. The two upper bits of the register are FIFO-enabled bits.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	FIFO_STATUS	FIFO enable status bits	
		00	FIFO disabled
		11	FIFO enabled
5:4	RES	Reserved. Must be written with zero. Contains zeros when read.	
3:0	IID	Used to identify the source of the interrupt	
		0000	Modem status changed
		0001	No interrupt pending
		0010	THR empty
		0100	Received data available
		0110	Receiver status
		1100	Character time out

7.2.7 FIFO Control (FCR)

Address: 0x18020018
Access: Write-Only
Reset: 0x0

This register sets the parameters for FIFO control. This register will also return current time values.

If FIFO mode is 0, this register has no effect. If FIFO mode is 1, this register will control the read and write data FIFO operation and the mode of operation for the DMA signals TXRDY_N and RXRDY_N.

If FIFO mode is enabled (FIFO mode = 1 and bit [0] is set to 1), bit [3], bit [6], and bit [7] are active.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	RCVR_TRIG	Sets the trigger level in the receiver FIFO for both the RXRDY_N signal and the Enable received data available interrupt (ERBFI)	
		00	1 byte in FIFO
		01	4 bytes in FIFO
		10	8 bytes in FIFO
		11	14 bytes in FIFO
5:4	RES	Reserved	
3	DMA_MODE	This bit determines the DMA signalling mode for TXRDY_N and RXRDY_N output signals	
2	XMIT_FIFO_RST	Writing this bit resets and flushes data in the transmit FIFO	
1	RCVR_FIFO_RST	Writing this bit resets and flushes data in the receive FIFO	
0	FIFO_EN	Setting this bit enables the transmit and receive FIFOs. The FIFOs are also reset any time this bit changes its value.	

7.2.8 Line Control (LCR)

Address: 0x1802001C
Access: Read/Write
Reset: 0x0

This register controls the format of the data that is transmitted and received by the UART0 controller.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7	DLAB	The divisor latch address bit. Setting this bit enables reading and writing of the Divisor Latch Low (DLL), page 7-97 and Divisor Latch High (DLH), page 7-98 registers to set the baud rate of the UART0. This bit must be cleared after the initial baud rate setup in order to access the other registers.	
6	BREAK	Setting this bit sends a break signal by holding the SOUT line low (when not in loopback mode, as determined by Modem Control (MCR), page 7-102 register bit [4]), until the BREAK bit is cleared. When in loopback mode, the break condition is internally looped back to the receiver.	
5	RES	Reserved	
4	EPS	Used to set the even/odd parity. If parity is enabled, this bit selects between even and odd parity. If this bit is a logic 1, an even number of logic 1s are transmitted or checked. If this bit is a logic 0, an odd number of logic 1s are transmitted or checked.	
3	PEN	Used to enable parity when set	
2	STOP	Used to control the number of stop bits transmitted. If this bit is a logic 0, one-stop bit is transmitted in the serial data. If this bit is a logic 1 and the data bits are set to 5, one and a half stop bits are generated. Otherwise, two stop bits are generated and transmitted in the serial data out.	
1:0	CLS	Used to control the number of bits per character	
		00	5 bits
		01	6 bits
		10	7 bits
		11	8 bits

7.2.9 Modem Control (MCR)

Address: 0x18020020
Access: Read/Write
Reset: See field description

This register controls the interface with the modem.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5	LOOPBACK	0x1	When set, the data on the SOUT line is held HIGH, while the serial data output is looped back to the SIN line, internally. In this mode, all the interrupts are fully functional. This feature is also used for diagnostic purposes. The modem control inputs (DSR_L, CTS_L, RI_L, DCD_L) are disconnected and the four modem control outputs (DTR_L, RTS_L, OUT1_L, OUT1_L) are looped back to the inputs, internally.
4	RES	0x0	Reserved
3	OUT2	0x1	Used to drive the UART0 output UART0_OUT2_L
2	OUT1	0x1	Used to drive the UART0 output UART0_OUT1_L
1	RTS	0x1	Used to drive the UART0 output RTS_L
0	DTR	0x1	Used to drive the UART0 output DTR_L. Not supported.

7.2.10 Line Status (LSR)

Address: 0x18020024
Access: Read/Write
Reset: 0x0

This register contains the status of the receiver and transmitter data transfers. This status may be read by the user at any time.

Bit	Bit Name	Description
31:8	RES	Reserved
7	FERR	The error in receiver FIFO bit. This bit is only active when the FIFOs are enabled. This bit is set when there is at least one parity error, framing error or break in the FIFO. This bit is cleared when the LSR is read AND the character with the error is at the top of the receiver FIFO AND there are no subsequent errors in the FIFO.
6	TEMT	The transmitter empty bit. This bit is set in FIFO mode whenever the Transmitter Shift Register and the FIFO are both empty. In non-FIFO mode, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	THRE	The transmitter holding register empty bit. When set, indicates the UART0 controller can accept a new character for transmission. This bit is set whenever data is transferred from the THR to the transmit shift register and no new data has been written to the THR. This also causes a THRE Interrupt to occur, if enabled.
4	BI	The break interrupt bit. This bit is set whenever the serial input (SIN) is held in a logic zero state for longer than the sum of (start time + data bits + parity + stop bits). A break condition on SIN causes one, and only one character, consisting of all zeros which will be received by the UART0. In FIFO mode, the character associated with the break condition is carried through FIFO and revealed when the character reaches the top of FIFO. Reading the LSR clears the BI bit. In non-FIFO mode, the BI direction occurs immediately and continues until the LSR has been read.
3	FE	The framing error bit. This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In FIFO mode, the framing error associated with the character received will come to the top of FIFO so it can be noticed. The OE, PE and FE bits are reset when a read of the LSR is performed.
2	PE	The parity error bit. This bit is set whenever there is a parity bit error in the receiver if the Parity Enable (PEN) bit in the LCR is set. In FIFO mode, the parity error associated with the character received will come to the top of FIFO so it can be noticed.
1	OE	The overrun error bit. When set, indicates an overrun error occurred because a new data character was received before the previous data was read. In non-FIFO mode, it is set when a new character arrives in the receiver before the previous character has been read from the RBR. In FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives in the receiver. The data in FIFO is retained and the data in the receive shift register is lost.
0	DR	The data ready bit. When set, indicates that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty when in FIFO mode.

7.2.11 Modem Status (MSR)

Address: 0x18020028
Access: Read/Write
Reset: 0x0

This register contains the current status of the modem control input lines and notes whether they have changed.

Bit	Bit Name	Description
31:8	RES	Reserved
7	DCD	Contains information on the current state of the modem control lines; complement of DCD_L
6	RI	Contains information on the current state of the modem control lines; complement of RI_L
5	DSR	Contains information on the current state of the modem control lines; complement of DSR_L
4	CTS	Contains information on the current state of the modem control lines; complement of CTS_L
3	DDCD	Notes whether modem control line DCD_L changed since the last time the CPU read the MSR
2	TERI	Indicates whether RI_L changed from an active low to inactive high since the last time MSR was read
1	DDSR	Notes whether DSR_L has changed since the last time the CPU read the MSR
0	DCTS	Notes whether CTS_L has changed since the last time the CPU read the MSR

7.3 USB Registers

Table 7-4 summarizes the USB registers for the QCA9531.

Table 7-4 USB Registers Summary

Address	Name	Description	Page
0x18030004	USB_CONFIG	USB Configuration Control	page 105

7.3.1 USB Configuration Control (USB_CONFIG)

Address: 0x18030004
Access: Read/Write
Reset: 0x1E

This register controls the basic configuration for the USB controller.

Bit	Bit Name	Description	
31:5	RES	Reserved	
4	HOST_OR_DEVICE	0	Reserved
		1	Indicates operation in host mode
3	AHB_HRDATA_SWAP	Swaps the read data on AHB bus	
2	AHB_HWDATA_SWAP	Swaps the write data on the AHB bus	
1	HS_MODE_EN	Enables high speed mode	
0	UTMI_PHY_EN	Asserted when selecting the UTMI mode	

7.4 GPIO Registers

Table 7-5 summarizes the GPIO registers for the QCA9531.

Table 7-5 General Purpose I/O (GPIO) Registers Summary

Address	Name	Description	Page
0x18040000	GPIO_OE	GPIO Output Enable	page 106
0x18040004	GPIO_IN	GPIO Input Value	page 107
0x18040008	GPIO_OUT	GPIO Output Value	page 107
0x1804000C	GPIO_SET	GPIO Per Bit Set	page 107
0x18040010	GPIO_CLEAR	GPIO Per Bit Clear	page 107
0x18040014	GPIO_INT	GPIO Interrupt Enable	page 108
0x18040018	GPIO_INT_TYPE	GPIO Interrupt Type	page 108
0x1804001C	GPIO_INT_POLARITY	GPIO Interrupt Polarity	page 108
0x18040020	GPIO_INT_PENDING	GPIO Interrupt Pending	page 108
0x18040024	GPIO_INT_MASK	GPIO Interrupt Mask	page 109
0x18040028	GPIO_IN_ETH_SWITCH_LED	GPIO Ethernet LED Routing Select	page 109
0x1804002C	GPIO_OUT_FUNCTION0	GPIO pins 0, 1, 2, 3 Output Multiplexing	page 110
0x18040030	GPIO_OUT_FUNCTION1	GPIO pins 4, 5, 6, 7 Output Multiplexing	page 110
0x18040034	GPIO_OUT_FUNCTION2	GPIO pins 8, 9, 10, 11 Output Multiplexing	page 111
0x18040038	GPIO_OUT_FUNCTION3	GPIO pins 12, 13, 14, 15 Output Multiplexing	page 111
0x1804003C	GPIO_OUT_FUNCTION4	GPIO pins 16, 17, 18, 19 Output Multiplexing	page 111
0x18040044	GPIO_IN_ENABLE0	UART0_SIN and SPI_DATA_IN Multiplexing	page 112
0x1804006C	GPIO_FUNCTION	Controls JTAG in GPIO	page 112

7.4.1 GPIO Output Enable (GPIO_OE)

Address: 0x18040000
Access: Read/Write
Reset: 0x3F30B

Bit	Bit Name	Description	
31:0	OE	Per bit output enable, where bit [22] sets GPIO22, bit [21] sets GPIO21, bit [20] sets GPIO20, and so on.	
		0	The bit is used as output
		1	Enables the bit as input

7.4.2 GPIO Input Value (GPIO_IN)

Address: 0x18040004
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	IN	Current values of each of the GPIO pins, where bit[22] sets GPIO22, bit [21] sets GPIO21, bit [20] sets GPIO20, and so on.

7.4.3 GPIO Output Value (GPIO_OUT)

Address: 0x18040008
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	OUT	Driver output value. If the corresponding bit in the GPIO_OE register is set to 0, the GPIO pin will drive the value in the corresponding bit of this register.

7.4.4 GPIO Per Bit Set (GPIO_SET)

Address: 0x1804000C
Access: Write-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	SET	On a write, any bit that is set causes the corresponding GPIO bit to be set; any bit that is not set will have no effect.

7.4.5 GPIO Per Bit Clear (GPIO_CLEAR)

Address: 0x18040010
Access: Write-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	CLEAR	On a write, any bit that is set causes the corresponding GPIO bit to be cleared; any bit that is not set will have no effect.

7.4.6 GPIO Interrupt Enable (GPIO_INT)

Address: 0x18040014
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	INT	Each bit that is set is considered an interrupt ORd into the GPIO interrupt line.

7.4.7 GPIO Interrupt Type (GPIO_INT_TYPE)

Address: 0x18040018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:0	TYPE	Interrupt type	
		0	Indicates the bit is a edge-sensitive interrupt
		1	Indicates the bit is an level-sensitive interrupt

7.4.8 GPIO Interrupt Polarity (GPIO_INT_POLARITY)

Address: 0x1804001C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:0	POLARITY	Interrupt polarity	
		0	Indicates that the interrupt is active low (level) or falling edge (edge)
		1	Indicates that the interrupt is active high (level) or rising edge (edge)

7.4.9 GPIO Interrupt Pending (GPIO_INT_PENDING)

Address: 0x18040020
Access: Read/Write (See field description)
Reset: 0x0

Bit	Bit Name	Description
31:0	PENDING	For each bit, indicates that an interrupt is currently pending for the particular GPIO; for edge-sensitive interrupts, this register is read-with-clear.

7.4.10 GPIO Interrupt Mask (GPIO_INT_MASK)

Address: 0x18040024
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	MASK	For each bit that is set, the corresponding interrupt in the register GPIO Interrupt Pending (GPIO_INT_PENDING), page 7-108 is passed on to the central interrupt controller.

7.4.11 GPIO Ethernet LED Routing Select (GPIO_IN_ETH_SWITCH_LED)

Address: 0x18040028
Access: Read-Only
Reset: 0x0

Selects routing of the signal indication groups to the LED signals: activity, collision, link, or duplex.

Bit	Bit Name	Description
31:20	RES	Reserved
19:15	LINK	The current value of LED_LINK100*n*_O and LED_LINK10*n*_O
14:10	DUPL	The current value of LED_DUPLEX*n*_O
9:5	COLL	The current value of LED_COLN*n*_O
4:0	ACTV	The current value of LED_ACT*n*_O

NOTE The GPIO_OUT_FUNCTION[5:0] registers, along with the GPIO Output Enable (GPIO_OE), page 7-106 register, determine which internal signal is driven to the GPIO pins. Each 32-bit GPIO_OUT_FUNCTION*x* register has select values for four GPIO pins (8 bits each). Each signal to output through the GPIO pin has a select value programmed in the particular GPIO field through which it is output (see Table 3-8).

NOTE These defaults are the default signal settings on the GPIO pin. On reset, GPIO[17:0] are configured with these default settings.

NOTE Apart from JTAG, all signals can use any GPIO and can use GPIO[3:0] by setting the DISABLE_JTAG bit to 1 in the GPIO_IN)ENABLE register. A value of zero in these fields selects the signal from the GPIO Output Value (GPIO_OUT), page 7-107 register.

7.4.12 GPIO Function 0 (GPIO_OUT_FUNCTION0)

Address: 0x1804002C
Access: Read/Write
Reset: 0x0

MUX values for GPIO[3:0].
Note that JTAG pins are available only in GPIO[3:0].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_3	GPIO3	TMS	Selected programmed value is available in GPIO3
23:16	ENABLE_GPIO_2	GPIO2	TDO	Selected programmed value is available in GPIO2
15:8	ENABLE_GPIO_1	GPIO1	TDI	Selected programmed value is available in GPIO1
7:0	ENABLE_GPIO_0	GPIO0	TCK	Selected programmed value is available in GPIO0

7.4.13 GPIO Function 1 (GPIO_OUT_FUNCTION1)

Address: 0x18040030
Access: Read/Write
Reset: 0x0

MUX values for GPIO[7:4].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_7	GPIO7	SPI_MOSI	Selected programmed value is available in GPIO7
23:16	ENABLE_GPIO_6	GPIO6	SPI_CLK	Selected programmed value is available in GPIO6
15:8	ENABLE_GPIO_5	GPIO5	SPI_CS0	Selected programmed value is available in GPIO5
7:0	ENABLE_GPIO_4	GPIO4	CLK_OBS4	Selected programmed value is available in GPIO4

7.4.14 GPIO Function 2 (GPIO_OUT_FUNCTION2)

Address: 0x18040034
Access: Read/Write
Reset: 0x0

MUX values for GPIO[11:8].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_11	GPIO11	Reserved	Selected programmed value is available in GPIO11
23:16	ENABLE_GPIO_10	GPIO10	UART0_SOUT	Selected programmed value is available in GPIO10
15:8	ENABLE_GPIO_9	GPIO9	UART0_SIN	Selected programmed value is available in GPIO9
7:0	ENABLE_GPIO_8	GPIO8	SPI_MISO	Selected programmed value is available in GPIO8

7.4.15 GPIO Function 3 (GPIO_OUT_FUNCTION3)

Address: 0x18040038
Access: Read/Write
Reset: 0x0

MUX values for GPIO[15:12].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_15	GPIO15	Reserved	Selected programmed value is available in GPIO15
23:16	ENABLE_GPIO_14	GPIO14	Reserved	Selected programmed value is available in GPIO14
15:8	ENABLE_GPIO_13	GPIO13	Reserved	Selected programmed value is available in GPIO13
7:0	ENABLE_GPIO_12	GPIO12	Reserved	Selected programmed value is available in GPIO12

7.4.16 GPIO Function 4 (GPIO_OUT_FUNCTION4)

Address: 0x1804003C
Access: Read/Write
Reset: 0x0

MUX values for GPIO[19:16].

Bit	Bit Name	GPIO	Default Function	Description
31:24	RES	RES	Reserved	Reserved
15:8	ENABLE_GPIO_17	GPIO17	Reserved	Selected programmed value is available in GPIO17
7:0	ENABLE_GPIO_16	GPIO16	Reserved	Selected programmed value is available in GPIO16

NOTE The GPIO_IN_ENABLE[9:0] registers, along with the GPIO Output Enable (GPIO_OE), page 7-106 register, drive internal logic. The registers indicate through which GPIO pins the particular input signal is available. Program the GPIO pin number through which these signals are input.

NOTE See Table 3-10.

NOTE Apart from JTAG, all signals listed in Table 3-10 can use any GPIO. GPIO[3:0] can be used by setting the DISABLE_JTAG bit to 1 in the GPIO_IN_ENABLE register.

7.4.17 GPIO In Signals 0 (GPIO_IN_ENABLE0)

Address: 0x18040044
Access: Read/Write
Reset: See field description

Program the GPIO pin number through which these signals are input. Legal values for this register are 0–17 for GPIO0 to GPIO17.

Bit	Bit Name	Reset	Default GPIO	Description
31:16	RES	0x0	—	Reserved
15:8	UART0_SIN	0x9	GPIO9	Programmed value indicates the GPIO that inputs UART0_SIN
7:0	SPI_DATA_IN	0x8	GPIO8	Programmed value indicates the GPIO pin that inputs SPI_MISO

7.4.18 GPIO Function (GPIO_FUNCTION)

Address: 0x1804006C
Access: Read/Write
Reset: See field description

This register indicates through which GPIO pins the particular input signal is available. Program the GPIO pin number through which these signals are input. If this bit is set enables or disables that specific function.

Bit	Bit Name	Reset	Description
31:9	RES	0x0	Reserved
8	CLK_OBS6_ENABLE	0x0	Enables observation of USB_CLK
7	CLK_OBS5_ENABLE	0x0	Enables observation of CPU_CLK/4
6	CLK_OBS4_ENABLE	0x1	Enables observation of AHB_CLK/2
5	CLK_OBS3_ENABLE	0x0	Enables observation of GMAC1_TX_CLK
4	CLK_OBS2_ENABLE	0x0	Enables observation of 125 MHz CLK
3	CLK_OBS1_ENABLE	0x0	Enables observation of PCIE RC CLK
2	CLK_OBS0_ENABLE	0x0	Enables observation of 25 MHz GMAC0 MII clock
1	DISABLE_JTAG	0x0	Disables JTAG port functionality to enable GPIO functionality
0	ENABLE_GPIO_SRIF	0x0	Enables the SRIF

7.5 PLL Control Registers

Table 7-6 summarizes the QCA9531 PLL control registers.

Table 7-6 PLL Control Registers Summary

Address	Name	Description	Page
0x18050000	CPU_PLL_CONFIG	CPU PLL Configuration	page 113
0x18050004	DDR_PLL_CONFIG	DDR PLL Configuration	page 114
0x18050008	CPU_DDR_CLOCK_CONTROL	CPU DDR Clock Control	page 115
0x1805000C	CPU_SYNC	CPU Sync Register	page 116
0x18050010	PCIE_PLL_CONFIG	PCIE PLL Configuration Register	page 116
0x18050014	PCIE_PLL_DITHER_DIV_MAX	PCIE Clock Jitter Control Maximum Register	page 117
0x18050018	PCIE_PLL_DITHER_DIV_MIN	PCIE Clock Jitter Control Minimum Register	page 117
0x1805001C	PCIE_PLL_DITHER_STEP	PCIE Clock Jitter Control Step Register	page 118
0x18050020	LDO_POWER_CONTROL	LDO Power Control Register	page 118
0x18050024	SWITCH_CLOCK_CONTROL	Switch Clock Source Control	page 119
0x18050028	CURRENT_PLL_DITHER	Current Dither Logic Output	page 119
0x1805002C	ETH_XMII	Ethernet XMII Configuration Register	page 120
0x18050040	BB_PLL CONFIG	Baseband PLL Configuration Register	page 120
0x18050044	DDR_PLL_DITHER	DDR PLL Dither Parameter	page 120
0x18050048	CPU_DLL_DITHER	CPU PLL Dither Parameter Register	page 120

7.5.1 CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG)

Address: 0x18050000
Access: Read/Write
Reset: See field description

This register configures the CPU PLL.

$$\text{Frequency} = \frac{\text{REFCLK\_FREQ}}{\text{REFDIV}} \times \left(\frac{\text{NFRAC}}{2^6} + \text{NINT}\right) \times \frac{1}{(2*\text{OUTDIV})}$$

Bit	Bit Name	Type	Reset	Description	
31	UPDATING	RO	0x1	This bit is set during the PLL update process. After the software configures CPU PLL, it takes about 32 µsec for the update to be finished. Software may poll this bit to see if the update has completed.	
				0	PLL update is complete
				1	PLL update is pending
30	PLLPWD	RW	0x1	Power down control for CPU PLL, write zero to this bit to power up the PLL	
29:22	RES	RW	0x0	Reserved	
21:19	OUTDIV	RW	0x0	Define the ratio between VCO output and PLL output. OUTDIV > 4 is unsupported.	
18:17	RES	RW	0x0	Reserved	
16:12	REFDIV	RW	0x20	Reference clock divider	

11:6	NINT	RW	0x0	The integer part of the DIV to CPU PLL
5:0	NFRAC	RO	0x0	Reflects the current NFRAC. Use “CPU PLL Dither Parameter (CPU_PLL_ DITHER)” on page 120 to set.

7.5.2 DDR PLL Configuration (DDR_PLL_CONFIG)

Address: 0x18050004
Access: Read / Write
Reset: See field description

This register is used to configure the DDR PLL.

$$\text{Frequency} = \frac{\text{REFCLK\_FREQ}}{\text{REFDIV}} \times \left(\frac{\text{NFRAC}}{2^{10}} + \text{NINT}\right) \times \frac{1}{(2*\text{OUTDIV})}$$

Bit	Bit Name	Type	Reset	Description
31	UPDATING	RO	0x1	This bit is set during the PLL update process. After the software configures CPU PLL, it takes about 32 µsec for the update to be finished. Software may poll this bit to see if the update has completed.
30	PLLPWD	RW	0x1	Power up control for the PLL, write zero to this bit to power up the PLL.
29:26	RES	RW	0x0	Reserved
25:23	OUTDIV	RW	0x0	Define the ratio between VCO output and PLL output. OUTDIV > 4 is unsupported.
22:21	RES	RW	0x0	Reserved
20:16	REFDIV	RW	0x2	Reference clock divider
15:10	NINT	RW	0x0	The integer part of the DIV to DDR PLL
9:0	NFRAC	RO	0x0	Reflects the current NFRAC. Use “Baseband PLL Configuration Register (BB_PLL_CONFIG)” on page 120 to set.

7.5.3 CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL)

Address: 0x18050008
Access: Read / Write
Reset: See field description

This register is used to set the CPU and DDR clocks. Any field in this register can be dynamically modified.

Bit	Bit Name	Type	Reset	Description	
31:25	RES	RW	0x0	Reserved	
24	AHBCLK_ FROM_DDRPLL	RW	0x1	AHB_CLK setting	
				0	AHB_CLK is derived from the CPU_PLL
				1	AHB_CLK is derived from the DDR_PLL
23	CPU_RESET_ EN_BP_DEASRT	RW	0x0	Enables reset to the CPU when the CPU_PLL bypass bit is reset	
22	CPU_RESET_ EN_BP_ASRT	RW	0x0	Enables reset to the CPU when the CPU_PLL bypass bit is set	
21	DDRCLK_ FROM_DDRPLL	RW	0x1	DDR_CLK setting. The DDR clock should be a 50% duty cycle clock	
				0	DDR_CLK is derived from the CPU_PLL
				1	DDR_CLK is derived from the DDR_PLL
20	CPUCLK_ FROM_CPUPLL	RW	0x1	CPU_CLK setting. Division of the AHB clock is:	
				0	CPU_CLK is derived from the DDR_PLL
				1	CPU_CLK is derived from the CPU_PLL
19:15	AHB_POST_DIV	RW	0x0	Division of the AHB clock: <AHB frequency> = <PLL or REFCLK frequency> / (AHB_POST_DIV+1)	
14:10	DDR_POST_DIV	RW	0x0	Division of the DDR PLL clock: <DDR frequency> = <PLL frequency> / (DDR_POST_DIV+1) or <REFCLK frequency>	
9:5	CPU_POST_DIV	RW	0x0	Division of the CPU PLL clock: <CPU frequency> = <PLL frequency> / (CPU_POST_DIV+1) or <REFCLK frequency>	
4	AHB_PLL_ BYPASS	RW	0x1	Enables bypassing of the AHB PLL path	
3	DDR_PLL_ BYPASS	RW	0x1	Enables bypassing of the DDR PLL	
2	CPU_PLL_ BYPASS	RW	0x1	Enables bypassing of the CPU PLL	
1	RESET_SWITCH	RW	0x0	Reset during clock switch trigger	
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

7.5.4 CPU Sync Register (CPU_SYNC)

Address: 0x1805000C
Access: Read/Write
Reset: See field description

This register is for the processor core SI_OCPSync generation.

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
19:16	LENGTH	0x0	Length of pattern + 1
15:0	PATTERN	0xFFFF	Pattern played out on SI_OCPSync from LSB to MSB

7.5.5 PCIE PLL Configuration Register (PCIE_PLL_CONFIG)

Address: 0x18050010
Access: Read/Write
Reset: See field description

This register is the PCIE RC Phase Lock Loop configuration register:

<PLL frequency> = <refclk frequency> / REFDIV * (DIV_INT + DIV_FRAC*2^4/(2^18-1)) / 6.

Frequency range is (530 ~ 830 MHz)/6.

Use PCIE_PLL_DITHER_DIV_MAX/MIN to set DIV_INT and DIV_FRAC.

Bit	Bit Name	Reset	Description
31	UPDATING	0x0	Poll for this bit to become zero to ensure PLL has settled.
30	PLLPWD	0x1	Write zero to this bit to power up the PLL.
29:17	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	BYPASS	0x1	Enables bypassing of the PCIE PLL
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:10	REFDIV	0x1	Reference clock divider
9:0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

7.5.6 PCIE Clock Jitter Control Maximum Register (PCIE_PLL_DITHER_DIV_MAX)

Address: 0x18050014
Access: Read/Write
Reset: See field description

This register is the PCIE Clock Jitter Control Maximum Value Register which controls the Jitter behavior of the PCIE PLL.

Bit	Bit Name	Reset	Description
31	EN_DITHER	0x1	Enable dither logic
30	USE_MAX	0x1	Uses DIV_MAX values when dither logic is disabled
29:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	DIV_MAX_INT	0x19	Maximum limit integer part of the divider
14:1	DIV_MAX_FRAC	0x3FFF	Maximum limit fractional part of the divider

7.5.7 PCIE Clock Jitter Control Minimum Register (PCIE_PLL_DITHER_DIV_MIN)

Address: 0x18050018
Access: Read/Write
Reset: See field description

This register is the PCIE Clock Jitter Control Minimum Value Register which controls the Jitter behavior of the PCIE PLL.

Bit	Bit Name	Reset	Description
31:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	DIV_MIN_INT	0x19	Minimum limit integer part of the divider
14:1	DIV_MIN_FRAC	0x3FFF	Minimum limit fractional part of the divider

7.5.8 PCIE Clock Jitter Control Step Register (PCIE_PLL_DITHER_STEP)

Address: 0x1805001C
Access: Read/Write
Reset: See field description

This register is the PCIE Clock Jitter Control Step Register which controls the Jitter behavior of the PCIE PLL.

Bit	Bit Name	Reset	Description
31:28	UPDATE_CNT	0x0	Count update frequency. and entry of 0 updates every clock
27:25	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
24:15	STEP_INT	0x0	Integer Part of the Step value of the divider
14:1	STEP_FRAC	0x010	Fractional Part of the Step value of the divider
0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

7.5.9 LDO Power Control Register (LDO_POWER_CONTROL)

Address: 0x18050020
Access: Read/Write
Reset: See the field description

This register reflects/controls the Analog LDO control bits Controls the LDO.

Bit	Bit Name	Reset	Description
31:5	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
4	PWDLDO_CPU	0x0	1.2 V signal to power down DDR regulator
3	PWDLDO_DDR	0x0	1.2 V signal to power down DDR regulator
2:1	CPU_REFSEL	0x3	Selects CPU regulator output voltage
0	SELECT_DDR	0x0	Reflects the input in PC_DDR_SEL pin

7.5.10 Switch Clock Source Control (SWITCH_CLOCK_CONTROL)

Address: 0x18050024
Access: Read / Write
Reset: See field description

This register controls the clock sources to the various blocks.

Bit	Bit Name	Type	Reset	Description
31:12	RES	RW	0x0	Reserved
11:8	USB _REFCLK _FREQ_SEL	RW	0x5	Used to select the REFCLK input of 25-MHz to the USB PLL
7	RES	RW	0x0	
6	MDIO_CLK_ SEL	RW	0x0	Selects the clock for the MDIO master operational clock
				0 REFCLK
				1 100 MHZ clock from the Ethernet PLL
5	OEN_ CLK125M_ PLL	RW	0x1	Enable for the PLL CLK 125M from the Ethernet PHY. Active low.
4	EN_PLL_ TOP	RW	0x1	Enable the Ethernet PHY PLL
3	EW_ ENABLE	RW	0x0	Enable for the switch
2	SWITCHCLK _OFF	RW	0x0	Shuts off the 25 MHz clock feed into the switch
1	RES	RW	0x0	Reserved
0	SWITCHCLK _SEL	RW	0x1	Used to select the 25 MHz REFCLK input to the Ethernet PHY
				0 RES
				1 25 MHz REFCLK

7.5.11 Current Dither Logic Output (CURRENT_PLL_DITHER)

Address: 0x18050028
Access: Read/ Write
Reset: See field description

This register sets the integer and fractional parts of the dither logic.

Bit	Bit Name	Type	Reset	Description
31:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	INT	RW	0x0	The integer part of the divider
14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	FRAC	RW	0x3FFF	The fractional part of the divider

7.5.12 Baseband PLL Configuration Register (BB_PLL_CONFIG)

Address: 0x18050040
Access: Read/Write
Reset: See field description

This register is the Baseband Phase Loop Lock configuration register.

Bit	Bit Name	Reset	Description
31	UPDATING	0x1	Poll for this bit to become 0 to ensure PLL has settled
30	PLLPWD	0x1	Write 0 to this bit to power up the PLL
29	SPARE	0x0	Spare bits
28:24	REFDIV	0x1	Reference clock divider
23:22	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
21:16	NINT	0x02	The integer part of the DIV to DDR PLL
15:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	NFRAC	14hccc	Reflects the current fraction of the PLL divider

7.5.13 DDR PLL Dither Parameter (DDR_PLL_DITHER)

Address: 0x18050044
Access: Read/Write
Reset: See field description

Controls the FRAC of the DDR_PLL. Should be enabled only if the DDR_CLK is from the DDR_ PLL.

Bit	Bit Name	Type	Reset	Description
31	DITHER_ EN	RW	0x0	The step value which increments every refresh period
30:27	UPDATE_ COUNT	RW	0x0	The number of refresh periods between two updates
26:20	NFRAC_ STEP	RW	0x0	7-bit LSB step value which increments every refresh period
19:10	NFRAC_ MIN	RW	0x0	The minimum NFRAC value
9:0	NFRAC_ MAX	RW	0x0	The maximum NFRAC value

7.5.14 CPU PLL Dither Parameter (CPU_PLL_DITHER)

Address: 0x18050048
Access: Read/Write
Reset: 0x0

Sets the parameters for the CPU PLL dither.

Bit	Bit Name	Description
31	DITHER_ EN	The step value which increments every refresh period
30:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:18	UPDATE_ COUNT	The number of 512 CPU clocks between two updates in NFRAC
17:12	NFRAC_ STEP	The step value increment
11:6	NFRAC_ MIN	Minimum NFRAC value. If DITHER_EN is set to 0, the min would be used.
5:0	NFRAC_ MAX	Maximum NFRAC value

7.6 Reset Registers

Table 7-7 summarizes the reset registers for the QCA9531.

Table 7-7 Reset Registers Summary

Address	Name	Description	Page
0x18060000	RST_GENERAL_TIMER	General Purpose Timer	page 122
0x18060004	RST_GENERAL_TIMER_RELOADx	General Purpose Timer Reload	page 122
0x18060008	RST_WATCHDOG_TIMER_CONTROL	Watchdog Timer Control	page 123
0x1806000C	RST_WATCHDOG_TIMER	Watchdog Timer	page 123
0x18060010	RST_MISC_INTERUPT_STATUS	Misc Interrupt Status	page 124
0x18060014	RST_MISC_INTERUPT_MASK	Misc Interrupt Mask	page 125
0x18060018	RST_GLOBAL_INTERUPT_STATUS	Global Interrupt Status	page 126
0x1806001C	RST_RESET	Reset	page 126
0x18060090	RST_REVISION_ID	Chip Revision ID	page 127
0x18060094	RST_GENERAL_TIMER2	General Purpose Timer 2	page 122
0x18060098	RST_GENERAL_TIMER2_RELOAD	General Purpose Timer2 Reload	page 122
0x1806009C	RST_GENERAL_TIMER3	General Purpose Timer 3	page 122
0x180600A0	RST_GENERAL_TIMER3_RELOAD	General Purpose Timer3 Reload	page 122
0x180600A4	RST_GENERAL_TIMER4	General Purpose Timer 4	page 122
0x180600A8	RST_GENERAL_TIMER4_RELOAD	General Purpose Timer4 Reload	page 122
0x180600AC	PCIE_WMAC_INTERRUPT_STATUS	PCIE WMAC Interrupt Status	page 127
0x180600B0	RST_BOOTSTRAP	Reset Bootstrap	page 128
0x180600B8	SPARE_STKY_REG[0:0]	Sticky Register Value	page 129
0x180600BC	RST_MISC2	Miscellaneous CPU Control Bits	page 129
0x180600C0	RST_CLKGAT_EN	AHB Clock Gating Reset Register	page 129

7.6.1 General Purpose Timers (RST_GENERAL_TIMERx)

Timer1 Address: 0x18060000
Timer2 Address: 0x18060094
Timer3 Address: 0x1806009C
Timer4 Address: 0x180600A4
Access: Read/Write
Reset: 0x0

This timer counts down to zero, sets, interrupts, and then reloads from the register General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 7-122. The timer operates with REF_CLK as reference input.

This definition holds true for timer1, timer2, timer3, and timer4.

Bit	Bit Name	Description
31:0	TIMER	Timer value

7.6.2 General Purpose Timers Reload (RST_GENERAL_TIMER_ RELOADx)

Timer1 Reload Address: 0x18060004
Timer2 Reload Address: 0x18060098
Timer3 Reload Address: 0x180600A0
Timer4 Reload Address: 0x180600A8
Access: Read/Write
Reset: 0x0

This register contains the value that will be loaded into the register General Purpose Timers (RST_ GENERAL_TIMERx), page 7-122 when it decrements to zero.

The timer operates with REF_CLK as reference input.

This definition holds true for timer1, timer2, timer3, and timer4.

Bit	Bit Name	Description
31:0	RELOAD_VALUE	Timer reload value

7.6.3 Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL)

Address: 0x18060008
Access: See field description
Reset: 0x0

Sets the action to take when the watchdog timer reaches zero. The options are reset, non-maskable interrupt and general purpose interrupt after reaching zero.

The timer operates with REF_CLK as reference input.

Bit	Bit Name	Type	Description	
31	LAST	RO	Indicates if the last reset was due to a watchdog timeout	
30:2	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
1:0	ACTION	RW	The action to be taken after the timer reaches zero	
			00	No action
			01	General purpose interrupt
			10	Non-maskable interrupt
			11	Full chip reset, same as power-on reset

7.6.4 Watchdog Timer (RST_WATCHDOG_TIMER)

Address: 0x1806000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	TIMER	Counts down to zero and stays at zero until the software sets this timer to another value. The timer operates with REF_CLK as reference input. These bits should be set to a non-zero value before updating the RST_WATCHDOG_ TIMER_CONTROL register to a non-zero number.

7.6.5 Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_ STATUS)

Address: 0x18060010
Access: Read/Write-to-Clear
Reset: 0x0

Sets the current state of the interrupt lines that are combined to form the MiscInterupt to the processor. All bits of this register need a write to clear.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21	USB_PLL_LOCK	USB PLL lock detection off an interrupt
20:19	RES	Reserved
18	DDR_ACTIVITY_ IN_SF	This interrupt is generated when the memory controller detects a DDR request when in self-refresh.
17	DDR_SF_EXIT	This interrupt is generated by the memory controller upon entering self-refresh
16	DDR_SF_ENTRY	This interrupt is generated by the memory controller upon entering self-refresh
15:13	RES	Reserved
12	S26_MAC_INT	The interrupt is generated from the Ethernet switch core. This bit is cleared after a write of this register.
11	RES	Reserved
10	TIMER4_INT	The interrupt corresponding to General Purpose Timer4. This bit is cleared after being read. The timer has been immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 7-122 register.
9	TIMER3_INT	The interrupt corresponding to General Purpose Timer3. This bit has been cleared after being read. The timer will be immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 7-122 register.
8	TIMER2_INT	The interrupt corresponding to General Purpose Timer2. This bit has been cleared after being read. The timer will be immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 7-122 register.
7:6	RES	Reserved
5	PC_INT	CPU performance counter interrupt. Generated whenever either of the internal CPU performance counters have bit [31] set. The relevant performance counter must be reset to clear this interrupt.
4	WATCHDOG_ INT	The watchdog timer interrupt. This interrupt is generated when the watchdog timer reaches zero and the watchdog configuration register is configured to generate a general-purpose interrupt.
3	UART_INT	The UART interrupt. UART0 interrupt registers must be read before this interrupt can be cleared.
2	GPIO_INT	The GPIO interrupt. Individual lines must be masked before this interrupt can be cleared.
1	ERROR_INT	The error interrupt.
0	TIMER_INT	Interrupt occurring in correspondence to the general purpose timer0. This bit is cleared after being read. The timer has already been reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 7-122 register.

7.6.6 Miscellaneous Interrupt Mask (RST_MISC_INTERRUPT_MASK)

Address: 0x18060014
Access: Read/Write
Reset: 0x0

Enables or disables a propagation of interrupts in the Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS) register.

Bit	Bit Name	Description
31:19	RES	Reserved. Must be written with zero. Contains zeros when read.
18	DDR_ACTIVITY_IN_SF_MASK	Enables the interrupt generated when the memory controller detects a DDR request when in self-refresh
17	DDR_SF_EXIT_MASK	Enables the interrupt generated when the memory controller enters self-refresh
16	DDR_SF_ENTRY_MASK	Enables the interrupt generated when the memory controller enters self-refresh
15:13	RES	Reserved
12	SW_MAC_INT_MASK	Enables the interrupt generated by the Ethernet switch core
11	RES	Reserved
10	TIMER4_MASK	When set, enables Timer3 interrupt
9	TIMER3_MASK	When set, enables Timer2 interrupt
8	TIMER2_MASK	When set, enables Timer1 interrupt
7:6	RES	Reserved
5	PC_MASK	When set, enables CPU performance counter interrupt
4	WATCHDOG_ MASK	When set, enables watchdog interrupt
3	UART_MASK	When set, enables the UART interrupt
2	GPIO_MASK	When set, enables GPIO interrupt
1	ERROR_MASK	When set, enables the error interrupt
0	TIMER_MASK	When set, enables timer interrupt

7.6.7 Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS)

Address: 0x18060018
Access: Read-Only
Reset: 0x0

This register indicates the cause of an interrupt to the CPU from various sources.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	TIMER_INT	Internal count/compare timer interrupt
4	MISC_INT	Miscellaneous interrupt; source of the interrupt available on the Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS), page 7-124 register
3	GE1_INT	Ethernet1 interrupt; information available in the Ethernet1 register space
2	GE0_INT	Ethernet0 interrupt; information available in the Ethernet0 register space
1	USB_INT	USB interrupt
0	PCIE_WMAC_INT	PCIE RC/WMAC interrupt

7.6.8 Reset (RST_RESET)

Address: 0x1806001C
Access: Read/Write
Reset: See field description

This register individually controls the reset to each of the chip's submodules.

Bit	Bit Name	Reset	Type	Description
31:30	RES	0x0	RO	Reserved
29	USB_EXT_PWR	0x1	RW	External power requirement for USB PHY
28	EXTERNAL_RESET	0x0	RW	Commands an external reset (SYS_RST_L pin) immediately; inverted before being sent to the pin.
27	RTC_RESET	0x1	RW	The RTC reset
26:25	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.
24	FULL_CHIP_RESET	0x0	RW	Used to command a full chip reset. This is the software equivalent of pulling the reset pin. The system will reboot with PLL disabled. Always zero when read.
23	RESET_GE1_MDIO	0x1	RW	Resets the Ethernet 1 MDIO
22	RESET_GE0_MDIO	0x1	RW	Resets the Ethernet 0 MDIO
21	CPU_NMI	0x0	RW	Used to send an NMI to the CPU. Always zero when read. The watchdog timer can also be used to generate NMI/full chip reset.
20	CPU_COLD_RESET	0x0	RW	Used to cold reset the entire CPU. This bit will be cleared automatically immediately after the reset. Always zero when read.
19:17	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.
16	DDR_RESET	0x0	RW	Resets the DDR controller. Self-cleared to 0 by hardware
15	USB_PHY_PLL_PWD_EXT	0x0	RW	Used to power down the USB PHY PLL
14	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.
13	GE1_MAC_RESET	0x1	RW	Used to reset the GE1 MAC
12	ETH_SWITCH_ARESET	0x1	RW	Resets the switch analog

11	USB_PHY_ARESET	0x1	RW	Resets the USB PHY's analog	
10	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.	
9	GE0_MAC_RESET	0x1	RW	Used to reset the GE0 MAC	
8	ETH_SWITCH_ RESET	0x1	RW	Resets the switch digital portion	
7	PCIE_PHY_RESET	0x1	RW	Resets the PCIE PHY	
6	PCIE_RESET	0x1	RW	Resets the PCIE host controller	
5	USB_HOST_RESET	0x1	RW	Used to reset the USB Host Controller	
4	USB_PHY_RESET	0x1	RW	Used to reset the USB PHYs	
3	USB_PHY_SUSPEND_ OVERRIDE	0x0	RW	Used to set the USB suspend state	
				0	Used to put the USB PHY in suspend state
				1	Delegates the Core to control the USB PHY suspend state
2:0	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.	

7.6.9 Chip Revision ID (RST_REVISION_ID)

Address: 0x18060090
Access: Read-Only
Reset: See field description

This register is the revision ID for the chip.

Bit	Bit Name	Reset	Description
31:0	VALUE	0x140	Revision ID value

7.6.10 PCIE WMAC Interrupt Status (RST_PCIE _WMAC_ INTERRUPT_STATUS)

Address: 0x180600AC
Access: Read-Only
Reset: 0x0

This register is used to read the interrupt statuses for PCIE RC and WMAC interrupts.

Bit	Bit Name	Description
31:9	RES	Reserved. Must be written with zero. Contains zeros when read.
8	PCIE_RC_INT3	PCIE RC MULTI-MSI interrupts (Vector 3) / INTA interrupt status
7	PCIE_RC_INT2	PCIE RC MULTI-MSI interrupts (Vector 2) / INTA interrupt status
6	PCIE_RC_INT1	PCIE RC MULTI-MSI interrupts (Vector 1) / INTA interrupt status
5	PCIE_RC_INT0	PCIE RC MULTI-MSI interrupts (Vector 0) / INTA interrupt status
4	PCIE_RC_INT	Master PCIE RC interrupt
3	WMAC_RXHP_INT	Interrupt corresponding to the WMAC high priority receive queue
2	WMAC_RXLP_INT	Interrupt corresponding to the WMAC low priority receive queue
1	WMAC_TX_INT	Interrupt corresponding to the WMAC transmission
0	WMAC_MISC_INT	Interrupt corresponding to the WMAC

7.6.11 Reset Bootstrap (RST_BOOTSTRAP)

Address: 0x180600B0
Access: Read-Only
Reset: See field descriptions

This register contains the bootstrap values latched during reset.

Bit	Bit Name	Reset	Description	
31:13	RES	0x0	Reserved	
12	SW_OPTION2	0x0	Software option 2	
11	SW_OPTION1	0x0	Software option 1	
10	TESTROM_ENABLE	0x0	Enables/disables TESTROM	
			0	Test ROM disabled
			1	Test ROM enabled
9	RES	0x0	Reserved	
8:6	RES	0x0	Reserved	
5	EJTAG_MODE	0x0	0	Selects JTAG mode (Default)
			1	Selects EJTAG mode
4	REF_CLK	0x0	0	Selects REF_CLK_25MHz (default)
			1	Reserved
3:1	RES	0x0	Reserved	
0	DDR_SELECT	0x1	0	Selects DDR2
			1	Selects DDR1 (default)

7.6.12 Sticky Register Value (SPARE_STKY_REG[0:0])

Address: 0x180600B8
Access: Read/Write
Reset: 0x0

This register is a generic register only affected by power-cycling. This register can be used by the CPU to save and restore critical state bits during a suspend/resume event for example.

Bit	Bit Name	Description
31:0	VALUE	Sticky register value. This value is reset only with power on reset (not on any other reset).

7.6.13 Miscellaneous CPU Control Bits (RST_MISC2)

Address: 0x180600BC
Access: Read/Write
Reset: See field description

This register contains miscellaneous CPU controllable bits.

Bit	Bit Name	Reset	Description
31:26	SPARE	0x0	Spare bits
25:20	RES	0x0	Reserved
19	PCIE_CLKOBS1_SEL	0x0	Select between different PCIE Common PHY clocks for observation
18:14	RES	0x0	Reserved
13	PERSTN_RCPHY	0x1	Bit for controlling perstn of PCIE RC PHY
12:0	RES	0x0	Reserved

7.6.14 AHB Clock Gating Reset Register (RST_CLKGAT_EN)

Address: 0x180600C0
Access: Read/Write
Reset: See field description

This register controls individual AHB clock gating for each interface.

Bit	Bit Name	Reset	Description
31:12	SPARE	0x0	Spare bits
11:10	RES	0x0	Reserved
9	WMAC	0x1	Enable AHB CLK to propagate for WMAC
8	RES	0x0	Reserved
7	USB1	0x1	Enable AHB CLK to propagate for USB1
6	GE1	0x1	Enable AHB CLK to propagate for GE1
5	GE0	0x1	Enable AHB CLK to propagate for GE0
4:2	RES	0x0	Reserved
1	PCIE_RC	0x1	Enable AHB CLK to propagate for PCIE RC
0	RES	0x0	Reserved

7.7 GMAC Interface Registers

Table 7-8 summarizes the GMAC interface registers for the QCA9531.

Table 7-8 GMAC Interface Registers Summary

Address	Name	Description	Page
0x18070000	ETH_CFG	Ethernet Configuration	page 130

7.7.1 Ethernet Configuration (ETH_CFG)

Address: 0x18070000
Access: Read/Write
Reset: 0x0

This register determines how GE0 is interfaced in the QCA9531. If SW_ONLY_MODE is set, then all five FE ports attach to the Ethernet switch (LAN ports).

Bit	Bit Name	Description
31:22	ETH_SPARE	Spare register bits
21:14	RES	Reserved
13	SW_ACC_ MSB_FIRST	Enables MSB data first during the Switch register write
12:10	RES	Reserved
9	SW_APB_ACCESS	Enables APB access to the Switch registers instead of the MDIO
8	SW_PHY_ADDR_SWAP	Enables swapping of PHY0 and PHY5 in the Switch for the WAN
7	SW_PHY_SWAP	Enables swapping of PHY0 and PHY5 in the Switch for the WAN
6	SW_ONLY_MODE	Enables the WAN port PHY to be connected to the Switch instead of GE0
5:0	RES	Reserved

7.8 PCIE RC Control Registers

Table 7-9 summarizes the PCIE RC control registers for the QCA9531.

Table 7-9 PCIE RC Control Registers

Address	Name	Description	Page
0x180F0000	PCIE_APP	PCIE Application Control	page 132
0x180F0004	PCIE_AER	PCIE Interrupt and Error	page 133
0x180F0008	PCIE_PWR_MGMT	PCIE Power Management	page 133
0x180F000C	PCIE_ELEC	PCIE Electromechanical	page 134
0x180F0010	PCIE_CFG	PCIE Configuration	page 134
0x180F0014	PCIE_RX_CNTL	PCIE Receive Completion	page 135
0x180F0018	PCIE_RESET	PCIE Reset	page 135
0x180F001C	PCIE_DEBUG	PCIE Debug and Control	page 136
0x180F0024	PCIE_PHY_RW_DATA	PCIE PHY Read/Write Data	page 136
0x180F0028	PCIE_PHY_TRG_RD_LOAD	PCIE PHY Serial Interface Load/Read Trigger	page 137
0x180F002C	PCIE_PHY_CFG_DATA	PCIE PHY Configuration Data	page 137
0x180F0030	PCIE_MAC_PHY	PCIE MAC-PHY Interface Signals	page 137
0x180F0034	PCIE_PHY_MAC	PCIE PHY-MAC Interface Signals	page 138
0x180F0038	PCIE_SIDEBAND1	PCIE Sideband Bus1	page 138
0x180F003C	PCIE_SIDEBAND2	PCIE Sideband Bus2	page 138
0x180F0040	PCIE_SPARE	PCIE Spare	page 139
0x180F0044	PCIE_MSI_ADDR	PCIE MSI Lower Address	page 139
0x180F0048	PCIE_MSI_DATA	PCIE MSI Data Value	page 139
0x180F004C	PCIE_INT_STATUS	PCIE Interrupt Status	page 139
0x180F0050	PCIE_INT_MASK	PCIE Interrupt Mask	page 141
0x180F0054	PCIE_ERR_CNT	PCIE Error Counter	page 142
0x180F0058	PCIE_REQ_LATENCY_W_INT	PCIE AHB Latency Interrupt Counter	page 142
0x180F005C	PCIE_MISC	Miscellaneous PCIE Bits	page 142

7.8.1 PCIE Application Control (PCIE_APP)

Address: 0x180F0000
Access: Read/Write
Reset: See field description

This register provides various control and status bits to configure the PCIE RC core from the application side.

Bit	Bit Name	Reset	Description
31:22	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
21:20	CFG_TYPE	0x0	0 Sending a configuration transaction to the immediate downstream component (switch, endpoint) (Default) 1 Sending a type 1 configuration transaction to multiple endpoints via a switch.
19:16	PCIE_BAR_MSN	0x1	Most significant nibble of the register PCIE Interrupt and Error (PCIE_AER).
15:12	CFG_BE	0xF	Used as the byte enable of the next configuration request sent out on the PCIE interface.
11:6	SLV_RESP_ ERR_MAP	0x3F	AHB slave response for a previous PCIE transaction. The response bits are mapped as: 6 bits == {completion_tlp_abort, completion_ecrc, completion_ep, completion_crs, completion_ca, completion_ur}, where: 0 SLVERR 1 DECERR
5:4	MSTR_RESP_ ERR_MAP	0x0	AHB master response error map. This signal allows the application to select a master response error report mechanism received from an AHB response channel to the CPL status of native PCIE core transmissions. MSB is not currently used. ■ When the LSB is set to 0, it will set an AHB response error to a CA of a PCIE completion: 2 bits == {decerr, slverr} ■ When the LSB is set to 1, it will set an AHB response error to a UR of a PCIE completion.
3	INIT_RST	0x0	Application request to initiate a training reset
2	PM_XMT_ TURNOFF	0x0	Application signal to generate PM turnoff messages for power management
1	UNLOCK_MSG	0x0	Wakeup status because of power fault
0	LTSSM_ENABLE	0x0	Application signal to enable the LTSSM. If set to zero, it indicates that the application is not ready.

7.8.2 PCIE Interrupt and Error (PCIE_AER)

Address: 0x180F0004
Access: Read-Only
Reset: 0x0

This register contains common transmit and receive advanced error (AER) counters, such as bad DLLP, BAD TLP, NAKS, REPLAY TIMEOUTS, and so on.

Bit	Bit Name	Description
31:24	ERR_CNT4	Counter for replay timeouts/replay rollover
23:16	ERR_CNT3	Counter for receive errors (coding and disparity errors)
15:8	ERR_CNT2	Counter for transmit NAKs
7:0	ERR_CNT1	Counter for bad TLP and DLLP errors

7.8.3 PCIE Power Management (PCIE_PWR_MGMT)

Address: 0x180F0008
Access: Read/Write
Reset: 0x0

This register controls application control and status signals needed for power management.

Bit	Bit Name	Description
31:9	RES	Reserved
8	PME_INT	Interrupt caused by PME
6	RADM_PM_TO_ACK	Receipt of a PME turnoff acknowledgement message (the signal that indicates that the RC received a PME_TO_ACK message)
5	RADM_PM_PME	Receipt of a PME message (the signal that indicates that the RC received a PM_PME message)
4	AUX_PM_EN	AUX power PM enable; enable device to draw auxiliary power independent of PME AUX power
3	READY_ENTR_L23	Indication from the application that it is ready to enter the L2/L3 state
2	REQ_EXIT_L1	Request from the application to exit ASPM state L1, only effective if L1 is enabled
1	REQ_ENTRY_L1	Capability for applications to request PM state to enter L1; only effective if ASPM of L1 is enabled
0	AUX_PWR_DET	Auxiliary power detected; indicates that auxiliary power (VAUX) is present

7.8.4 PCIE Electromechanical (PCIE_ELEC)

Address: 0x180F000C
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description
31:3	RES	RW	Reserved
2	SYS_ATTEN_ BUTTON_PRESSED	RW	Attention button pressed. Indicates that the system attention button was pressed, sets the attention button pressed bit in the Slot Status register
1	CLK_REQ_N	RO	Clock enable Allows the application clock generation module to turn off CORE_CLK based on the current power management state:
			0 CORE_CLK must be active for the current power state
			1 Current power state allows CORE_CLK to be shut down
0	WAKE_N	RO	Wake up from power management unit. PCIE RC core generates WAKE_L to request the system to restore power and clock when a beacon has been detected. Assertion of WAKE_L could be a clock or multiple clock cycles.

7.8.5 PCIE Configuration (PCIE_CFG)

Address: 0x180F0010
Access: Read/Write
Reset: 0x0

This registers controls application control and status signals to configure core behavior.

Bit	Bit Name	Description
31	RES	Reserved. Must be written with zero. Contains zeros when read.
30:26	INT_MSG_NUM	Advanced error interrupt message number Used when MSI or MSI-X is enabled. Assertion of CFG_AER_RC_ERR_MSI along with a value on CFG_AER_INT_MSG_NUM is equivalent to the RC core receiving an MSI with the CFG_AER_INT_MSG_NUM value as the MSI vector.
25	EML_CONTROL	Electromechanical interlock control; this bit denotes the state of the electromechanical interlock control bit in PCIE Electromechanical (PCIE_ELEC) register.
24	PWR_CTRLER_ CTRL	Power controller control; this bit controls the system power controller (from bit [10] of the PCIE Receive Completion (PCIE_RX_CNTL) register).
23:22	ATTEN_IND	Attention indicator control; these bits control the system attention indicator) from bits [7:6] of the PCIE Receive Completion (PCIE_RX_CNTL) register).
21:17	PBUS_DEV_NUM	Configured device number; denotes the device number assigned to the device.
16:9	PBUS_NUM	The configured primary bus number. These bits denote the primary bus number assigned to the device.
8	RCB	The read completion boundary (RCB). This bit denotes the value of the RCB bit in the Link Control register in the PCIE RC.
7:5	MAX_PAYLOAD_ SIZE	The maximum payload size. This bit denotes the value of the MAX_PAYLOAD_SIZE field in the Device Control register in the PCIE RC.
4:2	MAX_RDREQ_ SIZE	The maximum read request size. This bit denotes the value of the MAX_READ_ REQUEST_SIZE field in the Device Control register in the PCIE RC.
1	MEM_SPACE_EN	Memory space enable; this bit denotes the state of the Memory Space Enable bit in the PCI-compatible Command register in the PCIE RC.
0	BUS_MASTER_ EN	Bus master enable; this bit denotes the state of the Bus Master Enable bit in the PCI-compatible Command register in the PCIE RC.

7.8.6 PCIE Receive Completion (PCIE_RX_CNTL)

Address: 0x180F0014
Access: Read-Only
Reset: 0x0

This register is used to denote the field values related to the completion timeout of the PCIE.

Bit	Bit Name	Description
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.
28:21	TIMEOUT_CPL_ TAG	The tag field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted
20:9	TIMEOUT_CPL_ LEN	The length field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
8:7	TIMEOUT_CPL _ATTR	The attributes field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
6:4	TIMEOUT_CPL_ TC	The traffic class of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
3:1	TIMEOUT_FN_ NUM	The function number of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
0	CPL_TIMEOUT	The completion timeout. This bit indicates that the completion TLP for a request has not been received within the expected time window.

7.8.7 PCIE Reset (PCIE_RESET)

Address: 0x180F0018
Access: Read/Write
Reset: See field description

This register is used to set the bits for the PCIE reset.

Bit	Bit Name	Reset	Description	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	EP_RESET_L	0x1	The reset bit for indicating an endpoint reset through the PCIE PHY	
1	LINK_REQ_ RESET	0x0	The reset request due to a link down status. A high-to-low transition indicates that the RC Core is requesting external logic to reset the RC Core because the PHY link is down.	
0	LINK_UP	0x0	Indicates if the PHY link is up or down	
			0	Link is down
			1	Link is up

7.8.8 PCIE Debug and Control (PCIE_DEBUG)

Address: 0x180F001C
Access: Read/Write
Reset: See field description

This register controls application and status signals for additional debug and configuration of the core behavior.

Bit	Bit Name	Reset	Description
31:18	RES	0x0	Reserved
17	AHB_MSTR_DATA_SWAP_EN	0x0	AHB master: byte swap configuration option
16	PCIE_PHY_READY	0x0	PCIE PHy's ready signal
15	RXVALID_EXT_ENABLE	0x0	Enable bit for extending rxvalid from PHY by three clocks
14	BYTESWAP	0x1	AHB slave: byte swap configuration option
13	PM_STATUS	0x0	Power management status: PME status bit from the PMCSR
12	PM_PME_EN	0x0	Power management event (PME) enable: PME enable bit in the PMCSR
11:9	PM_DSTATE	0x0	Current power management D-state of the function
8:4	XMLH_LTSSM_STATE	0x0	Current LTSSM state
3:1	PM_CURNT_STATE	0x0	Current power state
0	RDLH_LINK_UP	0x0	DATA link layer up/down indicator This status from the flow control initialization state machine indicates that flow control has been initiated and the data link Layer is ready to transmit and receive packets.
			0 Link is down
			1 Link is up

7.8.9 PCIE PHY Read/Write Data (PCIE_PHY_RW_DATA)

Address: 0x180F0024
Access: Read/Write
Reset: 0x0

This register would trigger a read and a write to the PCIE PHY Serial Interface.

Bit	Bit Name	Description
31:0	PHY_DATA	PCIE PHY data read/write

7.8.10 PCIE PHY Serial Interface Load/Read Trigger (PCIE_PHY_TRG_RD_LOAD)

Address: 0x180F0028
Access: Read-Only
Reset: 0x0

This register triggers a read or a load for the PCIE PHY serial interface.

Bit	Bit Name	Description	
31:0	PARALLEL_LOAD_OP_DONE	Bit 0	Parallel Load: Trigger a Parallel Load to the PCIE PHY - Would be cleared on Operation Complete
		Bit 31	OP_DONE: Indicates that the previous Operation is completed. Read / Write - Gets cleared on read/write to PCIE_PHY_RW_DATA register

7.8.11 PCIE PHY Configuration Data (PCIE_PHY_CFG_DATA)

Address: 0x180F002C
Access: Read-Only
Reset: 0x0 (32'd5)

Bit	Bit Name	Description
31:0	PHY_CFG_DATA	PCIE PHY configuration data

7.8.12 PCIE MAC-PHY Interface Signals (PCIE_MAC_PHY)

Address: 0x180F0030
Access: Read-Only
Reset: See field description

This register is used to denote the interface signals for the MAC-PHY interface.

Bit	Bit Name	Description	
31:24	RES	Reserved	
23:22	PWRDOWN	The power control. Power control bits to the PHY. The MAC_PHY_POWERDOWN is a 2-bit signal that is shared by all Lanes.	
		00	P0 (normal operation)
		01	P0s (Low power, small latency for recovery)
		10	P1 (Much lower power but longer latency for recovery)
		11	P2 (Lowest power state)
21	RXPOLARITY	Inverted polarity on receive	
20	TXCOMPLIANCE	MAC_PHY_TX compliance status	
19	TXELECIDLE	Transmit electrical idle status	
18	TXDETRX_LOOPBACK	Status of MAC_PHY_TXDETECTRX from RC	
17:16	TXDATAK	Data/control indication for transmit data symbols. When set to 1, indicates a "K" or control symbol.	
15:0	TXDATA	PCIE RC transmit data from MAC to PHY	

7.8.13 PCIE PHY-MAC Interface Signals (PCIE_PHY_MAC)

Address: 0x180F0034
Access: Read-Only
Reset: 0x0

This register is used to denote the interface signals for the PHY-MAC interface.

Bit	Bit Name	Description
31:26	RES	Reserved. Must be written with zero. Contains zeros when read.
25	RXDETECT_DONE	Indicated a successful receiver detection
24	PHYSTATUS_ASSERTED	Indicates that PHYSTATUS (bit [22])has been asserted
23	RXVALID	Indicates PIPE Rx data valid
22	PHYSTATUS	Indicates PIPE PHY status
21:19	RXSTATUS	Indicates PIPE Rx status
18	RXELECIDLE	Indicates PIPE electrical idle
17:16	RXDATAK	Data/control for the receive data symbols
15:0	RXDATA	PIPE receive data

7.8.14 PCIE Sideband Bus1 (PCIE_SIDEBAND1)

Address: 0x180F0038
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_ PHY_CONTROL bus maps to the PHY control register.

7.8.15 PCIE Sideband Bus2 (PCIE_SIDEBAND2)

Address: 0x180F003C
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_ PHY_CONTROL bus maps to the PHY control register.

7.8.16 PCIE Spare (PCIE_SPARE)

Address: 0x180F0040
Access: Read-Only
Reset: 0x0

This register is contains spare bits for the PCIE.

Bit	Bit Name	Description
31:0	BITS	Spare bits for the PCIE

7.8.17 PCIE MSI Lower Address (PCIE_MSI_ADDR)

Address: 0x180F0044
Access: Read/Write
Reset: 0x0

This register holds the lower address for the MSI.

Bit	Bit Name	Description
31:0	LADDR	The lower address register for the MSI

7.8.18 PCIE MSI Data Value (PCIE_MSI_DATA)

Address: 0x180F0048
Access: Read/Write
Reset: 0x0

This register is used to hold the data for the MSI including vector.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	VALUE	These bits hold the data for the MSI including vector [4:0]. The pattern assigned by the system software.

7.8.19 PCIE Interrupt Status (PCIE_INT_STATUS)

Address: 0x180F004C
Access: Read/Write
Reset: 0x0

This register reflects the status of currently active interrupts. A 1 in a bit position indicates the corresponding interrupt is active.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	LINK_DOWN	XMLH link down interrupt
26	LINK_REQ_RST	Request for reset from the PCIE RC core to the application.
25:22	MSI_VEC	Indicates which MSI interrupt has happened

21	CPU_INTD	The status bit to indicate that an INTD assertion has occurred and the client needs to send a deassert interrupt
20	CPU_INTC	The status bit to indicate that an INTC assertion has occurred and the client needs to send a deassert interrupt
19	CPU_INTB	The status bit to indicate that an INTB assertion has occurred and the client needs to send a deassert interrupt
18	CPU_INTA	The status bit to indicate that an INTA assertion has occurred and the client needs to send a deassert interrupt
17	INTDL	PCI 3.0 compatible, level triggered INTD virtual wire interrupt. This interrupt is ON on reception of INTD assertion message and stays on till the corresponding deassertion message is received.
16	INTCL	PCI 3.0 compatible, level triggered INTC virtual wire interrupt. This interrupt is ON on reception of INTC assertion message and stays on till the corresponding deassertion message is received.
15	INTBL	PCI 3.0 compatible, level triggered INTB virtual wire interrupt. This interrupt is ON on reception of INTB assertion message and stays on till the corresponding deassertion message is received.
14	INTAL	PCI 3.0 compatible, level triggered INTA virtual wire interrupt. This interrupt is ON on reception of INTA assertion message and stays on till the corresponding deassertion message is received.
13	SYS_ERR	A system error. The RC Core asserts CFG_SYS_ERR_RC if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL.
12	AER_MSI	Advanced error MSI or MSI-X indication; CFG_AER_RC_ERR_MSI is set when: ■ MSI or MSI-X is enabled ■ A reported error condition causes a bit to be set in the Root Error Status register. ■ The associated error message reporting enable bit is set in the Root Error Command register.
11	AER_INT	Advanced error reporting interrupt; This interrupt is set when an internally generated error message is to be propagated to the software by PCIE root complex.
10	MSI_ERR	Error MSI interrupt Interrupt is set whenever an MSI error message is received by the PCIE root complex.
9	MSI	The interrupt caused by the MSI
8	INTD	PCI 3.0 compatible, edge triggered INTD virtual wire interrupt This interrupt is set on reception of INTD assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
7	INTC	PCI 3.0 compatible, edge triggered INTC virtual wire interrupt This interrupt is set on reception of INTC assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
6	INTB	PCI 3.0 compatible, edge triggered INTB virtual wire interrupt This interrupt is set on reception of INTB assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
5	INTA	PCI 3.0 compatible, edge triggered INTA virtual wire interrupt This interrupt is set on reception of INTA assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
4	RADMX_COMP_ LOOKUP_ERR	The RADMX response composer TAG lookup error. This is a fatal error condition.
3	GM_COMP_ LOOKUP_ERR	GM response composer TAG lookup error. This is a fatal error condition.
2	FATAL_ERR	The received fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_FATAL message
1	NONFATAL_ERR	The received non-fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_NONFATAL message
0	CORR_ERR	The received correctable error message. One clock cycle pulse that indicates that the RC core received an ERR_COR message.

7.8.20 PCIE Interrupt Mask (PCIE_INT_MASK)

Address: 0x180F0050
Access: Read/Write
Reset: 0x0

Selectively enables or disables propagation of interrupts. A “1” in a bit position enables the corresponding interrupt being asserted. A “0” in a bit position disables the corresponding interrupt being asserted.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	LINK_DOWN	XMLH link down interrupt mask
26	LINK_REQ_RST	PCIE RC link reset link request int mask
25:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17	INTDL	Mask for the assertion+deassertion of the INTD virtual wire level-triggered interrupt.
16	INTCL	Mask for the assertion+deassertion of the INTC virtual wire level-triggered interrupt.
15	INTBL	Mask for the assertion+deassertion of the INTB virtual wire level-triggered interrupt.
14	INTAL	Mask for the assertion+deassertion of the INTA virtual wire level-triggered interrupt.
13	SYS_ERR	System error interrupt mask
12	AER_MSI	Mask for advanced error (AER) MSI or MSI-X indication interrupt
11	AER_INT	AER interrupt mask
10	MSI_ERR	MSI error interrupt
9	MSI	Interrupt caused by the MSI
8	INTD	INTD virtual wire edge triggered interrupt mask
7	INTC	INTC virtual wire edge triggered interrupt mask
6	INTB	INTB virtual wire edge triggered interrupt mask
5	INTA	INTA virtual wire edge triggered interrupt mask
4	RADMX_COMP_ LOOKUP_ERR	RADMX response composer TAG lookup error mask
3	GM_COMP_ LOOKUP_ERR	GM response composer TAG lookup error mask
2	FATAL_ERR	Received fatal error message interrupt (RADM_FATAL_ERR) mask
1	NONFATAL_ERR	Received non-fatal error message (RADM_NONFATAL_ERR) mask
0	CORR_ERR	Received correctable error message interrupt (RADM_CORRECTABLE_ERR) mask

7.8.21 PCIE Error Counter (PCIE_ERR_CNT)

Address: 0x180F0054
Access: Read/Write
Reset: 0x0

This register keeps a count of the number of errors related to PCIE RC.

Bit	Bit Name	Description
31:0	VALUE	Indicates the number of errors related to PCIE RC; can include: bad DLLP, bad TLP, NAKS, REPLAY TIMEOUTS, and so on.

7.8.22 PCIE AHB Latency Interrupt Counter (PCIE_REQ_LATENCY_W_INT)

Address: 0x180F0058
Access: Read/Write
Reset: 0x0

This register is a counter to indicate the AHB Request to AHB Ready Latency of PCIE when an interrupt is asserted.

Bit	Bit Name	Description
31	ENABLE	Counter enable
30:0	VALUE	Indicates the latency

7.8.23 Miscellaneous PCIE Bits (PCIE_MISC)

Address: 0x180F005C
Access: Read/Write
Reset: 0x0

This register contains miscellaneous spare CPU writable bits.

Bit	Bit Name	Description
31:0	BITS	Spare bits for the PCIE

7.9 WDMA Registers

Table 7-10 shows the mapping of the general DMA and Rx-related (WMAC interface) registers.

Table 7-10 WDMA Registers

Offset	Name	Description	Page
0x18100008	CR	Command	page 144
0x18100014	CFG	Configuration and Status	page 144
0x18100018	RXBUFPTR_THRESH	Rx DMA Data Buffer Pointer Threshold	page 145
0x1810001C	TXDPPTR_THRESH	Tx DMA Descriptor Pointer Threshold	page 145
0x18100020	MIRT	Maximum Interrupt Rate Threshold	page 145
0x18100024	IER	Interrupt Global Enable	page 146
0x18100028	TIMT	Tx Interrupt Mitigation Thresholds	page 146
0x1810002C	RIMT	Rx Interrupt Mitigation Thresholds	page 146
0x18100030	TXCFG	Transmit Configuration	page 147
0x18100034	RXCFG	Receive Configuration	page 148
0x18100040	MIBC	MIB Control	page 148
0x18100060	DATABUF	Data Buffer Length	page 149
0x18100064	GTT	Global Transmit Timeout	page 149
0x18100068	GTTM	Global Transmit Timeout Mode	page 149
0x1810006C	CST	Carrier Sense Timeout	page 150
0x18100070	RXDP_SIZE	Size of High and Low Priority	page 150
0x18100074	RX_QUEUE_HP_RXDP	Lower 32 bits of MAC Rx High Priority Queue RXDP Pointer	page 150
0x18100078	RX_QUEUE_LP_RXDP	Lower 32 bits of MAC Rx Low Priority Queue RXDP Pointer	page 150
0x18100080	ISR_P	Primary Interrupt Status	page 151
0x18100084	ISR_S0	Secondary Interrupt Status 0	page 152
0x18100088	ISR_S1	Secondary Interrupt Status 1	page 153
0x1810008C	ISR_S2	Secondary Interrupt Status 2	page 153
0x18100090	ISR_S3	Secondary Interrupt Status 3	page 154
0x18100094	ISR_S4	Secondary Interrupt Status 4	page 154
0x18100098	ISR_S5	Secondary Interrupt Status 5	page 155
0x181000A0	IMR_P	Primary Interrupt Mask	page 156
0x181000A4	IMR_S0	Secondary Interrupt Mask 0	page 157
0x181000A8	IMR_S1	Secondary Interrupt Mask 1	page 157
0x181000AC	IMR_S2	Secondary Interrupt Mask 2	page 158
0x181000B0	IMR_S3	Secondary Interrupt Mask 3	page 158
0x181000B4	IMR_S4	Secondary Interrupt Mask 4	page 159
0x181000B8	IMR_S5	Secondary Interrupt Mask 5	page 159
0x181000C0	ISR_P_RAC	Primary Interrupt Status Read-and-Clear	page 160
0x181000C4	ISR_S0_S	Secondary Interrupt Status 0 (Shadow Copy)	page 160
0x181000C8	ISR_S1_S	Secondary Interrupt Status 1 (Shadow Copy)	page 160
0x181000D0	ISR_S2_S	Secondary Interrupt Status 2 (Shadow Copy)	page 160
0x181000D4	ISR_S3_S	Secondary Interrupt Status 3 (Shadow Copy)	page 161
0x181000D8	ISR_S4_S	Secondary Interrupt Status 4 (Shadow Copy)	page 161
0x181000DC	ISR_S5_S	Secondary Interrupt Status 5 (Shadow Copy)	page 161

7.9.1 Command (CR)

Offset: 0x18100008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:11	RES	Reserved
10:7	SPARE	Spare bits
6	SWI	Software interrupt; this bit is one-shot/auto-cleared, so it always reads as 0
5	RXD	Rx disabled
4	RES	Reserved
3	RXE_HP	Receive enabled; this read-only bit indicates RxDMA status for HP frames. Set when SW writes to the RxBP register and cleared when RxDMA runs out of RxBP or RxD is asserted.
2	RXE_LP	Receive enabled; this read-only bit indicates RxDMA status for LP frames. Set when software writes to RXBUFPTR_THRESH register and cleared when RxDMA runs out of RXBUFPTR_THRESH or when RxD is asserted.
1:0	RES	Reserved

7.9.2 Configuration and Status (CFG)

Offset: 0x18100014
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:19	RES	0x0	Reserved	
18:17	FULL_THRESHOLD	0x0	PCIE core master request queue full threshold	
			0	Use default value of 4
			3:1	Use indicated value
16:13	RES	0x0	Reserved	
12	CFG_HALT_ACK	0x0	DMA halt status	
			0	DMA has not yet halted
			1	DMA has halted
11	CFG_HALT_REQ	0x0	DMA halt in preparation for reset request	
			0	DMA logic operates normally
			1	Request DMA logic to stop so software can reset the MAC; Bit [12] indicates when the halt has taken effect; the DMA halt is not recoverable; once software sets bit [11] to request a DMA halt, software must wait for bit [12] to be set and reset the MAC.
10	CFG_CLKGATE_DIS	0x0	0	Allow clock gating in all DMA blocks to operate normally
			1	Disable clock gating in all DMA blocks (for debug use)
9:6	RES	0x0	Reserved	
5	REG_CFG_ADHOC	0x0	0	AP mode: MAC is operating either as an AP or as a STA in a BSS
			1	Ad hoc mode: MAC is operating as a STA in an IBSS
4	MODE_MMR	0x0	Byteswap register access (MMR) data words	
3	MODE_RCV_DATA	0x0	Byteswap Rx data buffer words	
2	MODE_RCV_DESC	0x0	Byteswap Rx descriptor words	
1	MODE_XMIT_DATA	0x0	Byteswap Tx data buffer words	
0	MODE_XMIT_DESC	0x0	Byteswap Tx descriptor words	

7.9.3 Rx DMA Data Buffer Pointer Threshold (RXBUFPTR_THRESH)

Offset: 0x18100018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:15	RES	Reserved
14:8	LP_DATA	Indicates the Rx DMA data buffer pointer threshold. An interrupt will be asserted (if enabled) if the number of available data buffer pointers is less than this threshold. There is a separate threshold for high and low priority buffers.
7:4	RES	Reserved
3:0	HP_DATA	Indicates the Rx DMA data buffer pointer threshold. An interrupt will be asserted (if enabled) if the number of available data buffer pointers is less than this threshold. The high and low priority buffers have separate thresholds.

7.9.4 Tx DMA Descriptor Pointer Threshold (TXDPPTR_THRESH)

Offset: 0x1810001C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	DATA	Indicates the Tx DMA descriptor pointer threshold. An interrupt will be asserted (if enabled) if the number of available descriptor pointers for any of the 10 queues is less than this threshold.

7.9.5 Maximum Interrupt Rate Threshold (MIRT)

Offset: 0x18100020
Access: Read/Write
Reset: 0x0

This register is described in ms up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The maximum interrupt rate timer is started when either the TXINTM or RXIMTM status bits are set. TXMINTR or RXMINTR are asserted at this time. No future TXINTM or RXINTM events can cause the TXMINTR or TXMINTR to be asserted until this timer has expired. If both the TXINTM and RXINTM status bits are set while the timer is expired then the TXMINTR and RXMINTR will round robin between the two.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	INTR_RATE_THRESH	Maximum interrupt rate threshold

7.9.6 Interrupt Global Enable (IER)

Offset: 0x18100024
Access: Read/Write
Reset: 0x0

Enables hardware signalling of interrupts.

Bit	Bit Name	Description
31:1	RES	Reserved
0	ENABLE	Writing a 0 enables hardware signaling of interrupts

7.9.7 Tx Interrupt Mitigation Thresholds (TIMT)

Offset: 0x18100028
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	TX_FIRST_ PKT_THRESH	Tx first packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx first packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The first Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.
15:0	TX_LAST_ PKT_THRESH	Tx last packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx last packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The last Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.

7.9.8 Rx Interrupt Mitigation Thresholds (RIMT)

Offset: 0x1810002C
Access: Read/Write
Reset: Undefined

This register is in ms up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Rx last packet timer starts counting after any receive completion. If the timer is still counting when the next receive completion occurs, it resets and starts over. The last receive packet timer expires when either the last receive packet threshold equals the last receive packet timer count or the first receive packet threshold equals the first receive packet timer count.

Bit	Bit Name	Description
31:16	RX_FIRST_PKT_THRESH	Receive first packet threshold
15:0	RX_LAST_PKT_THRESH	Receive last packet threshold

7.9.9 Tx Configuration (TXCFG)

Offset: 0x18100030
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:18	RES	0x0	Reserved	
17	DIS_RETRY _UNDERRUN	0x1	Disable retry of underrun packets	
			0	Underrun packets will retry indefinitely
			1	Underrun packets will quit after first underrun attempt and write status indicating underrun
16:15	RES	0x0	Reserved	
14	RTCI_DIS	0x0	ReadyTime/CBR disable for QCUs 8-9. When the MAC is running at a clock rate ≤ 32 MHz, this bit must be set and only the ASAP frame scheduling policy may be selected for QCUs 8-9. QCUs 0-7 may continue to use any frame scheduling policy. Since in normal operation the MAC clock rate is at least 40 MHz, this is meant as a debugging mode only. Resets to 0x0.	
			0	MAC clock rate at least 33 MHz; enable all frame scheduling policies for all QCUs.
			1	MAC clock rate is ≤ 32 MHz. Disable non-ASAP FSP for QCUs 8-9 so that CBR and ReadyTime logic will continue to operate correctly for QCUs 0-7.
13	RES	0x0	Reserved	
12	ATIM_DEFER_DIS	0x0	Fragment burst vs. ATIM window defer disable. Note: PCU does not currently support ATIM	
			0	In ad hoc mode only, if the ATIM window starts in the middle of a fragment burst, halt the burst and allow frames from other DCUs (e.g., DCUs generating beacon and CAB traffic) to proceed. Resume fragment burst after the ATIM window ends and after following normal DCF channel access procedures.
			1	Pause the fragment burst for the duration of the ATIM window, but do not allow frames from other DCUs to appear on the air; meant for debugging mode or if a problem is suspected with the fragment burst deferral logic.
11	BCN_PAST_ATIM_DIS	0x0	Ad hoc beacon ATIM window transmission policy. Note: PCU does not currently support ATIM.	
			0	If the ATIM window ends before the station can send its beacon, the station cancels its beacon transmission.
			1	The station continues to attempt to send its beacon until it is able to do so, regardless of the status of the ATIM window.
10	RES	0x0	Reserved	
9:4	TXCFG_TRIGLVL	0x1	Frame trigger level; Specifies the minimum number (in units of 64 bytes) to DMA into the PCU TXFIFO before the PCU initiates sending the frame on the air. Resets to 0x1 (meaning 64 Bytes or a full frame, whichever occurs first).	
3	RES	0x0	Reserved	
2:0	TXCFG_DMA_SIZE	0x5	Maximum DMA request size for master reads	
			0	4 B
			1	8 B
			2	16 B
			3	32 B
			4	64 B
			5	128 B
			6	256 B
			7	Reserved

7.9.10 Rx Configuration (RXCFG)

Offset: 0x18100034
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:8	RES	0x0	Reserved
7	SLEEP_RX_ PEND_EN	0x0	Sleep entry policy when frames are pending in the PCU RX FIFO.
			0 The DMA receive logic requires all frames to be drained from the PCU RX FIFO before allowing the chip to sleep (the desired and default setting)
			1 The DMA receive logic will allow the chip to sleep even when frames are pending in the PCU Rx FIFO. This setting should not be needed in normal use and is meant primarily as a debugging mode or if a bug is suspected in the DMA tracking of the PCU RX FIFO frame count.
6	JUMBO_ WRAP_EN	0x0	Jumbo descriptor wrap mode.
			0 After reaching end of the jumbo descriptor's data buffer, go to next descriptor
			1 After reaching end of the jumbo descriptor's data buffer, retransfer into the same descriptor's data buffer again. This means the descriptor's data buffer will be overwritten with data from the PCU repeatedly in an infinite loop.
5	RES	0x0	Reserved
4:3	ZERO_LEN_ DMA_EN	0x0	Zero-length frame DMA enable
			0 Disable DMA of all zero-length frames. In this mode, the DMA logic suppresses all zero-length frames. Reception of zero-length frames is invisible to the host (they neither appear in host memory nor consume a Rx descriptor).
			1 Reserved
			2 Enable DMA of all zero-length frames. In this mode, all zero-length frames (chirps, double-chirps, and non-chirps) are DMAed into host memory just like normal (non-zero-length) frames.
			3 Reserved
2:0	DMA_SIZE	0x4	Maximum DMA size for master writes; (See the encodings for the register “Tx Configuration (TXCFG)” on page 147)

7.9.11 MIB Control (MIBC)

Offset: 0x18100040
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:4	RES	0x0	Reserved
3	STROBE	0x0	MIB counter strobe. This bit is a one-shot and always reads as zero. For writes:
			0 No effect
			1 Causes every MIB counter to increment by one
2	CLEAR	0x1	Clear all counters
1	FREEZE	0x1	Freeze all counters
0	RES	0x0	Reserved

7.9.12 Data Buffer Length (DATABUF)

Offset: 0x18100060
Access: Read/Write
Reset: 0xFFF

Bit	Name	Description
31:12	RES	Reserved
11:0	BUF_LEN	Data buffer length; specifies the maximum size of the frame (4 KBytes) that can be written to this buffer (in bytes). The first 48 bytes of the 4 KBytes are for Rx status, the rest are for payload.

7.9.13 Global Tx Timeout (GTT)

Offset: 0x18100064
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	LIMIT	Timeout limit (in TU: 1024 µs); on reset, this value is set to 25 TU.
15:0	COUNT	Timeout counter (in TU: 1024 µs). The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or else the counter increments every 1024 µs. If the timeout counter is equal to or greater than the timeout limit, the global transmit timeout interrupt is set in the ISR. This mechanism can be used to detect whether a Tx frame is ready and is unable to be transmitted.

7.9.14 Global Tx Timeout Mode (GTTM)

Offset: 0x18100068
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:5	RES	Reserved
4	DISABLE_QCU_FR_ ACTIVE_GTT	Before the GTT logic was using the PCI_TX_QCU_STATUS signal for GTT. It didn't seem to cover all the cases such as retry. If this bit is set then the original functionality will be enabled. If this bit is clear then QCU_FR_ACTIVE is used instead.
3	CST_USEC_STROBE	CST µs strobe; if this bit is set, then the CST timer will not use the TU based strobe but rather use the µs strobe to increment the timeout counter.
2	RESET_ON_CHAN_IDLE	Reset count on chan idle low. Reset count every time channel idle is low.
1	IGNORE_CHAN_IDLE	Ignore channel idle; if this bit is set then the GTT timer does not increment if the channel idle indicates the air is busy or NAV is still counting down.
0	USEC_STROBE	µs strobe; if this bit is set then the GTT timer will not use the TU based strobe but rather use a µs strobe to increment the timeout counter.

7.9.15 Carrier Sense Timeout (CST)

Offset: 0x1810006C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	LIMIT	Timeout limit (in TU: 1024 µs). On reset, this value is set to 0 TU.
15:0	COUNT	Timeout counter (in TU: 1024 µs). The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or the counter increments every 1024 µs. If the timeout counter is equal to or greater than the timeout limit then carrier sense timeout (CST) interrupt is set in the ISR. This counter starts counting if any queues are ready for Tx. It continues counting when RX_CLEAR is low, which is useful to determine whether the transmit is stuck because RX_CLEAR is low for a long time.

7.9.16 Size of High and Low Priority (RXDP_SIZE)

Offset: 0x18100070
Access: Read-Only
Reset: 0x0Indicates the size of high and low priority RXDP FIFOs.

Bit	Bit Name	Description
31:12	RES	Reserved
12:8	HP	Indicates the size of high priority RXDP FIFO
7:0	LP	Indicates the size of low priority RXDP FIFO

7.9.17 MAC Rx High Priority Queue RXDP Pointer (RX_QUEUE_HP_RXDP)

Offset: 0x18100074
Access: Read/Write
Reset: 0x0

Lower 32 bits of the MAC Rx high priority queue RXDP pointer.

Bit	Bit Name	Description
31:0	ADDR	MAC Rx high priority queue RXDP pointer

7.9.18 MAC Rx Low Priority Queue RXDP Pointer (RX_QUEUE_LP_RXDP)

Offset: 0x18100078
Access: Read/Write
Reset: 0x0

Lower 32 bits of MAC Rx Low Priority Queue RXDP pointer.

Bit	Bit Name	Description
31:0	ADDR	MAC Rx low priority queue RXDP pointer for the lower 32 bits

7.9.19 Primary Interrupt Status (ISR_P)

Offset: 0x18100080
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE

- The bits that are logical ORs of bits in the secondary ISRs are generated by logically ORing the secondary ISR bits after the secondary ISR bits have been masked with the appropriate bits from the corresponding secondary interrupt mask register.
- A write of one to a bit that is a logical OR of bits in a secondary ISR clears the secondary ISR bits from which the primary ISR bit is generated. E.g.: A write of a one to TXOK (bit [6]) in ISR_P clears all 10 TXOK bits in ISR_S0 (bits [9:0] of Secondary Interrupt Status 0 (ISR_S0), page 7-152).
- Only the bits in this register (ISR_P) and the primary interrupt mask register (Primary Interrupt Mask (IMR_P), page 7-156) control whether the MAC's interrupt output is asserted. The bits in the several secondary interrupt status/mask registers control what bits are set in the primary interrupt status register; however, the IMR_S* registers do not determine whether an interrupt is asserted. That is, an interrupt is asserted only when the logical AND of ISR_P and IMR_P is non-zero. The secondary interrupt mask/status registers affect which bits are set in ISR_P, but do not directly affect whether an interrupt is asserted.

Bit	Bit Name	Description
31	RXINTM	Rx completion interrupt after mitigation; either the first Rx packet or last Rx packet interrupt mitigation count has reached its threshold (see the register "Rx Interrupt Mitigation Thresholds (RIMT)" on page 146)
30	TXINTM	Tx completion interrupt after mitigation; either the first Tx packet or last Tx packet interrupt mitigation count has reached its threshold (see the register "Tx Interrupt Mitigation Thresholds (TIMT)" on page 146)
29	RES	Reserved
28	GENTMR	Logical OR of all GENERIC TIMER bits in the secondary ISR 5 which include the GENERIC_TIMER_TRIGGER[7:0], GENERIC_TIMER_THRESH[7:0], GENERIC_TIMER_OVERFLOW
27	QTRIG	Logical OR of all QTRIG bits in secondary ISR 4; indicates that at least one QCU's frame scheduling trigger event has occurred
26	QCBRURN	Logical OR of all QCBRURN bits in secondary ISR 3; indicates that at least one QCU's frame scheduling trigger event occurred when no frames were present on the queue
25	QCBROVF	Logical OR of all QCBROVF bits in secondary ISR 3; indicates that at least one QCU's CBR expired counter has reached the value of the QCU's CBR_OVR_THRESH parameter (see CBR Configuration (Q_CBRCFG), page 7-164 register bits [31:24])
24	RXMINTR	RXMINTR maximum receive interrupt rate; same as RXINTM with the added requirement that maximum interrupt rate count has reached its threshold; this interrupt alternates with TXMINTR.
23	BCNMISC	Miscellaneous beacon-related interrupts This bit is the Logical OR of the CST, GTT, TIM, CABEND, DTIMSYNC, BCNTO, CABTO, TSFOOR, DTIM, and TBTT_TIME bits in secondary ISR 2.
22:21	RES	Reserved
20	BNR	Beacon not ready Indicates that the QCU marked as being used for beacons received a DMA beacon alert when the queue contained no frames.

Bit	Bit Name	Description
19	TXMINTR	TXMINTR maximum Tx interrupt rate
18	BMISS	The PCU indicates that is has not received a beacon during the previous *N* (*N* is programmable) beacon periods
17	BRSSI	The PCU indicates that the RSSI of a beacon it has received has fallen below a programmable threshold
16	SWBA	The PCU has signalled a software beacon alert
15	RXKCM	Key cache miss; a frame was received with a set key cache miss Rx status bit
14	RXPHY	The PHY signalled an error on a received frame
13	SWI	Software interrupt signalled; see the register “Command (CR)” on page 144
12	MIB	One of the MIB regs has reached its threshold
11	TXURN	Logical OR of all TXURN bits in secondary ISR 2. Indicates that the PCU reported a txfifo underrun for at least one QCU’s frame
10	TXEOL	Logical OR of all TXEOL bits in secondary ISR 1; indicates that at least one Tx desc fetch state machine has no more Tx descs available
9	RES	Reserved
8	TXERR	Logical OR of all TXERR bits in secondary ISR 1; indicates that at least one frame was completed with an error, regardless of whether the InterReq bit was set
7	RES	Reserved
6	TXOK	Logical OR of all TXOK bits in secondary ISR 0; indicates that at least one frame was completed with no errors and at the requested rate, regardless of whether the InterReq bit was set.
5	RXORN	RxFIFO overrrun
4	RXEOL	Rx descriptor fetch logic has no more Rx descs available
3	RXNOFR	No frame was received for RXNOFR timeout clocks
2	RXERR	The frame was received with errors
1	RXOK_LP	Low priority frame was received with no errors
0	RXOK_HP	High priority frame was received with no errors

7.9.20 Secondary Interrupt Status 0 (ISR_S0)

Offset: 0x18100084
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	TXOK[9]	TXOK for QCU 9
...	...	...
1	TXOK[1]	TXOK for QCU 1
0	TXOK[0]	TXOK for QCU 0

7.9.21 Secondary Interrupt Status 1 (ISR_S1)

Offset: 0x18100088
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	TXEOL[9]	TXEOL for QCU 9
...	...	...
17	TXEOL]1]	TXEOL for QCU 1
16	TXEOL[0]	TXEOL for QCU 0
15:10	RES	Reserved
9	TXERR[9]	TXERR for QCU 9
...	...	...
1	TXERR[1]	TXERR for QCU 1
0	TXERR[0]	TXERR for QCU 0

7.9.22 Secondary Interrupt Status 2 (ISR_S2)

Offset: 0x1810008C
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31	TBTT_TIME	TBTT-referenced timer interrupt; indicates the PCU's TBTT-referenced timer has elapsed.
30	TSFOOR	TSF out of range; indicates that the corrected TSF received from a beacon differs from the PCU's internal TSF by more than a (programmable) threshold
29	DTIM	A beacon was received with the DTIM bit set and a DTIM count value of zero. Beacons with a set DTIM bit but a non-zero DTIM count do not generate it.
28	CABTO	CAB timeout; a beacon was received that indicated that the STA should expect to receive CAB traffic. However, the PCU's CAB timeout expired either because the STA received no CAB traffic, or because the STA received some CAB traffic but never received a CAB frame with the more data bit clear in the frame control field (which would indicate the final CAB frame).
27	BCNTO	Beacon timeout; a TBTT occurred and the STA began waiting to receive a beacon, but no beacon was received before the PCU's beacon timeout expired
26	DTIMSYNC	DTIM synchronization lost; a beacon was received that was expected to be a DTIM but was not, or a beacon was received that was not expected to be a DTIM but was
25	CABEND	End of CAB traffic; a CAB frame was received with the more data bit clear in the frame control field
24	TIM	A beacon was received with the local STA's bit set in the TIM element
23	GTT	Global Tx timeout; indicates the GTT count ≥ than the GTT limit
22	CST	Carrier sense timeout; indicates the CST count ≥ than the CST limit
21:10	RES	Reserved
9	TXURN[9]	TXURN for QCU 9
...	...	...
1	TXURN[1]	TXURN for QCU 1
0	TXURN[0]	TXURN for QCU 0

7.9.23 Secondary Interrupt Status 3 (ISR_S3)

Offset: 0x18100090
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	QCBRURN[9]	QCBRURN for QCU 9
...	...	...
17	QCBRURN[1]	QCBRURN for QCU 1
16	QCBRURN[0]	QCBRURN for QCU 0
15:10	RES	Reserved
9	QCBROVF[9]	QCBROVF for QCU 9
1	QCBROVF[1]	QCBROVF for QCU 1
...	...	...
0	QCBROVF[0]	QCBROVF for QCU 0

7.9.24 Secondary Interrupt Status 4 (ISR_S4)

Offset: 0x18100094
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	QTRIG[9]	QTRIG for QCU 9
...	...	...
1	QTRIG[1]	QTRIG for QCU 1
0	QTRIG[0]	QTRIG for QCU 0

7.9.25 Secondary Interrupt Status 5 (ISR_S5)

Offset: 0x18100098
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE The trigger indicates that the TSF matched or exceeded the timer. The threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The GENERIC_TIMER 0 threshold was removed because timer 0 is special and does not generate threshold event.

Bit	Bit Name	Description
31	GENERIC_TIMER[15]	GENERIC_TIMER 15 threshold
...	...	...
17	GENERIC_TIMER[11]	GENERIC_TIMER 1 threshold
16	GENERIC_TIMER_OVERFLOW	GENERIC_TIMER overflow
15	GENERIC_TIMER_TRIGGER[15]	GENERIC_TIMER 15 trigger
...	...	...
1	GENERIC_TIMER_TRIGGER[1]	GENERIC_TIMER 1 trigger
0	GENERIC_TIMER_TRIGGER[0]	GENERIC_TIMER 0 trigger

7.9.26 Primary Interrupt Mask (IMR_P)

Offset: 0x181000A0
Access: Read/Write
Reset: 0x0

NOTE Only the bits in this register control whether the MAC's interrupt outputs are asserted. The bits in the secondary interrupt mask registers control what bits are set in the Primary Interrupt Mask (IMR_P), page 7-156 register; however, the IMR_S* registers do not determine whether an interrupt is asserted.

Bit	Bit Name	Description
31	RXINTM	RXINTM interrupt enable
30	TXINTM	TXINTM interrupt enable
29	RES	Reserved
28	GENTMR	GENTMR interrupt enable
27	QTRIG	QTRIG interrupt enable
26	QCBRURN	QCBRURN interrupt enable
25	QCBROVF	QCBROVF interrupt enable
24	RXMINTR	RXMINTR interrupt enable
23	BCNMISC	BCNMISC interrupt enable
22:21	RES	Reserved
20	BNR	BNR interrupt enable
19	TXMINTR	TXMINTR interrupt enable
18	BMISS	BMISS interrupt enable
17	BRSSI	BRSSI interrupt enable
16	SWBA	SWBA interrupt enable
15	RXKCM	RXKCM interrupt enable
14	RXPHY	RXPHY interrupt enable
13	SWI	SWI interrupt enable
12	MIB	MIB interrupt enable
11	TXURN	TXURN interrupt enable
10	TXEOL	TXEOL interrupt enable
9	TXNOFR	TXNOFR interrupt enable
8	TXERR	TXERR interrupt enable
7	RES	Reserved
6	TXOK	TXOK interrupt enable
5	RXORN	RXORN interrupt enable
4	RXEOL	RXEOL interrupt enable
3	RXNOFR	RXNOFR interrupt enable
2	RXERR	RXERR interrupt enable
1	RXOK_LP	RXOK_LP interrupt enable
0	RXOK_HP	RXOK_HP interrupt enable

7.9.27 Secondary Interrupt Mask 0 (IMR_S0)

Offset: 0x181000A4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	TXOK[9]	TXOK for QCU 9 interrupt enable
...	...	...
1	TXOK[1]	TXOK for QCU 1 interrupt enable
0	TXOK[0]	TXOK for QCU 0 interrupt enable

7.9.28 Secondary Interrupt Mask 1 (IMR_S1)

Offset: 0x181000A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	TXEOL[9]	TXEOL for QCU 9 interrupt enable
...	...	...
17	TXEOL[1]	TXEOL for QCU 1 interrupt enable
16	TXEOL[0]	TXEOL for QCU 0 interrupt enable
15:10	RES	Reserved
9	TXERR[9]	TXERR for QCU 9 interrupt enable
...	...	...
1	TXERR[1]	TXERR for QCU 1 interrupt enable
0	TXERR[0]	TXERR for QCU 0 interrupt enable

7.9.29 Secondary Interrupt Mask 2 (IMR_S2)

Offset: 0x181000AC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31	TBTT_TIME	TBTT_TIME interrupt enable
30	TSFOOR	TSFOOR interrupt enable
29	DTIM	DTIM interrupt enable
28	CABTO	CABTO interrupt enable
27	BCNTO	BCNTO interrupt enable
26	DTIMSYNC	DTIMSYNC interrupt enable
25	CABEND	CABEND interrupt enable
24	TIM	TIM interrupt enable
23	GTT	GTT interrupt enable
22	CST	CST interrupt enable
21:10	RES	Reserved
9	TXURN[9]	TXURN for QCU 9 interrupt enable
...	...	...
1	TXURN[1]	TXURN for QCU 1 interrupt enable
0	TXURN[0]	TXURN for QCU 0 interrupt enable

7.9.30 Secondary Interrupt Mask 3 (IMR_S3)

Offset: 0x181000B0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	QCBRURN[9]	QCBRURN for QCU 9 interrupt enable
...	...	...
17	QCBRURN[1]	QCBRURN for QCU 1 interrupt enable
16	QCBRURN[0]	QCBRURN for QCU 0 interrupt enable
15:10	RES	Reserved
9	QCBROVF[9]	QCBROVF for QCU 9 interrupt enable
...	...	...
1	QCBROVF[1]	QCBROVF for QCU 1 interrupt enable
0	QCBROVF[0]	QCBROVF for QCU 0 interrupt enable

7.9.31 Secondary Interrupt Mask 4 (IMR_S4)

Offset: 0x181000B4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	QTRIG[9]	QTRIG for QCU 9 interrupt enable
...	...	...
1	QTRIG[1]	QTRIG for QCU 1 interrupt enable
0	QTRIG[0]	QTRIG for QCU 0 interrupt enable

7.9.32 Secondary Interrupt Mask 5 (IMR_S5)

Offset: 0x181000B8
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE The trigger indicates the TSF matched or exceeded the timer; threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The threshold GENERIC_TIMER 0 was removed because timer 0 is special and does not generate a threshold event.

Bit	Bit Name	Description
31	GENERIC_TIMER_THRESHOLD[15]	GENERIC_TIMER_THRESHOLD 15
30	GENERIC_TIMER_THRESHOLD[14]	GENERIC_TIMER_THRESHOLD 14
...	...	...
18	GENERIC_TIMER_THRESHOLD[2]	GENERIC_TIMER_THRESHOLD 2
17	GENERIC_TIMER_THRESHOLD[1]	GENERIC_TIMER_THRESHOLD 1
16	GENERIC_TIMER_OVERFLOW	GENERIC_TIMER overflow enable
15	GENERIC_TIMER_TRIGGER[15]	GENERIC_TIMER 15 trigger enable
...	...	...
1	GENERIC_TIMER_TRIGGER[1]	GENERIC_TIMER 1 trigger enable
0	GENERIC_TIMER_TRIGGER[0]	GENERIC_TIMER 0 trigger enable

7.9.33 Primary Interrupt Status Read and Clear (ISR_P_RAC)

Offset: 0x181000C0
Access: Read-and-Clear (No Write Access)
Reset: 0x0

NOTE A read from this location atomically:

- Copies all secondary ISRs into the corresponding secondary ISR shadow registers (ISR_S0 is copied to ISR_S0_S, etc.)
- Clears all bits of the primary ISR (ISR_P) and all bits of all secondary ISRs (ISR_S0–ISR_S4)
- Returns the contents of the primary ISR (ISR_P)

Bit	Bit Name	Description
31:0	ISR_P	Same format as Primary Interrupt Status (ISR_P)

7.9.34 Secondary Interrupt Status 0 (ISR_S0_S)

Offset: 0x181000C4
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 0 (ISR_S0)

7.9.35 Secondary Interrupt Status 1 (ISR_S1_S)

Offset: 0x181000C8
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 1 (ISR_S1)

7.9.36 Secondary Interrupt Status 2 (ISR_S2_S)

Offset: 0x181000D0
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 2 (ISR_S2)

7.9.37 Secondary Interrupt Status 3 (ISR_S3_S)

Offset: 0x181000D4
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 3 (ISR_S3)

7.9.38 Secondary Interrupt Status 4 (ISR_S4_S)

Offset: 0x181000D8
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 4 (ISR_S4)

7.9.39 Secondary Interrupt Status 5 (ISR_S5_S)

Offset: 0x181000DC
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 5 (ISR_S5)

7.10 WQCU Registers

The WQCU registers occupy the offset range 0x18100800-0x18100A40 in the QCA9531 address space. The QCA9531 has ten QCUs, numbered from 0 to 9.

Table 7-11 WQCU Registers

Offset	Name	Description	Page
0x18100800 + (*Q* << 2)[1]	Q_TXDP	Tx Queue Descriptor Pointer	page 162
0x18100830	Q_STATUS_RING_START	QCU_STATUS_RING_START_ ADDRESS Lower 32 bits of Address	page 163
0x18100834	Q_STATUS_RING_END	QCU_STATUS_RING_END_ADDR Lower 32 Bits of Address	page 163
0x18100838	Q_STATUS_RING_CURRENT	QCU_STATUS_RING_CURRENT Address	page 163
0x18100840	Q_TXE	Tx Queue Enable	page 163
0x18100880	Q_TXD	Tx Queue Disable	page 164
0x181008C0 + (*Q* << 2)[1]	Q_CBRCFG	CBR Configuration	page 164
0x18100900 + (*Q* << 2)[1]	Q_RDYTIMECFG	ReadyTime Configuration	page 164
0x18100940	Q_ONESHOTARM_SC	OneShotArm Set Control	page 165
0x18100980	Q_ONESHOTARM_CC	OneShotArm Clear Control	page 165
0x181009C0 + (*Q* << 2)[1]	Q_MISC	Miscellaneous QCU Settings	page 166
0x18100A00 + (*Q* << 2)[1]	Q_STS	Miscellaneous QCU Status	page 167
0x18100A40	Q_RDYTIMESHDN	ReadyTimeShutdown Status	page 167
0x18100A44	Q_MAC_QCU_DESC_CRC_ CHK	Descriptor CRC Check	page 168

1. The variable Q in the register addresses refers to the QCU number.

7.10.1 Tx Queue Descriptor (Q_TXDP)

Offset: 0x18100800 + (*Q* < 2)
Access: Read/Write
Cold Reset: Undefined
Warm Reset: Unaffected

Bit	Bit Name	Description
31:2	TXDP	Tx descriptor pointer
1:0	RES	Reserved

7.10.2 QCU_STATUS_RING_START_ADDRESS Lower 32 bits of Address (Q_STATUS_RING_START)

Offset: 0x18100830
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	Lower 32 bits of QCU_STATUS_RING_START_ADDR

7.10.3 QCU_STATUS_RING_END_ADDR Lower 32 Bits of Address (Q_STATUS_RING_END)

Offset: 0x18100834
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	Lower 32 bits of QCU_STATUS_RING_END_ADDR

7.10.4 QCU_STATUS_RING_CURRENT Address (Q_STATUS_RING_CURRENT)

Offset: 0x18100838
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	MAC_QCU_STATUS_RING_CURRENT_ADDRESS

7.10.5 Tx Queue Enable (Q_TXE)

Offset: 0x18100840
Access: Read/Write
Reset: 0x0

NOTE Writing a 1 in bit position *N* sets the TXE bit for QCU *N*. Writing a 0 in bit position *N* has no effect; in particular, it does not clear the TXE bit for the QCU.

Bit	Bit Name	Description
31:10	RES	Reserved
9	QCU_EN[9]	Enable QCU 9
...	...	...
1	QCU_EN[1]	Enable QCU 1
0	QCU_EN[0]	Enable QCU 0

7.10.6 Tx Queue Disable (Q_TXD)

Offset: 0x18100880
Access: Read/Write
Reset: 0x0

NOTE To stop transmission for QCU *Q*:

1. Write a 1 to QCU Q's TXD bit
2. Poll the Tx Queue Enable (Q_TXE), page 7-163 register until QCU *Q*'s TXE bit is clear
3. Poll QCU *Q*'s Misc. QCU Status (Q_STS), page 7-167 register until its pending frame count (Q_STS bits [1:0]) is zero
4. Write a 0 to QCU *Q*'s TXD bit

NOTE At this point, QCU *Q* has shut down and has no frames pending in its associated DCU.

NOTE Software must not write a 1 to a QCU's TXE bit when that QCU's TXD bit is set; an undefined operation will result. Software must ensure that it sets a QCU's TXE bit only when the QCU's TXD bit is clear. It is fine to write a 0 to TXE when TXD is set, but this has no effect on the QCU.

Bit	Bit Name	Description
31:10	RES	Reserved
9	QCU_DIS[9]	Disable QCU 9
...	...	...
1	QCU_DIS[1]	Disable QCU 1
0	QCU_DIS[0]	Disable QCU 0

7.10.7 CBR Configuration (Q_CBRCFG)

Offset: 0x181008C0 + (*Q* < 2)
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:24	CBR_OVF_THRESH	CBR overflow threshold
23:0	CBR_INTV	CBR interval in µs

7.10.8 ReadyTime Configuration (Q_RDYTIMECFG)

Offset: 0x18100900 + (*Q* < 2)
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:25	RES	Reserved	
24	RDYTIME_EN	ReadyTime enable	
		0	Disable ReadyTime use
		1	Enable ReadyTime use
23:0	RDYTIME_DUR	ReadyTime duration in µs	

7.10.9 OneShotArm Set Control (Q_ONESHOTARM_SC)

Offset: 0x18100940
Access: Read/Write
Reset: 0x0

NOTE A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	ONESHOTARM[9]	0	No effect
		1	Set OneShot arm bit for QCU 9
...	...	...	
1	ONESHOTARM[1]	0	No effect
		1	Set OneShot arm bit for QCU 1
0	ONESHOTARM[0]	0	No effect
		1	Set OneShot arm bit for QCU 0

7.10.10 OneShotArm Clear Control (Q_ONESHOTARM_CC)

Offset: 0x18100980
Access: Read/Write
Reset: 0x0

NOTE A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	ONESHOT_CLEAR[9]	0	No effect
		1	Clear OneShot arm bit for QCU 9
...	...	...	
1	ONESHOT_CLEAR[1]	0	No effect
		1	Clear OneShot arm bit for QCU 1
0	ONESHOT_CLEAR[0]	0	No effect
		1	Clear OneShot arm bit for QCU 0

7.10.11 Misc. QCU Settings (Q_MISC)

Offset: 0x181009C0 + (Q < 2)
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:12	RES	0x0	Reserved	
11	QCU_FR_ABORT_REQ_EN	0x1	DCU frame early termination request control	
			0	Never request early frame termination. Once a frame enters the DCU, it will remain active until its normal retry count has been reached or the frame succeeds.
			1	Allow this QCU to request early frame termination. When requested, the DCU attempts to complete processing the frame more quickly than it normally would.
10	CBR_EXP_CNT_CLR_EN	0x0	CBR expired counter force-clear control. Write-only (always reads as zero). Write of:	
			0	No effect
			1	Resets the CBR expired counter to zero
9	TXE_CLR_ON_CBR_END	0x0	ReadyTime expiration and VEOL handling policy	
			0	On expiration of ReadyTime or on VEOL, the TXE bit is not cleared. Only reaching the physical end-of-queue (that is, a NULL LinkPtr) will clear TXE
			1	The TXE bit is cleared on expiration of ReadyTime, on VEOL, and on reaching the physical end-of-queue
8	CBR_EXP_INC_LIMIT	0x0	CBR expired counter limit enable	
			0	The maximum CBR expired counter value is 255, but a CBROVF interrupt is generated when the counter reaches the value set in the CBR overflow threshold field of the CBR Configuration (Q_CBRCFG) register.
			1	The maximum CBR expired counter is limited to the value of the CBR overflow threshold field of the CBR Configuration (Q_CBRCFG) register. Note that in addition to limiting the maximum CBR expired counter to this value, a CBROVF interrupt is also generated when the CBR expired counter reaches the CBR overflow threshold.
7	QCU_IS_BCN	0x0	Beacon use indication. Indicates whether the QCU is being used for beacons	
			0	QCU is being used for non-beacon frames only
			1	QCU is being used for beacon frames (and possibly for non-beacon frames)
6	CBR_EXP_INC_DIS_NOBCNFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the QCU marked as being used for beacon transmission (i.e., the QCU that has bit [7] set in its Misc. QCU Settings (Q_MISC) register) contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the beacon queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the beacon queue is valid (the beacon queue is valid whenever its TXE is asserted)
5	CBR_EXP_INC_DIS_NOFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the queue contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the queue is valid (the queue is valid whenever TXE is asserted)

Bit	Bit Name	Reset	Description	
4	ONESHOT_EN	0x0	OneShot enable	
			0	Disable OneShot function
			1	Enable OneShot function - Note that OneShot must not be enabled when the QCU is set to an ASAP frame scheduling policy.
3:0	FSP	0x0	Frame scheduling policy setting	
			0	ASAP- The QCU is enabled continuously.
			1	CBR - The QCU is enabled under control of the settings in the CBR Configuration (Q_CBRCFG) register.
			2	DBA-gated; the QCU is enabled at each occurrence of a DMA beacon alert.
			3	TIM-gated - The QCU will be enabled whenever: ■ In STA mode, the PCU indicates that a beacon frame has been received with the local STA's bit set in the TIM element ■ In IBSS mode, the PCU indicates that an ATIM frame has been received
			4	Beacon-sent-gated - The QCU will be enabled when the DCU that is marked as being used for beacon transmission (see bit [16] of the Misc. DCU-Specific Settings (D_MISC) register) indicates that it has sent the beacon frame on the air
			5	Beacon-received-gated - The QCU will be enabled when the PCU indicates that it has received a beacon.
			6	HCF Poll gated - The QCU will be enabled whenever the Rx HCF poll event occurs; the signals come from the PCU when a directed HCF poll frame type is received with valid FCS.
			15:7	Reserved

7.10.12 Misc. QCU Status (Q_STS)

Offset: 0x18100A00 + ($Q < 2$)
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:16	RES	Reserved
15:8	CBR_EXP	Current value of the CBR expired counter
7:2	RES	Reserved
1:0	FC	Pending frame count; Indicates the number of frames this QCU presently has pending in its associated DCU.

7.10.13 ReadyTimeShutdown Status (Q_RDYTIMESHDN)

Offset: 0x18100A40
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	READYTIME_SHUTDOWN[9]	ReadyTimeShutdown status for QCU 9
...	...	...

Bit	Bit Name	Description	
1	READYTIME_SHUTDOWN[1]	ReadyTimeShutdown status for QCU 1	
0	READYTIME_SHUTDOWN[0]	ReadyTimeShutdown status for QCU 0 On read, returns ReadyTimeShutdown indication. Write of:	
		0	No effect
		1	Set OneShot arm bit for QCU 0

7.10.14 Descriptor CRC Check (MAC_QCU_DESC_CRC_CHK)

Offset: 0x18100A44
Access: Read/Write
Reset: 0x1

Bit	Bit Name	Description	
31:1	RES	Reserved	
0	EN	QCU frame descriptor CRC check	
		0	Disable CRC check on the descriptor fetched from HOST
		1	Enable CRC check on the descriptor fetched from HOST

7.11 WDCU Registers

The WDCU registers occupy the offset range 0x18101000-0x181012F0 in the QCA9531 address space. The QCA9531 has ten DCUs, numbered from 0 to 9.

Table 7-12 WLAN DCU Registers

Offset	Name	Description	Page
0x18101000 + (*D* << 2)[1]	D_QCUMASK	QCU Mask	page 169
0x18101030	D_GBL_IFS_SIFS	DCU-Global SIFS	page 170
0x18101040 + (*D* << 2)[1]	D_LCL_IFS	DCU-Specific IFS Settings	page 170
0x18101070	D_GBL_IFS_SLOT	DCU-Global IFS Settings: Slot Duration	page 170
0x18101080 + (*D* << 2)[1]	D_RETRY_LIMIT	Retry Limits	page 171
0x181010B0	D_GBL_IFS_EIFS	DCU-Global IFS Settings: EIFS Duration	page 171
0x181010C0 + (*D* << 2)[1]	D_CHNTIME	ChannelTime Settings	page 171
0x181010F0	D_GBL_IFS_MISC	QCU Global IFS Miscellaneous	page 172
0x18101100 + (*D* << 2)[1]	D_MISC	Miscellaneous DCU-Specific Settings	page 173
0x18101140	D_SEQ	DCU Sequence	page 175
0x18101270	D_PAUSE	DCU Pause	page 176
0x181012F0	D_TXSLOTMASK	DCU Transmission Slot Mask	page 176
0x18101F00	SLEEP_STATUS	MAC Sleep Status	page 177
0x18101F04	LED_CONFIG	MAC LED Configuration	page 177

1. The variable *D* in the register addresses refers to the DCU number.

7.11.1 QCU Mask (D_QCUMASK)

Offset: 0x18101000 + (*D* < 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

NOTE To achieve lowest power consumption, software should set this register to 0x0 for all DCUs that are not in use. The hardware detects that the QCU mask is set to zero and shuts down certain logic in response, helping to save power.

Bit	Bit Name	Description
31:10	RES	Reserved
9:0	QCU_MASK	Setting bit *Q* means that QCU *Q* is associated with (i.e., feeds into) this DCU. These register have reset values which corresponding to a 1 to 1 mapping between QCUs and DCUs. A register offset of 0x1000 maps to 0x1, 0x1004 maps to 0x2, 0x1008 maps to 0x4, etc.

7.11.2 DCU-Global SIFS (D_GBL_IFS_SIFS)

Offset: 0x18101030
Access: Read/Write
Reset: 0x640

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	SIFS duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode

7.11.3 DCU-Specific IFS Settings (D_LCL_IFS)

Offset: 0x18101040 + ($D < 2$)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
When Long AIFS is 0:			
31:28	RES	0x0	Reserved
27:20	DATA_AIFS_D[7:0]	0x2	AIFS value, in slots beyond SIFS; e.g., a setting of 2 (the reset value) means AIFS is equal to DIFS. **NOTE** This field is 17 bits wide (including the 9 MSBs accessed using the AIFS field), but the maximum supported AIFS value is 0x1FFFC. Setting AIFS to 0x1FFFD, 0x1FFFE, or 0x1FFFF causes the DCU to hang.
19:10	DATA_CW_MAX	0x3FF	CW_MAX value; must be equal to a power of 2, minus 1
9:0	DATA_CW_MIN	0xF	CW_MIN value; must be equal to a power of 2, minus 1
When Long AIFS is 1:			
31:29	RES	0x0	Reserved
28	LONG_AIFS [DCU_IDX_D]	0x0	Long AIFS bit; used to read or write to the nine MSBs of the AIFS value
27:9	RES	0x0	Reserved
8:0	DATA_AIFS_D[16:8]	0x2	Upper nine bits of the AIFS value (see bits [27:20] listed in this register)

7.11.4 QCU Global IFS Slots (D_GBL_IFS_SLOT)

Offset: 0x18101070
Access: Read/Write
Reset: 0x360

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	Slot duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode)

7.11.5 Retry Limits (D_RETRY_LIMIT)

Offset: 0x18101080 + ($D < 2$)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
31:20	RES	0x20	Reserved
19:14	SDFL	0x20	STA data failure limit: Specifies the number of times a frame's data exchange may fail before CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
13:8	SRFL	0x20	STA RTS failure limit: Specifies the number of times a frame's RTS exchange may fail before the CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
7:4	RES	0x0	Reserved
3:0	FRFL	0x4	Frame RTS failure limit: Specifies the number of times a frame's RTS exchange may fail before the current transmission series is terminated. A frame's RTS exchange fails if RTS is enabled for the frame, but when the MAC sends the RTS on the air, no CTS is received. Note: A value of 0x0 is unsupported.

7.11.6 QCU Global IFS EIFS (D_GBL_IFS_EIFS)

Offset: 0x18101070
Access: Read/Write
Reset: 0x3480

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	EIFS duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode)

7.11.7 ChannelTime Settings (D_CHNTIME)

Offset: 0x181010C0 + ($D < 2$)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

Bit	Bit Name	Description
31:21	RES	Reserved
20	CHANNEL_TIME_EN	ChannelTime enable
19:0	DATA_CT_MMR	ChannelTime duration in µs

7.11.8 QCU Global IFS Miscellaneous (D_GBL_IFS_MISC)

Offset: 0x181010F0
Access: Read/Write
Reset: See field description

Determines which slice of the internal LFSR will be used to generate the random sequence used to determine backoff counts in the DCUs and scrambler seeds in the PCU. The intent is to have different stations have different LFSR slice values (perhaps by using some bits from the MAC address) to minimize the random sequence correlations among stations in the same BSS IBSS.

NOTE This field affects the MAC only when LFSR_SLICE_RANDOM_DIS (bit [24] of this register) is set. When random LFSR slice selection is enabled (default), it is ignored.

Bit	Bit Name	Reset	Description
31:30	RES	0x0	Reserved
29	SLOT_COUNT_ RST_UNCOND	0x0	Slot count reset policy. If set, slot count gets reset as soon as channel gets busy. If clear, slot count gets reset only after transmitting or receiving frame. Setting this bit will be helpful if performance is degraded by spur.
28	IGNORE_ BACKOFF	0x0	Ignore Back Off. Setting this bit will allow the DCU to ignore any backoff as well as EIFS. This should be set during fast channel change to guarantee low latency to flush the transmit pipe.
27	CHAN_SLOT_ ALWAYS	0x0	Force transmission always on slot boundaries. When bits [26:25] of this register are non-zero, the MAC will transmit on slot boundaries when the 802.11 spec requires it to do so. When bits [26:25] are not equal to 0x0 and this bit is non-zero, then the MAC will attempt to transmit on slot boundaries all the time, not just when the spec requires. This mainly affects the case in which a frame becomes available when the channel has been idle for an AIFS. If this bit is clear in this case, then the MAC will transmit immediately. If this bit is set, then the MAC will wait for the next slot boundary before transmitting. Note that the setting of this bit has no effect unless bits [26:25] are non-zero.
26:25	CHAN_SLOT_ WIN_DUR	0x0	Slot transmission window length. Under certain corner cases (most related to very slow PCI DMA), the MAC could send a frame not on a slot boundary, thus deslotting the network. The value in this field specifies the number of core clocks after a slot boundary during which the MAC is permitted to send a frame. Specified in units of 8 core clocks; if set to 0x0 (the reset value), the MAC is permitted to send at any point in the slot.
24	LFSR_SLICE_ RANDOM_DIS	0x0	Random LFSR slice selection disable. 0 Allow the IFS logic to randomly generate the LFSR slice select value (see bits [2:0] of this register). The random selection method is meant to ensure independence of the LFSR output values both for nodes on different PCI busses but on the same network as well as for multiple nodes connected to the same physical PCI bus. 1 Disable random LFSR slice selection. Instead, the value programmed into LFSR_SLICE_SEL (bits [2:0] of this register) will be used.
23:10	RES	0x0	Reserved
9:4	SIFS_DUR_ USEC	0x10	SIFS duration in Microseconds

Bit	Bit Name	Reset	Description
3	TURBO_MODE	0x0	Turbo mode indication. Software is required to keep this register consistent with the turbo non-turbo state of the overall system. In other words, this IS NOT a status bit generated by the MAC. Rather it is a control bit that must be maintained by software so that certain parts of the MAC that are sensitive to whether the system is in turbo mode will operate correctly. 0 Station is operating in non-turbo mode 1 Station is operating in turbo mode
2:0	LFSR_SLICE_SEL	0x0	LFSR slice select. Determines which slice of the internal LFSR generates the random sequence used to determine backoff counts in the DCUs and scrambler seeds in the PCU. The intent is to have different stations have different LFSR slice values (perhaps by using some bits from the MAC address) to minimize the random sequence correlations among stations in the same BSS IBSS. **NOTE** This field affects the MAC only when LFSR_SLICE_RANDOM_DIS (bit [24] of this register) is set. When random LFSR slice selection is enabled (the default), this field is ignored.

7.11.9 Misc. DCU-Specific Settings (D_MISC)

Offset: 0x18101100 + ($D < 2$)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
31:25	RES	0x0	Reserved
24	SIFS_BURST_CHAN_BUSY_IGNORE	0x1	SIFS burst medium sense policy. 0 MAC obeys medium busy during SIFS burst 1 MAC ignore medium busy during SIFS burst
23	RETRY_ON_BLOWN_IFS_EN	0x0	Blown IFS handling policy. This setting controls how the DCU handles the case in which the DMA of a frame takes so long that the IFS spacing is met before the frame trigger level is reached. 0 Send the frame on the air anyway (ignore the IFS violation); causes the frame to be sent on the air at a time that is later than called for in the 802.11 spec 1 Do not send the frame on the air. Instead, act as if the frame had been sent on the air but failed and initiate the retry procedure. A retry will be charged against the frame. If more retries are permitted, the frame will be retried. If the retry limit has been reached, the frame will fail.
22	VIRT_COLL_CW_INC_EN	0x0	Post-frame backoff disable. 0 DCU performs a backoff after each frame finishes, as required by the 802.11 spec 1 DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)
21	POST_BKOFF_SKIP	0x0	Post-frame backoff disable. 0 DCU performs a backoff after each frame finishes, as required by the 802.11 spec 1 DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)
20	SEQNUM_FREEZE	0x0	Sequence number increment disable. 0 Allow the DCU to use a normal sequence number progression (the DCU increments the sequence number for each new frame) 1 Force the sequence number to be frozen at its current value

Bit	Bit Name	Reset	Description	
19	LOCKOUT_ IGNORE	0x0	DCU arbiter lockout ignore control.	
			0	Obey DCU arbiter lockouts from higher-priority DCUs
			1	Ignore DCU arbiter lockouts from higher-priority DCUs (that is, allow the current DCU to arbitrate for access to the PCU even if one or more higher-priority DCUs is asserting a DCU arbiter lockout)
18	LOCKOUT_ GBL_EN	0x0	DCU arbiter lockout control	
			0	No lockout. Allows lower-priority DCUs to arbitrate for access to the PCU concurrently with this DCU.
			1	Intra-frame lockout only. Forces all lower-priority DCUs to defer arbitrating for access to the PCU while the current DCU arbitrates for access to the PCU or doing an intra-frame backoff.
			2	Global lockout. Forces all lower-priority DCUs to defer arbitration for access to the PCU when: ■ At least one QCU feeding to the current DCU has a frame ready ■ The DCU is actively processing a frame, including arbitrating for PCU access, performing intra- or post-frame backoff, DMAing frame data to the PCU, or waiting for the PCU to complete the frame.
			3	Reserved
17	ARB_ LOCKOUT_IF_ EN	0x0	DCU arbiter lockout control	
16	DCU_IS_BRN	0x0	Beacon use indication. Indicates whether the DCU is being used for beacons.	
			0	DCU is being used for non-beacon frames only
			1	DCU is being used for beacon frames only
15:14	VIRT_COL_ POLICY	0x0	Virtual collision handling policy. Resets to 0x0. 0 - 1 - 2 - Reserved 3 - Reserved	
			3:2	Reserved
			1	Ignore. Virtual collisions are ignored (i.e., the DCU immediately re-arbitrates for access to the PCU without doing a backoff and without incrementing the retry count)
			0	Default handling. A virtual collision is processed like a collision on the air except that the retry count for the frame is not incremented (that is, just do the backoff)
13	RES	0x0	Reserved	
12	BKOFF_PF	0x0	Backoff persistence factor setting.	
			0	New CW equals old CW
			1	Use binary-exponential CW progression
11	HCF_POLL_EN	0x0	HCF poll enable.	
			0	DCU operates in VDCF mode
			1	DCU operates in HCF mode
10	RES	0x0	Reserved	

Bit	Bit Name	Reset	Description	
9	FRAG_ BURST_ BKOFF_EN	0x0	Fragment burst backoff policy. This bit controls whether the DCU performs a backoff after each transmission of a fragment (that is, a frame with the MoreFrag bit set in the frame control field).	
			0	The DCU handles fragment bursts normally -- no backoff is performed after a successful transmission, and the next fragment is sent at SIFS.
			1	Modified handling. The DCU performs a backoff after all fragments, even those transmitted successfully. In addition, after the backoff count reaches zero, the DCU then follows the normal channel access procedure and sends at AIFS rather than at SIFS. This setting is intended to ease the use of fragment bursts in XR mode see bug 4454 for more details.
8	FRAG_ BURST_WAIT_ QCU_EN	0x0	Fragment burst frame starvation handling policy. This bit controls the DCU operation when the DCU is in the middle of a fragment burst and finds that the QCU sourcing the fragments does not have the next fragment available.	
			0	The DCU terminates the fragment burst. Note that when this occurs, the remaining fragments (when the QCU eventually has them available) will be sent as a separate fragment burst with a different sequence number
			1	The DCU waits for the QCU to have the next fragment available. While doing so, all other DCUs will be unable to transmit frames.
7	CW_RST_AT_ TS_END)DIS	0x0	End of transmission series CW reset policy. Note that this bit controls only whether the contention window is reset when transitioning from one transmission series to the next *within* a single frame. The CW is reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed).	
			0	Reset the CW to CW_MIN at the end of each intraframe transmission series.
			1	Do not reset the CW at the end of each intraframe transmission series.
6	SFC_RST_AT_ TS_END_EN	0x0	End of transmission series station RTS data failure count reset policy. Note that this bit controls only whether the two station failure counts are reset when transitioning from one transmission series to the next *within* a single frame. The counts are reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed).	
			0	Do not reset the station RTS failure count or the station data failure count at the end of each transmission series.
			1	Reset both the station RTS failure count and the station data failure count at the end of each transmission series
5:0	DATA_BKOFF _THRESH	0x2	Backoff threshold setting. Determines the backoff count at which the DCU will initiate arbitration for access to the PCU and commit to sending the frame.	

7.11.10 DCU Sequence (D_SEQ)

Offset: 0x18101140
Access: Read/Write
Reset: 0x0

MAC DCU sequence number register.

Bit	Bit Name	Description
31:12	RES	Reserved
11:0	NUM	Value of the sequence number to be inserted into the next frame. Shared across all DCUs.

7.11.11 DCU Pause (D_PAUSE)

Offset: 0x18101270
Access: Read/Write
Reset: See field description

MAC DCU pause register.

Bit	Bit Name	Reset	Description	
31:21	RES	0x0	Reserved	
20:17	SPARE	0x0	Spare bits	
16	STATUS	0x1	Transmit pause status. Resets to 0x1. 0 - 1 -	
			0	Transmit pause request has not yet taken effect. This means that some of the DCUs for which a transmission pause request has been issued via bits [9:0] of this register still are transmitting and have not yet paused.
			1	All DCUs for which a transmission pause request has been issued via bits [9:0] of this register, if any, have in fact paused their transmissions. Note that if no transmission pause request is pending (that is, bits [9:0] of this register are all set to 0), then this transmit pause status bit will be set to one.
15:10	RES	0x0	Reserved	
9:0	REQUEST	0x0	Request that some subset of the DCUs pause transmission. For bit D of this field (9<=D<=0.	
			0	Allow DCU D to continue to transmit normally
			1	Request that DCU D pause transmission as soon as it is able to do so.
11:0	NUM	Value of the sequence number to be inserted into the next frame. Shared across all DCUs.		

7.11.12 DCU Transmission Slot Mask (D_TXSLOTMASK)

Offset: 0x181012F0
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

Bit	Bit Name	Description	
31:16	RES	Reserved	
15	SLOT_TX[15]	Specifies whether transmission may start on slot numbers that are congruent to 15 (mod 16)	
		0	Transmission may start on such slots
		1	Transmission may not start on such slots
...	...	...	
1	SLOT_TX[1]	Specifies whether transmission may start on slot numbers that are congruent to 1 (mod 16)	
		0	Transmission may start on such slots
		1	Transmission may not start on such slots
0	SLOT_TX[0]	Specifies whether transmission may start on slot numbers that are congruent to 0 (mod 16)	
		0	Transmission may start on such slots
		1	Transmission may not start on such slots

7.11.13 MAC Sleep Status (SLEEP_STATUS)

Offset: 0x18101F00
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Sleep status

7.11.14 MAC LED Configuration (LED_CONFIG)

Offset: 0x18101F04
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	LED Configuration

7.12 WMAC Glue Registers

Table 7-13 summarizes the WMAC glue control registers.

Table 7-13 WMAC Glue Registers

Offset	Name	Description	Page
0x18104000	WMAC_GLUE_INTF_RESET_CONTROL	Interface Reset Control	page 179
0x18104008	WMAC_GLUE_INTF_INTR_SYNC_ENABLE	Synchronous Interrupt Enable	page 179
0x18104018	WMAC_GLUE_INTF_TIMEOUT	Interface Timeout	page 179
0x18104028	WMAC_GLUE_INTF_INTR_SYNC_CAUSE	Synchronous Interrupt Cause	page 179
0x1810402C	WMAC_GLUE_INTF_INTR_SYNC_ENABLE	Synchronous Interrupt Enable	page 180
0x18104030	WMAC_GLUE_INTF_INTR_ASYNC_MASK	Asynchronous Interrupt Mask	page 180
0x18104034	WMAC_GLUE_INTF_INTR_SYNC_MASK	Synchronous Interrupt Mask	page 180
0x18104038	WMAC_GLUE_INTF_INTR_ASYNC_ CAUSE	Asynchronous Interrupt Cause	page 180
0x1810403C	WMAC_GLUE_INTF_INTR_ASYNC_ ENABLE	Asynchronous Interrupt Enable	page 181
0x18104048	WMAC_GLUE_INTF_GPIO_IN	GPIO Input	page 181
0x1810404C	WMAC_GLUE_INTF_GPIO_INPUT_VALUE	WMAC Glue GPIO Input Value	page 181
0x18104050	WMAC_GLUE_INTF_SWCOM_GPIO_ FUNC_ENABLE	GPIO SWCOM Enable Function	page 181
0x1810405C	WMAC_GLUE_INTF_GPIO_INPUT_VALUE	WMAC Glue GPIO Input Value	page 182
0x18104074	WMAC_GLUE_INTF_GPIO_INPUT_STATE	Output Values from MAC to GPIO Pins	page 182
0x181040A0	WMAC_GLUE_INTF_MISC	WMAC Glue Miscellaneous	page 183
0x181040B4	WMAC_GLUE_INTF_MAC_TXAPSYNC	Synchronous AP Transmit	page 183
0x181040B8	WMAC_GLUE_INTF_MAC_TXSYNC_ INITIAL_SYNC_TMR	Synchronous Initial Timer	page 183
0x181040BC	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_CAUSE	Synchronous Priority Interrupt Cause	page 183
0x181040C0	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_ENABLE	Synchronous Priority Interrupt Enable	page 184
0x181040C4	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_MASK	Asynchronous Priority Interrupt Mask	page 184
0x181040C8	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_MASK	Synchronous Priority Interrupt Mask	page 184
0x181040CC	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_CAUSE	Asynchronous Priority Interrupt Cause	page 185
0x181040D4	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_ENABLE	Asynchronous Priority Interrupt Enable	page 185
0x181040F0	WMAC_GLUE_INTF_AXI_BYTE_SWAP	AXI to MAC and MAC to AXI Byte Swap Enable	page 185

7.12.1 Interface Reset Control (WMAC_GLUE_INTF_RESET_CONTROL)

Offset: 0x18104000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:2	RES	Reserved	
1	APB_RESET	0	Normal operation of the MAC APB interface
		1	Hold the MAC APB interface in reset
0	RES	Reserved	

7.12.2 Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)

Offset: 0x18104008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Writing a 1 to any bit in this register will allow the corresponding interrupt signal to set its corresponding bit in the synchronous interrupt cause register.

7.12.3 Interface Timeout (WMAC_GLUE_INTF_TIMEOUT)

Offset: 0x18104018
Access: Read/Write
Reset: 0x0

APB and AXI timeout counter.

Bit	Bit Name	Description
31:16	AXI_TIMEOUT_VAL	AXI timeout counter for DMA success
15:0	RES	Reserved

7.12.4 Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_SYNC_CAUSE)

Offset: 0x18104028
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in the synchronous mode. In order for any bit to be set in this register, the corresponding bit in the synchronous interrupt enable register must also be set.

7.12.5 Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)

Offset: 0x1810402C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the synchronous interrupt cause register.

7.12.6 Asynchronous Interrupt Mask (WMAC_GLUE_INTF_INTR_ASYNC_MASK)

Offset: 0x18104030
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a PCI/PCIE interrupt provided that the corresponding Async Interrupt cause register bit is set. Note that for the Async Interrupt Cause register bit to be set, the corresponding Async Interrupt Enable register bit must also be set by the software

7.12.7 Synchronous Interrupt Mask (WMAC_GLUE_INTF_INTR_SYNC_MASK)

Offset: 0x18104034
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a PCI/PCIE interrupt provided that the corresponding Sync Interrupt cause register bit is set. Note that for the Sync Interrupt Cause register bit to be set, the corresponding Sync Interrupt Enable register bit must also be set by the software

7.12.8 Asynchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_ASYNC_CAUSE)

Offset: 0x18104038
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in the asynchronous mode. In order for any bit to be set in this register, the corresponding bit in the asynchronous interrupt enable register must also be set.

7.12.9 Asynchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_ASYNC_ENABLE)

Offset: 0x1810403C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous interrupt cause register.

7.12.10 GPIO Output (WMAC_GLUE_INTF_GPIO_OUT)

Offset: 0x18104048
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	OUT	Output value of each GPIO. This value is only used if the corresponding GPIO enable bits and GPIO output MUX registers are set correctly.

7.12.11 GPIO Input (WMAC_GLUE_INTF_GPIO_IN)

Offset: 0x1810404C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:11	RES	Reserved
10:0	IN	Input value of each GPIO. This value is only used if the corresponding GPIO enable bits and GPIO output MUX registers are set correctly.

7.12.12 GPIO SWCOM Enable Function (WMAC_GLUE_INTF_SWCOM_GPIO_FUNC_ENABLE)

Offset: 0x18104050
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	OUT	Enables GPIO output signals on SWCOM pins

7.12.13 WMAC Glue GPIO Input Value (WMAC_GLUE_INTF_GPIO_INPUT_VALUE)

Offset: 0x1810405C
Access: Read/Write
Reset: 0x0

WMAC Glue GPIO input value

Bit	Bit Name	Description	
31:17	RES	Reserved	
16	RTC_RESET_OVRD_ENABLE	0	RTC reset is entirely controlled by software
		1	RTC reset is controlled by GPIO input as well as software
15	RFSILENT_BB_L_ENABLE	0	Set RFSILENT_BB_L to default value
		1	Connect RFSILENT_BB_L to GPIO input
14	CLK25_ENABLE	0	Set CLK25 to default value
		1	Connect CLK25 to GPIO input
13:9	RES	Reserved	
8	GPIO_RST_TSF_ENABLE	0	Set RST_TSF to default value
		1	Connect RST_TSF to GPIO input
7	RFSILENT_BB_L_VAL	Default value of RFSILENT_BB_L input	
6	CLK25_VAL	Default value of CLK25 input	
5:0	RES	Reserved	

7.12.14 Output Values from MAC to GPIO Pins (WMAC_GLUE_INTF_GPIO_INPUT_STATE)

Offset: 0x18104074
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:7	RES	Reserved
6	TX_FRAME	Tx frame
5	RX_CLEAR_EXTERNAL	Rx clear external
4	LED_POWER_EN	LED power
3	LED_NETWORK_EN	LED network
2	RES	Reserved
1	PWR_LED	LED power
0	ATT_LED	ATT LED

7.12.15 WMAC Glue Miscellaneous (WMAC_GLUE_INTF_MISC)

Offset: 0x181040A0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	AT_SPEED_EN	WMAC glue miscellaneous

7.12.16 Synchronous AP Transmit (WMAC_GLUE_INTF_MAC_ TXAPSYNC)

Offset: 0x181040B8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	DATA	

7.12.17 Synchronous Initial Timer (WMAC_GLUE_INTF_MAC_ TXSYNC_INITIAL_SYNC_TMR)

Offset: 0x181040BC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DATA	

7.12.18 Synchronous Priority Interrupt Cause (WMAC_GLUE_INTF_ INTR_PRIORITY_SYNC_CAUSE)

Offset: 0x181040C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in synchronous mode. For any bit to be set in this register, the corresponding bit in the synchronous priority interrupt enable register must also be set by software:	
		Bit[0]	Tx interrupt triggered
		Bit[1]	Rx low priority interrupt triggered
		Bit[2]	Rx high priority interrupt triggered

7.12.19 Synchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_SYNC_ENABLE)

Offset: 0x181040C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous priority interrupt cause register:	
		Bit[0]	Tx interrupt enable
		Bit[1]	Rx low priority interrupt enable
		Bit[2]	Rx high priority interrupt enable

7.12.20 Asynchronous Priority Interrupt Mask (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_MASK)

Offset: 0x181040C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a CPU interrupt provided that the corresponding synchronous priority interrupt cause register bit is set. For the priority asynchronous interrupt cause register bit to be set, the corresponding asynchronous priority interrupt enable register bit must also be set by software:	
		Bit[0]	Tx interrupt mask
		Bit[1]	Rx low priority interrupt mask
		Bit[2]	Rx high priority interrupt mask

7.12.21 Synchronous Priority Interrupt Mask (WMAC_GLUE_INTF_INTR_PRIORITY_SYNC_MASK)

Offset: 0x181040CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a CPU interrupt provided that the corresponding synchronous priority interrupt cause register bit is set. For the priority asynchronous interrupt cause register bit to be set, the corresponding asynchronous priority interrupt enable register bit must also be set by software:	
		Bit[0]	Tx interrupt mask
		Bit[1]	Rx low priority interrupt mask
		Bit[2]	Rx high priority interrupt mask

7.12.22 Asynchronous Priority Interrupt Cause (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_CAUSE)

Offset: 0x181040D0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in asynchronous mode. For any bit to be set in this register, the corresponding bit in the asynchronous priority interrupt enable register must also be set by software:	
		Bit[0]	Tx interrupt triggered
		Bit[1]	Rx low priority interrupt triggered
		Bit[2]	Rx high priority interrupt triggered

7.12.23 Asynchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_ENABLE)

Offset: 0x181040D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous priority interrupt cause register:	
		Bit[0]	Tx interrupt enable
		Bit[1]	Rx low priority interrupt enable
		Bit[2]	Rx high priority interrupt enable

7.12.24 AXI to MAC and MAC to AXI Byte Swap Enable (WMAC_GLUE_INTF_AXI_BYTE_SWAP)

Offset: 0x181040F0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:1	RES	Reserved	
0	ENABLE	0	Do not swap data bytes of a 32-bit word, transferred between Memory and MAC (Default)
		1	Swap data bytes of a 32-bit word, transferred between Memory and MAC

7.13 RTC Registers

RTC registers occupy the offset range 0x18107000-0x18107FFC in the QCA9531 address space. Within this address range, the 0x18107040-0x18107058 registers are always on and available for software access regardless of whether the RTC is asleep. Table 7-14 summarizes the RTC registers for the QCA9531.

Table 7-14 RTC Summary

Address	Name	Description	Page
0x18107000	RESET_CONTROL	Reset Control	page 186
0x18107004	XTAL_CONTROL	XTAL Control	page 187
0x18107014	WLAN_PLL_CONTROL	WLAN PLL Control Settings	page 188
0x18107018	PLL_SETTLE	PLL Settling Time	page 189
0x1810701C	XTAL_SETTLE	Crystal Settling Time	page 189
0x18107020	CLOCK_OUT	Pin Clock Speed Control	page 190
0x18107028	RESET_CAUSE	Reset Cause	page 191
0x1810702C	SYSTEM_SLEEP	System Sleep Status	page 191
0x18107034	KEEP_AWAKE	Keep Awake Timer	page 192
0x18107038	DERIVED_RTC_CLK	Derived RTC Clock	page 192
0x1810703C	PLL_CONTROL2	PLL Control	page 193
0x18107040	RTC_SYNC_REGISTER	RTC Sync Reset	page 193
0x18107044	RTC_SYNC_STATUS	RTC Sync Status	page 193
0x18107048	RTC_SYNC_DERIVED	RTC Derived	page 194
0x1810704C	RTC_SYNC_FORCE_WAKE	RTC Force Wake	page 194
0x18107050	RTC_SYNC_INTR_CAUSE	RTC Interrupt Cause	page 194
0x18107054	RTC_SYNC_INTR_ENABLE	RTC Interrupt Enable	page 195
0x18107058	RTC_SYNC_INTR_MASK	RTC Interrupt Mask	page 195

7.13.1 Reset Control (RESET_CONTROL)

Address: 0x18107000
Access: Read/Write
Reset: 0x0

This register is used to control individual reset pulses to functional blocks. Software can hold any target block in reset by writing a 1 to the corresponding bit in this register. Reset will be held asserted to the target block as long as the corresponding bit is set. Multiple blocks may be held in reset simultaneously.

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	COLD_RST	Cold reset
2	WARM_ RESET	Warm reset
1	MAC_COLD_RST	Holds MAC block in cold reset, including BB and Radio. To clear this reset, SW must write a 0 and poll (for 62-92 µsecs) till this bit returns a 0.
0	MAC_WARM_RST	Holds MAC block in warm reset, including BB and radio

7.13.2 XTAL Control (XTAL_CONTROL)

Address: 0x18107004
Access: Read/Write
Reset: See field description

This register controls the analog crystal interface, the regulator and the clock source selection between an TCXO and a crystal.

Bit	Bit Name	Reset	Description
31:1	RES	0x0	Reserved
0	TXCO	0x0	When a TCXO device is used, software should set this field to 1 **WARNING** If this field is set to 1 when a crystal is being used, the high speed clock will stop and the chip will hang. 0 The chip is being driven by a crystal. 1 The chip is being driven by a TCXO device

7.13.3 Switching Regulator Control Bits 0 (REG_CONTROL0)

Address: 0x18107008
Access: Read/Write
Reset: See field description

This register contains the regulator control bits for switching.

Bit	Bit Name	Reset	Description
31:0	SWREG_BITS	0x0	Switching regulator control bits

7.13.4 WLAN PLL Control Settings (WLAN_PLL_CONTROL)

Address: 0x18107014
Access: Read/Write
Reset: See field description

Control settings for the PLL.: This register provides access to the PLL setup control signals. Any write to this register will freeze all high speed clocks for 61 µsec. The clock select lines and PLL control lines will change after 30.5 µsec, then another 30.5 µsec passes before enable to allow the clocks to settle.

PLL freq = (refclk/refdiv) * (div_int + div_frac*2^4/(2^18-1)) * (1/f(clk_sel)).

Before applying f(clk_sel) frequency range is 530 ~ 830 MHz.

NOTE This reset values of some fields in this register must be kept in sync with the corresponding fields in bb reg 31

Bit	Bit Name	Type	Reset	Description
31	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
30	MAC_ OVERRIDE	RW	0x0	When set, a MAC clock request will deassert PLLBYPASS even if the BYPASS field is set to 1. This can be set when its the preferable time to select the ON state to use the PLL, instead of the SOC_ON state.
29	NOPWD	RW	0x0	Prevents the PLL from being powered down when the PLLBYPASS is asserted or when in light sleep
28	UPDATING	RO	0x0	This bit is set during the PLL update process. After software writes to the PLL_CONTROL, it takes about 45 secs for the update to occur. Software may poll this bit to see if the update has taken place.
				0 PLL update is complete
				1 PLL update is pending
27	BYPASS	RW	0x00000001	Bypass PLL. This defaults to 1 for test purposes. Software must enable the PLL for normal operation.
26:25	CLK_SEL	RW	0x0	Controls the final PLL select.
				00 1
				01 2
				10 4
				11 Bypass
24:20	REFDIV	RW	0x00000005	Reference clock divider
19:6	DIV_FRAC	RW	0x0	Primary multiplier
5:0	DIV_INT	RW	0x2C	Primary multiplier

7.13.5 PLL Settling Time (PLL_SETTLE)

Address: 0x18107018
Access: Read/Write
Reset: See field description

This register sets the PLL settling time. The PLL requires some time to settle once it is powered up or reprogrammed. Each time the PLL parameters change due to a write to the PLL register or a system event which changes the PLL control, hardware will gate off the clocks for PLL_SETTLE time while the PLL stabilizes. Units are in REFCLK periods.

NOTE The reset values of this register must be kept in sync with the corresponding field in the baseband register 31.

Bit	Bit Name	Reset	Description
31:11	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
10:0	TIME	0x00000400	Time required for the PLL to settle. Units are in REFCLK periods, so the default value of 1024 will result in a 25.6 µsec settling time. This register should never be set less than 100.

7.13.6 Crystal Settling Time (XTAL_SETTLE)

Address: 0x1810701C
Access: Read/Write
Reset: See field description

This register sets the crystal settling time. The external crystal requires some time to settle once it is powered up. The power occurs as chip passes through the WAKEUP state, between OFF and ON or between SLEEP an ON. This exact time will vary and must be characterized, so this register is provided to allow the XTAL power up FSM to transition in the minimal correct time. The default value of 63 will always allow the XTAL to be fully settled before clocks are enabled, but this value can be set to a smaller value if hardware characterization approves. The timer will expire in (XTAL_SETTLE + 1) clocks. Unlike most registers, XTAL_SETTLE will retain its programmed value in the RTC block during reset. The value programmed in this register should be matched to the MAC register Sleep Clock 32 KHz Wake, field 'SLEEP32_WAKE_XTL_TIME'. Note that the MAC register value is in microseconds.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	TIME	0x00000001	Time required for the XTAL to settle. Units are in 30 µsecs, so the default value of 66 will result in 2.0 msec settling time. this register should never be set to 0.

7.13.7 Pin Clock Speed Control (CLOCK_OUT)

Address: 0x18107020
Access: Read/Write
Reset: See field description

This register controls the CLK_OUT pin clock speed. The output clock can be used for testing or to drive external components.

Bit	Bit Name	Reset	Description	
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6:4	DELAY	0x00000000	Controls the tap selection point for CLK_OUT on a delay line when SELECT[2] is set. 000 corresponds to the least delay while 111 corresponds to the maximum display (100 to 180 degree delay).	
3:0	SELECT	0x00000000	Controls the CLK_OUT speed. The binary MUX select decode is as follows:	
			0000	Low
			0001	CLKOBSOUT (from the PCIE PHY)
			0010	CLK80_ADC
			0011	CLK160_DAC
			0100	LCL20A (delayed as specified by the DELAY field)
			0101	LCL40A (delayed as specified by the DELAY field)
			0110	LCL80A (delayed as specified by the DELAY field)
			0111	LCL160A (delayed as specified by the DELAY field)
			1000	CLK128
			1001	XTLCLK
			1010	CLK80_ADC
			1011	CLK160_DAC
			1100	RTC_CLK_W (delayed as specified by the DELAY field)
			1101	REFCLK_W (delayed as specified by the DELAY field)
			1110	PCI_CLK_W (delayed as specified by the DELAY field)
			1111	PCIE_CORE_CLK_W (delayed as specified by the DELAY field)

7.13.8 Reset Cause (RESET_CAUSE)

Address: 0x18107028
Access: Read/Write
Reset: See field description

This register holds the cause of the last reset event.

Bit	Bit Name	Reset	Description	
31:2	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
1:0	LAST	0x00000000	The value of this register holds the cause of the last reset, as stated:	
			0	Hard reset of the RTC
			1	Software wrote to the RTC_CONTOL_COLD_RST register
			2	Software wrote to the RTC_CONTOL_WARM_RST register
			3	Reserved

7.13.9 System Sleep Status (SYSTEM_SLEEP)

Address: 0x1810702C
Access: Read/Write
Reset: See field description

This register contains the system sleep status bits. System sleep state is entered when all high frequency clocks are gated and the high frequency crystal is shut down. This register is used to indicate the status of each sleep control interface. If any bit in this control register is 0, sleep is not permitted. If all bits are 1, sleep is permitted. The system will enter sleep as soon as the CPU executes a WAIT instruction. The LIGHT field will gate clocks off in SLEEP, but will keep the crystal running for faster wakeup. The DISABLE field will prevent the chip from entering SLEEP.

Bit	Bit Name	Reset	Description	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	MAC_IF	0x00000001	THE MAC block sleep state	
			0	The MAC block will not allow a sleep state
			1	The MAC block has enabled the sleep state
1	LIGHT	0x00000000	Controls whether or not the crystal is turned off during SLEEP. If the crystal is turned off, power consumption is lowered during sleep but the wakeup time is controlled by XTAL_SETTLE. If the crystal remains on, power consumption is higher but the wakeup time is about 45 µs.	
			0	System sleep is DEEP, resulting in minimal power consumption
			1	System sleep will be LIGHT
0	DISABLE	0x0000000	Enables or disables the system sleep	
			0	System sleep is enabled
			1	System sleep is disabled

7.13.10 Keep Awake Timer (KEEP_AWAKE)

Address: 0x18107034
Access: Read/Write
Reset: See field description

This register ensures that the chip does not enter the SLEEP state until at least the COUNT cycles have passed from the time of the last CLK_REQ event.

Bit	Bit Name	Reset	Description
31:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	COUNT	0x00000000	The keep awake timer measured in 32 KHz (30.5 µsecs) cycles

7.13.11 Derived RTC Clock (DERIVED_RTC_CLK)

Address: 0x18107038
Access: Read/Write
Reset: See field description

This register creates a 32 KHz clock, derived from the HF. This register controls a scaled output clock which can be used to generate lower frequency clocks based on the reference clock. For example, a 32.768 KHz clock can be generated by setting the divisor of the high speed clock accordingly. The accuracy will depend on how the divisors align with this integer count. RTC will start up normally using the derived RTC_CLK, and will switch to the LF_XTAL if it detects an LF_XTAL (this behavior can be modified using the fields in the RTC_SYNC_DERIVED register) since the external LF_XTAL is mostly unsupported.

Bit	Bit Name	Type	Reset	Description	
31:19	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
18	EXTERNAL_DETECT	RO	0x0	Detects external 32 KHz XTALs; if a LF XTAL is detected and RTC_SYNC_DERIVED clear, the RTC automatically uses the external XTAL.	
				0	No XTAL is detected
				1	LFXTAL not detected
17:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15:1	PERIOD	RW	0x262	The period of the derived clock is 2 * (PERIOD + 1). The reset value creates a 30.55 sec clock if the REFCLK is 40 MHz. The 30.5 µs value is closer to 32.768 KHz. To set it to 30.5 µs, the PERIOD value should be 0x261. To set to 30.48 µs, the PERIOD should be 0x17C. HALF_CLK_LATENCY and TSF_INC fields in MAC PCU should also be set appropriately.	
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

7.13.12 PLL Control (PLL_CONTROL2)

Address: 0x1810703C
Access: Read/Write
Reset: See field description

This register provides access to the PLL setup control signals for the additional bits required for the PLL.

Bit	Bit Name	Type	Reset	Description
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:3	DIV_FRAC	RW	0x0	Additional fractional bits
2:0	DIV_INT	RW	0x0	Additional int bits

7.13.13 RTC Sync Reset (RTC_SYNC_RESET)

Address: 0x18107040
Access: Read/Write
Reset: See field description

This register sets the RTC reset, force sleep and force wakeup.

Bit	Bit Name	Type	Reset	Description	
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RESET	RW	0x0	Active low signal setting	
				0	RTC is currently resetting
				1	RTC is not currently resetting

7.13.14 RTC Sync Status (RTC_SYNC_STATUS)

Address: 0x18107044
Access: Read-Only
Reset: 0x0

This register denotes the current use of RTC.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_ CHANGING	PLL_CHANGING signal from RTC
4	WRESET	Denotes the RTC was accessed while the MAC is asleep
3	WAKEUP_STATE	RTC is in the wakeup state
2	SLEEP_STATE	RTC is in the sleep state
1	ON_STATE	RTC is in the on state
0	SHUTDOWN_STATE	RTC is in the shutdown state

7.13.15 RTC Derived (RTC_SYNC_DERIVED)

Address: 0x18107048
Access: Read/Write
Reset: See field description

This register is for the Derived RTC.

Bit	Bit Name	Reset	Description
31:2	RSVD	0x0	Reserved
1	FORCE	0x0	Force Derived RTC
0	BYPASS	0x0	Bypass the Derived RTC

7.13.16 RTC Force Wake (RTC_SYNC_FORCE_WAKE)

Address: 0x1810704C
Access: Read/Write
Reset: See field description

This register enables a Force Wake to the MAC.

Bit	Bit Name	Reset	Description
31:2	RSVD	0x0	Reserved
1	INTR	0x1	Allows a MAC interrupt to assert a force wake enable
0	ESABLE	0x1	Enables a Force Wake to the MAC

7.13.17 RTC Interrupt Cause (RTC_SYNC_INTR_CAUSE)

Address: 0x18107050
Access: Read/Write
Reset: 0x0

This register is a controller that works the same way as the host interface interrupt controller. Each bit in the interrupt cause register pertains to an event as described here. A write of 1 to any bit in this register will clear that bit in the interrupt cause register until the corresponding event occurs again.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

7.13.18 RTC Interrupt Enable (RTC_SYNC_INTR_ENABLE)

Address: 0x18107054
Access: Read/Write
Reset: 0x0

This register is used for the RTC interrupts. Writing a 1 to any bit in this register allows that bit in the interrupt cause register to be set when the corresponding event occurs. Writing a 0 to any bit in this register will automatically clear the corresponding bit in the interrupt cause register regardless of the corresponding event.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

7.13.19 RTC Interrupt Mask (RTC_SYNC_INTR_MASK)

Address: 0x18107058
Access: Read/Write
Reset: 0x0

This register is the mask for RTC interrupts. Writing a 1 to any bit in this register will allow the corresponding event to generate an RTC Interrupt to the host interface, which can be programmed to generate a system interrupt. The corresponding bit in the RTC Interrupt Enable register must also be set.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

7.14 WPCU Registers

Table 7-15 shows the mapping of the WPCU registers.

Table 7-15 WPCU Registers

Address	Name	Description	Page
0x18108000	WMAC_PCU_STA_ADDR_L32	STA Address Lower 32 Bits	page 199
0x18108004	WMAC_PCU_STA_ADDR_U16	STA Address Upper 16 Bits	page 199
0x18108008	WMAC_PCU_BSSID_L32	BSSID Lower 32 Bits	page 200
0x1810800C	WMAC_PCU_BSSID_U16	BSSID Upper 16 Bits	page 200
0x18108010	WMAC_PCU_BCN_RSSI_AVE	Beacon RSSI Average	page 200
0x18108014	WMAC_PCU_ACK_CTS_TIMEOUT	ACK and CTS Timeout	page 201
0x18108018	WMAC_PCU_BCN_RSSI_CTL	Beacon RSSI Control	page 201
0x1810801C	WMAC_PCU_USEC_LATENCY	Millisecond Counter and Rx/Tx Latency	page 201
0x18108020	WMAC_PCU_RESET_TSF	Reset TSF	page 202
0x18108038	WMAC_PCU_MAX_CFP_DUR	Maximum CFP Duration	page 202
0x1810803C	WMAC_PCU_RX_FILTER	Rx Filter	page 203
0x18108040	WMAC_PCU_MCAST_FILTER_L32	Multicast Filter Mask Lower 32 Bits	page 204
0x18108044	WMAC_PCU_MCAST_FILTER_U32	Multicast Filter Mask Upper 32 Bits	page 204
0x18108048	WMAC_PCU_DIAG_SW	Diagnostic Switches	page 204
0x1810804C	WMAC_PCU_TSF_L32	TSF Lower 32 Bits	page 205
0x18108050	WMAC_PCU_TSF_U32	TSF Upper 32 Bits	page 206
0x1810805C	WMAC_PCU_AES_MUTE_MASK_0	AES Mute Mask 0	page 206
0x18108060	WMAC_PCU_AES_MUTE_MASK_1	AES Mute Mask 1	page 206
0x18108070	DYM_MIMO_PWR_SAVE	Dynamic MIMO Power Save	page 206
0x18108080	WMAC_PCU_LAST_BEACON_TSF	Last Receive Beacon TSF	page 207
0x18108084	WMAC_PCU_NAV	Current NAV	page 207
0x18108088	WMAC_PCU_RTS_SUCCESS_CNT	Successful RTS Count	page 207
0x1810808C	WMAC_PCU_RTS_FAIL_CNT	Failed RTS Count	page 208
0x18108090	WMAC_PCU_ACK_FAIL_CNT	FAIL ACK Count	page 208
0x18108094	WMAC_PCU_FCS_FAIL_CNT	Failed FCS Count	page 208
0x18108098	WMAC_PCU_BEACON_CNT	Beacon Count	page 209
0x181080D4	WMAC_PCU_SLP1	Sleep 1	page 209
0x181080D8	WMAC_PCU_SLP2	Sleep 2	page 209
0x181080E0	WMAC_PCU_ADDR1_MASK_L32	Address 1 Mask Lower 32 Bits	page 210
0x181080E4	WMAC_PCU_ADDR1_MASK_U16	Address 1 Mask Upper 16 Bits	page 210
0x181080E8	WMAC_PCU_TPC	Tx Power Control	page 210
0x181080EC	WMAC_PCU_TX_FRAME_CNT	Tx Frame Counter	page 211
0x181080F0	WMAC_PCU_RX_FRAME_CNT	Rx Frame Counter	page 211

Table 7-15 WPCU Registers (cont.)

Address	Name	Description	Page
0x181080F4	WMAC_PCU_RX_CLEAR_CNT	Rx Clear Counter	page 211
0x181080F8	WMAC_PCU_CYCLE_CNT	Cycle Counter	page 211
0x181080FC	WMAC_PCU_QUIET_TIME_1	Quiet Time 1	page 212
0x18108100	WMAC_PCU_QUIET_TIME_2	Quiet Time 2	page 212
0x18108108	WMAC_PCU_QOS_NO_ACK	QoS NoACK	page 213
0x1810810C	WMAC_PCU_PHY_ERROR_MASK	PHY Error Mask	page 214
0x18108114	WMAC_PCU_RXBUF	Rx Buffer	page 214
0x18108118	WMAC_PCU_MIC_QOS_CONTROL	QoS Control	page 215
0x1810811C	WMAC_PCU_MIC_QOS_SELECT	Michael QoS Select	page 215
0x18108120	WMAC_PCU_MISC_MODE	Miscellaneous Mode	page 216
0x18108124	WMAC_PCU_FILTER_OFDM_CNT	Filtered OFDM Counter	page 217
0x18108128	WMAC_PCU_FILTER_CCK_CNT	Filtered CCK Counter	page 217
0x1810812C	WMAC_PCU_PHY_ERR_CNT_1	PHY Error Counter 1	page 218
0x18108130	WMAC_PCU_PHY_ERR_CNT_1_MASK	PHY Error Counter 1 Mask	page 218
0x18108134	WMAC_PCU_PHY_ERR_CNT_2	PHY Error Counter 2	page 218
0x18108138	WMAC_PCU_PHY_ERR_CNT_2_MASK	PHY Error Counter 2 Mask	page 219
0x1810813C	WMAC_PCU_TSF_THRESHOLD	TSF Threshold	page 219
0x18108144	WMAC_PCU_PHY_ERROR_EIFS_MASK	PHY Error EIFS Mask	page 219
0x18108168	WMAC_PCU_PHY_ERR_CNT_3	PHY Error Counter 3	page 220
0x1810816C	WMAC_PCU_PHY_ERR_CNT_3_MASK	PHY Error Counter 3 Mask	page 220
0x18108180	WMAC_PCU_GENERIC_TIMERS2	MAC PCU Generic Timers 2	page 220
0x181081C0	WMAC_PCU_GENERIC_TIMERS2_MODE	MAC PCU Generic Timers Mode 2	page 220
0x181081D0	WMAC_PCU_TXSIFS	SIFS, Tx Latency and ACK Shift	page 221
0x181081EC	WMAC_PCU_TXOP_X	TXOP for Non-QoS Frames	page 221
0x181081F0	WMAC_PCU_TXOP_0_3	TXOP for TID 0 to 3	page 221
0x181081F4	WMAC_PCU_TXOP_4_7	TXOP for TID 4 to 7	page 222
0x181081F8	WMAC_PCU_TXOP_8_11	TXOP for TID 8 to 11	page 222
0x181081FC	WMAC_PCU_TXOP_12_15	TXOP for TID 0 to 3	page 222
0x18108200	WMAC_PCU_GENERIC_TIMERS[0:15]	Generic Timers	page 223
0x18108240	WMAC_PCU_GENERIC_TIMERS_MODE	Generic Timers Mode	page 223
0x18108244	WMAC_PCU_SLP32_MODE	32 KHz Sleep Mode	page 224
0x18108248	WMAC_PCU_SLP32_WAKE	32 KHz Sleep Wake	page 224
0x1810824C	WMAC_PCU_SLP32_INC	32 KHz Sleep Increment	page 225
0x18108250	WMAC_PCU_SLP_MIB1	Sleep MIB Sleep Count	page 225
0x18108254	WMAC_PCU_SLP_MIB2	Sleep MIB Cycle Count	page 225
0x18108258	WMAC_PCU_SLP_MIB3	Sleep MIB Control Status	page 226

Table 7-15 WPCU Registers (cont.)

Address	Name	Description	Page
0x18108284	1µS	1 µs Clocks	page 226
0x1810829C	PHY_ERR_CNT_MASK_CONT	PHY Error Counter Continued	page 226
0x18108318	WMAC_PCU_20_40_MODE	Global Mode	page 227
0x18108328	WMAC_PCU_RX_CLEAR_DIFF_CNT	Difference RX_CLEAR Counter	page 227
0x1810832C	SELF_GEN_ANTENNA_MASK	Self Generated Antenna Mask	page 228
0x18108330	WMAC_PCU_BA_BAR_CONTROL	Control Registers for Block BA Control Fields	page 228
0x18108334	WMAC_PCU_LEGACY_PLCP_SPOOF	Legacy PLCP Spoof	page 229
0x18108338	WMAC_PCU_PHY_ERROR_MASK_CONT	PHY Error Mask and EIFS Mask	page 229
0x1810833C	WMAC_PCU_TX_TIMER	Tx Timer	page 230
0x18108348	ALT_AES_MUTE_MASK	Alternate AES QoS Mute Mask	page 230
0x18108390	TSF2_L32	TSF 2 Lower 32	page 231
0x18108394	TSF2_U32	TSF 2 Upper 32	page 231
0x1810839C	BSSID2_U16	BSSID 2 Upper 16	page 231
0x181083A4	WMAC_PCU_TID_TO_AC	TID Value Access Category	page 231
0x181083A8	WMAC_PCU_HP_QUEUE	High Priority Queue Control	page 232
0x181083C8	WMAC_PCU_HW_BCN_PROC1	Hardware Beacon Processing 1	page 233
0x181083CC	WMAC_PCU_HW_BCN_PROC2	Hardware Beacon Processing 2	page 233
0x18108800	WMAC_PCU_KEY_CACHE[0:1023]	Key Cache	page 234

7.14.1 STA Address Lower 32 Bits (WMAC_PCU_STA_ADDR_L32)

Offset: 0x18108000

Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	ADDR_31_0	Lower 32 bits of STA MAC address (PCU_STA_ADDR[31:0])

7.14.2 STA Address Upper 16 Bits (WMAC_PCU_STA_ADDR_U16)

Offset: 0x18108004
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

This register contains the lower 32 bits of the STA address.

Bit	Name	Reset	Description
31	REG_ADHOC_MCAST_SEARCH	0x0	Enables the key cache search for ad hoc MCAST packets
30	PCU_CBCIV_ENDIAN	0x0	Endianess of IV in CBC nonce
29	REG_PRESERVE_SEQNUM	0x1	Stops PCU from replacing the sequence number
28	PCU_KSRCH_MODE	0x0	Search key cache first. If not, match use offset for IV = 0, 1, 2, 3. ■ If KSRCH_MODE = 0 then do not search ■ If IV = 1, 2, or 3, then search ■ If IV = 0, do not search
27	REG_CRPT_MIC_ENABLE	0x0	Enables the checking and insertion of MIC in TKIP
26	SECTOR_SELF_GEN	0x0	Use the default antenna for self-generated frames
25	PCU_BSRATE_11B	0x0	802.11b base rate 0 Use all rates 1 Use only 1–2 MBps
24	PCU_ACKCTS_6MB	0x0	Use 6 MBps rate for ACK and CTS
23	RTS_USE_DEF	0x0	Use the default antenna to send RTS
22	DEFANT_UPDATE	0x0	Update the default antenna with the Tx antenna
21	USE_DEFANT	0x0	When the descriptor chooses auto-select mode (0000), use the default antenna to transmit
20	PCU_PCF	0x0	Set if associated AP is PCF capable
19	KEYSRCH_DIS	0x0	Disable key search
18	PW_SAVE	0x0	Set if STA is in power-save mode
17	PCU_ADHOC	0x0	Set if STA is in an ad hoc network
16	PCU_AP	0x0	Set if STA is an AP
15:0	PCU_STA_ADDR[47:32]	0x0	Upper 16 bits of STA MAC address

7.14.3 BSSID Lower 32 Bits (WMAC_PCU_BSSID_L32)

Offset: 0x18108008
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

This register contains the lower 32 bits of the BSS identification information.

Bit	Name	Description
31:0	pcu_bssid[31:0]	Lower 32 bits of BSSID

7.14.4 BSSID Upper 16 Bits (WMAC_PCU_BSSID_U16)

Offset: 0x1810800C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0
This register contains the upper 32 bits of the BSS identification information.

Bit	Name	Description
31:17	RES	Reserved
26:16	PCU_AID	Association ID
15:0	PCU_BSSID[47:32]	Upper 16 bits of BSSID

7.14.5 Beacon RSSI Average (WMAC_PCU_BCN_RSSI_AVE)

Offset: 0x18108010
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x800
BCN_RSSI_AVE

Bit	Name	Description
31:12	RES	Reserved
11:0	REG_BCN_RSSI_AVE	Holds the average RSSI with 1/16 dB resolution. The RSSI is averaged over multiple beacons which matched our BSSID. AVE_VALUE is 12 bits with 4 bits below the normal 8 bits. These lowest 4 bits provide for a resolution of 1/16 dB. The averaging function is depends on the BCN_RSSI_WEIGHT; determines the ratio of weight given to the current RSSI value compared to the average accumulated value.

7.14.6 ACK and CTS Timeout (WMAC_PCU_ACK_CTS_TIMEOUT)

Offset: 0x18108014
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29:16	PCU_CTS_TIMEOUT	Timeout while waiting for CTS (in cycles)
15:14	RES	Reserved
13:0	PCU_ACK_TIMEOUT	Timeout while waiting for ACK (in cycles)

7.14.7 Beacon RSSI Control (WMAC_PCU_BCN_RSSI_CTL)

Offset: 0x18108018
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29	REG_BCN_RSSI_RST_ STROBE	The BCN_RSSI_RESET clears BCN_RSSI_AVE, page 7-200 to aid in changing channels
28:24	REG_BCN_RSSI_WEIGHT	Used to calculate BCN_RSSI_AVE, page 7-200
23:16	RES	Reserved
15:8	PCU_BCN_MISS_THR	Threshold at which the beacon miss interrupt asserts. Because the beacon miss counter increments at TBTT, it increments to 1 before the first beacon.
7:0	PCU_RSSI_THR	The threshold at which the beacon low RSSI interrupt is asserted when the average RSSI (BCN_RSSI_AVE, page 7-200) below this level

7.14.8 Ms Counter and Rx/Tx Latency (WMAC_PCU_USEC_ LATENCY)

Offset: 0x1810801C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
31:29	RES	Reserved
28:23	PCU_RXDELAY	Baseband Rx latency to start of SIGNAL (in µs)
22:14	PCU_TXDELAY	Baseband Tx latency to start of timestamp in beacon frame (in µs)
13:8	RES	Reserved
7:0	USEC	USEC defines the number of clock cycles minus 1 in 1 microsecond. For example, 40 cycles of a 40 MHz clock is 1 µsec, so this register would be programmed to be 39. If the clock frequency is 40 5/9 MHz, the fractional components need to be defined. In this case the numerator (register: MAC_PCU_MAX_CFP_DUR, field: USEC_FRAC_ NUMERATOR) should be set to 5 and the denominator (register: MAC_PCU_MAX_CFP_ DUR, field: USEC_FRAC_DENOMINATOR) should be set to 9. The USEC field would still be 39. Note that the D_GBL_IFS_MISC register, microsecond duration field in the DMA block has been removed and the function is now shared with the PCU logic.

7.14.9 Reset TSF (WMAC_PCU_RESET_TSF)

Offset: 0x18108020
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Controls beacon operation by the PCU.

Bit	Name	Description
31:26	RES	Reserved
25	ONE_SHOT2	Setting this bit causes the TSF2 to reset. This register clears immediately after reset.
24	ONE_SHOT	Setting this bit causes the TSF to reset. This register clears immediately after reset.
23:0	RES	Reserved

7.14.10 Maximum CFP Duration (WMAC_PCU_MAX_CFP_DUR)

Offset: 0x18108038
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Contains the maximum time for a contention free period.

Bit	Name	Description
31:28	RES	Reserved
27	USEC_FRAC _DENOMINATOR[27:24]	See description for USEC[7:0] in Ms Counter and Rx/Tx Latency (WMAC_ PCU_USEC_LATENCY)
23:20	RES	Reserved
16:16	USEC_FRAC _DENOMINATOR[19:16]	See description for USEC[7:0] in Ms Counter and Rx/Tx Latency (WMAC_ PCU_USEC_LATENCY)
15:0	VALUE[15:0]	Maximum contention free period duration (in µs)

7.14.11 Rx Filter (WMAC_PCU_RX_FILTER)

Offset: 0x1810803C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

This register determines Rx frame filtering.

NOTE If any bit is set, the corresponding packet types pass the filter and DMA. All filter conditions except the promiscuous setting rely on the no early PHY error and protocol version being checked to ensure it is version 0.

Bit	Name	Reset	Description
31:20	RES	0x0	Reserved
19	CONTROL_ WRAPPER	0x1	Enable receiving directed frames for control wrapper frames
18	MGMT_ACTION_ MCAST	0x0	Enable receive of multicast frames for management action frames
17	HW_BCN_PROC _ENABLE	0x0	If set, the beacon frame with matching BSSID is filtered per hardware beacon processing logic. See the HW_BCN_PROC register.
16	RST_DLMTR_CNT _DISABLE	0x0	Clearing this bit resets the ST_DLMTR_CNT to 0 when RXSM.STATE leaves the START_DELIMITER state.
15	MCAST_BCAST_ALL	0x0	Enables receipt of all multicast and broadcast frames
14	PS_POLL	0x0	Enables receipt of PS-POLL
13	ASSUME_RADAR	0x1	If set, a legacy PLCP rate of 0 indicates a radar packet that will not be filtered
12	UNCOMPRESSED_ BA_BAR	0x0	Uncompressed directed block ACK request or block ACK
11	COMPRESSED_BA	0x0	Compressed directed block ACK
10	COMPRESSED_BAR	0x0	Compressed directed block ACK request
9	MY_BEACON	0x0	Retrieves any beacon frame with matching SSID
8	RES	0x0	Reserved
7	PROBE_REQ	0x0	Probe request enable; enables reception of all probe request frames
6	XR_POLL	0x0	Any multicast or broadcast frame with a frame type matching the XR_POLL_ TYPE register
5	PROMISCUOUS	0x0	Promiscuous Rx enable; enables reception of all frames, including errors
4	BEACON	0x0	Beacon frame enable; enables reception of beacon frames.
3	CONTROL	0x0	Control frame enable; enables reception of control frames
2	BROADCAST	0x0	Broadcast frame enable; enables reception of non beacon broadcast frames that originate from the BSS whose ID matches BSSID
1	MULTICAST	0x0	Multicast frame enable; enables reception of multicast frames that match the multicast filter
0	UNICAST	0x0	Unicast frame enable; enables reception of unicast (directed) frames that match the STA address

7.14.12 Multicast Filter Mask Lower 32 Bits (WMAC_PCU_MCAST_FILTER_L32)

Offset: 0x18108040
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask low. Lower 32 bits of multicast filter mask.

7.14.13 Multicast Filter Mask Upper 32 Bits (WMAC_PCU_MCAST_FILTER_U32)

Offset: 0x18108044
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask high. Upper 32 bits of multicast filter mask.

7.14.14 Diagnostic Switches (WMAC_PCU_DIAG_SW)

Offset: 0x18108048
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Controls the operation of the PCU, including enabling/disabling acknowledgements, CTS, transmission, reception, encryption, loopback, FCS, channel information, and scrambler seeds.

Bit	Name	Description
31:30	RES	Reserved
29	RX_CLEAR_EXT_LOW	Force the RX_CLEAR_EXT signal to appear to the MAC as being low
28	RX_CLEAR_CTL_LOW	Force the RX_CLEAR_CTL signal to appear to the MAC as being low
27	OBS_SEL_2	Observation point select.
26	SATURATE_CYCLE_CNT	The saturate cycle count bit, if set, causes the Cycle Counter (WMAC_PCU_CYCLE_CNT) register to saturate instead of shifting to the right by 1 every time the count reaches 0xFFFFFFFF. This saturate condition also holds the RX_CLEAR, RX_FRAME, and TX_FRAME counts.
25	FORCE_RX_ABORT	Force Rx abort bit in conjunction with Rx block aids quick channel change to shut down Rx. The force Rx abort bit kills with the Rx_abort any frame currently transferring between the MAC and baseband. while the RX block bit prevents any new frames from getting started.

Bit	Name	Description
24	DUAL_CHAIN_CHAN_INFO	Dual chain channel information
23	PHYERR_ENABLE_EIFS_CTL	Used frame and WAIT_WEP in the PCU_RX_ERR logic if this bit is set to 0
22	CHAN_IDLE_HIGH	Force channel idle high
21	IGNORE_NAV	Ignore virtual carrier sense (NAV)
20	RX_CLEAR_HIGH	Force RX_CLEAR high
19:18	OBS_SEL_1	Observation point select
17	ACCEPT_NON_V0	Enable or disable protocol field
16:9	RES	Reserved
8	DUMP_CHAN_INFO	Dump channel information
7	CORRUPT_FCS	Corrupt FCS
6	LOOP_BACK	Enable or disable Tx data loopback
5	HALT_RX	Enable or disable reception
4	NO_DECRYPT	Enable or disable decryption
3	NO_ENCRYPT	Enable or disable encryption
2	NO_CTS	Enable or disable CTS generation
1	NO_ACK	Enable or disable acknowledgement generation for all frames
0	PCU_INVALKEY_NOACK	Enable or disable acknowledgement when a valid key is not found for the received frames in the key cache.

7.14.15 TSF Lower 32 Bits (WMAC_PCU_TSF_L32)

Offset: 0x1810804C

Access: Hardware = Read/Write

Software = Read/Write

Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in μs. Writes to this register do not cause the TSF to change. Rather, the value is held in a temporary staging area until this register is written, at which point both the lower and upper parts of the TSF are loaded. A read result of 0xFFFFFFFF indicates that the read occurred before TSF logic came out of sleep. It may take up to 45 μs after the chip is brought out of sleep for the TSF logic to wake.

7.14.16 TSF Upper 32 Bits (WMAC_PCU_TSF_U32)

Offset: 0x18108050

Access: Hardware = Read/Write

Software = Read/Write

Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in µs

7.14.17 AES Mute Mask 0 (WMAC_PCU_AES_MUTE_MASK_0)

Offset: 0x1810805C

Access: Hardware = Read-Only

Software = Read/Write

Reset Value: See field description

Bit	Name	Reset	Description
31:16	QOS_MUTEMASK	0xFFFF	AES mute mask for TID field
15:0	FC_MUTEMASK	0x478F	AES mute mask for frame control field

7.14.18 AES Mute Mask 1 (WMAC_PCU_AES_MUTE_MASK_1)

Offset: 0x18108060

Access: Hardware = Read-Only

Software = Read/Write

Reset Value: See field description

Bit	Name	Reset	Description
31:16	FC_MGMT	0xE7FF	AES mute mask for management frame control field
15:0	SEQ_MUTEMASK	0x000F	AES mute mask for sequence number field

7.14.19 Dynamic MIMO Power Save (DYM_MIMO_PWR_SAVE)

Address: 0x18108070

Access: Read/Write

Reset: See field description

This register is for the MAC PCU dynamic MIMO power save.

Bit	Bit Name	Reset	Description
31:11	RES	0x0	Reserved
10:8	HI_PWR_CHAIN_MASK	0x3	The high power setting of the Rx chain mask
7	RES	0x0	Reserved
6:4	LOW_PWR_CHAIN_ MASK	0x1	The low power setting of the Rx chain mask

3	RES	0x0	Reserved
2	SW_CHAIN_MASK_SEL	0x0	The software selection of the dynamic MIMO power save
1	HW_CTRL_EN	0x0	Enable the hardware control of the dynamic MIMO power save
0	USE_MAC_CTRL	0x0	The Rx chain mask will be controlled by MAC

7.14.20 Last Receive Beacon TSF (MAC_PCU_LAST_BEACON_TSF)

Offset: 0x18108080
Access: Hardware = Write-only
Software = Read-Only
Reset Value: 0x0

This threshold register indicates the minimum amount of data required before initiating a transmission.

Bit	Name	Description
31:0	LAST_TSTP	Beacon timestamp. Lower 32 bits of timestamp of the last beacon received.

7.14.21 Current NAV (WMAC_PCU_NAV)

Offset: 0x18108084
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:26	RES	Reserved
25:0	CS_NAV	Current NAV value (in µs)

7.14.22 Successful RTS Count (WMAC_PCU_RTS_SUCCESS_CNT)

Offset: 0x18108088
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of successful RTS exchanges. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_OK	RTS/CTS exchange success counter

7.14.23 Failed RTS Count (WMAC_PCU_RTS_FAIL_CNT)

Offset: 0x1810808C
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed RTS exchanges. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_FAIL	RTS/CTS exchange failure counter

7.14.24 FAIL ACK Count (WMAC_PCU_ACK_FAIL_CNT)

Offset: 0x18108090
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed acknowledgements. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	ACK_FAIL	DATA/ACK failure counter

7.14.25 Failed FCS Count (WMAC_PCU_FCS_FAIL_CNT)

Offset: 0x18108094
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed frame check sequences. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	FCS_FAIL	FCS failure counter

7.14.26 Beacon Count (WMAC_PCU_BEACON_CNT)

Offset: 0x18108098
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of valid beacon frames received. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	BEACONCNT	Valid beacon counter

7.14.27 MAC PCU Sleep 1 (SLP1)

Offset: 0x181080D4
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

The Sleep 1 register in conjunction with the Sleep 2 (WMAC_PCU_SLP2) register, controls when the QCA9531 should wake when waiting for AP Rx traffic. Sleep registers are only used when the QCA9531 is in STA mode.

Bit	Name	Reset	Description
31:21	CAB_TIMEOUT	0x5	Time in 1/8 TU the PCU waits for CAB after receiving the beacon or the previous CAB; insures that if no CAB is received after the beacon or if a long gap occurs between CABs, CAB powersave state returns to idle.
20	RES	0x0	Reserved
19	ASSUME_DTIM	0x0	A mode bit which indicates whether to assume a beacon was missed when the SLP_BEACON_TIMEOUT occurs with no received beacons, in which case is assumes the DTIM was missed, and waits for CAB.
18:0	RES	0x0	Reserved

7.14.28 Sleep 2 (WMAC_PCU_SLP2)

Offset: 0x181080D8
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x2

Bit	Name	Description
31:21	BEACON_TIMEOUT	Time in 1/8 TU that the PCU waits for a beacon after waking up. If this time expires, the PCU woke due to SLP_NEXT_DTIM, and SLP_ASSUME_DTIM is active, then it assumes the beacon was missed and goes directly to watching for CAB. Otherwise when this time expires, the beacon powersave state returns to idle.
20:0	RES	Reserved

7.14.29 Address 1 Mask Lower 32 Bits (WMAC_PCU_ADDR1_MASK_L32)

Offset: 0x181080E0

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0xFFFFFFFF

This STA register provides multiple BSSID support when the QCA9531 is in AP mode.

Bit	Name	Description
31:0	STA_MASK_L	STA address mask lower 32-bit register. Provides multiple BSSID support.

7.14.30 Address 1 Mask Upper 16 Bits (WMAC_PCU_ADDR1_MASK_U16)

Offset: 0x181080E4

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0xFFFF

This STA register provides multiple BSSID support when the QCA9531 is in AP mode.

Bit	Name	Description
31:16	RES	Reserved
15:0	STA_MASK_L	STA address mask upper 16-bit register. Provides multiple BSSID support.

7.14.31 Tx Power Control (WMAC_PCU_TPC)

Offset: 0x181080E8

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x3F

The 6-bit Tx power control sent from the MAC to the baseband is typically controlled using the Tx descriptor field. But self-generated response frames such as ACK, CTS, and chirp that do not have a Tx descriptor use the values in the Tx power control register instead.

Bit	Name	Description
31:30	RES	Reserved
29:24	RPT_PWR	Tx power control for self-generated action/NoACK frame
23:22	RES	Reserved
21:16	CHIRP_PWR	Tx power control for chirp
15:14	RES	Reserved
13:8	CTS_PWR	Tx power control for CTS
7:6	RES	Reserved
5:0	ACK_PWR	Tx power control for ACK

7.14.32 Tx Frame Counter (WMAC_PCU_TX_FRAME_CNT)

Offset: 0x181080EC

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The Tx frame counter counts the number of cycles the TX_FRAME signal is active.

Bit	Name	Description
31:0	TX_FRAME_CNT	Counts the number of cycles the TX_FRAME signal is active

7.14.33 Rx Frame Counter (WMAC_PCU_RX_FRAME_CNT)

Offset: 0x181080F0

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The receive frame counter counts the number of cycles the RX_FRAME signal is active.

Bit	Name	Description
31:0	RX_FRAME_CNT	Counts the number of cycles the RX_FRAME signal is active

7.14.34 Rx Clear Counter (WMAC_PCU_RX_CLEAR_CNT)

Offset: 0x181080F4

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The receive clear counter counts the number of cycles the RX_CLEAR signal is not active.

Bit	Name	Description
31:0	RX_CLEAR_CNT	Counts the number of cycles the RX_CLEAR signal is low (not active)

7.14.35 Cycle Counter (WMAC_PCU_CYCLE_CNT)

Offset: 0x181080F8

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The cycle counter counts the number of clock cycles.

Bit	Name	Description
31:0	CYCLE_CNT	Counts the number of clock cycles

7.14.36 Quiet Time 1 (WMAC_PCU_QUIET_TIME_1)

Offset: 0x181080FC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

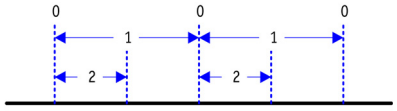
Bit	Name	Reset	Description
31:18	RES	0x0	Reserved
17	QUIET_ACK_CTS_ENABLE	0x1	If set, then the MAC sends an ACK or CTS in response to a received frame
16:0	RES	0x0	Reserved

7.14.37 Quiet Time 2 (WMAC_PCU_QUIET_TIME_2)

Offset: 0x18108100
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

NOTE QUIET_ENABLE is implemented as GENERIC_TIMER_ENABLE and NEXT_QUIET as GENERIC_TIMER_NEXT. QUIET_PERIOD is implemented as GENERIC_TIMER_PERIOD.



- 0 = NEXT_QUIET = TSF[31:0]
- 1 = QUIET_PERIOD
- 2 = QUIET_DURATION

(Chip remains awake during QUIET_DURATION)

Bit	Name	Description
31:16	QUIET_DURATION	The length of time in TUs (TU = 1024 µs) that the chip is required to be quiet
15:0	RES	Reserved

7.14.38 QoS NoACK (WMAC_PCU_QOS_NO_ACK)

Offset: 0x18108108

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x52

This register provides a mechanism to locate the NoACK information in the QoS field and determine which encoding means NoACK.

Bit	Name	Reset	Description	
31:9	RES	0x0	Reserved	
8:7	NOACK_ BYTE_ OFFSET	0x0	Number of bytes from the byte after end of the header of a data packet to the byte location where NoACK information is stored. (The end of the header is at byte offset 25 for 3-address packets and 31 for 4-address packets.)	
6:4	NOACK_BIT_ OFFSET	0x5	Offsets from the byte where the NoACK information should be stored; offset can range from 0 to 6 only	
3:0	NOACK_2_ BIT_VALUES	0x2	These values are of a two bit field that indicate NoACK	
			NOACK_2_BIT_VALUE	**Encoding Matching NoACK**
			xxx1	00
			xx1x	01
			x1xx	10
			1xxx	11

7.14.39 PHY Error Mask (WMAC_PCU_PHY_ERROR_MASK)

Offset: 0x1810810C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x2

NOTE Provides the ability to choose which PHY errors to filter from the BB; the number offsets into this register. If the mask value at the offset is 0, the error filters and does not show on the Rx queue.

Bit	Name	Description
31	ERROR CCK RESTART	CCK restart error
30	ERROR CCK SERVICE	CCK service error
29:28	RES	Reserved
27	ERROR CCK RATE_ILLEGAL	CCK illegal rate error
26	ERROR CCK HEADER_CRC	CCK CRC header error
25	ERROR CCK TIMING	False detection for CCK
24	RES	Reserved
23	ERROR OFDM RESTART	OFDM restart error
22	ERROR OFDM SERVICE	OFDM service error
21	ERROR OFDM POWER_DROP	OFDM power drop error
20	ERROR OFDM LENGTH_ILLEGAL	OFDM illegal length error
19	ERROR OFDM RATE_ILLEGAL	OFDM illegal rate error
18	ERROR OFDM SIGNAL_PARITY	OFDM signal parity error
17	ERROR OFDM TIMING	False detection for OFDM
16:8	RES	Reserved
7	ERROR TX_INTERRUPT_RX	Transmit interrupt
6	ERROR ABORT	Abort error
5	ERROR RADAR_DETECT	Radar detect error
4	ERROR PANIC	Panic error
3:1	RES	Reserved
0	ERROR TRANSMIT_UNDERRUN	Transmit underrun error

7.14.40 Rx Buffer (WMAC_PCU_RXBUF)

Offset: 0x18108114
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:12	RES	0x0	Reserved
11	REG_RD _ENABLE	0x0	When reading WMAC_PCU_BUF with this bit set, hardware returns the contents of the receive buffer.
10:0	HIGH_PRIORITY_ THRSHD	0x7FF	When number of valid entries in the receive buffer is larger than this threshold, the host interface logic gives the higher priority to receive side to prevent receive buffer overflow.

7.14.41 QoS Control (WMAC_PCU_MIC_QOS_CONTROL)

Offset: 0x18108118
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xAA

Bit	Name	Description	
31:17	RES	Reserved	
16	MIC_QOS_ENABLE	Enable MIC QoS control	
		0	Disable hardware Michael
		1	Enable hardware Michael
15:14	MIC_QOS_CONTROL [7]	MIC QoS control [7]. See options for MIC_QOS_CONTROL [0], page 7-215.	
13:12	MIC_QOS_CONTROL [6]	MIC QoS control [6]. See options for MIC_QOS_CONTROL [0], page 7-215.	
11:10	MIC_QOS_CONTROL [5]	MIC QoS control [5]. See options for MIC_QOS_CONTROL [0], page 7-215.	
9:8	MIC_QOS_CONTROL [4]	MIC QoS control [4]. See options for MIC_QOS_CONTROL [0], page 7-215.	
7:6	MIC_QOS_CONTROL [3]	MIC QoS control [3]. See options for MIC_QOS_CONTROL [0], page 7-215.	
5:4	MIC_QOS_CONTROL [2]	MIC QoS control [2]. See options for MIC_QOS_CONTROL [0], page 7-215.	
3:2	MIC_QOS_CONTROL [1]	MIC QoS control [1]. See options for MIC_QOS_CONTROL [0], page 7-215.	
1:0	MIC_QOS_CONTROL [0]	MIC QoS control [0]	
		0	Use 0 when calculating Michael
		1	Use 1 when calculating Michael
		2	Use MIC_QOS_SELECT when calculating Michael
		3	Use inverse of MIC_QOS_SELECT when calculating Michael

7.14.42 Michael QoS Select (WMAC_PCU_MIC_QOS_SELECT)

Offset: 0x1810811C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x3210

Bit	Name	Description
31:28	MIC_QOS_SELECT [7]	MIC QoS select [7]. Select the OOS TID bit when calculating Michael.
27:24	MIC_QOS_SELECT [6]	MIC QoS select [6]. Select the OOS TID bit when calculating Michael.
23:20	MIC_QOS_SELECT [5]	MIC QoS select [5]. Select the OOS TID bit when calculating Michael.
19:16	MIC_QOS_SELECT [4]	MIC QoS select [4]. Select the OOS TID bit when calculating Michael.
15:12	MIC_QOS_SELECT [3]	MIC QoS select [3]. Select the OOS TID bit when calculating Michael.
11:8	MIC_QOS_SELECT [2]	MIC QoS select [2]. Select the OOS TID bit when calculating Michael.
7:4	MIC_QOS_SELECT [1]	MIC QoS select [1]. Select the OOS TID bit when calculating Michael.
3:0	MIC_QOS_SELECT [0]	MIC QoS select [0]. Select the OOS TID bit when calculating Michael.

7.14.43 Miscellaneous Mode (WMAC_PCU_MISC_MODE)

Offset: 0x18108120
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:30	RES	0x0	Reserved
29	USE_EOP_PTR_ FOR_DMA_WR	0x0	When this bit is set, use LAST_EOP_PTR as an indication for DMA write When this bit is clear, use RD_PTR_TO_DMA instead.
28	ALWAYS_ PERFORM_KEY_ SEARCH	0x0	If this bit is set, key search is performed for every frame in an aggregate. If this bit is cleared, key search is only performed for the first frame of an aggregate. Unless the transmitter address is different between the frames in an aggregate. This bit has no effect on non-aggregate frame packets.
27	SEL_EVM	0x1	If set, the EVM field of the Rx descriptor status contains the EVM data received from the BB. If cleared, the EVM field of the Rx descriptor status contains 3 bytes of Legacy PLCP, 2 service bytes, and 6 bytes of HP PLCP.
26	CLEAR_BA_VALID	0x0	If set, the state of the block ACK storage is invalidated.
25	CLEAR_FIRST_HCF	0x0	If the CLEAR_FIRST_HCF bit is set then the FIRST_HCF state will be cleared. This should be set to enter fast channel change mode and cleared once fast channel change is over.
24	CLEAR_VMF	0x0	If the CLEAR_VMF bit is set then the VMF mode in the transmit state machine will be cleared. This should be set to enter fast channel change mode and cleared once fast channel change is over.
23	RX_HCF_POLL_ ENABLE	0x1	If the RX_HCF_POLL_ENABLE bit is set then the MAC is enabled to receive directed HCF polls. If this bit is not set the receive state machine will not tell the rest of the MAC that it has received a directed HCF poll.
22	HCF_POLL_ CANCELS_NAV	0x1	If the HCF_POLL_CANCELS_NAV bit is set, when a directed HCF poll is received, the current NAV is cancelled and HCF data burst can proceed at SIFS.
21	TBTT_PROTECT	0x1	If set, then the time from TBTT to 20 μs after TBTT is protected from transmit. Turn this off in ad hoc mode or if this MAC is used in the AP.
20:19	RES	0x0	Reserved
18	FORCE_QUIET_ COLLISION	0x0	If set, the PCU thinks that it is in quiet collision period, kills any transmit frame in progress, and prevents any new frame from starting.
17:15	RES	0x0	Reserved
14	MISS_BEACON_IN_ SLEEP	0x1	If the MISS_BEACON_IN_SLEEP bit is set, the missed beacon logic will not clear the missed beacon count when the chip is in sleep.
13	RES	0x0	Reserved
12	TXOP_TBTT _LIMIT_ENABLE	0x0	If this limit is set, then logic to limit the value of the duration to fit the time remaining in TXOP and time remaining until TBTT is turned on. This logic will also filter frames, which will exceed TXOP.
11	KC_RX_ANT	0x1	If KC_RX_ANT_UPDATE bit is set, the transmit antenna information in the key cache is updated based on the receive antenna results from baseband. Updates only occur when the selected antenna does not match the requested antenna which only occurs when the receive diversity is turned on in the baseband. This bit is only used with the dual chain antenna feature. The DUAL_CHAIN_ANT_MODE needs to be set to enable the KC_RX_ANT_ UPDATE.
10:6	RES	0x0	Reserved

Bit	Name	Reset	Description
5	RXSM2SVD_PRE_RST	0x0	If set to high when packets are received, SVD is always reset.
4	CCK_SIFS_MODE	0x0	If set, the chip assumes that it is using 802.11g mode where SIFS is set to 10 μs and non-CCK frames must add 6 to SIFS to make it CCK frames. This bit is needed in duration calculation, as is the SIFS_TIME register.
3	TX_ADD_TSF	0x0	If the TX_ADD_TSF bit is set, the TSF in the transmit packet will be added to the internal TSF value for transmit beacons and prob_response frames.
2	MIC_NEW_LOCATION_ENABLE	0x0	If MIC_NEW_LOCATION_ENABLE is set, the Tx Michael Key is assumed to be co-located in the same entry where the Rx Michael key is.
1	RES	0x0	Reserved
0	BSSID_MATCH_FORCE	0x0	If the BSSID_MATCH_FORCE bit is set, all logic based on matching the BSSID thinks that the BSSID matches.

7.14.44 Filtered OFDM Counter (WMAC_PCU_FILTER_OFDM_CNT)

Offset: 0x18108124
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The filtered OFDM counters use the MIB control signals.

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTOFDM_CNT	Counts the OFDM frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

7.14.45 Filtered CCK Counter (WMAC_PCU_FILTER_CCK_CNT)

Offset: 0x18108128
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTCCK_CNT	Counts the CCK frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

7.14.46 PHY Error Counter 1 (WMAC_PCU_PHY_ERR_CNT_1)

Offset: 0x1810812C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The PHY error counters count any PHY error matching the respective mask. The bits of 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to provide flexibility in counting. For example, if setting the mask bits to 0xFF0000FF, then all PHY errors from 0-7 and 24-31 are counted.

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT1	Counts any PHY error1 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. Counter saturates at the highest value and is writable. If the upper two counter bits are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

7.14.47 PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK)

Offset: 0x18108130
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK1	Counts any error that matches the PHY error1 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from [7:0] and [31:24] are counted).

7.14.48 PHY Error Counter 2 (WMAC_PCU_PHY_ERR_CNT_2)

Offset: 0x18108134
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT	Counts any error that matches the PHY error2 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

7.14.49 PHY Error Counter 2 Mask (WMAC_PCU_PHY_ERR_CNT_2_MASK)

Offset: 0x18108138

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ ERROR_ CNT_MASK2	Counts any PHY error2 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted, generating an interrupt.

7.14.50 TSF Threshold (WMAC_PCU_TSF_THRESHOLD)

Offset: 0x1810813C

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0xFFFF

Bit	Name	Description
31:16	RES	Reserved
15:0	TSF_THRESHOLD	Asserts the PCU_TSF_OUT_OF_RANGE_INTER if the corrected receive TSF in a beacon is different from the internal TSF by more than this threshold.

7.14.51 PHY Error EIFS Mask (WMAC_PCU_PHY_ERROR_EIFS_MASK)

Offset: 0x18108144

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	VALUE	This mask provides the ability to choose which PHY errors from the baseband cause EIFS delay. The error number is used as an offset into this mask. If the mask value at the offset is 1, then this error will not cause EIFS delay.

7.14.52 PHY Error Counter 3 (WMAC_PCU_PHY_ERR_CNT_3)

Offset: 0x18108168

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT3	Count of PHY errors that pass the PHY_ERR_CNT_3_MASK filter

7.14.53 PHY Error Counter 3 Mask (WMAC_PCU_PHY_ERR_CNT_3_MASK)

Offset: 0x1810816C

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK3	Mask of the PHY error number allowed to be counted

7.14.54 MAC PCU Generic Timers 2 (WMAC_PCU_GENERIC_TIMERS2)

Offset: 0x18108180
Access: Read/Write
Reset Value: Undefined

Bit	Name	Description
31:0	DATA	WMAC_PCU_GENERIC_TIMERS

7.14.55 MAC PCU Generic Timers Mode 2 (WMAC_PCU_GENERIC_TIMERS2_MODE)

Offset: 0x181081C0
Access: See field description
Reset Value: Undefined

Bit	Name	Access	Description
31:11	RES	RO	Reserved
10:8	OVERFLOW_INDEX	RO	Overflow index
7:0	ENABLE	RW	Enable

7.14.56 SIFS, Tx Latency and ACK Shift (WMAC_PCU_TXSIFS)

Offset: 0x181081D0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:15	RES	Reserved	
14:12	ACK_SHIFT	ACK_SHIFT is used to generate the ACK_TIME, which is used to generate the ACK_ SIFS_TIME. The ACK_TIME table in the hardware assumes a channel width of 2.5 MHz. This value should be 3 for CCK rates.	
		0	2.5 MHz
		1	5 MHz
		2	10 MHz (11j)
		3	20 MHz 802.11g
		4	40 MHz (turbo mode)
11:8	TX_LATENCY	TX_LATENCY is the latency in µs from TX_FRAME being asserted by the MAC to when the energy of the frame is on the air. This value is used to decrease the time to TBTT and time remaining in TXOP in the calculation to determine quiet collision.	
7:0	SIFS_TIME	SIFS_TIME is the number of µs in SIFS.	

7.14.57 TXOP for Non-QoS Frames (WMAC_PCU_TXOP_X)

Offset: 0x181081EC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SIFS_TIME	TXOP in units of 32 µs. A TXOP value exists for each QoS TID value. When a new burst starts, the TID is used to select one of the 16 TXOP values. This TXOP decrements until the end of the burst to make sure that the packets are not sent out by the time TXOP expires. This register is used for legacy non QoS frames.

7.14.58 TXOP for TID 0 to 3 (WMAC_PCU_TXOP_0_3)

Offset: 0x181081F0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_3	Value in units of 32 µs
23:16	VALUE_2	Value in units of 32 µs
15:8	VALUE_1	Value in units of 32 µs
7:0	VALUE_0	Value in units of 32 µs

7.14.59 TXOP for TID 4 to 7 (WMAC_PCU_TXOP_4_7)

Offset: 0x181081F4
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_7	Value in units of 32 µs
23:16	VALUE_6	Value in units of 32 µs
15:8	VALUE_5	Value in units of 32 µs
7:0	VALUE_4	Value in units of 32 µs

7.14.60 TXOP for TID 8 to 11 (WMAC_PCU_TXOP_8_11)

Offset: 0x181081F8
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_11	Value in units of 32 µs
23:16	VALUE_10	Value in units of 32 µs
15:8	VALUE_9	Value in units of 32 µs
7:0	VALUE_8	Value in units of 32 µs

7.14.61 TXOP for TID 0 to 3 (WMAC_PCU_TXOP_12_15)

Offset: 0x181081FC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_15	Value in units of 32 µs
23:16	VALUE_14	Value in units of 32 µs
15:8	VALUE_13	Value in units of 32 µs
7:0	VALUE_12	Value in units of 32 µs

7.14.62 Generic Timers (WMAC_PCU_GENERIC_TIMERS[0:15])

Offset: 0x18108200
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Address	Default	Description
0x8200–0x821C	0x0	GENERIC_TIMER_NEXT
0x8220–0x823C	0x0	GENERIC_TIMER_PERIOD

NOTE GENERIC _TIMER_0, unlike other generic timers, does not wake the MAC before timer expiration and its overflow mechanism does not generate an interrupt. Instead, it silently adds this period repeatedly until the next timer advances past the TSF. Thus when MAC wakes after sleeping for multiple TBTTs, the TGBTT does not assert repeatedly or cause the beacon miss count to jump.

Generic Timer	Function
0	TBTT
1	DMA beacon alert
2	SW beacon alert
3	Reserved
4	NEXT_TIM
5	NEXT_DTIM
6	Quiet time trigger
7	No dedicated function

7.14.63 Generic Timers Mode (WMAC_PCU_GENERIC_TIMERS_MODE)

Offset: 0x18108240
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: See Field Description

Bit	Name	Reset	Description
31:12	THRESH	0x100	Number of µs that generate a threshold interrupt if exceeded in TSF comparison
11	RES	0x0	Reserved
10:8	OVERFLOW_INDEX	UND	Indicates the last generic timer that overflowed
7:0	ENABLE	0x0	Timer enable

7.14.64 32 KHz Sleep Mode (WMAC_PCU_SLP32_MODE)

Offset: 0x18108244
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:25	RES	0x0	Reserved
24	TSF2_WRITE_ STATUS	0x1	This bit has the same function as TSF_WRITE_STATUS but this bit is the indication for TSF2.
23	FORCE_BIAS_ BLOCK_ON	0x0	When set, indicates that the Bias block is turned on and generating the reference current for PCIE PHY.
22	DISABLE_32KHZ	0x0	Indicates the 32 KHz clock is not used to control the TSF, but the MAC clock increments the TSF. Only used on AP class devices that do not go to sleep.
21	TSF_WRITE_STATUS	0x1	Since it takes such a long time to write the TSF, the effect of the TSF change may not occur until 10 µsec intervals after the write. Make sure that the write completes before the next read/write of the TSF is initiated. If the data is not stale, it may be read out. The SLEEP32_TSF_WRITE_STAT if set indicates that a configuration write or TSF reset (see register BEACON_PERIOD 0x8020) is in progress. Immediately after writing or resetting the TSF, this bit should be set between 15 to 45 µsec. If it does not get set, it may be because the TSF is being updated from a receive beacon and the writing or reset of the TSF will be lost. This is a read only register.
20	ENABLE	0x1	When set, indicates that the TSF should be allowed to increment on its own
19:0	HALF_CLK_LATENCY	0xF424	Defines the time in µsec from the detection of the falling edge of the 32 KHz clock to the rising edge of the 32 KHz clock. Whenever the TSF is updated by the configuration interface or by a receive beacon, the time in µsec is incremented until the falling edge of the 32 KHz clock then this time is added to the value of this register and is then is used to update the TSF. Since the 32 KHz clock is slow, if this modification is not done, the TSF will be off by 10s of µsecs. When there is no 32 KHz crystal the edges will be separated by 15.250 µsec which corresponds to the HALK_CLK_ LATENCY of 0xF400 for a 40 MHz reference clock.

7.14.65 32 KHz Sleep Wake (WMAC_PCU_SLP32_WAKE)

Offset: 0x18108248
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x800

Bit	Name	Description
31:16	RES	Reserved
15:0	XTL_TIME	Time in µs before a generic timer should expire that the wake signal asserts to the crystal wake logic. Add an extra 31 µs due to 32 KHz clock resolution.

7.14.66 32 KHz Sleep Increment (WMAC_PCU_SLP32_INC)

Offset: 0x1810824C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x1E848

Bit	Name	Description
31:20	RES	Reserved
19:0	TSF_INC	Time in $1/2^{12}$ of a µs the TSF increments on the rising edge of the 32 KHz clk (30.5176 µs period). The upper 8 bits are at µs resolution. The lower 12 bits are the fractional portion. $\frac{1 \text{ unit}}{1/212 \text{ ms}} = \frac{X}{30.5176 \text{ ms}}$ Where *X* = 125000, or 0x1E848 is the default setting for 32.768 MHz clock. The TSF_INC value needs to be programmed differently if there is no 32.768 KHz crystal and the 32 KHz clock is approximated using the 40 MHz reference clock. This is actually a more common system configuration. The closest to 30.5176 µsec using a divider on a 40 MHz reference clock is 30.500 µsec which corresponds to TSF_INC of 0x1E800. The HALF_CLK_LATENCY will then be 15.250 µsec which corresponds to 0x0F400.

7.14.67 Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1)

Offset: 0x18108250
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	SLEEP_CNT	Counts the number of 32 KHz clock cycles that the MAC has been asleep

7.14.68 Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2)

Offset: 0x18108254
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The SLEEP_CNT counts the number of 32 KHz clock cycles that the MAC has been asleep. The CYCLE_CNT counts the absolute number of 32 KHz clock cycles. When the CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. The SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing. The CLR_CNT will clear both the SLEEP_CNT and CYCLE_CNT. During the time that the clearing of these register are pending the PENDING will be asserted. SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the PENDING bit should be polled to verify any pending write has cleared.

Bit	Name	Description
31:0	CYCLE_CNT	Counts the absolute number of 32KHz clock cycles. When CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing.

7.14.69 Sleep MIB Control Status (WMAC_PCU_SLP_MIB3)

Offset: 0x18108258
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

See Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2).

Bit	Name	Description
31:2	RES	Reserved
1	PENDING	SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the pending bit should be polled to verify any pending write has cleared.
0	CLR_CNT	CLR_CNT clears both SLEEP_CNT and CYCLE_CNT. Pending is asserted while the clearing of these registers is pending.

7.14.70 1 µS Clocks (1µS)

Address: 0x18108284
Access: Read/Write
Reset: See field description

This register sets the number of clocks in one micro-second. See Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1) for more information.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved
6:0	SCALER	0x2C	The number of MAC clocks in one µs

7.14.71 PHY Error Counter Continued (PHY_ERR_CNT_MASK_CONT)

Address: 0x1810829C
Access: Read/Write
Reset: 0x0

This register is the MAC PCU PHY error counter 1, 2, and 3 continued. See PHY Error Counter 1 (WMAC_PCU_PHY_ERR_CNT_1).

Bit	Bit Name	Description
31:24	RES	Reserved
23:16	MASK3	Mask for PHY error count #1 for PHY errors 35 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.
15:8	MASK2	Mask for PHY error count #1 for PHY errors 39 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.
17:0	MASK1	Mask for PHY error count #1 for PHY errors 39 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.

7.14.72 Global Mode (WMAC_PCU_20_40_MODE)

Offset: 0x18108318

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

MAC PCU global mode register. There are only 4 allowable modes of operation:
A: Current HT2040 joined mode.
B: Current static HT20 mode.
C: Spec compliant mode.
D: Spec compliant but HT20 can Tx even when extension channel is busy mode.

Bit	Name	Description
31:16	RES	Reserved
15:4	PIFS_CYCLES	When EXT_PIFS_ENABLE is enabled, the PIFS_CYCLES register needs to be set to the appropriate value. In 11g mode PIFS is 10 µsec for SIFS and 9 µsec for slot. This register defines the number of clock cycles per PIFS. For HT2040 mode the number of cycles should be 1672 for 11g mode. For HT20 mode the number of cycles should be 836 for 11g mode.
3	SWAMPED_ FORCES_RX_ CLEAR_CTL_IDLE	Indicates that the baseband sees a strong signal on the extension channel and a weak signal on the control channel. This is likely caused by a transmitter on the extension channel that is so close that the spectral leakage onto the control channel is strong enough to cause RX_CLEAR on the control channel to indicate a busy signal.
2	TX_HT20_ON_ EXT_BUSY	When set, HT20 frames are permitted to be transmitted even when the extension channel has not been idle for PIFS. In fact it is permitted to transmit even if the extension channel is busy as long as the control channel is idle. The HT40 frames still depend on being idle for PIFS. This mode should only be enabled when capable of meeting the spectral mask requirement on the extension channel. To use this bit the JOINED_RX_CLEAR bit must be clear.
1	EXT_PIFS_ ENABLE	Enables the chips to be 802.11n compliant. The JOINED_RX_CLEAR must be clear to use this mode. When this bit is set, only the control channel RX_CLEAR is used to count down backoff. The only time that the extension channel is consulted is immediately prior to transmitting a frame. The PCU verifies that the extension channel has been clear for at least PIFS. See also PIFS_CYCLES register.
0	JOINED_RX_ CLEAR	Setting this bit causes the RX_CLEAR used in the MAC to be the AND of the control channel RX_CLEAR and the extension channel RX_CLEAR. If this bit is clear then the MAC will use only the control channel RX_CLEAR.

7.14.73 Difference RX_CLEAR Counter (WMAC_PCU_RX_CLEAR_ DIFF_CNT)

Offset: 0x18108328

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	RX_CLEAR_DIFF_ CNT	A cycle counter MIB register. On every cycle of the MAC clock, this counter increments every time the extension channel RX_CLEAR is low when the MAC is not actively transmitting or receiving. Due to a small lag between TX_FRAME and RX_CLEAR as well as between RX_CLEAR and RX_FRAME, the count may have some residual value even when no activity is on the extension channel.

7.14.74 Self Generated Antenna Mask (SELF_GEN_ANTENNA_MASK)

Address: 0x1810832C
Access: Read/Write
Reset: See field description

The antenna mask normally comes from the transmit descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Bit Name	Reset	Description
31:5	RES	0x0	Reserved
4	FORCE_CHAIN	0x0	Forces the SELF_GEN frame to be sent by chain 0 when location mode is on
3	ONE_RESP_EN	0x1	Forces the SELF_GEN frame to be sent by only one antenna when location mode is on
2:0	VALUE	0x7	

7.14.75 Control Registers for Block BA Control Fields (WMAC_PCU_BA_BAR_CONTROL)

Offset: 0x18108330
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

The MAC PCU control registers for block BA control fields. The antenna mask normally comes from the transmit descriptor. For self generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:13	RES	0x0	Reserved
12	UPDATE_BA_BITMAP_QOS_NULL	0x0	When set, it enables the update of BA_BITMAP on a QoS Null frame
11	TX_BA_CLEAR_BA_VALID	0x0	When set, enables the BA_VALID bits to be cleared upon transmit of the block ACK for an aggregate frame or on receiving a BAR
10	FORCE_NO_MATCH	0x0	Causes the BA logic to never find a match of previous saved bitmap in the memory
9	ACK_POLICY_VALUE	0x1	The value of the ACK policy bit
8	COMPRESSED_VALUE	0x1	The value of the compressed bit
7:4	ACK_POLICY_OFFSET	0x0	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the ACK policy bit.
3:0	COMPRESSED_OFFSET	0x2	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the COMPRESSED bit.

7.14.76 Legacy PLCP Spoof (WMAC_PCU_LEGACY_PLCP_SPOOF)

Offset: 0x18108334
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

The MAC PCU legacy PLCP spoof. The antenna mask normally comes from the transmit descriptor. For self generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:13	RES	0x0	Reserved
12:8	MIN_LENGTH	0xE	Defines the minimum spoofed legacy PLCP length
7:0	EIFS_MINUS_DIFS	0x0	Defines the number of µs to be subtracted from the transmit packet duration to provide fairness for legacy devices as well as HT devices.

7.14.77 PHY Error Mask and EIFS Mask (WMAC_PCU_PHY_ERROR_MASK_CONT)

Offset: 0x18108338
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

MAC PCU PHY error mask and EIFS mask continued. The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:24	AIFS_VALUE	This is a continuation of register MAC_PCU_PHY_ERROR_AIFS_MASK_VALUE. Bits [31] to [24] correspond to PHY errors 39 to 32. All others PHY errors above 39 will cause AIFS delay. Currently the baseband does not generate PHY errors above 39
23:16	EIFS_VALUE	Continuation of PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK), page 7-218. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All PHY errors above 39 cause EIFS delay.
15:8	RES	Reserved
7:0	MASK_VALUE	Continuation of PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK), page 7-218. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All PHY errors above 39 are filtered.

7.14.78 Tx Timer (WMAC_PCU_TX_TIMER)

Offset: 0x1810833C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: See field description

The MAC PCU transmit timer. The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:26	RES	0x0	Reserved
25	QUIET_TIMER_ ENABLE	0x1	The quiet timer is enabled when this bit is set to 1.
24:20	QUIET_TIMER	0x4	This timer is used to guarantee the transmit frame does not take less time than the values programmed in this timer in case a quiet collision occurs. The unit for this timer is µsecs.
19:16	RIFS_TIMER	0x0	This timer defines the RIFS interval in the unit of µsecs
15	TX_TIMER_ ENABLE	0x0	Enabled when this bit is set to 1
14:0	TX_TIMER	0x0	Guarantees the transmit frame does not take more time than the values programmed in this timer. The unit for this timer is in µsecs.

7.14.79 Alternate AES QoS Mute Mask (ALT_AES_MUTE_MASK)

Address: 0x18108348
Access: Read/Write
Reset: See field description

The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Bit Name	Reset	Description
31:16	QOS	0x008F	Used to mask off sections of the MAC header for use in the AES algorithm. The QoS control fields are bytes 25 and 26 of the three-address frame and bytes 31 and 32 of the 4 address frame. This alternate QoS mute mask is needed to support changes in 802.11n related to the setting the mask of bit 7 of the QoS field. For APs, the client device must allow selection of the QoS mute mask. Some may support this new mute mask and others will not.
15:0	RES	0x0	Reserved

7.14.80 TSF 2 Lower 32 (TSF2_L32)

Address: 0x18108390
Access: Read/Write
Reset: See field description

This register holds the lower 32 bits of the MAC PCU TSF2.

Bit	Bit Name	Reset	Description
31:0	VALUE	0xFFFFFFF	Same function as TSF and added support for dual BSSID/TSF which is needed for DirectConnect or Mesh networking

7.14.81 TSF 2 Upper 32 (TSF2_U32)

Address: 0x18108394
Access: Read/Write
Reset: See field description

This register holds the upper32 bits of the MAC PCU TSF2.

Bit	Bit Name	Reset	Description
31:0	VALUE	0xFFFFFFF	The upper 32 bits of the local clock

7.14.82 BSSID 2 Upper 16 (BSSID2_U16)

Address: 0x1810839C
Access: Read/Write
Reset: 0x0

This register holds the upper 16 bits of the MAC PCU BSSID2.

Bit	Bit Name	Description
31:17	RES	Reserved
16	ENABLE	Enables BSSID2
15:0	ADDR	The upper 16 bits of BSSID2 (PCU_BSSID2[47:32])

7.14.83 TID Value Access Category (WMAC_PCU_TID_TO_AC)

Offset: 0x181083A4
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:0	DATA	Maps the 16 user priority TID values to corresponding access category (AC). Two bits denote the AC for each TID. Bits [1:0] define the AC for TID 0 and next two bits are used for AC of TID 1, and finally bits [31:30] define the AC for TID 15. Default values are as specified in the 11e specification: TID 1 and 2 are BK, TID 0 and 3 are BK, TID 4 and 5 are VI, and TID 6 and 7 are V0. ACs:	
		00	BE
		01	BK
		10	VI
		11	VO

7.14.84 High Priority Queue Control (WMAC_PCU_HP_QUEUE)

Offset: 0x181083A8
Access: Read/Write
Reset Value: 0x0

Bit	Name	Reset	Description
31:23	RES	0x0	Reserved
22	NON_UAPSD_EN	0x1	If this bit is not set, only frames from UAPSD enabled devices having power management changes are placed into the HP QUEUE on power management change. Otherwise, all frames with power management changes are placed into the HP QUEUE. This bit is valid only if PM_ CHANGE bit is 1
21	PM_CHANGE	0x1	Place all frames which have power management state changes of a station into the HP QUEUE
20	UAPSD_EN	0x0	Enable detection and reporting in the Rx status of the UAPSD trigger frames and enable update of the PowerMgt bit in the key cache on error-free Rx-directed frames. If UAPSD enable is set for the AC of an error-free Rx directed QoS frame with the power management bit set, and the key cache entry of the sender has the PowerMgt bit set, it will be detected as a UAPSD trigger.
19:16	FRAME_SUBTYPE_ MASK0	0x0	Frame subtype mask for FRAME_SUBTYPE0, to be matched for the frame to be placed in high priority receive queue
15:12	FRAME_SUBTYPE0	0x0	Frame sub type to be matched for the frame to be placed in high priority receive queue
11:10	FRAME_TYPE_MASK0	0x3	Frame type mask for FRAME_TYPE0, to be matched for the frame to be placed in high priority receive queue
9:8	FRAME_TYPE0	0x0	Frame type to be matched for the frame to be placed in high priority receive queue
7	FRAME_BSSID_ MATCH0	0x0	If set to 1, frames with matching BSSID are only moved to high priority receive queue on a frame type match
6	FRAME_FILTER_ ENABLE0	0x0	Enables the mode where a frame is moved to high priority receive queue based on frame type
5	HPQON_UAPSD	0x0	Set to 1 if the Rx UAPSD trigger frame must be placed in the high priority Rx queue. Any frame that has a STA power management state change is also placed in the HP queue. HPQON_UAPSD = 1 with UAPSD_EN = 0 is not supported.
4	AC_MASK_VO	0x0	Set to 1 if BK traffic needs to be placed in high priority Rx queue
3	AC_MASK_VI	0x0	Set to 1 if VI traffic needs to be placed in high priority Rx queue
2	AC_MASK_BK	0x0	Set to 1 if BK traffic needs to be placed in high priority Rx queue
1	AC_MASK_BE	0x0	Set to 1 if BE traffic needs to be placed in high priority Rx queue
0	ENABLE	0x0	Enables high priority Rx queue

7.14.85 Hardware Beacon Processing 1 (HW_BCN_PROC1)

Address: 0x181083C8
Access: Read/Write
Reset: 0x0

This register is for Hardware Beacon Processing register 1.

Bit	Bit Name	Description
31:24	ELM2_ID	Element ID 2
23:16	ELM1_ID	Element ID 1
15:8	ELM0_ID	Element ID 0
7	EXCLUDE_ELM2	Exclude information with element ID ELM2 in CRC calculations
6	EXCLUDE_ELM1	Exclude information with element ID ELM1 in CRC calculations
5	EXCLUDE_ELM0	Exclude information with element ID ELM0 in CRC calculations
4	EXCLUDE_TIM_ELM	Exclude beacon TIME element in CRC calculations
3	EXCLUDE_CAP_INFO	Exclude beacon capability information in CRC calculations
2	EXCLUDE_BCN_INTVL	Exclude beacon intervals in CRC calculations
1	RESET_CRC	Reset the last beacon CRC calculated
0	CRC_ENABLE	Enables hardware beacon processing

7.14.86 Hardware Beacon Processing 2 (HW_BCN_PROC2)

Address: 0x181083CC
Access: Read/Write
Reset: See field description

This register is for Hardware Beacon Processing register 2.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved
23:16	ELM3_ID	0x0	Element ID 3
15:8	FILTER_INTERVAL	0x2	Filter interval for beacons
7:3	RES	0x0	Reserved
2	EXCLUDE_ELM3	0x0	Exclude information with element ID ELM3 in CRC calculations
1	RESET_INTERVAL	0x0	Reset internal interval counter
0	FILTER_INTERVAL_ENABLE	0x0	Enable filtering beacons based on filter intervals

7.14.87 Key Cache (WMAC_PCU_KEY_CACHE[0:1023])

Offset: 0x18108800
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Table 7-16 Offset to First Dword of *N*th Key [1]

Intra Key	Offset Bits	Description	
8*N* + 00	31:0	Key[31:0]	
8*N* + 04	15:0	Key[47:32]	
8*N* + 08	31:0	Key[79:48]	
8*N* + 0C	15:0	Key[95:79]	
8*N* + 10	31:0	Key[127:96]	
8*N* + 14	14:3	Reserved	
	9	Power Mgt bit of last error-free directed Rx frame (only if UAPSD = 1)	
	8:5	UAPSD mask for the four ACs.	
		8	UAPSD enabled for BE
		7	UAPSD enabled for BK
		6	UAPSD enabled for VI
		5	UAPSD enabled for VO
	2:0	Key type:	
		0	40b
		1	104b
		2	TKIP without MIC
		3	128b
		4	TKIP
		5	Reserved
		6	AES_CCM
		7	Do nothing
8*N* + 18	31:0	Addr[32:1]	
8*N* + 1C	17:16	Key ID for multicast keys	
	15	Key valid	
		0	Entry has multi/broadcast key
		1	Entry has unicast key
	14:0	Addr[47:33]	

1. Key = (Address: 8800 + 20 * *N*)

When the key type is 4 (TKIP) and key is valid, this entry + 64 contains the Michael key. TKIP keys may not reside in the entries 64-127 because they require the Michael key. Entries 64-67 are always reserved for Michael.

Table 7-17 Offset to First Dword of *N*th Key (Continued)

Intra Key	Offset Bits	Description
8*N* + 800	31:0	Rx Michael Key 0
8*N* + 804	15:0	Tx Michael Key 0 [31:16]
8*N* + 808	31:0	Rx Michael Key 1
8*N* + 80C	15:0	Tx Michael Key 0 [15:0]
8*N* + 810	31:0	Tx Michael Key 1
8*N* + 814	RES	Reserved
8*N* + 818	RES	Reserved
8*N* + 81C	RES	Reserved
	15	Key Valid = 0

NOTE Internally the memory is 50 bits wide, thus writing a line of the memory requires two 32-bit writes. All writes to registers with an offset of 0x0 or 0x8 actually write to a temporary holding register. A write to registers with an offset of 0x4 or 0xC writes to memory.

7.15 PMU Registers

Table 7-18 summarizes the PLL SRIF registers.

Table 7-18 PMU Summary

Address	Name	Description	Page
0xB16C40	PMU1	PMU register 1	page 236
0xB16C44	PMU2	PMU register 2	page 236

7.15.1 PMU1

Address Offset: 0xB16C40
Access: Read/Write

Bit	Bit Name	Description
31:1	RES	Reserved; must be set to 0x319E40BB
0	PWD	Forces switching regulator to turn off when this bit is set to 1 and PGM is set to 1; default is 0

7.15.2 PMU2

Address Offset: 0xB16C44
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:22	SWREGMSB	MSB control bits for SWREG
21	PGM	Must be set to 1 to control the switching regulator through the SRIF PMU1 and PMU2 registers
20:19	LDO_TUNE	DDR LDO tune
18	PWDLDO_DDR	When set to 1, disables the DDR regulator; default is 0
17	LPOPWD	PWD for DDR LDO
16:0	RES	Reserved; must be set to 0x0

7.16 PLL SRIF Registers

Table 7-19 summarizes the PLL SRIF registers.

Table 7-19 PLL SRIF Registers

Offset				Name	Page
Baseband	CPU	AUD	DDR		
0xB8116180	0xB81161C0	0xB8116200	0xB8116240	DPLL	page 237
0xB8116184	0xB81161C4	0xB8116204	0xB8116244	DPLL2	page 237
0xB8116188	0xB81161C8	0xB8116208	0xB8116248	DPLL3	page 238

7.16.1 DPLL

Address Offset:
Baseband: 0xB8116180
CPU: 0xB81161C0
DDR: 0xB8116240
Access: Read/Write

Bit	Bit Name	Description
31:27	REFDIV	Manual override PLL reference divider ratio
26:18	NINT	Manual override PLL feedback divide ratio
17:0	NFRAC	Manual override of PLL fractional value of PLL divide ratio

7.16.2 DPLL2

Address Offset:
Baseband: 0xB8116184
CPU: 0xB81161C4
DDR: 0xB8116244
Access: Read/Write

Bit	Bit Name	Description	
31	RANGE	Manual override for bias current control bits inside the DPLL to cover the required frequency range.	
		0	Set it to range = 0 for VCO frequency above 650MH.
		1	Set range = 1 for VCO frequency < 650 MHz
30	LOCAL_PLL	Selects if we want to manually set PLL control bits through the SRIF space	
29:26	KI	Integral path gain of loop filter in DPLL, please set to 0x4	
25:19	KD	Proportional gain of loop filter in DPLL, this sets the loop bandwidth of the PLL	
18:17	RES	Reserved; must be set to 0x0	
16	PLL_PWD	Manual override for PLL power down; set to 1 to power down the PLL; a falling edge on this signal is needed to latch in the PLL values and initialize the PLL	
15:13	OUTDIV	Manual override to divide output of VCO in DPLL by $2^{OUT\_DIV[2:0]}$	

Bit	Bit Name	Description
12:7	RES	Reserved; must be set to 0x1E
6	RES	Reserved; must be set to 0x0
5:0	RES	Reserved

7.16.3 DPLL3

Address Offset:
Baseband: 0xB8116188
CPU: 0xB81161C8
DDR: 0xB8116248
Access: Read/Write

Bit	Bit Name	Description
31:30	RES	Reserved; must be set to 0x0
29:23	PHASE_SHIFT	Programmable phase shift for DPLL, set it to 0x6
22:0	RES	Reserved; must be set to 0x0

7.17 PCIE Configuration Space Registers

Table 7-20 shows the PCI Express configuration space registers for the QCA9531.

Table 7-20 PCI Configuration Space Registers

Offset	Description	Page
0x180C0000	Vendor ID	page 239
0x180C0002	Device ID	page 240
0x180C0004	Command	page 240
0x180C0006	Status	page 241
0x180C0008	Revision ID	page 241
0x180C0009	Class Code	page 241
0x180C000C	Cache Line Size	page 242
0x180C000D	Master Latency Timer	page 242
0x180C000E	Header Type	page 242
0x180C0010	Base Address 0 (Read-Only)	page 242
0x180C0010	BAR0 Mask (Write-Only)	page 243
0x180C0018	Bus Number	page 243
0x180C001E	Secondary Status	page 244
0x180C0020	Memory Base	page 244
0x180C0022	Memory Limit	page 244
0x180C0024	Prefetchable Memory Base	page 245
0x180C0026	Prefetchable Memory Limit	page 245
0x180C0034	Capability Pointer	page 245
0x180C003C	Interrupt Line	page 245
0x180C003D	Interrupt Pin	page 246
0x180C003E	Bridge Control	page 246

7.17.1 Vendor ID

Address: 0x180C
Access: Read-Only

The default value is the hardware configuration parameter.

Bit	Bit Name	Description
15:0	CX_VENDOR_ID_0	Vendor ID

7.17.2 Device ID

Address: 0x180C0002
Access: Read-Only

The default value is the hardware configuration parameters.

Bit	Bit Name	Description
15:0	CX_DEVICE_ID_0	Device ID

7.17.3 Command

Address: 0x180C0004
Access: See field description
Reset: 0

Bit	Access	Description
15:11	RO	Reserved
10	R/W	INTx assertion disable
9	RO	Fast back-to-back enable. Not applicable for PCIE. Hard-wired to 0.
8	R/W	SERR# enable
7	RO	IDSEL stepping/wait cycle control. Not applicable for PCIE. Hard-wired to 0.
6	R/W	Parity error response
5	RO	VGA palette snoop. Not applicable for PCIE. Hard-wired to 0.
4	RO	Memory write and invalidate. Not applicable for PCIE. Hard-wired to 0.
3	RO	Special cycle enable. Not applicable for PCIE. Hard-wired to 0.
2	R/W	Bus master enable
1	R/W	Memory space enable
0	R/W	I/O space enable

7.17.4 Status

Address: 0x180C0006
Access: See field description
Reset: See field description

Bit	Access	Reset	Description
15	RW1C	0	Detected parity error
14	RW1C	0	Signalled system error
13	RW1C	0	Received master abort
12	RW1C	0	Received target abort
11	RW1C	0	Signalled target abort
10:9	RO	0x0	DEVSEL timing; not applicable for PCIE. Hard-wired to 0.
8	RW1C	0	Master data parity error
7	RO	0	Fast back-to-back capable; not applicable for PCIE. Hard-wired to 0.
6	RO	0	Reserved
5	RO	0	66 MHz capable; not applicable for PCIE. Hardwired to 0.
4	RO	1	Capabilities list. Indicates presence of an extended capability item. Hard-wired to 1.
3	RO	0	INTx status
2:0	RO	0x0	Reserved

7.17.5 Revision ID

Address: 0x180C0008
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
7:0	CX_REVISION_ID_0	Revision ID

7.17.6 Class Code

Address: 0x180C0009
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
23:16	BASE_CLASS_CODE_0	Base class code
15:8	SUB_CLASS_CODE_0	Sub class code
7:0	IF_CODE_0	Programming interface

7.17.7 Class Line Size

Address: 0x180C000C
Access: Read/Write
Reset: 0x0

Bit	Description
7:0	Cache line size This register is R/W for legacy compatibility purposes and is not applicable to PCI Express device functionality. Writing to the Cache Line Size register does not impact functionality of the RC.

7.17.8 Master Latency Timer

Address: 0x180C000D
Access: Read-Only
Reset: 0x0

Bit	Description
7:0	Master latency timer; not applicable to PCIE. Hardwired to 0.

7.17.9 Header Type

Address: 0x180C000E
Access: Read-Only
Reset: See field descriptions

Bit	Reset	Description
7	0x0	Multi-function device
6:0	0x01	Configuration header format. Hardwired to 0x01.

7.17.10 Base Address 0 (BAR0)

Address: 0x180C0010
Access: Read-Only
Reset: See field descriptions

The RC Core provides one 32-bit base address register.

Bit	Reset		Description
31:4	0x0000000		BAR0 base address bits. The BAR0 mask value determines which address bits are masked.
3	PREFETCHABLE0_0 for memory BAR		If BAR0 is a memory BAR, indicates if the memory region is prefetchable:
		0	Non-prefetchable
		1	Prefetchable
2:1	BAR0_TYPE_0 for memory BAR		If BAR 0 is a memory BAR, bits [2:1] determine the BAR type:
		00	32-bit BAR
		10	Unused
0	MEM0_SPACE_DECODER_0	0	BAR0 is a memory BAR
		1	Unused

7.17.11 BAR0 Mask

Address: 0x180C0010 (same as Base Address 0 (BAR0), page 7-242
Access: Write-Only
Reset: See field descriptions

Determines which bits in the BAR are non-writable by host software, which determines the size of the address space claimed by the BAR. This register only exists when the corresponding BAR*n*_MASK_WRITABLE_0 value is 1. Otherwise, the BAR*n*_MASK_0 value sets the BAR Mask value in hardware.

BAR Mask values indicate the range of low-order bits in each implemented BAR to not use for address matching. The BAR Mask value also indicates the range of low-order bits in the BAR that cannot be written from the host. The application can write to all BAR bits to set memory, I/O, and other BAR options. To disable a BAR, the application can write a 0 to bit [0] of the BAR Mask register. To change the BAR Mask value for a disabled BAR, the application must first enable the BAR by writing 1 to bit [0]. After enabling the BAR, the application can write a new value to the BAR Mask register. If the BAR Mask value for a BAR is less than that required for the BAR type, the RC Core uses the minimum BAR type value:

- BAR bits [11:0] are always masked for a memory BAR. The RC Core requires each memory BAR to claim at least 4 KB
- BAR bits [7:0] are always masked for an I/O BAR. The RC Core requires each I/O BAR to claim at least 256 bytes

Bit	Bit Name	Description	
31:1	BAR0 _MASK_0	Indicates which BAR0 bits to mask (make nonwritable) from host software, which in turn determines the size of the BAR. For example, writing 0xFFF to the BAR0 Mask register claims a 4096-byte BAR by masking bits 11:0 of the BAR from writing by host software. Application write access depends on the value of BAR0_MASK_WRITABLE_0: ■ If BAR0_MASK_WRITABLE_0 = 1, the BAR0 Mask register is writable ■ If BAR0_MASK_WRITABLE_0 = 0, BAR0 Mask is not writable	
0	BAR0 _ENABLED _0	BAR0 enable	
		0	BAR0 is disabled
		1	BAR0 is enabled
		Bit [0] is interpreted as BAR enable when writing to the BAR Mask register rather than as a mask bit because bit [0] of a BAR is always masked from writing by host software.	

7.17.12 Bus Number

Address: 0x180C0018
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
31:24	RO	Secondary latency timer; not applicable to PCI Express, hardwired to 0x00.
23:16	R/W	Subordinate bus number
15:8	R/W	Secondary bus number
7:0	R/W	Primary bus number

7.17.13 Secondary Status

Address: 0x180C001E
Access: See field descriptions
Reset: 0

Bit	Access	Description
15	RW1C	Detected parity error
14	RW1C	Received system error
13	RW1C	Received master abort
12	RW1C	Received target abort
11	RW1C	Signalled timer abort
10:9	RO	DEVSEL timing; not applicable to PCIE. Hardwired to 0.
8	RW1C	Master data parity error
7	RO	Fast back-to-back capable; not applicable to PCIE. Hardwired to 0.
6	RO	Reserved
5	RO	66 MHz; not applicable to PCIE. Hardwired to 0.
4:0	RO	Reserved

7.17.14 Memory Base

Address: 0x180C0020
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:4	R/W	Memory base address
3:0	RO	Reserved

7.17.15 Memory Limit

Address: 0x180C0022
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:5	R/W	Memory limit address
4:0	RO	Reserved

7.17.16 Prefetchable Memory Base

Address: 0x180C0024
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory start address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

7.17.17 Prefetchable Memory Limit

Address: 0x180C0026
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory end address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

7.17.18 Capability Pointer

Address: 0x180C0034
Access: Read-Only
Reset: 0x40

Bit	Description
7:0	First capability pointer. Points to power management capability structure by default.

7.17.19 Interrupt Line

Address: 0x180C003C
Access: Read/Write
Reset: 0xFF

Bit	Description
7:0	Interrupt line

7.17.20 Interrupt Pin

Address: 0x180C003D
Access: Read-Only
Reset: 0x1

Bit	Description	
7:0	Interrupt pin. Identifies the legacy interrupt Message that the device uses. Valid values are:	
	00	The device does not use legacy interrupt
	01	The device uses INTA

7.17.21 Bridge Control

Address: 0x180C003E
Access: See field descriptions
Reset: 0x0

Bit	Access	Description
15:12	RO	Reserved
11	RO	Discard timer SERR enable status; not applicable to PCIE. Hardwired to 0.
10	RO	Discard timer status; not applicable to PCIE. Hardwired to 0.
9	RO	Secondary discard timer; not applicable to PCIE. Hardwired to 0.
8	RO	Primary discard timer; not applicable to PCIE. Hardwired to 0.
7	RO	Fast back-to-back transactions enable; not applicable to PCIE. Hardwired to 0.
6	R/W	Secondary bus reset
5	RO	Master abort mode; not applicable to PCIE. Hardwired to 0.
4	R/W	VGA 16-bit decode
3	R/W	VGA enable
2	R/W	ISA enable
1	R/W	SERR enable
0	R/W	Parity error response enable

7.18 PCIE RC PHY Registers

Table 7-21 summarizes the PCIE RC PHY registers for the QCA9531.

Table 7-21 PCIE RC PHY Registers

Address	Name	Description	Page
0x18116200 0x18116C80	PLL Division	DPLL	page 247
0x18116204 0x18116C84	PLL Division 2	DPLL2	page 248
0x18116208 0x18116C88	PLL Division 3	DPLL3	page 248

7.18.1 PLL Division (DPLL)

Address: 0x18116200
: 0x18116C80
Access: Read/Write
Reset: See field description

This register manually overrides the PLL divide ratio calculations.

Bit	Bit Name	Reset	Description
31:27	REFDIV	0x1	Manual override of the PLL reference divide ratio
26:18	NINT	0x10	Manual override of the PLL feedback divide ratio
17:0	NFRAC	0x0	Manual override of the PLL fractional value of the PLL divide ratio, requires PWD_PLLSDM = 0 to be effective

7.18.2 PLL Division 2 (DPLL2)

Address: 0x18116204
: 0x18116C84
Access: Read/Write
Reset: See field description

This register holds the control bits for DPLL.

Bit	Bit Name	Reset	Description
31	RANGE	0x0	Manual override for bias current control bits inside the DPLL to cover the required frequency range
30	LOCAL_PLL	0x0	Chooses to manually set PLL control bits or not
29:26	KI	0x6	Integral path gain of loop filter in DPLL
25:19	KD	0x7F	Proportional gain of loop filter in DPLL
18	EN_NEGTRIG	0x0	Enables the negative trigger for the DPLL digital engine. Only use half cycles for computations
17	SEL_1SDM	0x0	Sets the DPLL SDM order.
			0 Second SDM order
			1 First SDM order
16	PLL_PWD	0x1	Manual override for PWD
15:13	OUTDIV	0x0	Manual override to divide output of VCO in DPLL by 2^out_div[2:0]
12:0	RES	0x0	Reserved

7.18.3 PLL Division 3 (DPLL3)

Address: 0x18116208
: 0x18116C88
Access: Read/Write
Reset: 0x0

This register holds the EVM estimation bits.

Bit	Bit Name	Description
31:30	RES	Reserved
29:23	PHASE_SHIFT	Programmable phase shift for DPLL
22:0	RES	Reserved

7.19 PCIE RC0 PHY Registers

Table 7-22 summarizes the PCIE RC0 PHY registers for the QCA9531.

Table 7-22 PCIE RC PHY Registers

Address	Name	Description	Page
0x18116DC0	PCIE_PHY_REG_1	PCIE PHY 1	page 249
0x18116CC4	PCIE_PHY_REG_2	PCIE PHY 2	page 250
0x18116CC8	PCIE_PHY_REG_3	PCIE PHY 3	page 251

7.19.1 PCIE PHY 1 (PCIE_PHY_REG_1)

Address: 0x18116DC0
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description	
31	SERDES_DIS_RXIMP	0x0	Disable the receiver impedance in SERDES	
30:29	SERDES_TXDR_CTRL	0x0	Transmit Amplitude control for the SERDES (used in conjunction with SERDES_HALFTXDR)	
28:27	PERSTDELAY	0x2	Controls delay of PERSTN_DIGITAL WRT PERSTN_SERDES	
			00	10 µs
			01	12 µs
			10	15 µs
			11	20 µs
26:25	CLKOBSSEL	0x0	Select different clocks for observation.	
			00	No clock
			01	CLK125M_TX
			10	CLK125M_RX
			11	CLK_PCIEREF
24	DATAOBSEN	0x0	Enables the receive Data Observe bus	
23	FUNCTEST_EN	0x0	Enables the low-speed functional test mode of the PCIE interface	
22	SERDES_DISABLE	0x0	Forces the SERDES into power down mode. Used during ATE testing of other interfaces	
21	RXCLKINV	0x1	Invert the CLK125M_RX before using for receive data latching	
20	FUNCTESTRXCLKINV	0x0	Invert the Functional Test Clock for receive latching	
19	FUNCTESTTXCLKINV	0x0	Invert the Functional Test Clock for Transmit latching	
18	ENABLECLKREQ	0x0	Enables assertion/deassertion of CLKREQ# pin upon L1-Entry/Exit	
17	FLORCELOOPBACK	0x0	Force PCIE PHY into looping back its Rx data back to Tx	
16:15	SEL_CLK	0x2	Overclock control	

14	SERDES_RX_EQ	0x0	Enables receiver equalization	
13	SERDES_EN_LCKDT	0x1	Enables the lock detect circuit	
12	SERDES_PLL_ DISABLE	0x0	When this bit is set the PLL is disabled in L1 state	
11	SERDES_POWER_ SAVE	0x0	When set, enables additional power saving of SERDES in L0s and L1 states	
10:9	SERDES_CDR_BW	0x3	CDR digital accumulator length control	
8:7	SERDES_TH_LOS	0x0	Threshold selection for RX loss-of-signal detection	
			00	Normal
			01	-2dB
			10, 11	+2dB
6	SERDESEN_DEEMP	0x1	Enable TX de-emphasis when high	
5	SERDES_HALFTXDR	0x0	Tx driver output amplitude is reduced to 500 mVppd when high	
4	SERDES_SEL_HSP	0x1	VCO frequency adjust	
3:0	SWITCH_CTRL	0xE	Resistor calibration switch control	

7.19.2 PCIE PHY 2 (PCIE_PHY_REG_2)

Address: 0x18116DC4
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description
31:24	PRBS_ERROR_COUNT	0x0	PRBS error count
23	SDS_SDM_RXELECIDLE	0x0	SERDES Rx electrical idle status
22	SDS_SDM_RXDETECTED	0x0	SERDES receiver detect status
21	PRBS_SCRAMBLE	0x0	Scramble during PRBS pattern
20	PRBS_START	0x0	Start the PRBS testing
19:13	PRBS_TS_NUM	0x40	Number of TS preceding PRBS
12	TXDETRXOVREN	0x0	Enable bit for overriding and controlling the TxDetRx trigger
11	TXDETRXOVRVALUE	0x0	Override value for TxDetRx trigger
10	DATAOBSPRBSERR	0x0	Enables observation of PRBS Error Count of the 20-bit observation bus
9:6	CDRREADYTIMER	0x7	RX_CLOCK ready timer in units of 8*8ns. Triggered by an exit from RXELECIDLE
5:1	TXDETRXTARGETDELAY	0xC	Programmable timer that gets enabled after assertion of Tx Elecidle and MAC-PHY TxDetRx trigger . Receiver detection status is checked after the completion of this timer.
0	FORCEDETECT	0x0	Overrides the PHY_MAC_RXSTATUS to 0x3 (successful receiver detection) on occurence of PHY_MAC_PHYSTATUS pulse and mac_ PHY_XDETECTRX (receiver detection request). Overrides the originial receiver detection indication.

7.19.3 PCIE PHY 3 (PCIE_PHY_REG_3)

Address: 0x18116DC8
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description
31:28	PRBS_COMMA_STATUS	0x0	PRBS Rx comma status
27:11	SPARE	0x00A0B	Spare bits
10	SEL_CLK100	0x0	Enable/disable for 100 MHz reference clock input to analog (used when serdes_disable is set)
9	EN_BEACONGEN	0x0	Enable SERDES beacon generation Controllability used in SRIF mode (pipe_mode = 0)
8	TXELECIDLE	0x0	Controllability for transmit electrical idle
7:6	SEL_CLK	0x0	Overclock control Controllability used in SRIF mode (pipe_mode = 0)
5	RX_DET_REQ	0x0	Receiver detection TxDetRx trigger - controllability used in SRIF mode (pipe_mode = 0)
4	MODE_OCLK_IN	0x0	Overclocking control 0 Non-overclocking 1 Overclocking
3	EN_PLL	0x0	Enable/disable SERDES PLL Controllability used in SRIF mode (pipe_mode = 0)
2	EN_LCKDT	0x1	Enable lock detect circuit Controllability used in SRIF mode (pipe_mode = 0)
1	EN_BUFS_RX	0x0	Enable SERDES Rx buffers Controllability used in SRIF mode (pipe_mode = 0)
0	EN	0x0	SERDES enable Controllability used in SRIF mode (pipe_mode = 0)

7.20 GMAC0/GMAC1 Registers

Table 7-23 summarizes the GMAC0/GMAC1 registers for the QCA9531.

Table 7-23 Ethernet Registers Summary

GMAC0 Address	GMAC1 Address	Description		Page
0x19000000	0x1A000000	MAC Configuration 1		page 255
0x19000004	0x1A000004	MAC Configuration 2		page 256
0x19000008	0x1A000008	IPG/IFG		page 257
0x1900000C	0x1A00000C	Half-Duplex		page 258
0x19000010	0x1A000010	Maximum Frame Length		page 258
0x19000020	0x1A100020	MII Configuration		page 259
0x19000024	0x1A000024	MII Command		page 260
0x19000028	0x1A000028	MII Address		page 260
0x1900002C	0x1A00002C	MII Control		page 260
0x19000030	0x1A000030	MII Status		page 261
0x19000034	0x1A000034	MII Indicators		page 261
0x19000038	0x1A000038	Interface Control		page 262
0x1900003C	0x1A00003C	Interface Status		page 263
0x19000040	0x1A000040	STA Address 1		page 264
0x19000044	0x1A000044	STA Address 2		page 264
0x19000048	0x1A000048	ETH Configuration 0		page 264
0x1900004C	0x1A00004C	ETH Configuration 1		page 265
0x19000050	0x1A000050	ETH Configuration 2		page 266
0x19000054	0x1A000054	ETH Configuration 3		page 266
0x19000058	0x1A000058	ETH Configuration 4		page 267
0x1900005C	0x1A00005C	ETH Configuration 5		page 268
0x19000080	0x1A000080	TR64	Tx/Rx 64 Byte Frame Counter	page 268
0x19000084	0x1A000084	TR127	Tx/Rx 65-127 Byte Frame Counter	page 269
0x19000088	0x1A000088	TR255	Tx/Rx 128-255 Byte Frame Counter	page 269
0x1900008C	0x1A00008C	TR511	Tx/Rx 256-511 Byte Frame Counter	page 269
0x19000090	0x1A000090	TR1K	Tx/Rx 512-1023 Byte Frame Counter	page 270
0x19000094	0x1A000094	TRMAX	Tx/Rx 1024-1518 Byte Frame Counter	page 270
0x19000098	0x1A000098	TRMGV	Tx/Rx 1519-1522 Byte VLAN Frame Counter	page 270
0x1900009C	0x1A00009C	RBYT	Receive Byte Counter	page 271
0x190000A0	0x1A0000A0	RPKT	Receive Packet Counter	page 271
0x190000A4	0x1A0000A4	RFCS	Receive FCS Error Counter	page 271
0x190000A8	0x1A0000A8	RMCA	Receive Multicast Packet Counter	page 272
0x190000AC	0x1A0000AC	RBCA	Receive Broadcast Packet Counter	page 272
0x190000B0	0x1A0000B0	RXCF	Receive Control Frame Packet Counter	page 272

Table 7-23 Ethernet Registers Summary (cont.)

GMAC0 Address	GMAC1 Address	Description		Page
0x190000B4	0x1A0000B4	RXPF	Receive Pause Frame Packet Counter	page 273
0x190000B8	0x1A0000B8	RXUO	Receive Unknown OPCode Packet Counter	page 273
0x190000BC	0x1A0000BC	RALN	Receive Alignment Error Counter	page 273
0x190000C0	0x1A0000C0	RFLR	Receive Frame Length Error Counter	page 274
0x190000C4	0x1A0000C4	RCDE	Receive Code Error Counter	page 274
0x190000C8	0x1A0000C8	RCSE	Receive Carrier Sense Error Counter	page 274
0x190000CC	0x1A0000CC	RUND	Receive Undersize Packet Counter	page 275
0x190000D0	0x1A0000D0	ROVR	Receive Oversize Packet Counter	page 275
0x190000D4	0x1A0000D4	RFRG	Receive Fragments Counter	page 275
0x190000D8	0x1A0000D8	RJBR	Receive Jabber Counter	page 276
0x190000DC	0x1A0000DC	RDRP	Receive Dropped Packet Counter	page 276
0x190000E0	0x1A0000E0	TBYT	Transmit Byte Counter	page 276
0x190000E4	0x1A0000E4	TPKT	Transmit Packet Counter	page 277
0x190000E8	0x1A0000E8	TMCA	Transmit Multicast Packet Counter	page 277
0x190000EC	0x1A0000EC	TBCA	Transmit Broadcast Packet Counter	page 277
0x190000F0	0x1A0000F0	TXPF	Transmit Pause Control Frame Counter	page 278
0x190000F4	0x1A0000F4	TDFR	Transmit Deferral Packet Counter	page 278
0x190000F8	0x1A0000F8	TEDF	Transmit Excessive Deferral Packet Counter	page 278
0x190000FC	0x1A0000FC	TSCL	Transmit Single Collision Packet Counter	page 279
0x19000100	0x1A000100	TMCL	Transmit Multiple Collision Packet	page 279
0x19000104	0x1A000104	TLCL	Transmit Late Collision Packet Counter	page 279
0x19000108	0x1A000108	TXCL	Transmit Excessive Collision Packet Counter	page 280
0x1900010C	0x1A00010C	TNCL	Transmit Total Collision Counter	page 280
0x19000110	0x1A000110	TPFH	Transmit Pause Frames Honored Counter	page 280
0x19000114	0x1A000114	TDRP	Transmit Drop Frame Counter	page 281
0x19000118	0x1A000118	TJBR	Transmit Jabber Frame Counter	page 281
0x1900011C	0x1A00011C	TFCS	Transmit FCS Error Counter	page 281
0x19000120	0x1A000120	TXCF	Transmit Control Frame Counter	page 282
0x19000124	0x1A000124	TOVR	Transmit Oversize Frame Counter	page 282
0x19000128	0x1A000128	TUND	Transmit Undersize Frame Counter	page 282
0x1900012C	0x1A00012C	TFRG	Transmit Fragment Counter	page 282
0x19000130	0x1A000130	CAR1	Carry Register 1	page 283
0x19000134	0x1A000134	CAR2	Carry Register 2	page 284
0x19000138	0x1A000138	CAM1	Carry Mask Register 1	page 285

Table 7-23 Ethernet Registers Summary (cont.)

GMAC0 Address	GMAC1 Address	Description		Page
0x1900013C	0x1A00013C	CAM2	Carry Mask Register 2	page 286
0x19000180	0x1A000180	DMATXCNTRL_Q0	DMA Transfer Control for Queue 0	page 286
0x19000184	0x1A000184	DMATXDESCR_Q0	Descriptor Address for Queue 0 Tx	page 287
0x19000188	0x1A000188	**DMA Tx Status**		page 287
0x1900018C	0x1A00018C	DMARXCTRL	Rx Control	page 288
0x19000190	0x1A000190	DMARXDESCR	Pointer to Rx Descriptor	page 288
0x19000194	0x1A000194	DMARXSTATUS	Rx Status	page 288
0x19000198	0x1A000198	DMAINTRMASK	Interrupt Mask	page 289
0x1900019C	0x1A00019C	**Interrupts**		page 290
0x190001A0	0x1A0001A0	ETH_TX_BURST	Ethernet Tx burst	page 291
0x190001A4	0x1A0001A4	ETH_TXFIFO_TH	Ethernet Tx FIFO Max and Min Threshold	page 291
0x190001A8	0x1A0001A8	ETH_XFIFO_DEPTH	Current Tx and Rx FIFO Depth	page 292
0x190001AC	0x1A0001AC	ETH_RXFIFO_TH	Ethernet Rx FIFO	page 292
0x190001B8	0x1A0001B8	ETH_FREE_TIMER	Ethernet Free Timer	page 292
0x190001C0	0x1A0001C0	DMATXCNTRL_Q1	DMA Transfer Control for Queue 1	page 292
0x190001C4	0x1A0001C4	DMATXDESCR_Q1	Descriptor Address for Queue 1 Tx	page 293
0x190001C8	0x1A0001C8	DMATXCNTRL_Q2	DMA Transfer Control for Queue 2	page 293
0x190001CC	0x1A0001CC	DMATXDESCR_Q2	Descriptor Address for Queue 2 Tx	page 293
0x190001D0	0x1A0001D0	DMATXCNTRL_Q3	DMA Transfer Control for Queue 3	page 294
0x190001D4	0x1A0001D4	DMATXDESCR_Q3	Descriptor Address for Queue 3 Tx	page 294
0x190001D8	0x1A0001D8	DMATXARBCFG	DMA Tx Arbitration Configuration	page 294
0x190001E4	0x1A0001E4	DMATXSTATUS_123	Tx Status and Packet Count for Queues 1 to 3	page 295
0x19000200	—	LCL_MAC_ADDR_DW0	Local MAC Address Dword0	page 295
0x19000204	—	LCL_MAC_ADDR_DW1	Local MAC Address Dword1	page 295
0x19000208	—	NXT_HOP_DST_ADDR_DW0	Next Hop Router MAC Address Dword0	page 296
0x1900020C	—	NXT_HOP_DST_ADDR_DW1	Next Hop Router MAC Destination Address Dword1	page 296
0x19000210	—	GLOBAL_IP_ADDR0	Local Global IP Address 0	page 296
0x19000214	—	GLOBAL_IP_ADDR1	Local Global IP Address 1	page 297
0x19000218	—	GLOBAL_IP_ADDR2	Local Global IP Address 2	page 297
0x1900021C	—	GLOBAL_IP_ADDR3	Local Global IP Address 3	page 297

7.20.1 MAC Configuration 1

GMAC0 Address: 0x19000000
GMAC1 Address: 0x1A000000
Access: See field description
Reset: See field description

This register is used to set the actions for transmitting and receiving frames.

Bit	Bit Name	Type	Reset	Description
31	SOFT_RESET	RW	0x1	Setting this bit resets all modules except the host interface. The host interface is reset via HRST.
30	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
29:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	RESET_RX_MAC_ CONTROL	RW	0x0	Resets the receive (Rx) MAC control block
18	RESET_TX_MAC_ CONTROL	RW	0x0	Resets the transmit (Tx) MAC control
17	RESET_RX_ FUNCTION	RW	0x0	Resets the Rx function
16	RESET_TX_ FUNCTION	RW	0x0	Resets the Tx function
15:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	LOOP_BACK	RW	0x0	Setting this bit causes MAC Rx outputs to loop back to the MAC Rx inputs. Clearing this bit results in normal operation.
7:6	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	RX_FLOW _CONTROL	RW	0x0	Setting this bit causes the Rx MAC control to detect and act on pause flow control frames.
4	TX_FLOW_ CONTROL	RW	0x0	Setting this bit causes the Tx MAC control to send requested flow control frames. Clearing this bit prevents the MAC from sending flow control frames. The default is 0.
3	SYNCHRONIZED_RX	RO	0x0	Rx enable synchronized to the receive stream
2	RX_ENABLE	RW	0x0	Setting this bit will allow the MAC to receive frames from the PHY. Clearing this bit will prevent the reception of frames.
1	SYNCHRONIZED_TX	RO	0x0	Tx enable synchronized to the Tx stream
0	TX_ENABLE	RW	0x0	Allows the MAC to transmit frames from the system. Clearing this bit will prevent the transmission of frames.

7.20.2 MAC Configuration 2

GMAC0 Address: 0x19000004
GMAC1 Address: 0x1A000004
Access: Read/Write
Reset: See field description

This register is used to set the parameters relating to the MAC, including duplex, CRC, and oversized frames.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:12	PREAMBLE_ LENGTH	0x7	Determines the length of the preamble field of the packet, in bytes.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:8	RES	0x0	Reserved. Must be set to 0x01
7:6	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	HUGE_FRAME	0x0	Set this bit to allow frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAME LENGTH value, which is contained in the Maximum Frame Length, page 7-258 register.
4	LENGTH_FIELD	0x0	Set this bit to cause the MAC to check the frame's length field to ensure it matches the data field length. Clear this bit for no length field checking.
3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	PAD/CRC ENABLE	0x0	Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC.
1	CRC_ENABLE	0x0	Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC.
0	FULL_DUPLEX	0x0	Setting this bit configures the MAC to operate in full-duplex mode. Clearing this bit configures the MAC to operate in half-duplex mode only.

7.20.3 IPG/IFG

GMAC0 Address: 0x19000008
GMAC1 Address: 0x1A000008
Access: Read/Write
Reset: See field description

This register is used to configure settings for the inter-packet gap and the inter-frame gap.

Bit	Bit Name	Reset	Description
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:24	NON_BACK_TO_ BACK_INTER _PACKET_GAP1	0x40	Represents the carrier sense window. If a carrier is detected, MAC defers to the carrier. If the carrier becomes active, MAC continues timing and Tx, knowingly causing a collision to ensure fair access to the medium.
23	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
22:16	NON_BACK_TO_ BACK_INTER _PACKET_GAP2	0x60	This programmable field represents the non-back-to-back inter-packet gap in bit times
15:8	MINIMUM_IFG_ ENFORCEMENT	0x50	Represents the minimum IFG size to enforce between frames (expressed in bit times). Frames with a IFG of less than programmed are dropped.
7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	BACK_TO_BACK_ INTER_PACKET_ GAP	0x60	Represents the IPG between back-to-back packets (expressed in bit times). This IPG parameter is used in full- duplex mode when two Tx packets are sent back-to-back. Set this field to the desired number of bits.

7.20.4 Half-Duplex

GMAC0 Address: 0x1900000C
GMAC1 Address: 0x1A00000C
Access: Read/Write
Reset: See field description

This register is used to configure the settings for half-duplex, including back pressure, excessive defer and collisions.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:20	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION	0xA	Used when bit [19] is set. The value programmed is substituted for the Ethernet standard value of ten.
19	ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	0x0	Setting this bit configures the Tx MAC to use the setting of bits [23:20] instead of the tenth collision. Clearing this bit will cause the TX MAC to follow the standard binary exponential backoff rule, which specifies that any collision after the tenth uses 210-1 as the maximum backoff time.
18	BACKPRESSURE_ NO_BACKOFF	0x0	Setting this bit configures the Tx MAC to immediately retransmit following a collision during backpressure operation. Clearing this bit causes the Tx MAC to follow the binary exponential backoff rule.
17	NO_BACKOFF	0x0	Setting this bit configures the Tx MAC to immediately retransmit following a collision. Clearing this bit causes the Tx MAC to follow the binary exponential backoff rule.
16	EXCESSIVE_ DEFER	0x1	Setting this bit configures the Tx MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit will cause the Tx MAC to abort the transmission of a packet that has been excessively deferred.
15:12	RETRANSMISSION_ MAXIMUM	0xF	This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The maximum number of attempts is defined by 802.11 standards as 0xF.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	COLLISION_ WINDOW	0x37	This programmable field represents the slot time or collision window during which collisions might occur in a properly configured network. Since the collision window starts at the beginning of a transmission, the preamble and SFD are included. The reset value (0x37) corresponds to the count of frame bytes at the end of the window. If the value is larger than 0x3F the TPST single will no longer work correctly.

7.20.5 Maximum Frame Length

GMAC0 Address: 0x19000010
GMAC1 Address: 0x1A000010
Access: Read/Write
Reset: 0x600

This register is used to set the maximum allowable frame length.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MAX_FRAME _LENGTH	This programmable field sets the maximum frame size in both the Tx and Rx directions

7.20.6 MII Configuration

GMAC0 Address: 0x19000020
GMAC1 Address: 0x1A000020
Access: Read/Write
Reset: 0x0

This register is used to set the MII management parameters.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>31</td><td>RESET_MII_ MGMT</td><td>Setting this bit resets the MII Management. Clearing this bit allows MII Management to perform management read/write cycles as requested by the Host interface.</td></tr>
<tr><td>30:6</td><td>RES</td><td>Reserved. Must be written with zero. Contains zeros when read.</td></tr>
<tr><td>5</td><td>SCAN_AUTO_ INCREMENT</td><td>Setting this bit causes MII Management to continually read from a set of contiguous PHYs. The starting address of the PHY is specified by the PHY address field recorded in the MII Address register. The next PHY to be read will be PHY address + 1. The last PHY to be queried in this read sequence will be the one residing at address 0x31, after which the read sequence will return to the PHY specified by the PHY address field.</td></tr>
<tr><td>4</td><td>PREAMBLE_ SUPRESSION</td><td>Setting this bit causes MII Management to suppress preamble generation and reduce the management cycle from 64 clocks to 32 clocks. Clearing this bit causes MII Management to perform Management read/write cycles with the 64 clocks of preamble.</td></tr>
<tr><td>3:0</td><td>MGMT_CLOCK_ SELECT</td><td>This field determines the clock frequency of the management clock (MDC).
<table>
<tr><th>Management Clock Select</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Source clock divided by 4</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Source clock divided by 4</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Source clock divided by 6</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Source clock divided by 8</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Source clock divided by 10</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Source clock divided by 14</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Source clock divided by 20</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Source clock divided by 28</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Source clock divided by 34</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Source clock divided by 42</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Source clock divided by 50</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Source clock divided by 58</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Source clock divided by 66</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Source clock divided by 74</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Source clock divided by 82</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Source clock divided by 98</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

7.20.7 MII Command

GMAC0 Address: 0x19000024
GMAC1 Address: 0x1A000024
Access: Read/Write
Reset: 0x0

This register is used to cause MII management to perform read cycles.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	SCAN_CYCLE	Causes MII management to perform read cycles continuously (e.g. to monitor link fail).
0	READ_CYCLE	Causes MII management to perform a single read cycle.

7.20.8 MII Address

GMAC0 Address: 0x19000028
GMAC1 Address: 0x1A000028
Access: Read/Write
Reset: 0x0

All MAC/PHY registers are accessed via the MII address and MII control registers of GMAC0 only. GMAC1 MII address and control registers are not used. The details of the Ethernet MAC/PHY that are accessible through the MAC 0 MII address.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:8	PHY_ADDRESS	Represents the five-bit PHY address field used in management cycles. Up to 31 PHYs can be addressed (0 is reserved).
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.
4:0	REGISTER ADDRESS	Represents the five-bit register address field used in management cycles. Up to 32 registers can be accessed.

7.20.9 MII Control

GMAC0 Address: 0x1900002C
GMAC1 Address: 0x1A00002C
Access: Write-Only
Reset: 0x0

All MAC/PHY registers are accessed via the MII Address and MII Control registers.
This register is used to perform write cycles using the information in the MII Address register.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ CONTROL	When written, an MII management write cycle is performed using the 16-bit data and the pre-configured PHY and register addresses from “MII Address, page 7-260” (0x0A).

7.20.10 MII Status

GMAC0 Address: 0x19000030
GMAC1 Address: 0x1A000030
Access: Read-Only
Reset: 0x0

This register is used to read information following an MII management read cycle.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ STATUS	After an MII management read cycle, 16-bit data can be read from this register.

7.20.11 MII Indicators

GMAC0 Address: 0x19000034
GMAC1 Address: 0x1A000034
Access: Read-Only
Reset: 0x0

This register is used indicate various functions of the MII management are currently being performed.

Bit	Bit Name	Description
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	NOT_VALID	When a 1 is returned, this bit indicates that the MII management read cycle has not yet completed and that the read data is not yet valid
1	SCANNING	When a 1 is returned, this bit indicates that a scan operation (continuous MII management read cycles) is in progress
0	BUSY	When a 1 is returned, this bit indicates that the MII management block is currently performing an MII management read or write cycle

7.20.12 Interface Control

MAC 0 Address: 0x19000038
MAC 1 Address: 0x1A000038
Access: Read/Write
Reset: 0x0

This register is used to configure and set the interface modules

Bit	Bit Name	Description	
31	RESET_ INTERFACE_ MODULE	Setting this bit resets the interface module. Clearing this bit allows for normal operation. This bit can be used in place of bits [23], [15] and [7] when any interface module is connected.	
30:25	RES	Reserved. Must be written with zero. Contains zeros when read.	
24	PHY_MODE	Setting this bit configures the serial MII module to be in PHY Mode. Link characteristics are taken directly from the RX segments supplied by the PHY.	
23	RESET_PERMII	Setting this bit resets the PERMII module. Clearing this bit allows for normal operation.	
22:17	RES	Reserved. Must be written with zero. Contains zeros when read.	
16	SPEED	This bit configures the reduced MII module with the current operating speed.	
		0	Selects 10 Mbps mode
		1	Selects 100 Mbps mode
15	RESET_PE100X	This bit resets the PE100X module, which contains the 4B/5B symbol encipher/decipher code.	
14:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10	FORCE_QUIET	Affects PE100X module only.	
		0	Normal operation
		1	Tx data is quiet, allowing the contents of the cipher to be output
9	NO_CIPHER	Affects PE100X module only.	
		0	Normal ciphering occurs
		1	The raw transmit 5B symbols are transmitting without ciphering
8	DISABLE_LINK_ FAIL	Affects PE100X module only.	
		0	Normal Operation
		1	Disables the 330-ms link fail timer, allowing shorter simulations. Removes the 330-ms link-up time before stream reception is allowed.
7	RESET GPSI	This bit resets the PE10T module which converts MII nibble streams to the serial bit stream of ENDEC PHYs. Affects PE10T module only.	
6:1	RES	Reserved. Must be written with zero. Contains zeros when read.	
0	ENABLE_ JABBER_ PROTECTION	This bit enables the Jabber Protection logic within the PE10T in ENDEC mode. Jabber is the condition where a transmitter is on for longer than 50 ms preventing other stations from transmitting. Affects PE10T module only.	

7.20.13 Interface Status

GMAC0 Address: 0x1900003C
GMAC1 Address: 0x1A00003C
Access: Read-Only
Reset: 0x0

Identifies the interface statuses. The range of bits that are active are dependant upon the optional interfaces connected at the time.

Bit	Bit Name	Description	
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.	
9	EXCESS_DEFER	This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high.	
8	CLASH	Used to identify the serial MII module mode	
		0	In PHY mode or in a properly configured MAC to MAC mode
		1	MAC to MAC mode with the partner in 10 Mbps and/or half-duplex mode indicative of a configuration error
7	JABBER	Used to identify a jabber condition as detected by the serial MII PHY	
		0	No jabber condition detected
		1	Jabber condition detected
6	LINK_OK	Used to identify the validity of a serial MII PHY link	
		0	No valid link detected
		1	Valid link detected
5	FULL_DUPLEX	Used to identify the current duplex of the serial MII PHY	
		0	Half-duplex
		1	Full-duplex
4	SPEED	Used to identify the current running speed of the serial MII PHY	
		0	10 Mbps
		1	100 Mbps
3	LINK_FAIL	Used to read the PHY link fail register. For asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY.	
		0	The MII management module has read the PHY link fail register to be 0
		1	The MII management module has read the PHY link fail register to be 1
2	CARRIER_LOSS	Carrier status. This bit latches high.	
		0	No carrier loss detection
		1	Loss of carrier detection
1	SQE_ERROR	0	Has not detected an SQE error. Latches high.
		1	Has detected an SQE error.
0	JABBER	0	Has not detected a Jabber condition. Latches high.
		1	Has detected a Jabber condition

7.20.14 STA Address 1

GMAC0 Address: 0x19000040
GMAC1 Address: 0x1A000040
Access: Read/Write
Reset: 0x0

This register holds the first four octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_1	This field holds the first octet of the station address
23:16	STATION_ ADDRESS_2	This field holds the second octet of the station address
15:8	STATION_ ADDRESS_3	This field holds the third octet of the station address
7:0	STATION_ ADDRESS_4	This field holds the fourth octet of the station address

7.20.15 STA Address 2

GMAC0 Address: 0x19000044
GMAC1 Address: 0x1A000044
Access: Read/Write
Reset: 0x0

This register holds the last two octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_5	This field holds the fifth octet of the station address
23:16	STATION_ ADDRESS_6	This field holds the sixth octet of the station address
15:0	RES	Reserved

7.20.16 ETH_FIFO RAM Configuration 0

GMAC0 Address: 0x19000048
GMAC1 Address: 0x1A000048
Access: See field description
Reset: 0x0

This register is used to assert and negate functions concerning the ETH module.

Bit	Bit Name	Access	Description	
31:21	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
20	FTFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
19	STFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
18	FRFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled

17	SRFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
16	WTMENRPLY	RO	Asserted	The eth_wtm module is enabled
			Negated	The eth_wtm module is disabled
15:13	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
12	FTFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
11	STFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
10	FRFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
9	SRFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
8	WTMENREQ	RW	Asserted	Requests enabling of the eth_wtm module
			Negated	Requests disabling of the eth_wtm module
7:5	RES	RW	Reserved. Must be written with zero. Contains zeros when read.	
4	HSTRSTFT	RW	When asserted, this bit places the eth_fab module in reset	
3	HSTRSTST	RW	When asserted, this bit places the eth_sys module in reset	
2	HSTRSTFR	RW	When asserted, this bit places the eth_fab module in reset	
1	HSTRSTSR	RW	When asserted, this bit places the eth_sys module in reset	
0	HSTRSTWT	RW	When asserted, this bit places the eth_wtm module in reset	

7.20.17 ETH Configuration 1

GMAC0 Address: 0x1900004C
GMAC1 Address: 0x1A00004C
Access: Read/Write
Reset: 0xFFFF

This register is used to configure the ETH storage area.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGFRTH [11:0]	This hex value represents the minimum number of 4-byte locations to store simultaneously in the receive RAM, relative to the beginning of the frame being input, before FRRDY may be asserted. Note that FRRDY will be latent a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on FRACPT assertion. When set to the maximum value, FRRD may be asserted only after the completion of the input frame. The value of this register must be greater than 18D when HSTDRPLT64 is asserted.
15:0	CFGXOFFRTX	This hexadecimal value represents the number of pause quanta (64-bit times) after an XOFF pause frame has been acknowledged until the ETH reasserts TCRQ if the ETH receive storage level has remained higher than the low watermark.

7.20.18 ETH Configuration 2

MAC 0 Address: 0x19000050
MAC 1 Address: 0x1A000050
Access: Read/Write
Reset: See field description

This register is used to number the minimum amount of 8-byte words in the Rx RAM before pause frames are transmitted.

Bit	Bit Name	Reset	Description
31:29	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
28:16	CFGHWM [12:0]	0xAAA	This hex value represents the maximum number of 8-byte words to store simultaneously in the Rx RAM before TCRQ and PSVAL facilitates an XOFF pause control frame.
15:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
12:0	CFGLWM [12:0]	0x555	This hex value represents the minimum number of 8-byte words to store simultaneously in Rx RAM before TCRQ and PSVAL facilitate an XON pause control frame in response to a transmitted XOFF pause control frame.

7.20.19 ETH Configuration 3

GMAC0 Address: 0x19000054
GMAC1 Address: 0x1A000054
Access: Read/Write
Reset: See field description

This register is used denote the minimum number of 4-byte locations to simultaneously store in the Tx RAM before assertion.

Bit	Bit Name	Reset	Description
31:28	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGHWMFT [11:0]	0x555	This hex value represents the maximum number of 4-byte locations to store simultaneously in Tx RAM before FTHWM is asserted. Note that FTHWM has two FTCLK clock periods of latency before assertion or negation, as should be considered when calculating required headroom for maximum size packets.
15:12	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
11:0	CFGFTTTH [11:0]	0xFFF	This hex value represents the minimum number of 4-byte locations to store simultaneously in the Tx RAM, relative to the beginning of the frame being input, before TPSF is asserted. Note that TPSF is latent for a certain amount of time due to fabric Tx clock system Tx clock time domain crossing. When set to the maximum value, TPSF asserts only after the completion of the input frame.

7.20.20 ETH Configuration 4

GMAC0 Address: 0x19000058
GMAC1 Address: 0x1A000058
Access: Read/Write
Reset: 0x0

This register is used to signal drop frame conditions internal to the Ethernet.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
HSTFLTRFRM [17:0]: These configuration bits are used to signal the drop frame conditions. The setting of these bits along with their don't care values in the ETH Configuration 5, page 7-268 register (bits [17:0]), determines if the packet is dropped by the GMAC. Drop condition is (|((Pkt_extracted_field[17:0] ~^ eth_configuration_4[17:0]) & ~eth_configuration_5[17:0])) == 1) For example: ■ if it is desired to drop a frame that contains a FCS Error, HSTFLTRFRM[4] would be set and bit 4 in ETH Configuration 5, page 7-268 is not set. ■ if it is desired to drop a multicast frame, HSTFLTRFRM[8] would be set and bit 8 in ETH Configuration 5, page 7-268 is not set. ■ if it is desired to drop a broadcast frame, HSTFLTRFRM[9] would be set and bit 9 in ETH Configuration 5, page 7-268 is not set.		
17	Unicast MAC address match	Unicast Address Match. Destination MAC port matched the STA MAC address configured.
16	Truncated frame	Receive Frame Truncated. Frame length greater than Max frame configured.
15	Long event	Receive Long Event. rx_dv did not get asserted even after long time: 10 Mbps - 50,000 bit time, 100/1000 Mbps - 80,000 bit times.
14	VLAN tag detected	Receive VLAN Tag Detected. Frame's length/type field contained 0x8100 which is the VLAN Protocol Identifier
13	Unsupported op. code	Receive Unsupported Op-code. Current Frame was recognized as a Control frame by the PEMCS, but it contained an Unknown Op-code. Customer may wish to qualify with inverse of CRCERR (~RSV[20]), and with length (64 - 1518) to verify that the frame was a valid Control Frame.
12	Pause frame	Receive PAUSE Control Frame. Current frame was recognized as a Control frame containing a valid PAUSE Frame Op-code and a valid address. Customer may wish to qualify with inverse of CRCERR (~RSV[20]), and with length (64 - 1518) to verify that the frame was a valid Control Frame
11	Control frame	Receive Control Frame. Current Frame was recognized as a Control frame for having a valid Type-Length designation. Customer may wish to qualify with inverse of CRCERR (~RSV[20]), and with length (64 - 1518) to verify that the frame was a valid Control Frame.)
10	Dribble nibble	Receive Dribble Nibble. Indicates that after the end of the packet an additional 1 to 7 bits were received. A single nibble, called the dribble nibble, is formed but not sent to the system (10/100 Mbps only)
9	Broadcast	Receive Broadcast. Packet's destination address contained the broadcast address
8	Multicast	Receive Multicast. Packet's destination address contained a multicast address
7	OK	Receive OK. Frame contained a valid CRC and did not have a code error
6	Out of range	Receive Length Out of Range. Indicates that frame's Length was larger than 1518 bytes but smaller than the Host's Maximum Frame Length Value (Type Field)
5	Length mismatch	Receive Length Check Error. Indicates that frame length field value in the packet does not match the actual data byte length and is not a Type Field
4	CRC error	Receive CRC Error. The packet's CRC did not match the internally generated CRC
3	Code error	Receive Code Error. One or more nibbles were signaled as errors during the reception of the packet

2	False carrier	Receive False Carrier. Indicates that at some time since the last receive statistics vector, a false carrier was detected, noted and reported with this the next receive statistics. The false carrier is not associated with this packet. False carrier is activity on the receive channel that does not result in a packet receive attempt being made. Defined to be RX_ER = 1, RX_DV = 0, RXD[3:0] = 0xE (RXD[7:0] = 0x0E)
1	RX_DV event	Receive RX_DV Event. indicates that the last receive event seen was not long enough to be a valid packet
0	Drop event	Receive Previous Packet Dropped. indicates that since the last RSV a packet was dropped (i.e. IFG too small)

7.20.21 ETH Configuration 5

GMAC0 Address: 0x1900005C
GMAC1 Address: 0x1A00005C
Access: Read/Write
Reset: See field description

This register is used to control the drop behavior of the GMAC.

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	BYTE/NIBBLE	0x0	This bit should be set to 1 for 1000 Mbps, else set to 0.
18	SHORT FRAME	0x0	If set to 1, all frames under 64 bytes are dropped.
17:0	RX FILTER[17:0]	0x3FFFF	HSTFLTRFRMDC [17:0]: These configuration bits indicate which are don't cares for frame drop circuitry. Clearing the bit will look for a matching level on the corresponding HSTFLTRFRM bit in ETH_Configuration 4. If a match is made then the frame is dropped. If a HSTFLTRFRMDC bit is set in this register, no frames are dropped for this condition.

7.20.22 Tx/Rx 64 Byte Frame Counter (TR64)

GMAC0 Address: 0x19000080
GMAC1 Address: 0x1A000080
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were up to 64 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR64	The transmit and receive 64 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).

7.20.23 Tx/Rx 65-127 Byte Frame Counter (TR127)

GMAC0 Address: 0x19000084
GMAC1 Address: 0x1A000084
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 65–127 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR127	The transmit and receive 65–127 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 65-127 bytes in length inclusive (excluding framing bits but including FCS bytes).

7.20.24 Tx/Rx 128-255 Byte Frame Counter (TR255)

GMAC0 Address: 0x19000088
GMAC1 Address: 0x1A000088
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 128–255 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR255	The transmit and receive 128-255 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 128-255 bytes in length inclusive (excluding framing bits but including FCS bytes).

7.20.25 Tx/Rx 256-511 Byte Frame Counter (TR511)

GMAC0 Address: 0x1900008C
GMAC1 Address: 0x1A00008C
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 256–511 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR511	The transmit and receive 256–511 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 256–511 bytes in length inclusive (excluding framing bits but including FCS bytes).

7.20.26 Tx/Rx 512-1023 Byte Frame Counter (TR1K)

GMAC0 Address: 0x19000090
GMAC1 Address: 0x1A000090
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 512–1023 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR1K	The transmit and receive 512–1023 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 512–1023 bytes in length inclusive (excluding framing bits but including FCS bytes).

7.20.27 Tx/Rx 1024-1518 Byte Frame Counter (TRMAX)

GMAC0 Address: 0x19000094
GMAC1 Address: 0x1A000094
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1024–1518 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMAX	The transmit and receive 1024-1518 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1024-1518 bytes in length inclusive (excluding framing bits but including FCS bytes).

7.20.28 Tx/Rx 1519-1522 Byte VLAN Frame Counter (TRMGV)

GMAC0 Address: 0x19000098
GMAC1 Address: 0x1A000098
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1519–1522 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMGV	The transmit and receive 1519–1522 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1519–1522 bytes in length inclusive (excluding framing bits but including FCS bytes).

7.20.29 Receive Byte Counter (RXBT)

GMAC0 Address: 0x1900009C
GMAC1 Address: 0x1A00009C
Access: Read/Write
Reset: 0x0

This register is used to count incoming frames and then increment this register accordingly.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	RBYT	The receive byte counter. This statistic count register is incremented by the byte count of all frames received, including bad packets but excluding framing bits but including FCS bytes.

7.20.30 Receive Packet Counter (RPKT)

GMAC0 Address: 0x190000A0
GMAC1 Address: 0x1A0000A0
Access: Read/Write
Reset: 0x0

This register is used to count packets received.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RPKT	The receive packet counter. This register is incremented for each received packet (including bad packets, all Unicast, broadcast and Multicast packets).

7.20.31 Receive FCS Error Counter (RFCS)

GMAC0 Address: 0x190000A4
GMAC1 Address: 0x1A0000A4
Access: Read/Write
Reset: 0x0

This register is used to count frames received between 64–1518 in length and has a FCS error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFCS	The received FCS error counter. This register is incremented for each frame received that has an integral 64–1518 length and contains a frame check sequence error.

7.20.32 Receive Multicast Packet Counter (RMCA)

GMAC0 Address: 0x190000A8
GMAC1 Address: 0x1A0000A8
Access: Read/Write
Reset: 0x0

This register is used to count received good standard multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RMCA	The receive multicast packet counter. This register is incremented for each multicast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding broadcast frames. This does not include range/length errors.

7.20.33 Receive Broadcast Packet Counter (RBCA)

GMAC0 Address: 0x190000AC
GMAC1 Address: 0x1A0000AC
Access: Read/Write
Reset: 0x0

This register is used to count received good broadcast frames.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21:0	RBCA	The receive broadcast packet counter. This register is incremented for each broadcast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding multicast frames. This does not include range or length errors.

7.20.34 Receive Control Frame Packet Counter (RXCF)

GMAC0 Address: 0x190000B0
GMAC1 Address: 0x1A0000B0
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RXCF	The receive control frame packet counter. This register is incremented for each MAC control frame received (pause and unsupported).

7.20.35 Receive Pause Frame Packet Counter (RXPF)

GMAC0 Address: 0x190000B4
GMAC1 Address: 0x1A0000B4
Access: Read/Write
Reset: 0x0

This register is used to count received pause frame packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXPF	The receive pause frame packet counter. This register is incremented each time a valid pause MAC control frame is received.

7.20.36 Receive Unknown OPCode Packet Counter (RXUO)

GMAC0 Address: 0x190000B8
GMAC1 Address: 0x1A0000B8
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames that contain an opcode.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXUO	The receive unknown OPcode counter. This bit is incremented each time a MAC control frame is received which contains an opcode other than a pause.

7.20.37 Receive Alignment Error Counter (RALN)

GMAC0 Address: 0x190000BC
GMAC1 Address: 0x1A0000BC
Access: Read/Write
Reset: 0x0

This register is used to count received packets with an alignment error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RALN	The receive alignment error counter. This register is incremented for each received frame from 64–1518 bytes that contains an invalid FCS and is not an integral number of bytes.

7.20.38 Receive Frame Length Error Counter (RFLR)

GMAC0 Address: 0x190000C0
GMAC1 Address: 0x1A0000C0
Access: Read/Write
Reset: 0x0

This register is used to count received frames that have a length error.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	RFLR	The received frame length error counter. this register is incremented for each received frame in which the 802.3 length field did not match the number of data bytes actually received (46–1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.

7.20.39 Receive Code Error Counter (RCDE)

GMAC0 Address: 0x190000C4
GMAC1 Address: 0x1A0000C4
Access: Read/Write
Reset: 0x0

This register is used to count the number of received frames that had a code error counter.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCDE	The receive code error counter. This register is incremented each time a valid carrier was present and at least one invalid data symbol was detected.

7.20.40 Receive Carrier Sense Error Counter (RCSE)

GMAC0 Address: 0x190000C8
GMAC1 Address: 0x1A0000C8
Access: Read/Write
Reset: 0x0

This register is used to count the number of frames received that had a false carrier.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCSE	The receive false carrier counter. This register is incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an 0xE on RXD. This event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.

7.20.41 Receive Undersize Packet Counter (RUND)

GMAC0 Address: 0x190000CC
GMAC1 Address: 0x1A0000CC
Access: Read/Write
Reset: 0x0

This register is used to count the number of received packets that were undersized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RUND	The receive undersize packet counter. This register is incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not include Range Length errors

7.20.42 Receive Oversize Packet Counter (ROVR)

GMAC0 Address: 0x190000D0
GMAC1 Address: 0x1A0000D0
Access: Read/Write
Reset: 0x0

This register is used to count received packets that were oversized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	ROVR	The receive oversize packet counter., This register is incremented each time a frame is received which exceeded 1518 (non-VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not include Range Length errors.

7.20.43 Receive Fragments Counter (RFRG)

GMAC0 Address: 0x190000D4
GMAC1 Address: 0x1A0000D4
Access: Read/Write
Reset: 0x0

This register is used to count received fragmented frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFRG	The receive fragments counter. This register is incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS. This includes integral and non-integral lengths.

7.20.44 Receive Jabber Counter (RJBR)

GMAC0 Address: 0x190000D8
GMAC1 Address: 0x1A0000D8
Access: Read/Write
Reset: 0x0

This register is used to count received jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RJBR	The received jabber counter. This register is incremented for frames which exceed 1518 (non-VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, including alignment errors.

7.20.45 Receive Dropped Packet Counter (RDRP)

GMAC0 Address: 0x190000DC
GMAC1 Address: 0x1A0000DC
Access: Read/Write
Reset: 0x0

This register is used to count received dropped packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RDRP	The received dropped packets counter. this register is incremented for frames received which are streamed to the system but are later dropped due to a lack of system resources.

7.20.46 Transmit Byte Counter (TXBT)

GMAC0 Address: 0x190000E0
GMAC1 Address: 0x1A0000E0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted bytes.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	TXBT	The transmit byte counter. This register is incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.

7.20.47 Transmit Packet Counter (TPKT)

GMAC0 Address: 0x190000E4
GMAC1 Address: 0x1A0000E4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TPKT	The transmit packet counter. This register is incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast and Multicast packets.

7.20.48 Transmit Multicast Packet Counter (TMCA)

GMAC0 Address: 0x190000E8
GMAC1 Address: 0x1A0000E8
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TMCA	Transmit multicast packet counter. Incremented for each multicast valid frame transmitted (excluding broadcast frames).

7.20.49 Transmit Broadcast Packet Counter (TBCA)

GMAC0 Address: 0x190000EC
GMAC1 Address: 0x1A0000EC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted broadcast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TBCA	Transmit broadcast packet counter. Incremented for each broadcast frame transmitted (excluding multicast frames).

7.20.50 Transmit Pause Control Frame Counter (TXPF)

GMAC0 Address: 0x190000F0
GMAC1 Address: 0x1A0000F0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted pause control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXPF	Transmit pause frame packet counter. Incremented each time a valid pause MAC control frame is transmitted.

7.20.51 Transmit Deferral Packet Counter (TDFR)

GMAC0 Address: 0x190000F4
GMAC1 Address: 0x1A0000F4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDFR	Transmit deferral packet counter. Incremented for each frame that was deferred on its first transmission attempt. Does not include frames involved in collisions.

7.20.52 Transmit Excessive Deferral Packet Counter (TEDF)

GMAC0 Address: 0x190000F8
GMAC1 Address: 0x1A0000F8
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TEDF	Transmit excessive deferral packet counter. Incremented for frames aborted that were deferred for an excessive period of time (3036 byte times).

7.20.53 Transmit Single Collision Packet Counter (TSCL)

GMAC0 Address: 0x190000FC
GMAC1 Address: 0x1A0000FC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted single collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TSCL	Transmit single collision packet counter. Incremented for each frame transmitted that experienced exactly one collision during transmission.

7.20.54 Transmit Multiple Collision Packet (TMCL)

GMAC0 Address: 0x19000100
GMAC1 Address: 0x1A000100
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multiple collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TMCL	Transmit multiple collision packet counter. Incremented for each frame transmitted that experienced 2–15 collisions (including any late collisions) during transmission as defined using the RETRY[3:0] field of the Tx function control register.

7.20.55 Transmit Late Collision Packet Counter (TLCL)

GMAC0 Address: 0x19000104
GMAC1 Address: 0x1A000104
Access: Read/Write
Reset: 0x0

This register is used to count transmitted late collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TLCL	Transmit late collision packet counter. Incremented for each frame transmitted that experienced a late collision during a transmission attempt. Late collisions are defined using the LCOL[5:0] field of the Tx function control register.

7.20.56 Transmit Excessive Collision Packet Counter (TXCL)

GMAC0 Address: 0x19000108
GMAC1 Address: 0x1A000108
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCL	Transmit excessive collision packet counter. Incremented for each frame that experienced 16 collisions during transmission and was aborted.

7.20.57 Transmit Total Collision Counter (TNCL)

GMAC0 Address: 0x1900010C
GMAC1 Address: 0x1A00010C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted total collision packets.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:0	TNCL	Transmit total collision counter. Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (i.e., transmitting and receiving at the same time). Note, this register does not include collisions that result in an excessive collision condition).

7.20.58 Transmit Pause Frames Honored Counter (TPFH)

GMAC0 Address: 0x19000110
GMAC1 Address: 0x1A000110
Access: Read/Write
Reset: 0x0

This register is used to count honored transmitted pause frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TPFH	Transmit pause frames honored counter. Incremented each time a valid pause MAC control frame is transmitted and honored.

7.20.59 Transmit Drop Frame Counter (TDRP)

GMAC0 Address: 0x19000114
GMAC1 Address: 0x1A000114
Access: Read/Write
Reset: 0x0

This register is used to count transmitted drop frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDRP	Transmit drop frame counter. Incremented each time input PFH is asserted.

7.20.60 Transmit Jabber Frame Counter (TJBR)

GMAC0 Address: 0x19000118
GMAC1 Address: 0x1A000118
Access: Read/Write
Reset: 0x0

This register is used to count transmitted jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TJBR	Transmit jabber frame counter. Incremented for each oversized transmitted frame with an incorrect FCS value.

7.20.61 Transmit FCS Error Counter (TFCS)

GMAC0 Address: 0x1900011C
GMAC1 Address: 0x1A00011C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted FCS errors.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFCS	Transmit FCS error counter. Incremented for every valid sized packet with an incorrect FCS value.

7.20.62 Transmit Control Frame Counter (TXCF)

GMAC0 Address: 0x19000120
GMAC1 Address: 0x1A000120
Access: Read/Write
Reset: 0x0

This register is used to count transmitted control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCF	Transmit control frame counter. Incremented for every valid size frame with a type field signifying a control frame.

7.20.63 Transmit Oversize Frame Counter (TOVR)

GMAC0 Address: 0x19000124
GMAC1 Address: 0x1A000124000128
Access: Read/Write
Reset: 0x0

This register is used to count transmitted oversize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TOVR	Transmit oversize frame counter. Incremented for each oversized transmitted frame with an correct FCS value.

7.20.64 Transmit Undersize Frame Counter (TUND)

GMAC0 Address: 0x19000128
GMAC1 Address: 0x1A000128
Access: Read/Write
Reset: 0x0

This register is used to count transmitted undersize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TUND	Transmit undersize frame counter. Incremented for every frame less then 64 bytes, with a correct FCS value.

7.20.65 Transmit Fragment Counter (TFRG)

GMAC0 Address: 0x1900012C
GMAC1 Address: 0x1A00012C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted fragments.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFRG	Transmit fragment counter. Incremented for every frame less then 64 bytes, with an incorrect FCS value.

7.20.66 Carry Register 1 (CAR1)

GMAC0 Address: 0x19000130
GMAC1 Address: 0x1A000130
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31	C1_64	Carry register 1 TR64 counter carry bit
30	C1_127	Carry register 1 TR127 counter carry bit
29	C1_255	Carry register 1 TR255 counter carry bit
28	C1_511	Carry register 1 TR511 counter carry bit
27	C1_1K	Carry register 1 TR1K counter carry bit
26	C1_MAX	Carry register 1 TRMAX counter carry bit
25	C1_MGV	Carry register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	C1_RBY	Carry register 1 RBYT counter carry bit
15	C1_RPK	Carry register 1 RPKT counter carry bit
14	C1_RFC	Carry register 1 RFCS counter carry bit
13	C1_RMC	Carry register 1 RMCA counter carry bit
12	C1_RBC	Carry register 1 RBCA counter carry bit
11	C1_RXC	Carry register 1 RXCF counter carry bit
10	C1_RXP	Carry register 1 RXPF counter carry bit
9	C1_RXU	Carry register 1 RXUO counter carry bit
8	C1_RAL	Carry register 1 RALN counter carry bit
7	C1_RFL	Carry register 1 RFLR counter carry bit
6	C1_RCD	Carry register 1 RCDE counter carry bit
5	C1_RCS	Carry register 1 RCSE counter carry bit
4	C1_RUN	Carry register 1 RUND counter carry bit
3	C1_ROV	Carry register 1 ROVR counter carry bit
2	C1_RFR	Carry register 1 RFRG counter carry bit
1	C1_RJB	Carry register 1 RJBR counter carry bit
0	C1_RDR	Carry register 1 RDRP counter carry bit

7.20.67 Carry Register 2 (CAR2)

GMAC0 Address: 0x19000134
GMAC1 Address: 0x1A000134
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	C2_TJB	Carry register 2 TJBR counter carry bit
18	C2_TFC	Carry register 2 TFCS counter carry bit
17	C2_TCF	Carry register 2 TXCF counter carry bit
16	C2_TOV	Carry register 2 TOVR counter carry bit
15	C2_TUN	Carry register 2 TUND counter carry bit
14	C2_TFG	Carry register 2 TFRG counter carry bit
13	C2_TBY	Carry register 2 TBYT counter carry bit
12	C2_TPK	Carry register 2 TPKT counter carry bit
11	C2_TMC	Carry register 2 TMCA counter carry bit
10	C2_TBC	Carry register 2 TBCA counter carry bit
9	C2_TPF	Carry register 2 TXPF counter carry bit
8	C2_TDF	Carry register 2 TDFR counter carry bit
7	C2_TED	Carry register 2 TEDF counter carry bit
6	C2_TSC	Carry register 2 TSCL counter carry bit
5	C2_TMA	Carry register 2 TMCL counter carry bit
4	C2_TLC	Carry register 2 TLCL counter carry bit
3	C2_TXC	Carry register 2 TXCL counter carry bit
2	C2_TNC	Carry register 2 TNCL counter carry bit
1	C2_TPH	Carry register 2 TPFH counter carry bit
0	C2_TDP	Carry register 2 TDRP counter carry bit

7.20.68 Carry Mask Register 1 (CAM1)

GMAC0 Address: 0x19000138
GMAC1 Address: 0x1A000138
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit NaM1e	Description
31	M1_64	Mask register 1 TR64 counter carry bit
30	M1_127	Mask register 1 TR127 counter carry bit
29	M1_255	Mask register 1 TR255 counter carry bit
28	M1_511	Mask register 1 TR511 counter carry bit
27	M1_1K	Mask register 1 TR1K counter carry bit
26	M1_MAX	Mask register 1 TRMAX counter carry bit
25	M1_MGV	Mask register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	M1_RBY	Mask register 1 RBYT counter carry bit
15	M1_RPK	Mask register 1 RPKT counter carry bit
14	M1_RFC	Mask register 1 RFCS counter carry bit
13	M1_RMC	Mask register 1 RMCA counter carry bit
12	M1_RBC	Mask register 1 RBCA counter carry bit
11	M1_RXC	Mask register 1 RXCF counter carry bit
10	M1_RXP	Mask register 1 RXPF counter carry bit
9	M1_RXU	Mask register 1 RXUO counter carry bit
8	M1_RAL	Mask register 1 RALN counter carry bit
7	M1_RFL	Mask register 1 RFLR counter carry bit
6	M1_RCD	Mask register 1 RCDE counter carry bit
5	M1_RCS	Mask register 1 RCSE counter carry bit
4	M1_RUN	Mask register 1 RUND counter carry bit
3	M1_ROV	Mask register 1 ROVR counter carry bit
2	M1_RFR	Mask register 1 RFRG counter carry bit
1	M1_RJB	Mask register 1 RJBR counter carry bit
0	M1_RDR	Mask register 1 RDRP counter carry bit

7.20.69 Carry Mask Register 2 (CAM2)

GMAC0 Address: 0x1900013C
GMAC1 Address: 0x1A00013C
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	M2_TJB	Mask register 2 TJBR counter carry bit
18	M2_TFC	Mask register 2 TFCS counter carry bit
17	M2_TCF	Mask register 2 TXCF counter carry bit
16	M2_TOV	Mask register 2 TOVR counter carry bit
15	M2_TUN	Mask register 2 TUND counter carry bit
14	M2_TFG	Mask register 2 TFRG counter carry bit
13	M2_TBY	Mask register 2 TBYT counter carry bit
12	M2_TPK	Mask register 2 TPKT counter carry bit
11	M2_TMC	Mask register 2 TMCA counter carry bit
10	M2_TBC	Mask register 2 TBCA counter carry bit
9	M2_TPF	Mask register 2 TXPF counter carry bit
8	M2_TDF	Mask register 2 TDFR counter carry bit
7	M2_TED	Mask register 2 TEDF counter carry bit
6	M2_TSC	Mask register 2 TSCL counter carry bit
5	M2_TMA	Mask register 2 TMCL counter carry bit
4	M2_TLC	Mask register 2 TLCL counter carry bit
3	M2_TXC	Mask register 2 TXCL counter carry bit
2	M2_TNC	Mask register 2 TNCL counter carry bit
1	M2_TPH	Mask register 2 TPFH counter carry bit
0	M2_TDP	Mask register 2 TDRP counter carry bit

7.20.70 DMA Transfer Control for Queue 0 (DMATXCNTRL_Q0)

GMAC0 Address: 0x19000180
GMAC1 Address: 0x1A000180
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 0

7.20.71 Descriptor Address for Queue 0 Tx (DMATXDESCR_Q0)

GMAC0 Address: 0x19000184
GMAC1 Address: 0x1A000184
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 0
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

7.20.72 Transmit Status (DMATXSTATUS)

GMAC0 Address: 0x19000188
GMAC1 Address: 0x1A000188
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its transferring status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	TXPKTCOUNT	This 8-bit Tx packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to TXPKTSENT (bit [0]).
15:12	RES	Reserved.
11	TX_UNDERRUN_Q3	Indicates TXUNDERRUN_Q3 as an interrupt source
10	TX_UNDERRUN_Q2	Indicates TXUNDERRUN_Q2 as an interrupt source
9	TX_UNDERRUN_Q1	Indicates TXUNDERRUN_Q1 as an interrupt source
8:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUS_ERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TXUNDERRUN_Q0	This bit is set when the DMA controller reads a set (1) empty flag in the descriptor it is processing
0	TXPKTSENT	Indicates that one or more packets transferred successfully. This bit is cleared when TXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces TXPKTCOUNT by one.

7.20.73 Receive Control (DMARXCTRL)

GMAC0 Address: 0x1900018C
GMAC1 Address: 0x1A00018C
Access: Read/Write
Reset: 0x0

This register is used to enable the DMA to receive packets.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXENABLE	Allows the DMA to receive packet transfers. When set, the built-in DMA controller begins receiving packets as the FIFO indicates they are available (FRSOF asserted). The DMA controller clears this bit when it encounters an RX overflow or bus error state.

7.20.74 Pointer to Receive Descriptor (DMARXDESCR)

GMAC0 Address: 0x19000190
GMAC1 Address: 0x1A000190
Access: Read/Write
Reset: 0x0

This register is used to find the location of the first TX packet descriptor in the memory.

Bit	Bit Name	Description
31:2	DESCRIPTOR_ ADDRESS	The descriptor address. When the RXENABLE (bit [0] of the Receive Control (DMARXCTRL), page 7-288 register) is set by the host, the DMA controller reads this register to find the host memory location of the first receive packet descriptor.
1:0	RES	Ignored by the DMA controller, because it is a requirement of the system that all descriptors are 32-bit aligned in the host memory.

7.20.75 Receive Status (DMARXSTATUS)

GMAC0 Address: 0x19000194
GMAC1 Address: 0x1A000194
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its receiving status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	RXPKTCOUNT	This 8-bit receive packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to RXPKTRECEIVED (bit [0]).
15:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUSERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RXOVERFLOW	This bit is set when the DMA controller reads a set empty flag in the descriptor it is processing
1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXPKT RECEIVED	Indicates that one or more packets were received successfully. This bit is cleared when the RXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces RXPKTCOUNT by one.

7.20.76 Interrupt Mask (DMAINTRMASK)

GMAC0 Address: 0x19000198
GMAC1 Address: 0x1A000198
Access: Read/Write
Reset: 0x0

This register is used to configure interrupt masks for the DMA. Setting a bit to 1 enables the corresponding status signal as an interrupt source. The register "DMA Interrupts" is the AND of DMA status bits with this register.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3_MASK	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
10	TX_UNDERRUN_Q2_MASK	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
9	TX_UNDERRUN_Q1_MASK	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the Receive Status (DMARXSTATUS), page 7-288 register) as an interrupt source
6	RX_OVERFLOW_MASK	Setting this bit to 1 enables RXOVERFLOW (bit [1] in the Receive Status (DMARXSTATUS), page 7-288 register) as in interrupt source
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKTRECEIVED_MASK	Enables RXPKTRECEIVED (bit [0] in the Receive Status (DMARXSTATUS), page 7-288 register) as an interrupt source
3	BUSERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0_MASK	Setting this bit 1 enables TXUNDERRUN_Q0 (bit [1] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
0	TXPKTSENT_MASK	Setting this bit to 1 enables TXPKTSENT (bit [0] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source

7.20.77 Interrupts (DMAINTERRUPT)

GMAC0 Address: 0x1900019C
GMAC1 Address: 0x1A00019C
Access: Read/Write
Reset: 0x0

This register is used to configure interrupts for the DMA. Flags in this register clear when their corresponding Status bit is cleared.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
10	TX_UNDERRUN_Q2	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
9	TX_UNDERRUN_Q1	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the Transmit Status (DMATXSTATUS), page 7-287 register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 records an Rx bus error interrupt when BUS_ERROR (bit [3] in the Receive Status (DMARXSTATUS), page 7-288 register) and BUS_ERROR_MASK (bit [7] of the Interrupt Mask (DMAINTRMASK), page 7-289 register) are both set
6	RX_OVERFLOW_MASK	Setting this bit to 1 records an Rx overflow error interrupt when RX_OVERFLOW (bit [1] in the Receive Status (DMARXSTATUS), page 7-288 register) and RX_OVERFLOW_MASK (bit [6] of the Interrupt Mask (DMAINTRMASK), page 7-289 register) are both set
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKT_RECEIVED_MASK	Records a RX_PKT_RECEIVED error interrupt when RX_PKT_RECEIVED (bit [0] in the Receive Status (DMARXSTATUS), page 7-288 register) and RXPKT_RECEIVED_MASK (bit [4] of the Interrupt Mask (DMAINTRMASK), page 7-289 register) are both set
3	BUS_ERROR	Setting this bit to 1 enables BUSERROR (bit [3] in the Transmit Status (DMATXSTATUS), page 7-287 register) and BUSERROR_MASK (bit [3] of the Interrupt Mask (DMAINTRMASK), page 7-289 register) are both set
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0	Setting this bit to 1 enables TX_UNDERRUN (bit [1] in the Transmit Status (DMATXSTATUS), page 7-287 register) and TX_UNDERRUN_MASK (bit [1] of the Interrupt Mask (DMAINTRMASK), page 7-289 register) are both set
0	TXPKTSENT	Set this bit to 1 enables TXPKTSENT (bit [0] in the Transmit Status (DMATXSTATUS), page 7-287 register) and TXPKTSENT_MASK (bit [0] of the Interrupt Mask (DMAINTRMASK), page 7-289 register) are both set

7.20.78 Ethernet TX Burst (ETH_ARB_TX_BURST)

GMAC0 Address: 0x190001A0
GMAC1Address: 0x1A0001A0
Access: Read/Write
Reset: 0x48

Tx and Rx requests are arbitrated based on these parameters. These parameters ensure DDR bandwidth is available to both Tx and Rx until the specified number of DWs transfer. Note that this affects the bandwidth/latency of the data for transmit and receive.

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	MAX_RCV_BURST	Maximum number of DWs to be continuously allowed for Rx
15:10	RES	Reserved
9:0	MAX_TX_BURST	Maximum number of DWs to be continuously allowed for Tx

7.20.79 Current Tx and Rx FIFO Depth (ETH_XFIFO_DEPTH)

GMAC0 Address: 0x190001A8
GMAC1Address: 0x1A0001A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	CURRENT_RX_FIFO_DEPTH	Current Rx FIFO depth
15:10	RES	Reserved
9:0	CURRENT_TX_FIFO_DEPTH	Current Tx FIFO depth

7.20.80 Ethernet Transmit FIFO Throughput (ETH_TXFIFO_TH)

GMAC0 Address: 0x190001A4
GMAC1 Address: 0x1A0001A4
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Tx FIFO. It is use to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
25:16	TXFIFO_MAXTH	0x1D8	This bit represents the maximum number of double words in the Tx FIFO, and once this limit is surpassed, this bit should be de-asserted
15:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	TXFIFO_MINTH	0x160	This bit specifies the minimum number of double words in the Tx FIFO, and if it is less than this value, this bit needs to be asserted.

7.20.81 Ethernet Receive FIFO Threshold (ETH_RXFIFO_TH)

GMAC0 Address: 0x190001AC
GMAC1 Address: 0x1A0001AC
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Rx FIFO. It is used to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:10	SCRATCHREG_0	0x28	This bit is a pure scratch pad register that can be used by the CPU for any general purpose.
9:0	RCVFIFO_MINTH	0x0	The minimum number of double words in the receive FIFO. Once this number is reached, this bit needs to be asserted.

7.20.82 Ethernet Free Timer (ETH_FREE_TIMER)

GMAC0 Address: 0x190001B8
GMAC1 Address: 0x1A0001B8
Access: Read/Write
Reset: See field description

This register updates the Ethernet descriptors with time stamps

Bit	Bit Name	Reset	Description	
31	TIMER_UPDATE	0x1	0	Timer update at the AHB_CLK
			1	Free timer at the AHB_CLK/4
30:21	SCRATCHREG_1	0x0	The pure general purpose register for use by the CPU	
20:0	FREE_TIMER	0x3FFFFF	Free timer	

7.20.83 DMA Transfer Control for Queue 1 (DMATXCNTRL_Q1)

GMAC0 Address: 0x190001C0
GMAC1 Address: 0x1A0001C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 1

7.20.84 Descriptor Address for Queue 1 Tx (DMATXDESCR_Q1)

GMAC0 Address: 0x190001C4
GMAC1 Address: 0x1A0001C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 1
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

7.20.85 DMA Transfer Control for Queue 2 (DMATXCNTRL_Q2)

GMAC0 Address: 0x190001C8
GMAC1 Address: 0x1A0001C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 2

7.20.86 Descriptor Address for Queue 2 Tx (DMATXDESCR_Q2)

GMAC0 Address: 0x190001CC
GMAC1 Address: 0x1A0001CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 2
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

7.20.87 DMA Transfer Control for Queue 3 (DMATXCNTRL_Q3)

GMAC0 Address: 0x190001D0
GMAC1 Address: 0x1A0001D0 Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 3

7.20.88 Descriptor Address for Queue 3 Tx (DMATXDESCR_Q3)

GMAC0 Address: 0x190001D4
GMAC1 Address: 0x1A0001D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 3
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

7.20.89 DMA Transfer Arbitration Configuration (DMATXARBCFG)

GMAC0 Address: 0x190001D8
GMAC1 Address: 0x1A0001D8
Access: Read/Write
Reset: See field description

This register is used to select the type of arbitration used for the QoS feature and the weight to be assigned to a particular queue. Note that a weight of zero is not permitted and causes the hardware to misbehave.

Bit	Bit Name	Reset	Description	
31:26	WGT3	0x1	The weight for Queue 3, if WRR has been selected	
25:20	WGT2	0x2	The weight for Queue 2, if WRR has been selected	
19:14	WGT1	0x4	The weight for Queue 1, if WRR has been selected	
13:8	WGT0	0x8	The weight for Queue 0, if WRR has been selected	
7:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RRMODE	0x4	Round robin mode	
			0	Simple priority (Q0 highest priority)
			1	Weighted round robin (WRR)

7.20.90 Tx Status and Packet Count for Queues 1 to 3 (DMATXSTATUS_123)

GMAC0 Address: 0x190001E4
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	RES	Reserved
23:16	TXPKTCOUNT_CH3	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 3, and decrements when the host writes a 1 to bit TXPKTSENT for chain 3 in the DMATXSTATUS register. Default is 0.
15:8	TXPKTCOUNT_CH2	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 2, and decrements when the host writes a 1 to bit TXPKTSENT for chain 2 in the DMATXSTATUS register. Default is 0.
7:0	TXPKTCOUNT_CH1	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 1, and decrements when the host writes a 1 to bit TXPKTSENT for chain 1 in the DMATXSTATUS register. Default is 0.

7.20.91 Local MAC Address Dword0 (LCL_MAC_ADDR_DW0)

GMAC0 Address: 0x19000200
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_MAC_ADDR_DW0	Bits [31:0] of the local L2 MAC address

7.20.92 Local MAC Address Dword1 (LCL_MAC_ADDR_DW1)

GMAC0 Address: 0x19000204
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	LOCAL_MAC_ADDR_DW1	Bits [47:32] of the local L2 MAC address

7.20.93 Next Hop Router MAC Address Dword0 (NXT_HOP_DST_ADDR_DW0)

GMAC0 Address: 0x19000208
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_MAC_DST_ADDR_DW0	Bits [31:0] of the next hop router's local L2 MAC address

7.20.94 Next Hop Router MAC Destination Address Dword1 (NXT_HOP_DST_ADDR_DW1)

GMAC0 Address: 0x1900020C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	LOCAL_MAC_DST_ADDR_DW1	Bits [47:32] of the local L2 MAC address

7.20.95 Local Global IP Address 0 (GLOBAL_IP_ADDR0)

GMAC0 Address: 0x19000210
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR0	Local IP address 0 (up to 4 global IP addresses are supported)

7.20.96 Local Global IP Address 1 (GLOBAL_IP_ADDR1)

GMAC0 Address: 0x19000214
GMAC1 Address: 0x1A000214
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR1	Local IP address 1 (up to 4 global IP addresses are supported)

7.20.97 Local Global IP Address 2 (GLOBAL_IP_ADDR2)

GMAC0 Address: 0x19000218
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR2	Local IP address 2 (up to 4 global IP addresses are supported)

7.20.98 Local Global IP Address 3 (GLOBAL_IP_ADDR3)

GMAC0 Address: 0x1900021C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR3	Local IP address 3 (up to 4 global IP addresses are supported)

7.21 Serial Flash SPI Controller Registers

Table 7-24 summarizes the serial flash SPI controller registers for the QCA9531.

Table 7-24 Serial Flash SPI Controller Registers Summary

Address	Name	Description	Page
0x1F000000	FUNCTION_SELECT_ADDR	SPI Controller GPIO Mode Select	page 298
0x1F000004	SPI_CONTROL_ADDR	SPI Address Control	page 298
0x1F000008	SPI_IO_CONTROL_ADDR	SPI I/O Address Control	page 299
0x1F00000C	SPI_READ_DATA_ADDR	SPI Read Data Address	page 299
0x1F000010	SPI_SHIFT_DATAOUT_ADDR	SPI Data to Shift Out	page 299
0x1F000014	SPI_SHIFT_CNT_ADDR	SPI Content to Shift Out or In	page 300
0x1F000018	SPI_SHIFT_DATAIN_ADDR	SPI Data to Shift In	page 300

7.21.1 SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR)

Address: 0x1F000000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FUNCTION_SELECT	Writing a non-zero value to this register selects the GPIO mode for the SPI controller.

7.21.2 SPI Address Control (SPI_CONTROL_ADDR)

Address: 0x1F000004
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:14	RES	Reserved
13:8	TSHSL_CNT	Minimum time for which CS has must be deasserted between two SPI transactions.
7	SPI_RELOCATE	When this bit is set, 16 MB of SPI space is mapped to 0x1E00_0000, else it is mapped to 0x1F00_0000.
6	REMAP_DISABLE	Disables the alias of the lower 4 MB of SPI space, enabling the ROM to boot from 0x1FC_0000 to alias to 0x1F0_0000 until software disables the aliasing.
5:0	CLOCK_DIVIDER	The clock divider is based on the AHB clock. The generated clock is AHBclock/((CLOCK_DIVIDER+1) * 2).

7.21.3 SPI I/O Address Control (SPI_IO_CONTROL_ADDR)

Address: 0x1F000008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:19	RES	Reserved	
18	IO_CS2	Chip select 2. Active low signal.	
		0	Enable chip select 2
		1	Disable chip select 2
17	IO_CS1	Chip select 1. Active low signal.	
16	IO_CS0	Chip select 0. Active low signal.	
15:9	RES	Reserved	
8	IO_CLK	SPI clock	
7:1	RES	Reserved	
0	IO_DO	Data out	

7.21.4 SPI Read Data Address (SPI_READ_DATA_ADDR)

Address: 0x1F00000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	READ_DATA	The SPI read data is shifted in and sampled every cycle

7.21.5 SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR)

Address: 0x1F000010
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	SHIFT_DATAOUT	The data (either CMD, ADDR, or DATA) to be shifted out every clock cycle

7.21.6 SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR)

Address: 0x1F000014
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31	SHIFT_EN	Enables shifting data out
30	SHIFT_CHNL	If set to 1, enables chip select 2
29		If set to 1, enables chip select 1
28		If set to 1, enables chip select 0
27	SHIFT_CLKOUT	Initial value of the clock signal
26	TERMINATE	When set to 1, deasserts the chip select
25:7	RES	Reserved
6:0	SHIFT_COUNT	The number of bits to be shifted out or shifted in on the data line

7.21.7 SPI Data to Shift In (SPI_SHIFT_DATAIN_ADDR)

Address: 0x1F000018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	SHIFT_DATAIN	SPI read data

7.22 Ethernet Switch Registers

This section describes the internal registers of the Ethernet Switch registers. Table 7-25 summarizes the Ethernet registers for the Ethernet switch.

Table 7-25 Ethernet Switch Registers Summary

Address	Name	Page
0x0000-0x00B8	Global Control Registers	page 302
0x0100-0x0130, 0x0200-0x0230, 0x0300-0x0330, 0x0400-0x0430, 0x0500-0x0530, 0x0600-0x0630	Port Control Registers	page 321
0x00-0x1E	PHY Registers	page 332
0x0B-0x3C	Debug Port Registers	page 345
0x00-0x16	MMD3 PCS Registers	page 349
0x00-0x8000	MMD7 AutoNegotiation Registers	page 351

NOTE Access to switch internal registers through a dedicated internal MDIO interface. The internal MDIO interface is controlled through GMAC1 MII registers described in MII Configuration, page 7-259 through MII Indicators, page 7-261.

7.23 Global Control Registers

Table 7-26 summarizes the global control registers.

Table 7-26 Global Control Register Summary

Offset	Description	Page
0x0000	Mask Control	page 302
0x0004	Operational Mode 0	page 303
0x0008	Operational Mode 1	page 303
0x0014	Global Interrupt	page 304
0x0018	Global Interrupt Mask	page 305
0x0020 — 0x0024	Global MAC Address	page 306
0x0028	Loop Check Result	page 306
0x002C	Flood Mask	page 307
0x0030	Global Control	page 308
0x0034	Flow Control 0	page 309
0x0038	Flow Control 1	page 309
0x003C	QM Control	page 309
0x0040 — 0x0044	VLAN Table Function	page 311
0x0050 — 0x0058	Address Table Function	page 311
0x005C	Address Table Control	page 312
0x0060 — 0x006C	IP Priority Mapping 2	page 315
0x0070	Tag Priority	page 317
0x0074	Service Tag	page 317
0x0078	CPU Port	page 317
0x007C	LPI	page 318
0x0080	MIB Function	page 318
0x0098	MDIO Control	page 319
0x00B0 — 0x00B8	LED Control	page 319

7.23.1 Mask Control

Address Offset: 0x0000
Access: See field description
Reset: See field description

This register can only be reset by a hardware reset.

Bit	Bit Name	Type	Reset	Description
31	SOFT_RET	WO/SC	0x0	Set to 1 for a software reset; set by the software to initiate the hardware. It should be self-cleared by the hardware after the initialization is done.
30:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:8	DEVICE_ID	RO	0x02	Device identifier
7:0	REV_ID	RO	0x01	Revision identifier

7.23.2 Operational Mode 0

Address Offset: 0x0004

Access: Read/Write
Reset: 0x0

This register can only be reset by a hardware reset.

Bit	Bit Name	Description
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.
10	MAC0_PHY_MII_EN	Set to 1 to connect mac0 to CPU through MII interface, PHY mode
9:7	RES	Reserved
6	MAC0_MAC_GMII_EN	Set to 1 to connect mac0 to CPU through GMII interface, MAC mode
5:0	RES	Reserved

7.23.3 Operational Mode 1

Address Offset: 0x0008

Access: Read/Write

Reset: 0x0

This register can only be reset by a hardware reset.

Bit	Bit Name	Description
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.
28	PHY4_MII_EN	Set to 1 to connect phy4 to CPU through MII interface
27:1	RES	Reserved
0	MAC5_MAC_MII_RXCLK_SEL	Set to 1 to select invert clock input for port0 MAC mode, MII interface RXCLK

7.23.4 Global Interrupt

Address Offset: 0x0014

Access: Read/Write

Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:19	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
18	LOOP_CHECK_INT	RW1C	0x0	Interrupt when loop checked by hardware
17:15	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
14	HARDWARE_INI_DONE	RW1C	0x1	Interrupt when hardware memory initialization is complete
13	MIB_INI_INT	RW1C	0x1	Interrupt when MIB memory initialization is complete
12	MIB_DONE_INT	RW1C	0x0	Interrupt when MIB access by CPU is complete
11	BIST_DONE_INT	RW1C	0x0	Interrupt when BIST test is complete
10	VT_MISS_VIO_INT	RW1C	0x0	Interrupt when the VID is not found in the VLAN table
9	VT_MEM_VIO_INT	RW1C	0x0	Interrupt when the VID is in the VLAN table, but the source port is not a member of the VLAN
8	VT_DONE_INT	RW1C	0x0	Interrupt when the CPU has completed an access of the VLAN table
7	QM_INI_INT	RW1C	0x1	Interrupt when the QM memory initialization is complete
6	AT_INI_INT	RW1C	0x1	Interrupt when the Address table initialization is complete
5	ARL_FULL_INT	RW1C	0x0	Interrupt when a new address is “learned” by being added to the address table, but the two addresses are both valid
4	ARL_DONE_INT	RW1C	0x0	Interrupt when the CPU access of the Address table is complete
3	MDIO_DONE_INT	RW1C	0x0	Interrupt when MDIO access of the switch register is complete
2	PHY_INT	RW1C	0x0	Physical layer interrupt
1	EEPROM_ERR_INT	RW1C	0x0	Interrupt when an error is detected during the loading of an EEPROM
0	EEPROM_INT	RW1C	0x0	Interrupt when the loading of an EEPROM is complete

7.23.5 Global Interrupt Mask

Address Offset: 0x0018

Access: Read/Write

Reset: 0x0

Each bit in this register is corresponding to a bit in the GLOBAL INTERRUPT REGISTER. Interrupts are allowed to be sent out when both the interrupt event and mask bit are set.

Bit	Bit Name	Type	Description
31:19	RES	RW	Reserved. Must be written with zero. Contains zeros when read.
18	LOOP_CHECK_INT_EN	RW	Enable loop check interrupt
17:15	RES	RW	Reserved. Must be written with zero. Contains zeros when read.
14	HARDWARE_INI_DONE_EN	RW	Enable interrupt when hardware memory initiation is complete
13	MIB_INI_INT_EN	RW	MIB was accessed by the CPU
12	MIB_DONE_INT_EN	RW	Enable the interrupt of MIB accesses done by CPU
11	BIST_DONE_INT_EN	RW	Enable BIST test complete interrupt
10	VT_MISS_VIO_INT_EN	RW	Interrupt when the VID of the received frame is not in the VLAN table
9	VT_MEM_VIO_INT_EN	RW	Interrupt when the VID of the received frame is in the VLAN table, but the source port is not the member of the VID
8	VT_DONE_INT_EN	RW	The VLAN table was accessed by the CPU
7	QM_INI_INT_EN	RW	Enable interrupt when QM memory initiation is complete
6	AT_INI_INT_EN	RW	Enable interrupt when address table initiation is complete
5	ARL_FULL_INT_EN	RW	Interrupt when a new address to learn is in the address table, but the address's two entries are both valid
4	ARL_DONE_INT_EN	RW	The address table was accessed by the CPU
3	MDIO_DONE_INT_EN	RW	The MDIO access switch register was interrupted
2	PHY_INT_EN	RW	Physical layer interrupt
1	EEPROM_ERR_INT_EN	RW	Interrupt when an error occurred during load EEPROM
0	EEPROM_INT_EN	RW	Interrupt when an EEPROM load has completed

7.23.6 Global MAC Address

Address Offset: 0x0020, 0x0024

Access: Read/Write

Reset: See field description

These registers can only be reset by hardware.

Offset	Bit	Bit Name	Type	Reset	Description
0x0020	31:16	Reserved	RO	0x0	Reserved
	15:8	MAC_ADDR_BYTE4	RW	0x0	Station address of switch. Used as source address in pause frame or other management frames
	7:0	MAC_ADDR_BYTE5	RW	0x01	
0x0024	31:24	MAC_ADDR_BYTE0	RW	0x0	Station address of the switch, used as source address in pause frame or other management frames
	23:16	MAC_ADDR_BYTE1	RW	0x0	
	15:8	MAC_ADDR_BYTE2	RW	0x0	
	7:0	MAC_ADDR_BYTE3	RW	0x0	

7.23.7 Loop Check Result

Address Offset: 0x0028

Access: Read Only

Reset: 0x0

These registers can only be reset by hardware.

Bit	Bit Name	Type	Description
31:8	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
7:4	PORT_NUM_NEW	RO	When hardware checked loops occur, these bits indicate MAC address new port number.
4:0	PORT_NUM_OLD	RO	When hardware checked loops occur, these bits indicate MAC address old port number.

7.23.8 Flood Mask

Address Offset: 0x002C

Access: Read/Write

Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:25	BROAD_DP	RW	0x7E	If the MAC receives broadcast frames, use these bits to determine the destination port	
24	ARL_UNI_LEAKY_EN	RW	0x0	Configures unicast frame leaky VLANs	
				0	USE LEAKY_EN bit in ARL table to control unicast frame leaky VLAN and ignore “UNI_LEAKY_EN”
				1	Ignore LEAKY_EN bit in ARL table to control unicast frame leaky VLAN. Only use port-based UNI_LEAKY_EN to control unicast frame leaky VLAN
23	ARL_MULTI_LEAKY_EN	RW	0	Configures multicast frame leaky VLANs	
				0	Use LEAKY_EN bit in ARL table to control multicast frame leaky VLAN, and ignore MULTI_LEAKY_EN.
				1	Ignore LEAKY_EN bit in ARL table to control multicast frame leaky VLAN. Only use port base MULTI_LEAKY_EN to control multicast frame leaky VLAN.
22:16	MULTI_FLOOD_DP	RW	0x7E	If the MAC receives unknown a multicast frame which the DA is not contained in the ARL table, use these bits to determine the destination port.	
15:14	RES	RO	0	Reserved. Must be written with zero. Contains zeros when read.	
13:8	IGMP_JOIN_LEAVE_DP	RW	0x6	If the MAC receives an IGMP/MLD fast join or leave frame, use these bits to determine the destination port	
7:6	RES	RO	0	Reserved. Must be written with zero. Contains zeros when read.	
6:0	UNI_FLOOD_DP	RW	0x7E	If the MAC receives unknown unicast frames in which the DA is not contained in the ARL table, use these bits to determine the destination port	

7.23.9 Global Control

Address Offset: 0x0030

Access: Read/Write

Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:30	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
29	RATE_DROP_EN	RW	0x1	Drop packet enable due to rate limit.	
				0	Switch would use flow control to the source port due to rate limit, if the port won't stop switch will drop frame from that port.
				1	Switch will drop frames due to rate limit.
28:26	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
25:24	ING_RATE_TIME_SLOT	RW	0x1	Ingress rate limit control timer slot. Note: If the port rate limit set to less than 96 Kbps, do not select 100 µs as time slot.	
				00	100 µs
				01	1 ms
				10	10 ms
				11	100 ms
23:20	RELOAD_TIMER	RW	0xF	Reload EEPROM timer If the EEPROM can't be read from, the EEPROM should be reloaded when the timer is completed. The timer is set by multiplying the number here by 8 ms. If these bits are zero, the EEPROM will not be reloaded	
19	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
18	BROAD_DROP_EN	RW	0x0	Broadcast storm control drop packet enable.	
				0	When broadcast storm occur, switch will use flow control to the source port first, if the port will not stop, the switch will drop frame.
				1	Switch will drop frames if broadcast storm occur.
17:14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
13:0	MAX_FRAME_SIZE	RW	0x5EE	Max frame sized can be received and transmitted by MAC. If a packet's size is larger than MX_FRAME_SIZE, it will be dropped by the MAC. The value is for a normal packet. It should add 4 by MAC if VLANs are supported, add 8 for double VLANs, and add 2 for a Qualcomm Atheros header. For Jumbo frames, the maximum frame size is 9 Kbytes.	

7.23.10 Flow Control 0

Address Offset: 0x0034
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:24	PORT_XON _THRES_0	RO	0x16	Port-based transmit on threshold for MAC0. When block memory is used by one port less than this value, the MAC sends out a pause off-frame, and the link partner starts transmitting frames.
23:16	GOL_XON_ THRES	RW	0x60	Global-based transmit on threshold. When the block memory used by all the ports is less than the value entered here, the MAC sends out a pause off-frame, and the link partner starts transmitting frames.
15:8	PORT_XOFF _THRES_0	RO	0x20	Port-based transmit off threshold for MAC0. When block memory is used by one port more than this value, the MAC sends out a pause on-frame, and the link partner stops transmitting frames.
7:0	GOL_XOFF_ THRES	RW	0x90	Global-based transmit off threshold. When block memory used by all the ports is more than the value entered here, the MAC sends out a pause on frame, and the link partner stops transmitting frames.

7.23.11 Flow Control 1

Address Offset: 0x0038
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:24	PORT_XON _THRES_2	RW	0x16	Port-based transmit on threshold for MAC5 and MAC6. When block memory is used by one port less than this value, the MAC sends out a pause off-frame, and the link partner starts transmitting frames.
23:16	PORT_XON_ THRES	RW	0x16	Port-based transmit on threshold for MAC1 through MAC4. When block memory is used by one port is less than this value, the MAC sends out a pause off-frame, and the link partner starts transmitting frames.
15:8	PORT_XOFF _THRES_2	RO	0x20	Port-based transmit off threshold for MAC5 and MAC6. When block memory is used by one port more than this value, the MAC sends out a pause on-frame, and the link partner stops transmitting frames.
7:0	PORT_XOFF_ THRES	RW	0x20	Port-based transmit off threshold. When block memory used by one port is more than this value, the MAC sends out a pause on frame, and the link partner stops transmitting frames.

7.23.12 QM Control

Address Offset: 0x003C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:28	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
27:24	IGMP_JOIN_ STATUS	RW	—	Use for IGMP packet learn in ARL table, define the status	
				0	Indicates entry is empty
				7:1	Indicates entry is dynamic and valid
				14:8	Reserved
				15	Indicates entry is static and will not be aged out or changed by the hardware

Bit	Bit Name	Type	Reset	Description
23	IGMP_JOIN_ LEAKY_EN	RW	0x1	IGMP join address leaky VLAN enable.
				0 IGMP join address should clear the LEAKY_EN bit in ARL table
				1 IGMP join address should set the LEAKY_EN bit in ARL table
22	IGMP_JOIN_ NEW_EN	RW	0x0	Enable hardware. Add a new address to ARL table when IGMP/MLD join frame are received and remove address from ARL when IGMP/MLD leave frames are received.
21	ACL_EN	RW	0x0	ACL rule enable. If this bit is set to zero, ACL check is disable.
20	PPPOE_ REDIRECT_ EN	RW	0x0	Enable sending PPPoE discovery frames to the CPU. If this bit is set to 1, PPPoE discovery frames are sent to the CPU port. If this bit is set to 0, PPPoE discovery frames are transmitted as normal frames
19	IGMP_V3_EN	RW	0x0	Set to 1 for hardware to acknowledge IGMP v3 frame and MLD v2 frame, and multicast address can join or leave hardware
18	IGMP_JOIN_ PRI_REMAP_ EN	RW	0x0	Use for IGMP packet learning in ARL table. Defines DA priority remap enable
17:16	IGMP_JOIN_ PRI	RW	0x0	Use for IGMP packet learning in ARL table. Defines the DA priority when IGMP_JOIN_PRI_REMAP_EN is enabled.
15	ARP_EN	RW	0x0	ARP frame acknowledge enable
14	ARP_ REDIRECT_EN	RW	0x0	Used to denote the destination of the redirected ARP frame
				0 ARP frame redirect to CPU port
				1 ARP frame copy to CPU
13	RIP_COPY_EN	RW	0x0	Choose to copy or not copy the RIP v1 frame
				0 Do not copy RIP v1 frame to CPU
				1 RIP v1 frame copy to CPU
12	EAPOL_ REDIRECT_ EN	RW	0x0	Used to process the 802.1x frame
				0 802.1x frame redirected to CPU
				1 802.1x frame copy to CPU
11	IGMP_COPY_ EN	RW	0x0	Used to process the IGMP/MLD frames
				0 QM will copy IGMP/MLD frames to the CPU port
				1 QM will redirect IGMP/MLD frames to the CPU port
10	PPPOE_EN	RW	0x0	Set to 1 to enable hardware acknowledgement of PPPoE frames
9:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6	MANAGE_VID_ VIO_DROP _EN	RW	0x1	Used to configure management frames if a VLAN violation occurs
				0 Management frames are transmitted out if a VLAN violation occurs
				1 Management frames should be dropped if a VLAN violation occurs
5:0	FLOW_DROP_ CNT	RW	0xE	Max free queue could be use after the port has been flow control. Then packets should be drop except the highest priority. Default value 0xE is set to normal packets which length is no more than 1518 bytes. For jumbo frame, 0x21 is commanded.

7.23.13 VLAN Table Function 0

Address Offset: 0x0040
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Type	Description	
31	VT_PRI_EN	RW	When VT_PRI_EN is set, then VT_PRI will replace the VLAN priority in the frame as its QoS classification	
30:28	VT_PRI	RW	When VT_PRI_EN is set, the VT_PRI will replace VLAN priority in the frame as its QoS classification	
27:16	VID	RW	VLAN ID to be added or purged	
15:12	RES	RO	Reserved. Must be written with zero. Contains zeros when read	
11:8	VT_PORT_NUM	RW	Port number to be removed	
7:4	RES	RO	Reserved. Must be written with zero. Contains zeros when read	
3	VT_BUSY	RW	VLAN table is busy. This bit must be set to 1 to start a VT operation and cleared to 0 after the operation is done. If this bit is set to 1, the CPU can not request another operation	
2:0	VT_FUNC	RW	VLAN table operation control	
			000	No operation
			001	Flush all entries
			011	Load an entry. If these bits are set, the CPU will load an entry form the VLAN table
			011	Purge an entry. If these bits are set, the CPU will purge an entry form the VLAN table
			100	Remove a port form the VLAN table. The port number which will be removed is indicted in VT_PORT_NUM
			101	Get the next VID. If VID is 12'b0 and VT_BUSY is set by software, hardware will search for the first valid entry in the VLAN table If VID is 12'b0 and VT_Busy is reset by hardware, then there is no valid entry from VID set by the software
			110	Read one entry

7.23.14 VLAN Table Function 1

Address Offset: 0x0044
Access: Read/Write
Reset 0x0

Bit	Bit Name	Type	Description	
31:12	Reserved	RO	Reserved. Must be written with zero. Contains zeros when read	
11	VT_VALID	RW	Used to indicate the validity for the VLAN table	
			0	Indicates the entry is empty
			1	Indicates entry is valid
10:7	Reserved	RO	Reserved. Must be written with zero. Contains zeros when read	
6:0	VID_MEM	RW	VID member in the VLAN table. These bits are used to indicate which ports are members of the VLAN. Bit 0 is assigned to port0, 1 to port1, 2, to port2, and so on.	

7.23.15 Address Table Function 0

Address Offset: 0x0050

Access: Read/Write

Reset:0x0

Bit	Bit Name	Type	Description	
31:24	AT_ADDR_BYTE4	RW	Byte 4 of the address	
23:16	AT_ADDR_BYTE5	RW	The last byte of the address	
15:13	RES	RO	Reserved. Must be written with zero. Contains zeros when read	
12	AT_FULL_VIO	RW1C	ARL table-full violation. This bit is set to 1 if the ARL table is full when the CPU wants to add a new entry to the ARL table; it can also be set to 1 if the ARL table is empty when the CPU wants to purge and entry to the ARL table.	
11:8	AT_PORT_NUM	RW	Port number to be flushed. If AT_FUNC is set to 101, lookup module must flush all the unicast entries for the port (or flush the port from the ARL table)	
7:5	RES	RO	Reserved. Must be written with zero. Contains zeros when read	
4	FLUSH_STATIC_EN	RW	Used to select dynamic or static ACL entries	
			0	When AT_FUNC is set to 101, only dynamic entries in the ARL table will be flushed
			1	When AT_FUNC is set to 101, all static entries in the ARL table can be flushed.
3	AT_BUSY	RW	Address table busy. This bit must be set to 1 to start an AT operation and cleared to 0 when the operation is complete. If this bit is set to 1, the CPU can not request another operation	
2:0	AT_FUNC	RW	Address table function	
			000	No operation
			001	Flush all entries
			010	Load an entry. If these bits are set to 3'b010, the CPU will load an entry into the ARL table
			011	Purge an entry. If these bits are set, the CPU will purge an entry from the ARL table.
			100	Flush all unlocked entries in the ARL
			101	Flush one port from the ARL table
			110	Get the next valid or static entry in the ARL table If the address and AT_STATUS are all zero, the hardware will search for the first valid entry from entry0 If the address and AT_STATUS is not zero, the hardware will search for the next valid entry whose address is 48'h0. If hardware returns with the address and AT_STATUS all zero, there is no next valid entry in the ARL table.
			111	Search MAC address

7.23.16 Address Table Function 1

Address Offset: 0x0054
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Type	Description
31:24	AT_ADDR_BYTE0	RW	The first byte of the address to operate. This byte is the highest byte of the MAC address for the MSB.
23:16	AT_ADDR_BYTE1	RW	The second byte of the address
15:18	AT_ADDR_BYTE2	RW	The third byte of the address
7:0	AT_ADDR_BYTE3	RW	The forth byte of the address

7.23.17 Address Table Function 2

Address Offset: 0x0058
Access: Read/Write
Reset: 0x0

Bit	Bit Name	RW	Description	
31:27	RES	RO	Reserved. Must be written with zero. Contains zeros when read	
26	COPY_TO_CPU	RW	Set to 1 so packets received with this address will be copied to the CPU port	
25	REDIRECT_TO_CPU	RW	Set to 1 so packets received with this address will be redirected to the CPU port. If no CPU is connected to the switch, this packet will be discarded	
24	LEAKY_EN	RW	Setting this bit to 1 enables leaky VLANs for this MAC address. This bit can be used for unicast and multicast frames, control by ARL_UNI_LEAKY_EN and ARL_MULTI_LEAKY_EN	
23:20	RES	RO	Reserved. Must be written with zero. Contains zeros when read	
19:16	AT_STATUS	RW	Destination address status, associated to STATUS bits in the address table	
			0	Indicates entry is empty
			7:1	Indicates the entry is dynamic and valid
			14:8	Reserved
			15	Indicates entry is static and won't be aged out or changed by the hardware.
15	MAC_CLONE	RW	MAC clone address. Set to 1 to clone this MAC address. CPU cannot age-out. Other ports learn and age as normal. If DA and VID result is CPU port, send the packet to normal ports only.	
14	SA_DROP_EN	RW	SA drop enable Drop packet enable when source address in this entry. If this bit is set to 1, the packet with an Source Address (SA) of this entry will be dropped	
13	MIRROR_EN	RW	Port mirror enable	
			0	Indicates packet will be sent only to the destination port
			1	Indicates packets will be sent to the mirror port and the destination port.
12	AT_PRIORITY_EN	RW	DA priority enable Set to 1 to indicate AT_PRIORITY can override any other priority determined by the frame's data	

Bit	Bit Name	RW	Description
11:10	AT_PRIORITY	RW	DA priority These priority bits can be used as a frame's priority when AT_PRIORITY_EN is set to one.
9	HASH_HIGH_ ADDR	RW	MAC hash address max bit, used for CPU_FUNC (get next valid)
8	CROSS_PORT_ STATE_EN	RW	Set to 1 to enable cross PORT_STATE.
7	RES	RW	Reserved. Must be written with zero. Contains zeros when read
6:0	DES_PORT	RW	Destination port bits for address. These bits indicate which ports are associated with the MAC address when they are set to one. Bit 0 is assigned to port 0, 1 to port1, 2 to port2, and so on.

7.23.18 Address Table Control

Address Offset: 0x005C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:27	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read	
26:24	LOOP_CHECK_ TIMER	RW	0x0	Used to set the loop back timer	
				0	Disable loop back check
				1	1 ms
				2	10 ms
				3	100 ms
				4	500 ms
				7:5	Reserved
23	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read	
22	VID_4095_DROP_EN	RW	0x0	Set to 1 to drop a frame with VID ='d4095i, if received by the switch	
21	SWITCH_STAG_ MODE	RW	0x0	Select switch work VLAN mode.	
				0	S-TAG mode
				1	C-TAG mode
20:19	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read	
18	LEARN_CHANGE_EN	RW	0x0	Used to select new address learning due to a hash violation.	
				0	If a hash violation occur when learning, no new address be learned to ARL.
				1	Enable new MAC address change if a hash violation occurs when learning
17	AGE_EN	RW	0x1	Enable age operation. Set to 1 to use the lookup module to age the address in the address table.	
16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read	
15:0	AGE_TIME	RW	0x2B	Address Table Age Timer. These bits determine the time that each entry remains valid in the address table, since last accessed. For the time is times 7s, maximum age time is about 10,000 minutes. The default value is 'h2B for five minutes. If AGE_EN is set to 1, these bits should not be set to zero.	

7.23.19 IP Priority Mapping 2

Address Offset: 0x0060,0x0064,0x0068,0x006C
Access: Read/Write
Reset: 0x0

Offset	Bit	Bit Name	Type	Reset	Description
0x0060	31:30	IP_0x3C	RW	0x0	Priority mapping value of IPv4 ToS or IPv6 TC field. Bit[7] to Bit[2] are used to map queue priority, but bit1 and bit0 are ignored. If ToS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	IP_0x38	RW	0x0	
	27:26	IP_0x34	RW	0x0	
	25:24	IP_0x30	RW	0x0	
	23:22	IP_0x2C	RW	0x0	
	21:20	IP_0x28	RW	0x0	
	19:18	IP_0x24	RW	0x0	
	17:16	IP_0x20	RW	0x0	
	15:14	IP_0x1C	RW	0x0	
	13:12	IP_0x18	RW	0x0	
	11:10	IP_0x14	RW	0x0	
	9:8	IP_0x10	RW	0x0	
	7:6	IP_0x0C	RW	0x0	
	5:4	IP_0x08	RW	0x0	
	3:2	IP_0x04	RW	0x0	
	1:0	IP_0x00	RW	0x0	
0x0064	31:30	IP_0x7C	RW	0x1	Priority mapping value of IPv4 TOS or IPv6 TC field Bits [7:2] map queue priority, but bits [1:0] are ignored. If TOS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	IP_0x78	RW	0x1	
	27:26	IP_0x74	RW	0x1	
	25:24	IP_0x70	RW	0x1	
	23:22	IP_0x6C	RW	0x1	
	21:20	IP_0x68	RW	0x1	
	19:18	IP_0x64	RW	0x1	
	17:16	IP_0x60	RW	0x1	
	15:14	IP_0x5C	RW	0x1	
	13:12	IP_0x58	RW	0x1	
	11:10	IP_0x54	RW	0x1	
	9:8	IP_0x50	RW	0x1	
	7:6	IP_0x4C	RW	0x1	
	5:4	IP_0x48	RW	0x1	
	3:2	IP_0x44	RW	0x1	
	1:0	IP_0x40	RW	0x1	

Offset	Bit	Bit Name	Type	Reset	Description
0x0068	31:30	IP_0xBC	RW	0x2	Priority mapping value of IPv4 TOS or IPv6 TC field Bits [7:2] map queue priority, but bits [1:0] are ignored. If TOS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	IP_0xB8	RW	0x2	
	27:26	IP_0xB4	RW	0x2	
	25:24	IP_0xB0	RW	0x2	
	23:22	IP_0xAC	RW	0x2	
	21:20	IP_0xA8	RW	0x2	
	19:18	IP_0xA4	RW	0x2	
	17:16	IP_0xA0	RW	0x2	
	15:14	IP_0x9C	RW	0x2	
	13:12	IP_0x98	RW	0x2	
	11:10	IP_0x94	RW	0x2	
	9:8	IP_0x90	RW	0x2	
	7:6	IP_0x8C	RW	0x2	
	5:4	IP_0x88	RW	0x2	
	3:2	IP_0x84	RW	0x2	
	1:0	IP_0x80	RW	0x2	
0x006C	31:30	IP_0xFC	RW	0x3	Priority mapping value of IPv4 TOS or IPv6 TC field Bits [7:2] map queue priority, but bits [1:0] are ignored. If TOS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	IP_0xF8	RW	0x3	
	27:26	IP_0xF4	RW	0x3	
	25:24	IP_0xF0	RW	0x3	
	23:22	IP_0xEC	RW	0x3	
	21:20	IP_0xE8	RW	0x3	
	19:18	IP_0xE4	RW	0x3	
	17:16	IP_0xE0	RW	0x3	
	15:14	IP_0xDC	RW	0x3	
	13:12	IP_0xD8	RW	0x3	
	11:10	IP_0xD4	RW	0x3	
	9:8	IP_0xD0	RW	0x3	
	7:6	IP_0xCC	RW	0x3	
	5:4	IP_0xC8	RW	0x3	
	3:2	IP_0xC4	RW	0x3	
	1:0	IP_0xC0	RW	0x3	

7.23.20 Tag Priority Mapping

Address Offset: 0x0070
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read
15:14	TAG_0X07	RW	0x3	Priority mapping value of TAG. If pri[2:0] in the tag is equal to 0x07, the queue priority should be mapped to value of these bits.
13:12	TAG_0X06	RW	0x3	
11:10	TAG_0X05	RW	0x2	
9:8	TAG_0X04	RW	0x2	
7:6	TAG_0X03	RW	0x1	
5:4	TAG_0X02	RW	0x1	
3:2	TAG_0X01	RW	0x0	
1:0	TAG_0X00	RW	0x0	

7.23.21 Service Tag

Address Offset: 0x0074
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read
15:0	SERVICE_TAG	RW	0x88A8	Service tag. These bits are used to recognize double tagged packets at ingress and inserts double tags on egress.

7.23.22 CPU Port

Address Offset: 0x0078
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read	
8	CPU_PORT_EN	RW	0x0	Used to enable the CPU port	
				0	No CPU is connected to switch
				1	CPU is connected to port0
7:4	MIRROR_PORT_NUM	RW	0xF	Port number which packet should be mirrored to. 0 is port0, 1 is port1,etc. If the value is more than 4, no mirror port is connected to the switch	
3:0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read	

7.23.23 LPI

Address Offset: 0x007C

Access: Read/Write

Reset: See field description

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved
15:0	SLEEP_TIMER	0x100	The timer controls the length of time the OQ is empty before the PHY enters the LPI state

7.23.24 MIB Function 0

Address Offset: 0x0080

Access: Read/Write

Reset: See field Description

Bit	Bit Name	Type	Reset	Description	
31	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read	
30	MIB_EN	RW	0x0	Set to 1 to enable the MIB count If this bit set to zero, the MIB module does not count.	
29:27	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read	
26:24	MIB_FUNC	RW	0x0	Used to set the MIB counters	
				000	No operation
				001	Flush all counters for all ports
				010	Reserved
				011	Capture all counters for all ports and auto-cast to CPU port
				1xx	Reserved
23:18	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read	
17	MIB_BUSY	RW	0x0	Configures the MIB setting when busy	
				0	MIB module is busy now, and cannot access another new command
				1	MIB module is empty now, and can access new command
16	MIB_AT_HALF_EN	RW	0x1	MIB auto-cast enable due to half flow. If this bit is set to 1, MIB would be auto-cast when any counter's highest bit count to 1.	
15:0	MIB_TIMER	RW	0x15	MIB auto-cast timer. If these bits are set to zero, MIB will not auto-cast due to timer time out. The timer is set in multiples of 8.4 ms, and the recommended value is 0x100.	

7.23.25 MDIO Control

Address Offset: 0x0098
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Type	Description
31	MDIO_BUSY	RW	Set to 1 if the internal MDIO interface is busy. This bit should be set to 1 when CPU reads or writes PHY register through the internal MDIO interface, and should be cleared after hardware finish the command.
30	MDIO_MASTER_EN	RW	Set to 1 to use the MDIO master to configure the PHY register. MDC should be changed to internal MDC to PHY.
29:28	RES	RO	Reserved. Must be written with zero. Contains zeros when read
27	MDIO_CMD	RW	Denotes the current MDIO command
			0 Write
			1 Read
26	MDIO_SUP_PRE	RW	Set to 1 to enable suppose preamble
25:21	PHY_ADDR	RW	PHY address
20:16	REG_ADDR	RW	PHY register address
15:0	MDIO_DATA	RW	When write, these bits are data written to the PHY register. When read, these bits are data read out from the PHY register.

7.23.26 LED Control

Address Offset: 0x00B0, 0x00B4, 0x00B8, 0x00BC
Access: Read/Write
Reset: See field description
This register can be reset by hardware only.

Offset	Bit	Bit Name	Type	Reset	Description
0x00B0	31:16	LED_CTRL_RULE_1	RW	0XC935	WAN port LED_LINK1000n_4 control rule
	15:0	LED_CTRL_RULE_0	RW	0xC935	LAN port LED_LINK1000n_[3:0] control rule
0x00B4	31:16	LED_CTRL_RULE_3	RW	0xCA35	WAN port LED_LINK100n_4 control rule
	15:0	LED_CTRL_RULE_2	RW	0xCA35	LAN port LED_LINK100n_[3:0] control rule
0x00B8	31:16	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read
	15:0	MAC_LED_CTRL_RULE	RW	0xCF35	MAC LED control rule [15:14] only control pattern enable for port0, other LAN ports controlled by MAC_LED_PATTERN_EN_**.

Offset	Bit	Bit Name	Type	Reset	Description	
0x00BC	31:26	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
	25:24	LED_PATTERN_EN_31	RW	0x3	Pattern enable for port3 LED1	
	23:22	LED_PATTERN_EN_30	RW	0x3	Pattern enable for port3 LED0	
	21:20	LED_PATTERN_EN_21	RW	0x3	Pattern enable for port2 LED0	
	19:18	LED_PATTERN_EN_20	RW	0x3	Pattern enable for port2 LED0	
	17:16	LED_PATTERN_EN_11	RW	0x3	Pattern enable for port1 LED1	
	15:14	LED_PATTERN_EN_10	RW	0x3	Pattern enable for port1 LED0	
	13:12	MAC_LED_PATTERN_EN_6	RW	0x3	LED control pattern for MAC6	
	11:10	MAC_LED_PATTERN_EN_5	RW	0x3	LED control pattern for MAC5	
	9:2	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
	1:0	BLINK_HIGH_TIME	RW	0xCF35	When the LED is blinking, these bits determine the LED light time	
					00	50% of blinking period. 250 ms for 2 Hz, 125 ms for 4 Hz, 62.5 ms for 8 Hz
					01	12.5%
					10	25%
					11	75%

7.24 Port Control Registers

Table 7-27 summarizes the port control registers.

Table 7-27 Port Control Registers Summary

Port 0 (0x0100–0x01FC)	Port 1 (0x0200–0x02FC)	Port 2 (0x0300–0x03FC)	Port 3 (0x0400–0x04FC)	Port 4 (0x0500–0x05FC)	Port 5 (0x0600–0x06FC)	Name	Page
0x0100	0x0200	0x0300	0x0400	0x0500	0x0600	Port Status	page 321
0x0104	0x0204	0x0304	0x0404	0x0504	0x0604	Port Control	page 322
0x0108	0x0208	0x0308	0x0408	0x0508	0x0608	Port-Based VLAN	page 324
0x010C	0x020C	0x030C	0x040C	0x050C	0x060C	Port-Based VLAN 2	page 325
0x0110	0x0210	0x0310	0x0410	0x0510	0x0610	Rate Limit	page 326
0x0114	0x0214	0x0314	0x0414	0x0514	0x0614	Priority Control	page 327
0x0118	0x0218	0x0318	0x0418	0x0518	0x0618	Storm Control	page 327
0x011C	0x021C	0x031C	0x041C	0x051C	0x061C	Queue Control	page 328
0x0120	0x0220	0x0320	0x0420	0x0520	0x0620	Rate Limit 1	page 329
0x0124	0x0224	0x0324	0x0424	0x0524	0x0624	Rate Limit 2	page 330
0x0128	0x0228	0x0328	0x0428	0x0528	0x0628	Rate Limit 3	page 330
0x012C	0x022C	0x032C	0x042C	0x052C	0x062C	Robin	page 331
0x0130	0x0230	0x0330	0x0430	0x0530	0x0630	LPI Control	page 331

7.24.1 Port Status

Address Offset:
Port 0**:** 0x0100, ***Port 1***: 0x0200 ***Port 2***: 0x0300, ***Port 3***: 0x0400, ***Port 4***: 0x0500, ***Port 5:*** 0x0600
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
12	FLOW_LINK_EN	RW	0x1	PHY link mode enable.	
				0	Enable MAC flow control. Configures auto-negotiation with the PHY.
				1	MAC can be configured by software
11	LINK_ASYN_PAUSE_ EN	RO	0x0	Link partner support ASYN flow control	
10	LINK_PAUSE_EN	RO	0x0	Link partner support flow control	
9	LINK_EN	RW	0x1	PHY link mode enable	
				0	Software can configure the MAC
				1	Enable PHY link status to configure the MAC

Bit	Bit Name	Type	Reset	Description
8	LINK	RO	0x0	Link status
				0 PHY link down
				1 PHY link up
7	TX_HALF_ FLOW_EN	RW	0x1	Set to 1 to enable flow control, transmitting in half-duplex mode
6	DUPLEX_ MODE	RW	0x0	Duplex mode
				0 Half-duplex mode
				1 Full-duplex mode
5	RX_FLOW_ EN	RW	0x0	Enables RXMAC Flow Control
4	TX_FLOW_EN	RW	0x0	Enables TXMAC Flow Control
3	RXMAC_EN	RW	0x0	RXMAC enable
2	TXMAC_EN	RW	0x0	TXMAC enable
1:0	SPEED	RW	0x0	Speed mode
				00 10 Mbps
				01 100 Mbps
				10 1000 Mbps
				11 Error speed mode

7.24.2 Port Control

Address Offset:
Port 0**:** 0x0104, ***Port 1***: 0x0204 ***Port 2***: 0x0304, ***Port 3***: 0x0404, ***Port 4***: 0x0504, ***Port 5:*** 0x0604
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:24	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
23	EAPOL_EN	RW	0x0	Set to 1 so hardware acknowledges 802.1x frames, and sends a frame copy, or redirects to CPU controlled by EAPAL_REDIRECT_EN
22	ARP_LEAKY_EN	RW	0x0	Sets the VLAN rule for ARP frames entering VLANs
				0 ARP frame cannot cross VLANs
				1 If the MAC receives an ARP frame from this port, it can cross all VLANs (including port base VLAN and 802.1q)
21	IGMP_LEAVE_EN	RW	0x0	Set to 1 to enable IGMP/MLD fast leave
20	IGMP_JOIN_EN	RW	0x0	Set to 1 to enable MLD hardware join
19	DHCP_EN	RW	0x0	Set to 1 to enable acknowledgement of DHCP frames
18	IPG_DEC_EN	RW	0x0	Set to 1 mac will decrease two bytes of IPG when sending out frames and receiving checks.
17	ING_MIRROR_EN	RW	0x0	Ingress port mirror. If this bit is set to 1, all packets received from this port will be copied to the mirror port.

Bit	Bit Name	Type	Reset	Description
16	EG_MIRROR_EN	RW	0x0	Egress port mirror. If this bit is set to 1, all packets send out through this port should be copied to the mirror port.
15	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.
14	LEARN_EN	RW	0x1	Enable learn operation. Set to 1 to enable the lookup module to learn new address in the address table.
13	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.
12	MAC_LOOP_ BACK	RW	0x0	Set to 1 to enable MAC loop back at MII interface
11	HEAD_EN	RW	0x0	Enables frames transmitted out and received to add the Qualcomm Atheros header. If this bit is set to 1, all frames transmitted and received will add 2 bytes of the Qualcomm Atheros header.
10	IGMP_MLD_EN	RW	0x0	IGMP/MLD snooping enable. If this bit is set to 1'b1, the port will examine all received frames and copy or redirect to CPU port controlled by IGMP_COPY_EN.
9:8	EG_VLAN_MODE	RW	0x0	Egress VLAN mode. 00 Egress transmits frames unmodified. 01 Egress transmits frames without VLAN 10 Egress transmits frames with VLAN
7	LEARN_ONE_ LOCK	RW	0x0	Used to configure the learning mode for source addresses 0 Normal learning mode 1 This port should not learn the source address, except the first packet, and locked the address to static.
6	PORT_LOCK_EN	RW	0x0	Set to 1 to enable port lock. All packets received with a source address not in the ARL table or the source address is in the ARL table but no port members are the source port will redirect packets to the CPU or be dropped. Controlled by LOCK_DROP_EN.
5	LOCK_DROP_EN	RW	0x0	Used to configure the port lock 0 If the source address is not in the ARL table or the source address is in the ARL but no port member is the source port, the packet should be redirected to the CPU when PORT_LOCK_EN is set to 1. 1 If the source address is not in the ARL table or the source address is in the ARL but no port member is the source port, the packet will be dropped when PORT_LOCK_EN is set to 1.
4:3	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

Bit	Bit Name	Type	Reset	Description	
2:0	PORT_STATE	RW	0x4	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree.	
				000	Disable mode. The port is completely disabled, and cannot receive or transmit any frames.
				001	Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames cannot be transmitted or received by the port, and without learning any source address.
				010	Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any source address. Any other frames cannot be transmitted or received by the port.
				011	Learning Mode. In this state, the port will learning all source addresses, and discard all frames except management frames, and only management frames are allowed to be transmitted out.
				100	Forward Mode. In this state, the port will learning all source addresses, transmit and receive all frames as normal.

7.24.3 Port-Based VLAN

Address Offset:
Port 0**:** 0x0108, ***Port 1***: 0x0208 ***Port 2***: 0x0308, ***Port 3***: 0x0408, ***Port 4***: 0x0508, ***Port 5:*** 0x0608
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:29	ING_PORT_PRI	RW	0x0	Port default priority for received frames.	
28	FORCE_PORT_ VLAN_EN	RW	0x0	Set to 1 to force enable using port-base VLANs. If this bit is set to 1, use port-base VLANs and use this table to determine the destination port.	
27:16	PORT_DEFAULT_ CVID	RW	0x1	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.	
15	PORT_CLONE_EN	RW	0x0	Used to set the port cloning mechanism	
				0	Enable port replace
				1	Enable port cloning
14	PORT_VLAN_ PROP_EN	RW	0x0	Set to 1 to enable the port-base VLAN propagation function.	
13	PORT_TLS_MODE	RW	0x0	Used to set the port TLS mode	
				0	Port works in TLS mode
				1	Port works in NON-TLS mode

Bit	Bit Name	Type	Reset	Description
12	FORCE_ DEFAULT_VID_EN	RW	0x0	Used to set the default VID for received frames
				0 Use frame tags only
				1 Force using port default VID and priority for received frames, when 802.1Q mode is not disabled.
11:0	PORT_DEFAULT_ SVID	RW	0x1	Port Default VID. This field is used to add Tagged VIDs to untagged frames when received from this port.

7.24.4 Port-Based VLAN 2

Address Offset:
Port 0**:** 0x010C, ***Port 1***: 0x020C ***Port 2***: 0x030C, ***Port 3***: 0x040C, ***Port 4***: 0x050C, ***Port 5:*** 0x060C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:30	802.1Q_MODE	0x0	Used to set the 802.1Q mode for this port
			00 802.1Q disable. Use port base VLAN only.
			01 Fallback. Enable 802.1Q for all received frames. Do not discard ingress membership violations and use the port base VLAN if the frame's VID is not contained in the VLAN Table.
			10 Check. Enable 802.1Q for all received frames. Do not discard ingress membership violations but discard frames when the VID is not contained in the VLAN Table.
			11 Secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violations or whose VID is not contained in the VLAN Table.
29	CORE_PORT_ EN	0x0	Used to enable core ports
			0 Edge port
			1 Core port
28:27	ING_VLAN_ MODE	0x0	Use to configure types of packets that can be received in the VLAN
			00 All frames can be received, including untagged and tagged
			01 Only frames with tags can be received by this port
			10 Only untagged frames can be received by this port, including no VLAN and priority VLAN.
			11 Reserved
26:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23	VLAN_PRI_ PRO_EN	0x0	Set to 1 to enable VLAN priority propagation
22:16	PORT_VID_ MEM	Port0: 111110 Port1: 111101 ……	Port base VLAN member. Each bit restricts to which port frames can be sent. To send frames to port0, bit 16 must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they were received in.
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

Bit	Bit Name	Reset	Description	
14	UNI_LEAKY_EN	0x0	Enable unicast frame leaky VLANs Also use this bit and LEAKY_EN bit in the ARL table to control unicast leaky VLAN. If the MAC receives unicast frames from this port, which should forward packets as a leaky VLAN, the frame could be switched to the destination port defined in ARL table and cross all VLANs (including port base and 802.1q).	
			0	Only UNI_LEAKE_EN controls unicast frame leaky VLANs
			1	Only frames with a destination address (DA) in the ARL table with the LEAKY_EN bit is set to 1 can be forwarded as leaky VLAN. Ignore UNI_ LEAKY_EN.
13	MULTI_LEAKY_ EN	0x0	Enables multicast frame leaky VLAN. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in the ARL table to control unicast leaky VLAN. If the MAC receives multicast frames from this port which should forward as leaky VLAN, the frame could be switched to a destination port defined in the ARL table, and cross all VLANs (include port-base VLANs and 802.1q).	
			0	Only MULTI_LEAKE_EN controls multicast frame leaky VLANs
			1	Only frames with the destination address (DA) in the ARL table with LEAKY_ EN bit set to 1, can be forwarded as leaky VLANs. Ignore MULTI_LEAKE_ EN.
12:0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	

7.24.5 Rate Limit

Address Offset:
Port 0**:** 0x0110, ***Port 1***: 0x0210 ***Port 2***: 0x0310, ***Port 3***: 0x0410, ***Port 4***: 0x0510, ***Port 5:*** 0x0610
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:24	ADD_RATE_BYTE	RW	0x18	Byte number should be added to a frame when calculating the rate limit. The default is 24 bytes for IPG, preamble, CRC and SFD.
23	EGRESS_RATE_EN	RW	0x0	Enable port-base rate limit. Rate should be set at EG_PRI3_ RATE.Enables port-based rate limit. EG_PRI3_RATE is duplicated for port-based and queue-based) Also enables port-based max burst size. Max burst size should be set at max_burst_size_pri3. (Enables port-based max burst size. MAX_BURST_SIZE_PRI3 is duplicated for port based and queue based
22	EGRESS_MANAGE_ RATE_EN	RW	0x0	Enables management frames to be calculated to the egress rate limit
21	INGRESS_ MANAGE_RATE_EN	RW	0x0	Enables management frames to be calculated to the ingress rate limit
20	INGRESS_MULTI_ RATE_EN	RW	0x0	Enables calculating the ingress rate limit of multicast frames in which the destination address (DA) can be found in ARL table
19:15	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:0	ING_RATE	RW	0x7FFF	Ingress Rate Limit for all priorities. The rate is limited to configurations of steps of 32 Kbps. Default 15'h7FFF is used to disable rate limit for egress priority 2. If these bits are set to 15'h0, no frame should be received from this port.

7.24.6 Priority Control

Address Offset:
Port 0**:** 0x0114, ***Port 1***: 0x0214 ***Port 2***: 0x0314, ***Port 3***: 0x0414, ***Port 4***: 0x0514, ***Port 5:*** 0x0614
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	PORT_PRI_ EN	0x1	Set to 1 so port base priority can be used for QOS.
18	DA_PRI_EN	0x0	Set to 1 so DA priority can be used for QOS.
17	VLAN_PRI_EN	0x0	Set to 1 so VLAN priority can be used for QOS.
16	IP_PRI_EN	0x0	Set to 1 for TOS/TC to be used for QOS.
15:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:6	DA_PRI_SEL	0x0	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority is set to n-1.
5:4	VLAN_PRI_SEL	0x1	VLAN priority selected level for QOS.
3:2	IP_PRI_SEL	0x2	IP priority selected level for QOS.
1:0	PORT_PRI_SEL	0x3	Port-base priority selected level for QOS

7.24.7 Storm Control

Address Offset:
Port 0**:** 0x0118, ***Port 1***: 0x0218 ***Port 2***: 0x0318, ***Port 3***: 0x0418, ***Port 4***: 0x0518, ***Port 5:*** 0x0618
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10	MULTI_STORM_EN	Set to 1 to enable unknown multicast frames to be calculated towards storm control	
9	UNI_STORM_EN	Set to 1 to enable unknown unicast frame to be calculated towards storm control	
8	BROAD_STORM_EN	Set to 1 to enable broadcast frames to be calculated towards storm control	
7:4	RES	Reserved. Must be written with zero. Contains zeros when read.	
3:0	STORM_RATE	Storm control rate	
		0x0	Storm control disable
		0x1	1K frames per second
		0x2	2K frame per second
		0x3	4K frame per second
		0x4	8K frame per second
		0x5	16K frame per second
		0x6	32K frame per second
		0x7	64K frame per second
		...	...
		0xB	1M frame per second

7.24.8 Queue Control

Address Offset:
Port 0**:** 0x011C, ***Port 1***: 0x021C, ***Port 2***: 0x031C, ***Port 3***: 0x041C, ***Port 4***: 0x051C, ***Port 5:*** 0x061C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31:28	ING_BUF_NUM	RW	Port 0: 0x6 Other Ports: 0x2	Buffer number is times of 4	
				0x0	0
				0x1	No more than 4
				0x2	No more than 8
				...	...
				0xF	No more than 60
27:26	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
25	PORT_QUEUE_CTRL_EN	RW	0x1	Set to 1 to enable using PORT_QUEUE_NUM to control queue depth in this port.	
24	PRI_QUEUE_CTRL_EN	RW	0x1	Set to 1 to enable using PRI*_QUEUE_NUM to control queue depth in this port.	
23:22	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
21:16	PORT_QUEUE_NUM	RW	0x2A	Most buffers can be used for this port. Buffer number is set in multiples of 4.	
				0x0	0
				0x1	No more than 4
				0x2	No more than 8
				...	...
				0x1F	No more than 252
15:12	PRI3_QUEUE_NUM	RW	0x8	Most buffer can be used for priority 3 queue. Buffer number is set in multiples of 4.	
				0x0	0
				0x1	No more than 4
				0x2	No more than 8
				...	...
				0xF	No more than 60
11:8	PRI2_QUEUE_NUM	RW	0x8	Most buffer can be used for priority 2 queue. Buffer number is set in multiples of 4.	
				0x0	0
				0x1	No more than 4
				0x2	No more than 8
				...	...
				0xF	No more than 60

Bit	Bit Name	Type	Reset	Description	
7:4	PRI1_QUEUE_NUM	RW	0x8	Most buffer can be used for priority 1 queue. Buffer number is set in multiples of 4.	
				0x0	0
				0x1	No more than 4
				0x2	No more than 8
				...	...
				0xF	No more than 60
3:0	PRI0_QUEUE_NUM	RW	0x8	Most buffer can be used for priority 0 queue. Buffer number is set in multiples of 4.	
				0x0	0
				0x1	No more than 4
				0x2	No more than 8
				...	...
				0xF	No more than 60

7.24.9 Rate Limit 1

Address Offset:
Port 0**:** 0x0120, ***Port 1***: 0x0220, ***Port 2***: 0x0320, ***Port 3***: 0x0420, ***Port 4***: 0x0520, ***Port 5:*** 0x0620
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:16	EG_PRI1_RATE	RW	0x7FFF	Egress Rate Limit for priority 1. Rate is limited to multiples of 32 Kbps. Default 0x7FFF is for disable rate limit for egress priority 2. If these bits are set to 0x0, no priority 1 frame should be send out from this port.
15	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:0	EG_PRI0_RATE	RW	0x7FFF	Egress Rate Limit for priority 0. Rate is limited to multiples of 32 Kbps. Default 0x7FFF is for disable rate limit for egress priority 2. If these bits are set to 0x0, no priority 0 frame should be send out from this port.

7.24.10 Rate Limit 2

Address Offset:
Port 0**:** 0x0124, ***Port 1***: 0x0224, ***Port 2***: 0x0324, ***Port 3***: 0x0424, ***Port 4***: 0x0524, ***Port 5:*** 0x0624
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:16	EG_PRI3_ RATE	RW	0x7FFF	Egress Rate Limit for priority 3. Rate is limited to times of 32 Kbps. Default 0x7FFF is for disable rate limit for egress priority 2. If these bits are set to 0x0, no priority 3 frame should be send out from this port.
15	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:0	EG_PRI2_ RATE	RW	0x7FFF	Egress Rate Limit for priority 2. Rate is limited to times of 32 kbps. Default 0x7FFF is for disable rate limit for egress priority 2. If these bits are set to 0x0, no priority 2 frame should be send out from this port.

7.24.11 Rate Limit 3

Address Offset:
Port 0**:** 0x0128, ***Port 1***: 0x0228, ***Port 2***: 0x0328, ***Port 3***: 0x0428, ***Port 4***: 0x0528, ***Port 5:*** 0x0628
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Type	Description	
31:3	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
2:0	EG _TIME_ SLOT	RW	Egress rate limit time slot control register	
			0x0	1/128 ms
			0x1	1/64 ms
			0x2	1/32 ms
			0x3	1/16 ms
			0x4	1/4 ms
			0x5	1 ms
			0x6	10 ms
			0x7	100 ms

7.24.12 Robin

Address Offset:
Port 0**:** 0x012C, ***Port 1***: 0x022C, ***Port 2***: 0x032C, ***Port 3***: 0x042C, ***Port 4***: 0x052C, ***Port 5:*** 0x062C
Access: Read/Write

Reset: See field description

Bit	Bit Name	Type	Reset	Description	
31	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
30:29	WEIGHT_PRI_CTRL	RW	0x0	Used to set the queue weight priority	
				00	Strict priority
				01	Only the highest queue uses strict priority, others use weighted-fair queuing scheme
				10	The highest two queues use strict priority, other two queues use weighted-fair queuing scheme.
				11	All queues use weighted-fair queuing scheme which is defined by WRR_PRI3/2/1/0.
28:24	WRR_PRI3	RW	0x8	Weighted round-robin (WRR) setting for priority 3	
23:21	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
20:16	WRR_PRI2	RW	0x4	WRR setting for priority 2	
15:13	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
12:8	WRR_PRI1	RW	0x2	WRR setting for priority 1	
7:5	RES	RW	0x0	Reserved. Must be written with zero. Contains zeros when read.	
4:0	WRR_PRI0	RW	0x1	WRR setting for priority 0	

7.24.13 LPI Control

Address Offset:
Port 0**:** 0x0130, ***Port 1***: 0x0230, ***Port 2***: 0x0330, ***Port 3***: 0x0430, ***Port 4***: 0x0530, ***Port 5:*** 0x0630
Access: Read/Write

Reset: See field description

Bit	Bit Name	Reset	Description	
31	LPI_EN	0x0	0	Disable the switch to give out LPI control
			1	Enable the switch to give out LPI control to send the PHY into LPI state
30:16	RES	0x0	Reserved	
15:0	WAKEUP_TIMER	0x20	Set the timer to control how long the PHY requires to wakeup from LPI state	

7.25 PHY Control Registers

Table 7-26 summarizes the PHY Control registers.

Table 7-28 PHY Register Summary

Offset	Description	Page
0x0	Control	page 332
0x1	Status	page 334
0x2	PHY Identifier	page 335
0x3	PHY Identifier 2	page 335
0x4	Auto-Negotiation Advertisement	page 335
0x5	Link Partner Ability	page 337
0x6	Auto-Negotiation Expansion	page 338
0x0D	MMD Access Control	page 338
0x0E	MMD Access Address Data	page 338
0x10	Function Control	page 339
0x11	PHY-Specific Status	page 340
0x12	Interrupt Enable	page 341
0x13	Interrupt Status	page 342
0x15	Receive Error Counter	page 343
0x16	Virtual Cable Tester Control	page 343
0x1C	Virtual Cable Tester Status	page 344
0x1D	Debug Port 1 (Address Offset)	page 344
0x1E	Debug Port 2 (Data Port)	page 344

7.25.1 Control

Address Offset: 0x00
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description	
15	RESET	RW/SC	PHY Software Reset. Writing a 1 to this bit causes the PHY the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately.	
			0	Normal operation
			1	PHY reset
14	LOOPBACK	RW	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled.	
			0	Disable Loopback
			1	Enable Loopback

Bit	Bit Name	Access	Description	
13	SPEED_ SELECTION	RW	Used to select the speed mode	
			00	10 Mbps
			01	100 Mbps
			11:10	Reserved
12	AUTO_ NEGOTIATION	RW	Enables/disables the auto-negotiation process	
			0	Disable Auto-Negotiation Process
			1	Enable Auto-Negotiation Process
11	POWER_DOWN	RW	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user.	
			0	Normal operation
			1	Power down
10	ISOLATE	RW	The MII output pins are tri-stated when this bit is set to 1. The MII inputs are ignored.	
			0	Normal operation
			1	Isolate
9	RESTART_ AUTO_ NEGOTIATION	RW/SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.	
			0	Normal operation
			1	Restart Auto-Negotiation Process
8	DUPLEX_MODE	RW/SC	Selects the flow control mode	
			0	Half Duplex
			1	Full Duplex
7	COLLISION_ TEST	RW	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted.	
			0	Disable COL signal test
			1	Enable COL signal test
6	SPEED_ SELECTION (MSB)	RW	Used to select the speed mode	
			00	10 Mbps
			01	100 Mbps
5:0	RES	RO	11:10	Reserved

7.25.2 Status

Address Offset: 0x01
Access: See field description
Reset: See field description

Bit	Bit Name	Access	Reset	Description
15	100BASE_T4	RO	0x0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X_FULL-DUPLEX	RO	0x1	Capable of 100-Tx full duplex operation
13	100BASE-X_HALF-DUPLEX	RO	0x1	Capable of 100-Tx half duplex operation
12	10MBPS_FULL-DUPLEX	RO	0x1	Capable of 10BASE-T full duplex operation
11	10_MBPS_HALF-DUPLEX	RO	0x1	Capable of 10BASE-T half duplex operation
10	100BASE_T2 _FULL_DUPLEX	RO	0x0	Not able to perform 100BASE-T2
9	100BASE-T2_HALF_ DUPLEX	RO	0x0	Not able to perform 100BASE-T2
8:7	RES	RO	0x1	Reserved
6	MF_PREAMBLE_ SUPPRESSION	RO	0x1	PHY accepts management frames with preamble suppressed
5	AUTO-NEGOTIATION_ COMPLETE	RO	0x0	Denotes the current status of the auto-negotiation process
				0 Auto-negotiation process not complete
				1 Auto-negotiation process complete
4	REMOTE_FAULT	RO/ LH	0x0	Denotes if a fault was detected
				0 Remote fault condition not detected
				1 Remote fault condition detected
3	AUTO-NEGOTIATION_ ABILITY	RO	0x1	Denotes the ability of the PHY to perform auto-negotiation
				0 PHY unable to perform auto-negotiation
				1 PHY able to perform auto-negotiation
2	LINK_STATUS	RO/LL	0x0	This register bit indicates whether the link was lost since the last read. For the current link status, read register bits [17:10] of link real time.
1	JABBER_DETECT	RO/ LH	0x0	Denotes if a Jabber condition was detected
0	EXTENDED_ CAPABILITY	RO	0x1	Denotes the availability of the register capabilities

7.25.3 PHY Identifier

Address Offset: 0x02
Access: Read-Only
Reset: 0x004D

Bit	Bit Name	Description
15:0	Organizationally Unique Identifier Bit 3:18	Organizationally Unique Identifier bits [18:3]

7.25.4 PHY Identifier 2

Address Offset: 0x03
Access: Read-Only
Reset: 0xD041

Bit	Bit Name	Description
15	OUI LSB Model Number Revision Number	Organizationally Unique Identifier bits [24:19]

7.25.5 Auto-Negotiation Advertisement

Address Offset: 0x04
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Reset	Description
15	RES	RW	0x0	Always 0
14	ACK	RO	0x0	Must be 0
13	REMOTE_ FAULT	RW	0x0	Used to set the remote fault bit
12	RES	RO	0x0	Always 0
11	ASYMMETRIC_ PAUSE	RW	0x1	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (bit [15]) ■ Restart auto-negotiation is asserted (bit [9]) ■ Power down (register bit [11]) transitions from power down to normal operation ■ Link goes down
10	PAUSE	RW	0x1	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (bit [15]) ■ Restart Auto-Negotiation is asserted (bit [9]) ■ Power down (register bit [11]) transitions from power down to normal operation ■ Link goes down
9	100BASE-T4	RO	0x0	Not able to perform 100BASE-T4

Bit	Bit Name	Access	Reset	Description
8	100BASE-TX	RW	0x1	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (bit [15]) ■ Restart Auto-Negotiation is asserted (bit [9]) ■ Power down (register bit [11]) transitions from power down to normal operation ■ Link goes down
7	100BASE_TX _HALF _DUPLEX	RW	0x1	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (bit [15]) ■ Restart Auto-Negotiation is asserted (bit [9]) ■ Power down (register bit [11]) transitions from power down to normal operation ■ Link goes down
6	10BASE_ TX_FULL _DUPLEX	RW	0x1	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (bit [15]) ■ Restart Auto-Negotiation is asserted (bit [9]) ■ Power down (register bit [11]) transitions from power down to normal operation ■ Link goes down
5	10BASE _TX_HALF_ DUPLEX	RW	0x1	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: ■ Software reset is asserted (bit [15]) ■ Restart Auto-Negotiation is asserted (bit [9]) ■ Power down (register bit [11]) transitions from power down to normal operation ■ Link goes down
4:0	SELECTOR_ FIELD	RO	0x00001	Selector field mode: 00001 = 802.3

7.25.6 Link Partner Ability

Address Offset: 0x05
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description	
15	RES	Always 0	
14	ACK	Acknowledge Received code word bit [14]	
		0	Link partner does not have Next Page ability
		1	Link partner received link code word
13	REMOTE_ FAULT	Remote fault Received code word bit [13]	
		0	Link partner has not detected remote fault
		1	Link partner detected remote fault
12	TECHNOLOGY_ ABILITY	Technology ability field Received code word bit [12]	
11	ASYMMETRIC_ PAUSE	Technology ability field Received code word bit [11]	
		0	Link partner does not request asymmetric pause
		1	Link partner requests asymmetric pause
10	PAUSE	Technology ability field Received code word bit [10]	
		0	Link partner is not capable of pause operation
		1	Link partner is capable of pause operation
9	100BASE_T4	Technology ability field Received code word bit [9]	
		0	Link partner is not 100BASE-T4 capable
		1	Link partner is 100BASE-T4 capable
8	100BASE _TX_FULL _DUPLEX	Technology ability field Received code word bit [8]	
		0	Link partner is not 100BASE-TX full-duplex capable
		1	Link partner is 100BASE-TX full-duplex capable
7	100BASE_TX _HALF _DUPLEX	Technology ability field Received code word bit [7]	
		0	Link partner is not 100BASE-TX half-duplex capable
		1	Link partner is 100BASE-TX half-duplex capable
6	10BASE_TX _FULL _DUPLEX	Technology ability field Received code word bit [6]	
		0	Link partner is not 10BASE-T full-duplex capable
		1	Link partner is 10BASE-T full-duplex capable
5	10BASE_TX _HALF _DUPLEX	Technology ability field Received code word bit [5]	
		0	Link partner is not 10BASE-T half-duplex capable
		1	Link partner is 10BASE-T half-duplex capable
4:0	SELECTOR_ FIELD	Selector field Received code word bit [4:0]	

7.25.7 Auto-negotiation Expansion

Address Offset: 0x06
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description	
15:5	RES	RO	Reserved. Must be 0.	
4	PARALLEL_ DETECTION_ FAULT	RO/LH	Used to denote the parallel detection fault	
			0	No fault has been detected
			1	A fault has been detect
3:1	RES	RO	Always 0	
0	LINK_PARTNER_ AUTO-NEGOTIATION_ ABLE	RO	Used to denote the auto negational capability of the link partner	
			0	Link partner is not auto negotiation capable
			1	Link partner is auto negotiation capable

7.25.8 MMD Access Control

Address Offset: 0x0D
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description	
15:14	FUNCTION	R/W	00	Address
			01	No post increment
			10	Post increment on reads and writes
			11	Post increment on writes only
13:5	RES	RO	Reserved	
4:0	DEVAD	R/W	Device address	

7.25.9 MMD Access Address Data

Address Offset: 0x0E
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
15:0	ADDRESS_DATA	If set to 00, sets the address to the MMD DEVAD address register. Otherwise, the MMD DEVAD data register as indicated by the contents of its address register.

7.25.10 Function Control

Address Offset: 0x10
Access: See field description
Reset: See field description

Bit	Bit Name	Access	Reset	Description	
15:12	RES	RO	0x0	Always 0	
11	ASSERT_CRS_ ON_TRANSIT	RW	0x0	Always 0	
10:7	RES	RO	0x0	Always 0	
6:5	MDI_ CROSSOVER_ MODE	RW	0x11	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by a software reset to take effect.	
				00	Manual MDI configuration
				01	Manual MDIX configuration
				10	Reserved
				11	Enable automatic crossover for all modes
4:3	RES	RO	0x0	Always 0	
2	SQE_TEST	RW	0x0	SQE test is automatically disabled in full-duplex mode	
				0	SQE test disabled
				1	SQE test enabled
1	POLARITY_ REVERSAL	RW	0x0	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T.	
				0	Polarity Reversal Enabled
				1	Polarity Reversal Disabled
0	DISABLE_ JABBER	RW	0x0	Jabber has effect only in 10BASE-T half-duplex mode.	
				0	Enable jabber function
				1	Disable jabber function

7.25.11 PHY Specific Status

Address Offset: 0x11
Access: Read-Only
Reset: See field descripiton

Bit	Bit Name	Reset	Description	
15:14	SPEED	0x0	These status bits are valid when auto-negotiation is completed or auto-negotiation is disabled.	
			00	10 Mbps
			01	100 Mbps
			10	Reserved
			11	Reserved
13	DUPLEX	0x0	This status bit is valid only if auto-negotiation is completed or auto-negotiation is disabled.	
			0	Half-duplex
			1	Full-duplex
12	PAGE_ RECEIVED (Real Time)	0x0	Denotes if a page was received in real time or not	
			0	Page not received
			1	Page received
11	SPEED_AND_ DUPLEX_ RESOLVED	0x0	When auto-negotiation is not enabled for force speed mode.	
			0	Not resolved
			1	Resolved
10	LINK (Real Time)	0x0	Denotes the link status in real time	
			0	Link down
			1	Link up
9:7	RES	0x0	Always 0	
6	MDI_ CROSSOVER_ STATUS	0x0	This status bit is valid only when auto-negotiation is completed or auto-negotiation is disabled.	
			0	MDI
			1	MDIX
5	WIRESPEED_ DOWNGRADE	0x0	Used to denote if a wire speed downgrade was performed	
			0	No Downgrade
			1	Downgrade
4	ENERGY_ DETECT_ STATUS	0x0	Denotes the status of the Energy Detect mechanism	
			0	Active
			1	Sleep
3	TRANSMIT_ PAUSE_ENABLE	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
			0	Transmit pause disabled
			1	Transmit pause enabled
2	RECEIVE_ PAUSE_ENABLE	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
			0	Receive pause disabled
			1	Receive pause enabled

Bit	Bit Name	Reset	Description	
1	POLARITY (Real Time)	0x0	Denotes the status of the polarity in real time	
			0	Normal
			1	Reversed
0	JABBER (Real Time)	0x0	Denotes if the Jabber is present or not	
			0	No jabber
			1	Jabber

7.25.12 Interrupt Enable

Address Offset: 0x12
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
15	AUTO-NEGOTIATION_ ERROR_ INTERRUPT_ ENABLE	Auto negotiation error interrupt	
		0	Interrupt disable
		1	Interrupt enable
14	SPEED_CHANGED _INTERRUPT_ ENABLE	Speed change interrupt	
		0	Interrupt disable
		1	Interrupt enable
13	RES	Reserved	
12	PAGE_RECEIVED_ INTERRUPT_ ENABLE	Page received interrupt	
		0	Interrupt disable
		1	Interrupt enable
11	AUTO-NEGOTIATION_ COMPLETED_ INTERUPT_ ENABLE	Auto negotiation completed interrupt	
		0	Interrupt disable
		1	Interrupt enable
10	LINK_STATUS_ CHANGED_ INTERRUPT_ ENABLE	Link status changed interrupt	
		0	Interrupt disable
		1	Interrupt enable
9:7	RES	Reserved	
6	MDI_CROSSOVER_ CHANGED_ INTERRUPT_ ENABLE	MDI crossover changed interrupt	
		0	Interrupt disable
		1	Interrupt enable
5	WIRESPEED_ DOWNGRADE_ INTERRUPT_ ENABLE	Wirespeed downgrade interrupt	
		0	Interrupt disable
		1	Interrupt enable
4:2	RES	Always 00	
1	POLARITY_ CHANGED_ INTERRUPT_ ENABLE	Polarity changed interrupt	
		0	Interrupt disable
		1	Interrupt enable
0	JABBER__ INTERRUPT_ ENABLE	Jabber interrupt	
		0	Interrupt disable
		1	Interrupt enable

7.25.13 Interrupt Status

Address Offset: 0x13
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description	
15	AUTO_ NEGOTIATION_ ERROR	RO, LH	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed.	
			0	No Auto-Negotiation Error
			1	Auto-Negotiation Error
14	SSPEED_ CHANGED	RO/LH	Denotes if the speed has changed or not	
			0	Speed not changed
			1	Speed changed
13	RES	RO/LH	Reserved	
12	PAGE_ RECEIVED	RO	Denotes if a page was received or not	
			0	Page not received
			1	Page received
11	AUTO _NEGOTIATION _COMPLETED	RO	Denotes the current completion status of the auto-negotiation	
			0	Auto-negotiation not completed
			1	Auto-negotiation completed
10	LINK_STATUS_ CHANGED	RO/LH	Denotes is the link status has changed or not	
			0	Link status not changed
			1	Link status changed
9:7	RES	RO	Reserved	
6	MDI_ CROSSOVER_ CHANGED	RO/LH	Denotes if there was an MDI Crossover change	
			0	Crossover not changed
			1	Crossover changed
5	WIRESPEED_ DOWNGRADE _INTERRUPT	RO/LH	Wirespeed downgrade detection	
			0	No Wirespeed-downgrade.
			1	Wirespeed-downgrade detected
4:2	RES	RO	Reserved	
1	POLARITY_ CHANGED	RO/LH	Denotes if the polarity changed or not	
			0	Polarity not changed
			1	Polarity Changed
0	JABBER	RO/LH	Denotes if there is a jabber or not	
			0	No jabber
			1	Jabber

7.25.14 Smart Speed

Address Offset: 0x14
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
15:6	RES	0x0	Reserved
5	SMARTSPEED_EN	0x1	If this bit is set to 1, a cable inhibits completion of the training phase, then after a few failed attempts, the PHY automatically downgrades the highest ability to the next lower speed, from 100 to 10. (Default = 1)
4:2	SMARTSPEED _RETRY_LIMIT	0x3	If these bits are set to three, then the PHY attempts five times before downgrading; the number of attempts can be changed through setting these bits. (Default = 3)
1	BYPASS_ SMARTSPEED_TIMER	0x0	If set to one, the Smartspeed FSM bypasses the timer used for stability. (Default = 0)
0	RES	0x0	Reserved. Must be 0.

7.25.15 Receive Error Counter

Address Offset: 0x15
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
15:0	RECEIVE_ ERROR_ COUNT	Counter will peg at 0xFFFF and will not roll over. (When RX_DV is valid, count RX_ER numbers)

7.25.16 Virtual Cable Tester Control

Address Offset: 0x16
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
15:10	RES	Reserved	
9:8	MDI_PAIR_SELECT	Virtual Cable Tester™ Control registers. Use the Virtual Cable Tester Control Registers to select which MDI pair is shown in the Virtual Cable Tester Status register.	
		00	MDI[0] pair
		01	MDI[1] pair
		10	MDI[3] pair
		11	MDI[4] pair
7:1	RES	Always 0	
0	ENABLE_ TEST	When set, hardware automatically disable this bit when VCT is done.	
		0	Disable VCT Test
		1	Enable VCT Test

7.25.17 Virtual Cable Tester Status

Address Offset: 0x1C
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description	
15:10	RES	RO	Reserved.	
9:8	STATUS	RO	The content of the Virtual Cable Tester Status Registers applies to the cable pair selected in the Virtual Cable Tester™ Control Registers.	
			00	Valid test, normal cable (no short or open in cable)
			01	Valid test, short in cable for MDI pair 0/2. Open in cable for MDI pair 1/3
			10	Valid test, open in cable for MDI pair 0/2. Short in cable for MDI pair 1/3
			11	linkup state, no open or short in cable.
7:0	DELTA_ TIME	RW	Delta time to indicate distance. Length = Delta_Time * 0.824	

7.25.18 Debug Port (Address Offset)

Address Offset: 0x1D
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
15:6	RES	Reserved
5:0	ADDRESS_ OFFSET	The address index of the register will be write or read.

7.25.19 Debug Port 2 (RW Port)

Address Offset: 0x1E
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
15:0	DEBUG_DATA_ PORT	The data port of debug register. Before accessing this register, the address offset must be first set.

7.26 Debug Port Registers

Table 7-29 summarizes the debug port registers.

Table 7-29 Debug Port Register Summary

Offset	Description	Page
0x00	Analog Test Control	page 344
0x05	System Mode Control	page 346
0x0B	Hibernate Control	page 346
0x10	100 Base-Tx Test Mode Select	page 347
0x12	10 Base-Tx Test Mode Select	page 347
0x29	Power Saving Control	page 348
0x37	PHY Control	page 348
0x3C	Cable LTH Detect Debug 1	page 348

7.26.1 Analog Test Control

Address Offset: 0x00
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
15	RXCLK_DELAY	Control bit for RGMII interface RX clock delay:	
		0	Enable RGMII Rx clock delay
		1	Disable RGMII Rx clock delay
14:5	RES	Reserved	
4	10_CLASSA	This bit is 10BT Class AB, class A select bit	
		0	10BT in Class AB mode
		1	10BT in Class A mode
3:0	RES	Reserved	

7.26.2 System Mode Control

Address Offset: 0x05
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
15:9	RES	0x0	Reserved3	
8	GTXCLK_ DELAY	RW	RGMII Tx clock delay control bit	
		0	0	Disable RGMII Tx clock delay
		Retain	1	Enable RGMII Tx clock delay
7:2	RES	0x0	Reserved	
1	100_CLASSA	0x1	This bit is 100BT ClassA and ClassAB mode select bit.	
			0	100BT ClassAB
			1	100BT ClassA
0	RES	0x0	Reserved	

7.26.3 Hibernate Control

Address Offset: 0x0B
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
15	PS_HIB_EN	Power hibernate control bit	
		0	Hibernate disable
		1	Hibernate enable
14:0	RES	Reserved	

7.26.4 100 Base-Tx Test Mode Select

Address Offset: 0x10
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
15	TM100_ENA	Enable dig100 loopback test mode	
14:8	RES	Reserved	
7:5	TEST_MODE	100BASE-TX Active Output Interface (AOI) test mode select:	
		000	Normal mode
		001	Duty cycle distortion test; The output waveform consists of the MLT-3 transitions generated by a 01010101… NRZ bit sequence.
		010	Overshoot test; The output waveform consists of 14 bit times of no transition preceded by a transition from zero to either plus or minus V_{out}.
		011	Overshoot test; The output waveform consists of 12 bit times of no transition preceded by a transition from zero to either plus or minus Vout. This is for some special testers.
		100	Jitter test; The output waveform consists of the MLT-3 transitions generated by scrambled HALT line state.
		Others: Reserved	
4:0	RES	Reserved	

7.26.5 10 Base-Tx Test Mode Select

Address Offset: 0x12
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
15:6	RES	Reserved	
5	TEST_MODE	Test_mode[2:0] is for 10BT test mode select:	
		001	Packet with all ones, 10-MHz sine wave; for harmonic test
		010	Pseudo random, for TP_IDLE/jitter/differential voltage test
		011	Normal link pulse only
		100	5-MHz sin wave
4	RES	Reserved	
3	RGMII_MODE	Used to select the RGMII mode	
		0	Select GMII/MII interface with MAC
		1	Select RGMII interface with MAC
2	RES	Reserved	
1:0	TEST_MODE	Test_mode[2:0] is for 10BT test mode select; see bit [5]	

7.26.6 Power Saving Control

Address Offset: 0x29
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
15	TOP_PS_EN	0x1	0	Top-level power saving disable
			1	Top-level power saving enable
14:0	RES	0x36C4	Reserved	

7.26.7 PHY Control

Address Offset: 0x37
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
15	RES	0x1	Reserved	
14:11	RES	0x10	Reserved	
10	RES	0x1	Reserved	
9	BP_CABLE_1TH_DET_PHY	0x0	0	Use cable LTH det function to detect cable length in PHY control state machine
			1	Use vcode to detect cable length in PHY control state machine
8:0	RES	0x0	Reserved	

7.26.8 CABLE_LTH_DETECT_DEBUG1

Address Offset: 0x3C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
15:10	FLP_NECHO_RNG	0x18	For debug purposes
9:5	RES	0x14	Reserved
4:0	FECH_CNT_TH	0x16	For debug purposes

7.27 MMD3 PCS Registers

Table 7-30 summarizes the MMD3 PCS registers.

Table 7-30 MMD3 PCS Register Summary

Offset	Description	Page
0x0	PCS Control 1	page 349
0x1	PCS Status 1	page 349
0x14	EEE Capability	page 350
0x16	EEE Wake Error Counter	page 350

7.27.1 PCS Control 1

Address Offset: 0x0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
15	PCS_RST	Reset bit, self clear	
		1	Reset the registers (not vendor-specific) in MMD3/MMD7
		2	Causes a software reset in the register CONTROL bit[15]
14:0	RES	Reserved; must be set to 0	

7.27.2 PCS Status 1

Address Offset: 0x1
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description
15:12	RES	RO	Reserved; must be set to 0
11	TX_LP_IDLE_RECEIVED	ROC	When read as 1, indicates the transmit PCS has received low power idle signaling one or more times since the register was last read. Latch high.
10	RX_LP_IDLE_RECEIVED	ROC	When read as 1, indicates the receive PCS has received low power idle signaling one or more times since the register was last read. Latch high.
9	TX_LP_IDLE_INDICATION	RO	When read as 1, indicates the transmit PCS is receiving low power idle signals.
8	RX_LP_IDLE_INDICATION	RO	When read as 1, indicates the receive PCS is receiving low power idle signals.
7:0	RES	RO	Reserved; must be set to 0

7.27.3 EEE Capability

Offset: 0x14
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
15:3	RES	Reserved; must be set to 0
2	1000BT_EEE	EEE is not supported for 1000 Base-T
1	100BT_EEE	EEE is supported to 100 Base-T
0	RES	Reserved; must be set to 0

7.27.4 EEE Wake Error Counter

Offset: 0x16
Access: See field description
Reset: 0x0

Bit	Bit Name	Description
15:0	EEE_WAKE_ERROR _COUNTER	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. This counter is clear after read, and hold at all ones in the case of overflow.

7.28 MMD7 Auto-Negotiation Registers

Table 7-30 summarizes the MMD7 auto-negotiation registers.

Table 7-31 MMD7 Auto-Negotiation Register Summary

Offset	Description	Page
0x0	Auto-Negotiation Control	page 351
0x1	Auto-Negotiation Status	page 351
0x3C	EEE Advertisement	page 352
0x3D	EEE LP Advertisement	page 352
0x8000	EEE Ability Auto-Negotiation Result	page 352

7.28.1 Auto-Negotiation

Offset: 0x0
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
15	AN_RST	0x0	Reset bit, self clear.	
			1	Resets the registers (not vendor-specific) in MMD3/MMD7
			2	Cause a software reset in the register CONTROL bit [15]
14	RES	0x0	Reserved; must be set to 0	
13	XNP_CTRL	0x1	If MII register 4 bit [12] is set to 0, setting this bit has no effect.	
			0	Local device will not enable the exchange of extended next page
			1	Local device enables the exchange of extended next page
12:0	RES	0x0	Reserved; must be set to 0	

7.28.2 Auto-Negotiation Status

Offset: 0x1
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description	
15:8	RES	Reserved; must be set to 0	
7	XNP_STATUS	0	Extended next page shall not be used
		1	Both local device and link partner have indicated support for extended next page
6:0	RES	Reserved; must be set to 0	

7.28.3 EEE Advertisement

Offset: 0x3C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
15:2	RES	Reserved; must be set to 0
1	EEE_100BT	If the local device supports EEE operation for 100BT, and EEE operation is desired, this bit will be set to 1
0	RES	Reserved; must be set to 0

7.28.4 EEE LP Advertisement

Offset: 0x3D
Access: Read-Only
Reset: 0x0

Bit	Bit Name		Description
15:3	RES	Reserved; must be set to 0	
2	EEE_1000BT	0	The link partner does not support EEE operation for 1000BT, or EEE operation is not desired
		1	The link partner supports EEE operation for 1000BT, and EEE operation is desired
1	EEE_100BT	0	The link partner does not support EEE operation for 100BT, or EEE operation is not desired
		1	The link partner supports EEE operation for 100BT, and EEE operation is desired
0	RES	Reserved; must be set to 0	

7.28.5 EEE Ability Auto-Negotiation Result

Offset: 0x8000
Access: Read/Write
Reset: 0x0

Bit	Bit Name		Description
15:3	RES	Reserved; must be set to 0	
2	EEE_1000BT_EN	0	1000BT auto-negotiation disable; neither side supports EEE operation for 1000BT, or EEE operation is not desired
		1	1000BT auto-negotiation enable; both sides support EEE operation for 1000BT, and EEE operation is desired
1	EEE_100BT_EN	0	100BT auto-negotiation disable; neither side supports EEE operation for 100BT, or EEE operation is not desired
		1	100BT auto-negotiation enable; both sides support EEE operation for 100BT, and EEE operation is desired
0	RES	Reserved; must be set to 0	

8 Ethernet Subsystem

8.1 GMAC0 and GMAC1

The two QCA9531 GB Ethernet MACs connect to the switch.

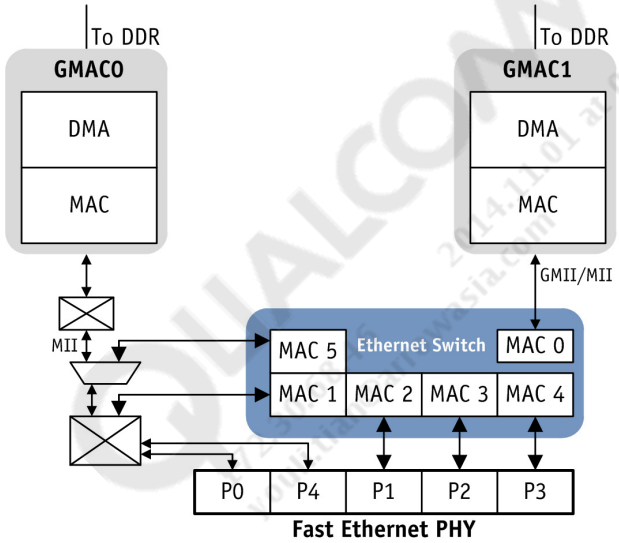


Figure 8-1 Ethernet Subsystem

GMAC1 connects to the internal Ethernet switch through a GMII/MII interface. GMAC0 connectivity can be configured multiple ways:

- GMAC0 could connect to P0 or P4 FE PHY port and GMAC1 connects to the Ethernet switch that controls rest of the 4 FE ports.
- If SW_ONLY_MODE is set, GMAC0 does not connect anywhere. All five PHY ports connect to the Ethernet switch.

8.2 Ethernet Switch

The QCA9531 integrates a 5-port fast Ethernet switch with these features:

- QoS support with four traffic classes based on arrival port, IEEE802.1p, IPv4 TOS, IPv6 TC and Destination MAC Address
- Supports strict priority, WRR, and mixed mode (1 SP + 3 WRR or 2 SP + 2 WRR)
- Full IEEE 802.1Q VLAN ID processing per port and VLAN tagging for 4096 VLAN IDs; and port based VLANs supported
- Support VLAN tag insert or remove function on per-port basis
- Support QinQ double tag, and 16 entry of VLAN translation table
- IGMPv1/v2/v3 and MLDv1/v2 Snooping with hardware join and fast leave function
- Support 32 ACL rules/rule-based counters
- Support 16 PPPoE sessions header remove
- Port states and BPDU handling support IEEE802.1D spanning tree protocol
- High performance lookup engine with 1024 MAC address with automatic learning and aging and support for static addresses
- Support 40 MIB counters per port
- Autocast MIB counters to CPU port
- Support ingress and egress rate limit
- Broadcast storm suppression
- Supports port mirror
- Support MAC and PHY loopback function for diagnosis
- Fully compliant with IEEE 802.3/802.3u auto-negotiation function
- Flow control fully supported IEEE 802.3x flow control for full duplex and back pressure for half duplex
- Supports port lock function
- Supports hardware looping detection
- Power saving on no link and low traffic rate for 10Base-T
- Access to switch internal registers through dedicated internal MDIO interface. The internal MDIO interface is controlled through GMAC1 MII registers described in MII Configuration, page 7-259 through MII Indicators, page 7-261.

8.3 Five-Port Ethernet Switch

The Ethernet switch is a highly integrated two-Gb MAC plus 5-port fast Ethernet switch with non-blocking switch fabric, a high-performance lookup unit with 1024 MAC address, 4096 VLAN table, 32 ACL rule table, and a 4-traffic class QoS engine. It supports various networking applications as well as many offload functions to increase system performance. The fast Ethernet in the Ethernet switch complies with IEEE 802.3 standards. The Ethernet switch implements power saving to facilitate low power consumption and is designed to work in all environments. True Plug-n-Play is supported with auto-crossover, auto-polarity, and auto- negotiation in PHYs.

8.3.1 Overview

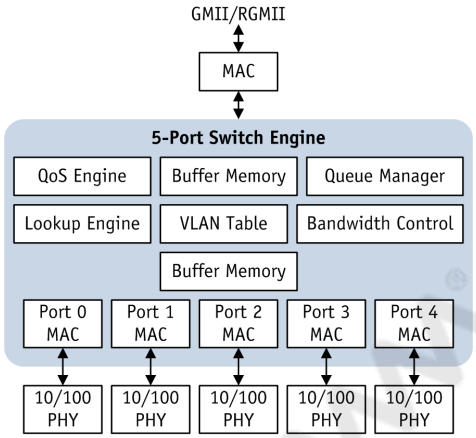


Figure 8-2 5-Port Ethernet Switch

The 5-port Ethernet switch supports many operating modes configurable using the MDC/MDIO interface and controlled by GMAC1 management interface registers. It also supports a CPU header mode that appends two bytes to each frame. The CPU can use headers to configure the switch register, address lookup table, VLAN, and receive auto-cast MIB frames. The fifth port (PHY4) supports a PHY interface as a WAN port. The first port (port0) supports a MAC interface and can be configured to connect to an external management CPU or an integrated CPU in a routing or xDSL/802.11n/PON engine. The Ethernet switch contains a 2-K entry address lookup table with two entries per bucket to avoid hash collision and maintain non-blocking forwarding performance. The address table provides read/write access from the serial and CPU interfaces; each entry can be configured as a static entry. The Ethernet switch supports 4096 VLAN entries configurable as port-based VLANs or 802.1Q tag-based VLANs. It also supports a QinQ function and VLAN translation.

To provide non-blocking switching performance in all traffic environments, the Ethernet switch supports several QoS function types with four-level priority queues based on port, IEEE 802.1p, IPv4 DSCP, IPv6 TC, 802.1Q VID, MAC address, or ACL layer 1 to layer 4 rule result. Included back pressure and pause frame-based flow control schemes support zero packet loss in temporary traffic congestion. The QoS switch architecture supports ingress policing and egress rate limiting.

The Ethernet switch supports IPv4 IGMP snooping and IPv6 MLD snooping to significantly improve the performance of streaming media and other bandwidth-intensive IP multicast applications. The Ethernet switch also supports PPPoE header remove for multicast stream within 16 PPPoE session. That can offload the CPU loading and improve the system performance.

IEEE 802.3x full duplex flow control and back-pressure half duplex flow control schemes are supported to ensure zero packet loss during temporary traffic congestion. A broadcast storm control mechanism prevents the packets from flooding into other parts of the network. The Ethernet switch device has an intelligent switch engine to prevent head-of-line blocking problems on a per-CoS basis for each port.

8.3.2 Basic Switch Operation

The Ethernet switch automatically learns the port number of an attached end station by looking at the source MAC address of all incoming packets at wire speed. If the source address is not found in the address table, the Ethernet switch device adds it to the table. Once the MAC address/port number mapping is learned, all packets directed to that end station MAC address are forwarded to the learned port number only. When the Ethernet switch device receives incoming packets from one of its ports, it searches in its address table for the destination MAC address, then forwards the packet to the appropriate port within the VLAN group. If the destination MAC address is not found (a new, unlearned MAC address), the Ethernet switch handles the packet as a broadcast packet and transmits it to all ports within the VLAN group except to the port where it came in.

8.3.3 Media Access Controllers (MAC)

The Ethernet switch integrates six independent Fast Ethernet MACs that perform all functions in the IEEE 802.3 specifications, for example, frame formatting, frame stripping, CRC checking, CSMA/ CD, collision handling, and back pressure flow control. Each MAC supports 10 Mbps, or 100 Mbps operation in either full-duplex or half-duplex mode. 1000 Mbps is supported in full-duplex mode.

8.3.4 ACL

The Ethernet switch supports up to 32 ACL rule table entries. Each rule can support filtering of the incoming packets based on these fields in the packet:

- Source MAC address
- Destination MAC address
- VID
- Ethertype
- Source IP address
- Destination IP address
- Protocol
- Source TCP/UDP port number
- Destination TCP/UDP port number
- Physical port number

When the incoming packets match an entry in the rules table, these actions can be taken and defined in the result field:

- Change VID field
- Drop the packet

Figure 8-3 shows the ACL rule architecture. Each rule is defined by rule control and rule result. Rule control is 4 bytes wide, with four indexes in each control field. Each index points to one rule entry in the rule table. Each rule entry in the rule table can be one of these rules:

- MAC rule
- IPv4 rule
- IPv6 rule

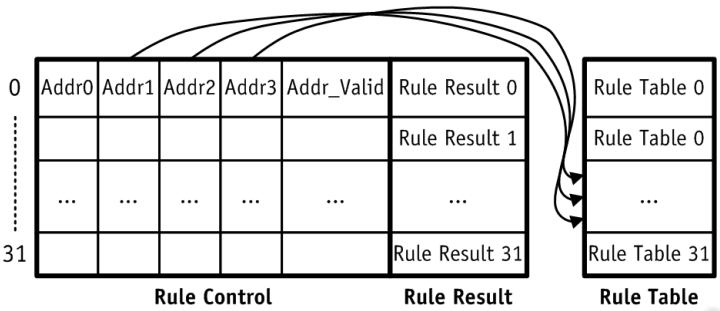


Figure 8-3 ACL Rule Architecture

Note that this ACL engine is available only when switch ports are being accessed through GMAC1, and is independent of the ACL engine available as part of the Ethernet subsystem accessed through GMAC0.

8.3.5 Register Access

The MDIO interface allows access to Ethernet switch and MII registers. The format to access MII registers in the embedded PHY is:

Start	OP	0x0	PHY_ADDR[2:0]	REG_ADDR[4:0]	TA[1:0]	DATA[15:0]

Where the PHY address is 0x00–0x04. OP code 10 indicates the read command, 01 the write command. Ethernet switch internal registers are 32 bits wide, but MDIO access only 16 bits; thus it requires 2x access to complete internal register access. Also, the address spacing has more than 10 bits supported by MDIO, thus it must write the upper address bits to internal registers. For example:

1. Register address bits [18:9] are treated as page address and written out first as HIGH_ ADDR[9:0]:

Start	OP	0x3	8’b0	TA [1:0]	6’b0	HIGH_ADDR[9:0]

   Where HIGH_ADDR[9:0] is ADDRESS[18:9] of the register.

2. Then LOW_ADDR can be re-accessed:

Start	OP	2’b10	LOW_ADDR[7:0]	TA[1:0]	DATA[15:0]

   Where LOW_ADDR[7:1] is the address bit [8:2] of the register and LOW_ADDR[0] is 0 for DATA[15:0] or 1 forDATA[31:16].

8.3.6 LED Control

LED control consists of five rules: two control PHY0-PHY3 LEDS, two control PHY4 LEDs, and one controls the MAC0, MAC5, and MAC6 LED. Each PHY port has two LEDs; default behavior is 100_LINK_ACTIVITY and 10_LINK_ACTIVITY. Each MAC0/5/6 has one LED; default LED behavior is LINK_ACTIVITY. Thus two can be connected to indicate OR operation of the original LEDs. Another way to achieve this operation is to modify LED control. See Table 8-1.

Table 8-1 LED Control Rules

Bit	Name	MAC_LED_ RULE	LED_ RULE_0/1	LED_ RULE_2/3	Description	
15:14	PATTERN_EN	0xCF35	0xC935	0xCA35	00	LED always off
					01	LED blinking at 4 Hz
					10	LED always on
					11	LED controlled by the following bits
13	FULL_LIGHT_EN	0x3	0x3	0x3	The LED lights when linked up at full duplex	
12	HALF_LIGHT_EN	0x0	0x0	0x0	The LED lights when linked up at half duplex	
11	POWER_ON _LIGHT_EN	0x0	0x0	0x0	When set, the module should enter POWER_ ON_RESET status after reset	
10	LINK_1000M _LIGHT_EN	0x1	0x1	0x1	When set, the LED will light when linked up at 1000 Mbps	
9	LINK_100M _LIGHT_EN	0x1	0x0	0x0	When set, the LED will light when linked up at 100 Mbps	
8	LINK_10M _LIGHT_EN	0x1	0x0	0x1	When set, the LED will light when linked up at 10 Mbps	
7	COL_BLINK_EN	0x1		0x0	When set, the LED will blink when a collision is detected	
6	RES	—			Reserved	
5	RX_BLINK_EN	0x1	0x1	0x0	When set, the LED will blink when a frame is being received	
4	TX_BLINK_EN	0x1	0x1	0x0	The LED blinks when receiving a frame	
3	RES	—			Reserved	
2	LINKUP _OVER_EN	0x1	0x1	0x1	0	Rx/Tx blinking ignored at LINKUP speed.
					1	If LINKUP LED is on, allow Tx/Rx blinking. Otherwise the LED is off.
1:0	LED_BLINK_ FREQ	0x1: 4 Hz	0x1: 4 Hz	0x1: 4 Hz	LED blink frequency select. If linked up at 1000 Mbps, use 4 Hz; at 10 Mbps, use 2 Hz.	
					00	2 Hz
					01	4 Hz
					10	8 Hz

8.3.7 VLANs

The Ethernet switch supports many VLAN options including IEEE 802.1Q and port-based VLANs. The Ethernet switch supports 4096 IEEE 802.1Q VLAN groups and 4000 VLAN table entries, and it checks VLAN port membership from the VLAN ID extracted from the tag header of the frame. The port-based VLAN is enabled according to the user-defined PORT VID value. The Ethernet switch supports optional discards of tagged, untagged frames, and priority tagged frames; the QCA9531 also supports untagging the VLAN ID for packets going on untagged ports on a per-port basis.

8.3.8 IEEE Port Security

The Ethernet switch supports 802.1Q security features. Its discards ingress frames that do not meet security requirements and ensures those frames that do meet the requirements are sent to the designated ports only. Levels of security can be set differently on each port, and options are processed using the ingress frame VID:

Mode	Description
Secure	The frame is discarded and its VID is not in the VLAN table, or the ingress port is not a member of the VLAN. The frame can exit only the ports that are members of the frame VLAN.
Check	The frame is discarded if its VID is not in the VLAN table. It can exit only the ports that are members of the frame VLAN.
Fallback	If the frame VID is in the VLAN table, the frame can exit only ports that are members of the frame VLAN. Otherwise the switch decides forwarding policy based on the port-based VLAN. If a frame arrives untagged, the QCA9531 forwards it based on the port-based VLAN, even if the ingress port's 802.1Q mode is enabled.
Egress	The QCA9531 supports port-based egress, both unmodified and force untagged.

The Ethernet switch identifies packet priority based on QoS priority information: port-based, 802.1p CoS, IPv4 TOS/diffserv, and IPv6 TC. It supports up to four queues per egress port. For tagged packets, incoming packet priority maps to one of four CoS queues based on either the priority field in the tag header or the result of classification lookup. For untagged packets, CoS priority comes from a configurable field in the VLAN address tables or from classification lookup results. After packets map to an egress queue, they are forwarded using either strict priority or weighted fair queuing scheduler.

8.3.9 Mirroring

Mirroring monitors traffic to gather information or troubleshoot higher-layer protocol operations. Users can specify that a desired mirrored-to port (sniffer port) receive a copy of all traffic passing through a designated mirrored port. The Ethernet switch supports mirror frames that:

- Come from an ingress specified port (ingress mirroring)
- Are destined for egress-specified port (egress mirroring)
- Mirror all ingress and egress traffic to a designated port
- Mirror frames to a specific MAC address

8.3.10 Broadcast/Multicast/Unknown Unicast

The Ethernet switch supports port-based broadcast suppression including unregistered multicast, unregistered unicast and broadcast. If broadcast/multicast strom control is enabled, all broadcast/ multicast/unknown unicast packets beyond the default threshold of 10 ms (for 100 Mbps operations) and 100 ms (for 10 Mbps operations) are discarded.

8.3.11 IGMP/MLD Snooping

The Ethernet switch supports IPv4 IGMP (v1/v2/v3) snooping and IPv6 MLD (v1/v2) snooping. By setting IGMP_MLD_EN in the port control registers, the Ethernet switch can look inside IPv4 and IPv6 packets and redirect IGMP/MLD frames to the CPU for processing. The Ethernet switch also supports hardware IGMP join and fast leave functions. By setting IGMP_JOIN_EN and IGMP_LEAVE_EN in the port control registers, the Ethernet switch updates the ARL table automatically when it receives an IGMP/MLD join or leave packet, then forwards it to the router port directly if the CPU is not acting as a router or when enabling multicast VLAN LEAKY to bypass multicast traffic directly from WAN to LAN.

The statistics counter block maintains 40 MIB counters per port; counters provide Ethernet statistics for frames received on ingress and transmitted on egress. The CPU can capture, read, or clear counter values via the registers. All MIB counters clear once read. Hardware join/fast leave supports these packet types:

- IGMPv1 join
- IGMPv2/MLDv1 join/leave
- IGMPv3/MLDv2 report (excluding NONE or including NONE)

8.3.12 Spanning Tree

IEEE 802.1D spanning tree allows bridges to automatically prevent and resolve Layer 2 forwarding loops. Switches exchange BPDUs and configuration messages and selectively enable and disable forwarding on specified ports. A tree of active forwarding links ensures an active path between any two nodes in the networks. Spanning tree can be enabled globally or on a per-port basis by configuring the port status registers.

8.3.13 MIB/Statistics Counters

The statistics counter block maintains a set of 40 MIB counters per port, which provide a set of Ethernet statistics for frames received on ingress and transmitted on egress. A register interface allows the CPU to capture, read, or clear the counter values. All MIB counters are cleared when read.

The counters support:

- RMON MIB
- Ethernet-like MIB
- MIB II
- Bridge MIB
- RFC2819

The CPU interface supports:

- Autocast MIB counters after half-full
- Autocast MIB counters after time out
- Autocast MIB counters when requested
- Clearing all MIB counters

Table 8-2 MIB Counters

Counter	Width (Bits)	Offset	Description
RxBroad	32	0x00	The number of good broadcast frames received
RxPause	32	0x04	The number of PAUSE frame received
RxMulti	32	0x08	The number of good multicast frames received
RxFCSErr	32	0x0C	The number of frames received with a valid length, but an invalid FCS and an integral number of octets
RxAlignErr	32	0x10	The total number of frame received with a valid length that do not have an integral number of octets and an invalid FCS
RxRunt	32	0x14	The number of frames received that are <64 bytes long and have a bad FCS
RxFragment	32	0x18	The number of frames received that are <64 bytes long and have a bad FCS
Rx64Byte	32	0x1C	The number of frames received that are exactly 64 bytes long including errors
Rx128Byte	32	0x20	The number of frames received whose length is between 65 and 127 bytes, including those with errors
Rx256Byte	32	0x24	The number of frames received whose length is between 128 and 255 bytes, including those with errors
Rx512Byte	32	0x28	The number of frames received whose length is between 256 and 511 bytes, including those with errors
Rx1024Byte	32	0x2C	The number of frames received whose length is between 512 and 1023 bytes, including those with errors
Rx1518Byte	32	0x30	The number of frames received whose length is between 1024 and 1518 bytes, including those with errors

Table 8-2 MIB Counters (cont.)

RxMaxByte	32	0x34	The number of frames received whose length is between 1519 and maxlength, including those with errors (Jumbo)
RxTooLong	32	0x38	The number of frames received whose length exceeds maxlength, including those with FCS errors
RxGoodByte	64	0x3C, 0x40	Total octets received in frame with a valid FCS. All frame sizes are included
RxBadByte	64	0x44, 0x48	Total valid frames received that are discarded due to lack of buffer space
RxOverflow	32	0x4C	Total valid frames received that are discarded due to lack of buffer space
Filtered	32	0x50	Port disabled and unknown VID
TxBroad	32	0x54	The number of good broadcast frames transmitted
TxPause	32	0x58	The number of PAUSE frame transmitted
TxMulti	32	0x5C	The number of good multicast frames transmitted
TxUnderrun	32	0x60	Total valid frames discarded that were not transmitted due to transmit FIFO buffer underflow
Tx64Byte	32	0x64	The number of frames transmitted exactly 64 bytes long including errors
Tx128Byte	32	0x68	The number of frames transmitted whose length is between 65 and 127 bytes, including those with errors
Tx256Byte	32	0x6C	The number of frames transmitted whose length is between 128 and 255 bytes, including those with errors
Tx512Byte	32	0x70	The number of frames transmitted whose length is between 256 and 511 bytes, including those with errors
Tx1024Byte	32	0x74	The number of frames transmitted whose length is between 512 and 1023 bytes, including those with errors
Tx1518Byte	32	0x78	The number of frames transmitted whose length is between 1024 and 1518 bytes, including those with errors
TxMaxByte	32	0x7C	The number of frames transmitted whose length is between 1519 and maxlength, including those with errors (Jumbo)
TxOversize	32	0x80	Total frames over maxlength but transmitted truncated with bad FCS
TxByte	64	0x84, 0x88	Total data octets transmitted from counted, including those with a bad FCS
TxCollision	32	0x8C	Total collisions experienced by a port during packet transmission
TxAbortCol	32	0x90	Total number of frames not transmitted because the frame experienced 16 transmission attempts and was discarded
TxMultiCol	32	0x94	Total number of successfully transmitted frames that experienced more than one collision
TxSignalCol	32	0x98	Total number of successfully transmitted frames that experienced exactly one collision
TxExcDefer	32	0x9C	The number of frames that deferred for an excessive period of time
TxDefer	32	0xA0	Total frame whose transmission was delayed on its first attempt because the medium way was busy
TxLateCol	32	0xA4	Total number of times a collision is detected later than 512 bit-times into the transmission of a frame

8.3.14 Qualcomm Atheros Header Configuration

Table 8-3 describes the Qualcomm Atheros header configuration. The Qualcomm Atheros header is a two-byte header that the CPU uses to configure the Ethernet switch. The Qualcomm Atheros header will be located after the packet SA.

Table 8-3 Qualcomm Atheros Header Configuration

<table>
<tr><th>Bit</th><th>Name</th><th colspan="8">Description</th></tr>
<tr><td>15:14</td><td>VERSION</td><td colspan="8">2’b10</td></tr>
<tr><td>13:12</td><td>PRIORITY</td><td colspan="8">Packet priority</td></tr>
<tr><td rowspan="11">11:8</td><td rowspan="11">TYPE</td><td colspan="8">Packet Type:</td></tr>
<tr><td>0</td><td>Normal Packet</td><td colspan="6">Normal packet from Ethernet including management. The destination port is determined by the ARL and VLAN table.</td></tr>
<tr><td>1</td><td>RES</td><td colspan="6">Reserved</td></tr>
<tr><td>2</td><td>MIB</td><td colspan="6">Auto-cast MIB frame</td></tr>
<tr><td>4:3</td><td>RES</td><td colspan="6">Reserved</td></tr>
<tr><td rowspan="3">5</td><td rowspan="3">READ_ WRITE_REG</td><td colspan="6">Read or write the register frame:</td></tr>
<tr><td>8-Byte</td><td>4-Byte</td><td>2-Byte</td><td>0–12-Byte</td><td>34–46-Byte</td><td>4-Byte</td></tr>
<tr><td>Command (low byte first)</td><td>Data (low byte first)</td><td>Header (high byte first)</td><td>Data (low byte first)</td><td>Padding</td><td>CRC</td></tr>
<tr><td>6</td><td>READ_ WRITE_ REG_ACK</td><td colspan="6">Read or write register ACK frame from the CPU</td></tr>
<tr><td>15:7</td><td>RES</td><td colspan="6">Reserved</td></tr>
<tr><td rowspan="3">7</td><td rowspan="3">FROM_CPU</td><td colspan="8">Indicates the forwarding method:</td></tr>
<tr><td>0</td><td colspan="7">Forwarding based on the VLAN table result and PORT_NUM (bit [6:0])</td></tr>
<tr><td>1</td><td colspan="7">Forwarding based on the PORT_NUM (bit [6])</td></tr>
<tr><td>6:0</td><td>PORT_NUM</td><td colspan="8">If bit [6] (FROM_CPU) is set to 1, these bites define the port number to send the packet to. If the packet is destined to the CPU, then PORT_NUM indicates the source port number.</td></tr>
</table>

8.3.15 IEEE 802.3 Reserved Group Addresses Filtering Control

The Ethernet switch supports the ability to drop/redirect/copy 802.1D specified reserved group MAC addresses 01-80-C2- 00-00-04 to 01-80-C2-00-00-0F by adding the address to the ARL table.

The Ethernet switch can be configured to prevent the forwarding of unicast frames and multicast frames with unregistered destination MAC address on per port base by setting UNI_FLOOD_DP and MULTI_FLOOD_DP, where a bit represents a port of the Ethernet switch.

8.3.16 PPPoE Header Removal

The Ethernet switch supports PPPoE header removal for multicast streaming to offload CPU loading and improve CPU performance. The PPPoE session supports is 16 sessions. See Figure 8-4:

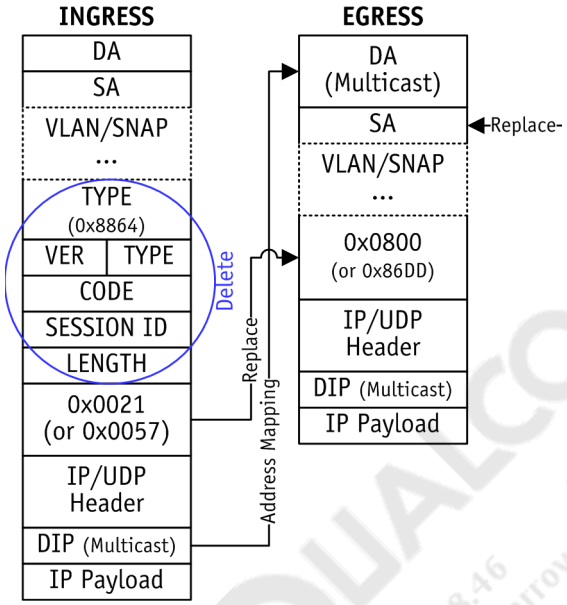


Figure 8-4 PPPoE Header Removal

Table 8-4 shows the possible results.

Table 8-4 PPPoE Session ID

Bit	Name	Description	
19	Session ID Valid	0	No valid session ID to compare to
		1	Session ID is valid (drop PPPoE header)
18:16	RES	Reserved	
15:0	Session ID	Session ID to be compared with PPPoE session frame	

Table 8-5 shows the Ethernet switch memory map.

Table 8-5 Memory Map

Global Register	Offset
Global Register	0x0000–0x000FC
Port Register	0z0100–0x0012C
MIB Register	0x20*00–0x20*A4
ACL Table	0x58000–0z58FEC
Translation Table	0x59000–0x5907C
Session ID Table	0x59100–0x5913F

8.4 Ethernet Core Reset

Reset of the QCA9531 Ethernet core is controlled by software writing to the register, 0x1806001C Reset (RST_RESET), page 7-126：

Table 8-6 RST_RESET Register

Bit	Name	Description
24	FULL_CHIP_RESET	Used to command a full chip reset. This is the software equivalent of pulling the rest pin. The system will reboot with PLL disabled.
20	CPU_COLD_RESET	Used to cold reset the entire CPU. This bit will be cleared automatically immediately after the reset.
12	ETH_SWITCH_ARESET	Resets the switch analog circuitry.
8	ETH_SWITCH_RESET	Resets the switch digital circuitry.

When the chip is brought out of cold reset or hardware reset, or watchdog reset, software should control the ETH_SWITCH_ARESET and ETH_SWITCH_RESET bits such that the timing requirement as shown in Figure 8-5 is observed.

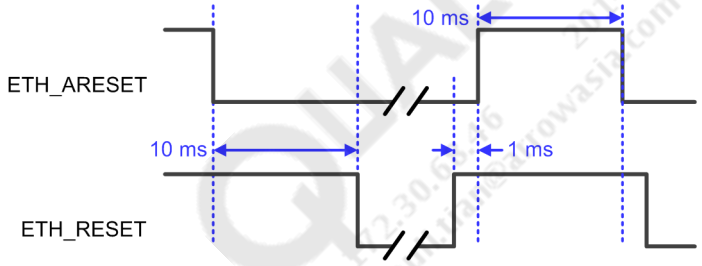


Figure 8-5 Ethernet Core Reset Timing Requirement for Full Chip Reset

ETH_SWITCH_RESET should be taken out of reset at least 10 msec after ETH_SWITCH_ ARESET is taken out of reset (from high to low).

ETH_SWITCH_RESET should enter reset at least 1 msec before ETH_SWITCH_ARESET enters reset (from low to high); the duration of ETH_SWITCH_ARESET should be at least 10 msec.

A read-modify-write operation is recommended when writing to the RST_RESET register.

The reset sequence should be:

- Read-modify-write to bit [8], ETH_SWITCH_RESET, wait 1 msec, then read-modify-write bit [12], ETH_SWITCH_ARESET, then wait 10 msec.

The de-assertion of reset sequence should be:

- Read-modify-write to bit [12], ETH_SWITCH_ARESET, wait 10 msec, then read-modify-write bit 8, EHT_SWITCH_RESET.

During a complete chip software reset, the sequence should be:

- Read-modify-write bit [8], ETH_SWITCH_RESET, wait 1 msec, then read-modify-write bit 12, ETH_SWITCH_ARESET; wait 1 msec, then read modify write bit [24], FULL_CHIP_ RESET. At least 10 msec should pass before Ethernet subsystems are released from reset again.

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 9-1 summarizes the absolute maximum ratings and Table 9-2 lists the recommended operating conditions for the QCA9531.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 9-1 Absolute Maximum Ratings

Symbol	Parameter	Max Rating	Unit
V_{DD33}	Supply Voltage	-0.3 to 3.6	V
V_{DD25}	Maximum I/O Supply Voltage	-0.3 to 3.0	V
V_{DD12}	Core Voltage	-0.3 to 1.8	V
T_{store}	Storage Temperature	-65 to 150	°C
T_j	Junction Temperature	125	°C
ESD	Electrostatic Discharge Tolerance	2000	V

9.2 Recommended Operating Conditions

Table 9-2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	Supply Voltage	±5%	3.135	3.3	3.465	V
V_{DD25}	I/O Supply Voltage[1]	±5%	2.49	2.62	2.75	V
V_{DD12}	Core Voltage	±5%	1.17	1.23	1.29	V
A_{VDD12}	Analog Voltage	±5%	1.17	1.23	1.29	V
A_{VDD20}	Voltage for Ethernet PHY[1]	—	1.9	2.0	2.15	V
V_{DD_DDR}	DDR1 I/O Voltage[1]	±5%	2.47	2.6	2.73	V
	DDR2 I/O Voltage[1]	±5%	1.71	1.8	1.89	V
V_{DDR_VREF}	DDR1 Reference Level for SSTL Signals[2]	—	1.24	1.3	1.37	V
	DDR2 Reference Level for SSTL Signals[2]	—	0.86	0.9	0.95	V
T_{case}	Case Temperature	—	0	—	105	°C
Psi_{JT}	Thermal Parameter[3]	—	—	—	2.5	°C/W

1. Voltage regulated internally by the QCA9531
2. Divide VDD_DDR voltage by two externally, see reference design schematic
3. The thermal parameter is for the 12x12 mm DRQFN package

9.3 Radio Characteristics

The following conditions apply to the typical characteristics unless otherwise specified:

- VDD12 = 1.2 V
- VDD33 = 3.3 V, Tamb = 25 °C

9.3.1 Radio Receiver Characteristics

Table 9-3 summarizes the QCA9531 receiver characteristics. These conditions apply to the typical characteristics unless otherwise specified: V_{DD12} = 1.2 V, V_{DD33} = 3.3 V, T_{amb} = 25°C.

Table 9-3 Radio Receiver Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receiver input frequency range	5 MHz center frequency	2.412	—	2.472	GHz
NF	Receive chain noise figure (max gain)	See Note[1]	—	5.5	—	dB
S_{rf}	Sensitivity					
	CCK, 1 Mbps	See Note[2]	—	-97	—	dBm
	CCK 11 Mbps		-76	-88		
	OFDM, 6 Mbps		-82	-91	—	
	OFDM, 54 Mbps		-65	78	—	
	HT20, MCS0, 1 stream, 2 Tx, 2 Rx		-82	-90	—	
	HT20, MCS7, 1 stream, 2 Tx, 2 Rx		-64	-75	—	
	HT20, MCS8, 2 stream, 2 Tx, 2 Rx		-82	-90	—	
	HT20, MCS15, 2 stream 2 Tx, 2 Rx		-64	-71	—	
	HT40, MCS0, 1 stream, 2 Tx, 2 Rx		-79	-81	—	
	HT40, MCS7, 1 stream, 2 Tx, 2 Rx		-61	-73	—	
	HT40, MCS8, 2 stream, 2 Tx, 2 Rx		-79	-89	—	
	HT40, MCS15, 2 stream 2 Tx, 2 Rx		-61	-69		
IP1	Input 1 dB compression (min. gain)	—	—	-0.5	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	8	—	dBm
Z_{RFin_input}	Recommended LNA differential drive impedance	Note[3]	—	25.6-j1.2	—	Ω
ER_{phase}	I,Q phase error	Note[4] [5]	—	2.2	—	°
ER_{amp}	I, Q amplitude error		—	0.15	—	dB
R_{adj}	Adjacent channel rejection					
	CCK, 2L	10 to 20 MHz[6]	35	39	—	dB
	OFDM, 6 Mbps		16	34	—	
	OFDM, 54 Mbps		-1	19	—	
	HT20, MCS0		16	34	—	
	HT40, MCS0		16	24	—	
TR_{powup}	Time for power up (from synthesizer)	—	—	1.5	—	µs

1. The noise figure computation includes the baseband gain stages along with LNA.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes Tx/Rx antenna switch. Minimum values based on IEEE 802.11 specifications.
3. Estimated Values
4. These are residual values after applying IQ calibration at chip level
5. This data represents values before applying chip level calibration co-efficients
6. Typical values measured with reference design. Minimum values based on IEEE 802.11 specifications.

9.3.2 Transmitter Characteristics

Table 9-4 summarizes the transmitter characteristics for the QCA9531.

Table 9-4 Transmitter Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.412	—	2.472	GHz
P_{out}	Mask Compliant power					
	1 Mbps	See Note[1]	—	20	—	dBm
	6 Mbps		—	19	—	
	HT20, MCS0		—	18	—	
	HT40, MCS0		—	17	—	
	EVM Compliant Power					
	54 Mbps	See Note[1]	—	15	—	
	HT20, MCS15		—	13	—	
	HT40, MCS15		—	12	—	
SP_{gain}	PA gain step	See Note[2]	—	0.5	—	dB
A_{pl}	Accuracy of power leveling loop	See Note[3]	—	±2	—	dB
Z_{RFout_load}	Recommended PA differential load impedance	See Note[4]	—	172+j147	—	Ω
OP1dB	Output P1dB (max. gain)	See Note[5]	21.5	22.5	—	dBm
OIP3	Output third order intercept point (max. gain)	—	31	32	—	dBm
ER_{phase}	I,Q phase error	—	—	±/-0.11	—	°
ER_{amp}	I,Q amplitude error	—	—	±/-0.08	—	dB
RS	Synthesizer reference spur	—	< -45	-52	—	dBc
TTpowup	Time for power up	—	—	1.5	—	µs

1. Measures using the Internal PA recommended by Qualcomm Atheros under open-loop power control.
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.
5. Measured at the antenna connector port of the reference design, which includes Tx/Rx antenna switch.

9.3.3 Synthesizer Characteristics

Table 9-5 summarizes the synthesizer characteristics for the QCA9531.

Table 9-5 Synthesizer Composite Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)		2.412	—	2.472	
	At 30 KHz offset	—	-90	–92	—	dBc/Hz
	At 100 KHz offset		-90	-94	—	
	At 500 KHz offset		-105	-111	—	
	At 1 MHz offset		-110	-117	—	
F_C	Center channel frequency	± 20 ppm[1]	2.412	—	2.472	GHz
F_{ref}	Reference oscillator frequency		—	25	—	MHz
TS_{powup}	Time for power up	—	—	200	—	µs

1. Manufacturing calibration is required; And is over temperature and aging.

9.4 Power Consumption

Table 9-6 Power Consumption for 2.4 GHz Operation (internal PA)

Operating Mode[1]	3.3 V Supply (mA)[2]	VDD_DDR (mA)[3]	VDD12 (mA)[3]	VDD25 (mA)[3]	AVDD20 (mA)[3]
TX (two-chain at 21 dBm, Rx (Two-chain	685	20	600	20	50

1. Internal 2.4 GHz radio, internal PA, PCIE RC interface, USB and internal switch are all in maximum data transfer condition and the CPU in maximum utilization.
2. The current consumption from 3.3 V includes analog, RF, USB and the 1.2 V power as the internal switching regulator is used
3. Current consumption of the VDD_DDR, VDD25, AVDD20 and VDD12 power rails from the QCA9531

9.5 AC Specifications

9.5.1 SPI Timing

Figure 9-1 shows the SPI timing. See Table 9-7 for timing values.

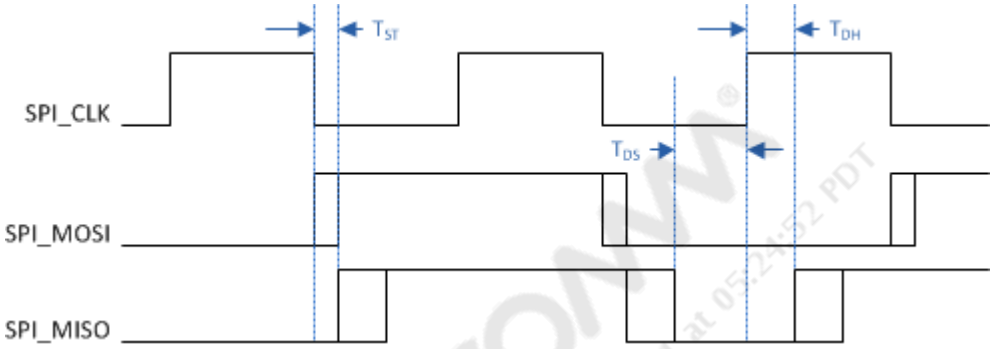


Figure 9-1 SPI Timing

Table 9-7 SPI Timing Values

Parameter	Min	Max	Comments
T_{DS}	11.0 ns	—	Minimum needed by the QCA9531
T_{ST}	—	3 ns	Maximum time by which data is available
T_{DH}	1 ns	—	Minimum hold duration

Actual SPI operating frequency is dependent on the CLK-to-SO flash delay and the CLK/MISO signals propagation delay in the board. The minimum SPI_CLK period is 2 * (TDS + (CK-to-SO flash delay) + (board propagation delay of CLK + board propagation delay of MISO signals).

9.5.2 DDR Timing

Figure 9-2 shows the DDR output timing. See Table 9-8 and Table 9-9 for timing values.

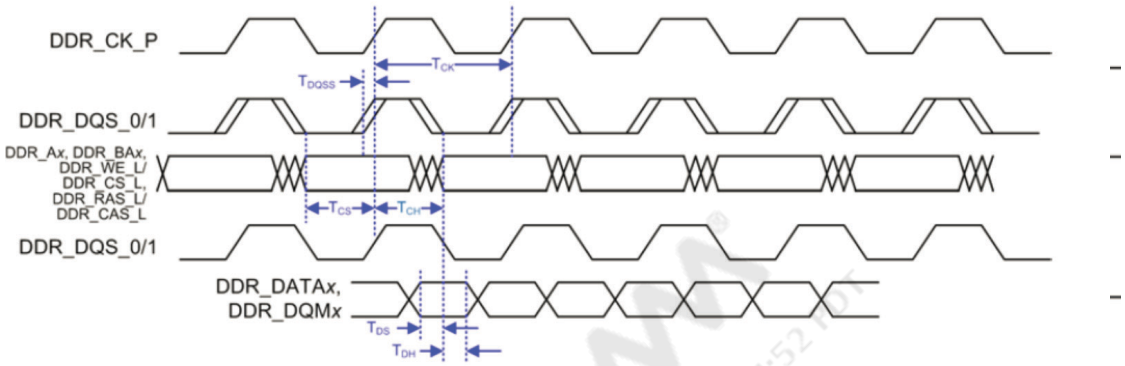


Figure 9-2 DDR Timing

Table 9-8 DDR1 Timing Parameters

Parameter	Reference Signal	Minimum	Maximum	Comment
T_{CK}	—	5 ns[1]	—	Normal periods of CK_P clock output signal
T_{IS}	DDR_CK_P	1.4 ns	—	CLK-ADDR/CMD setup time
T_{IH}	DDR_CK_P	2.0 ns	—	CLK-ADDR/CMD hold time
T_{DS}	DDR_DQS_0/1	0.5 ns	—	DQS_DQ setup time
T_{DH}	DDR_DQS_0/1	1.3 ns	—	DQS_DQ holdtime
T_{DQSS}	DDR_CK_P	—	0.3 ns	CLK-DQS skew

1. Does not include clock jitter effects

Table 9-9 DDR2 Timing Parameters

Parameter	Reference Signal	Minimum	Maximum	Comment
T_{CK}	—	3.3 ns[1]	—	Normal periods of CK_P clock output signal
T_{IS}	DDR_CK_P	1.25 ns	—	CLK-ADDR/CMD setup time
T_{IH}	DDR_CK_P	1.8 ns	—	CLK-ADDR/CMD hold time
T_{DS}	DDR_DQS_0/1	450 ps	—	DQS_DQ setup time
T_{DH}	DDR_DQS_0/1	650 ps	—	DQS_DQ holdtime
T_{DQSS}	DDR_CK_P	—	0.3 ns	CLK-DQS skew

1. Does not include clock jitter effects

9.5.3 DDR Timing Input

Figure 9-3 shows the DDR input timing. See Table 9-10 for timing values.

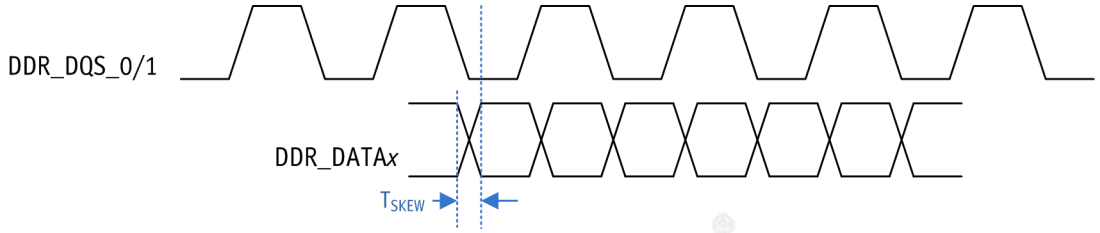


Figure 9-3 DDR Input Timing

Table 9-10 DDR Input Timing Parameters

Parameter	Ref Signal	Min	Max	Comment
T_{SKEW}	DDR_DQS_0/1	—	0.45 ns	Maximum skew from DQS to DQ being stable from memory

9.5.4 Reset Timing

The VDD33 voltage needs to come up first, VDD25 and VDD12 voltages can come up in any sequence. The last one to come up determines when the internal reset is deasserted. If an external VDD_DDR supply is used, it should be stable within 100 µs maximum with respect to the last of the three other power rails (VDD33, VDD25, an d VDD12). If the internal regulator is used to generate VDD_DDR, typically VDD_DDR is available approximately 10 µs after VDD33, VDD25 and VDD12 are stable. It is desirable for VDD12 to come up before VDD25. Figure 9-4 shows an example of a reset timing. Figure 9-5 shows the bootstrap timing.

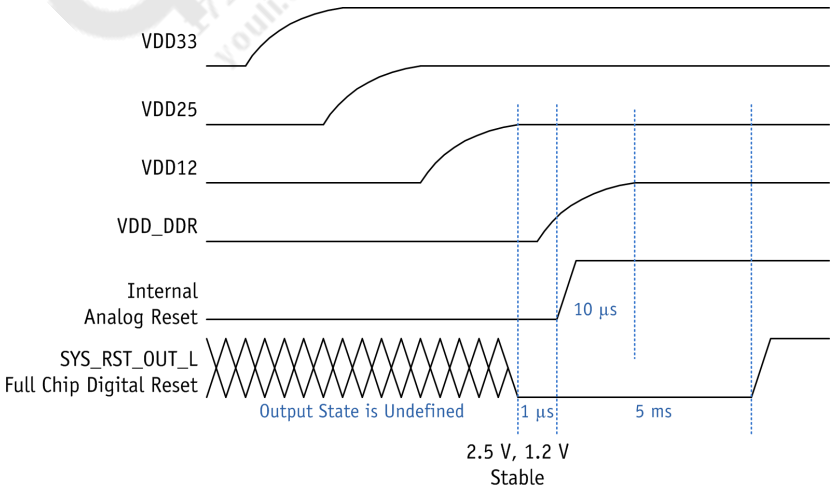


Figure 9-4 Reset timing example

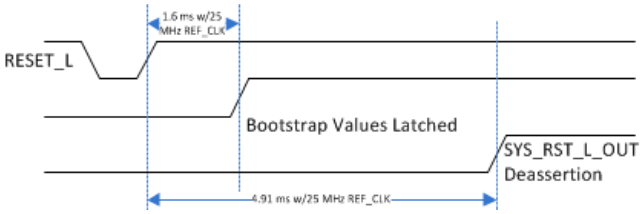


Figure 9-5 Bootstrap Timing

10 Part Reliability

10.1 Reliability Qualifications Summary

Table 10-1 QCA9531 Reliability Evaluation Report for 12x12 Cu DRQFN 156

Reliability Tests, Standards and Conditions	Sample Size	Results
Average failure rate (AFR, λ) in FIT **Failure in billion device-hours** Functional HTOL: JESD22-A108 (Total samples from 3 different wafer lots)	240 (3 lots of 80)	AFR = 36 FIT
Mean time to failure (MTTF, million hours) t = 1000/λ in million hours (Total samples from 3 different wafer lots)	240 (3 lots of 80)	27.8 million hours
ESD – (HBM) human body model rating ANSI/ESDA/JEDEC JS-001-2012 Target: 2000 V (Total samples from one wafer lot)	3	Pass; ± 2000 V; all pins
ESD – (CDM) charge device model rating JESD22-C101, Target: 500V (Total samples from one wafer lot)	3	Pass; ± 500V; all pins
Latch-up (I-test): JESD78 Trigger current: ±100 mA; Temperature: 85°C	3	Pass
Latch-up (Vsupply overvoltage): JESD78 Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification. Temperature: 85°C	3	Pass
Preconditioning: J-STD-020, JESD22-A113 MSL 3, reflow temperature: 260C+0/-5°C Total samples from three different assembly lots	2x3x77 2x3x77 2x3x77 2x3x77	TBD
Temperature cycle: JESD22-A104 Temperature: -65°C to +150°C Number of cycles: 1000 Cycle rate: 2 cycles per hour (cph) Preconditioning: JESD22-A113 MSL: 3; 260°C reflow temperature	3x77 3x77 3x77 3x77	TBD

Table 10-1 QCA9531 Reliability Evaluation Report for 12x12 Cu DRQFN 156

Biased highly accelerated stress test (BHAST) JESD22-A110 110C / 85% RH ; 264 hrs duration Preconditioning: JESD22-A113 MSL 3, 260°C reflow temperature	3x77 3x77 3x77 3x77	TBD
High temperature storage life: JESD22-A103 Temperature 150°C, 1000 hours duration	3x77 3x77 3x77 3x77	TBD

10.2 Qualification Sample Description

Table 10-2 QCA9531 Device Characteristics

Device name	QCA9531
Package type	DRFQN
Package body size	12 mm x 12 mm
Lead count	156
Lead composition	Matte Tin
Fab process	55 nm CMOS
Pin pitch	0.5 mm

11 Package Dimensions

The QCA9531 is packaged in a dual-row QFN package. The body size is 13 mm by 13 mm.

Moisture Sensitivity Level (MSL) for this device is L3 per JSTD020D-01.

The package drawings and dimensions are provided in Figure 11-1 and Table 11-1.

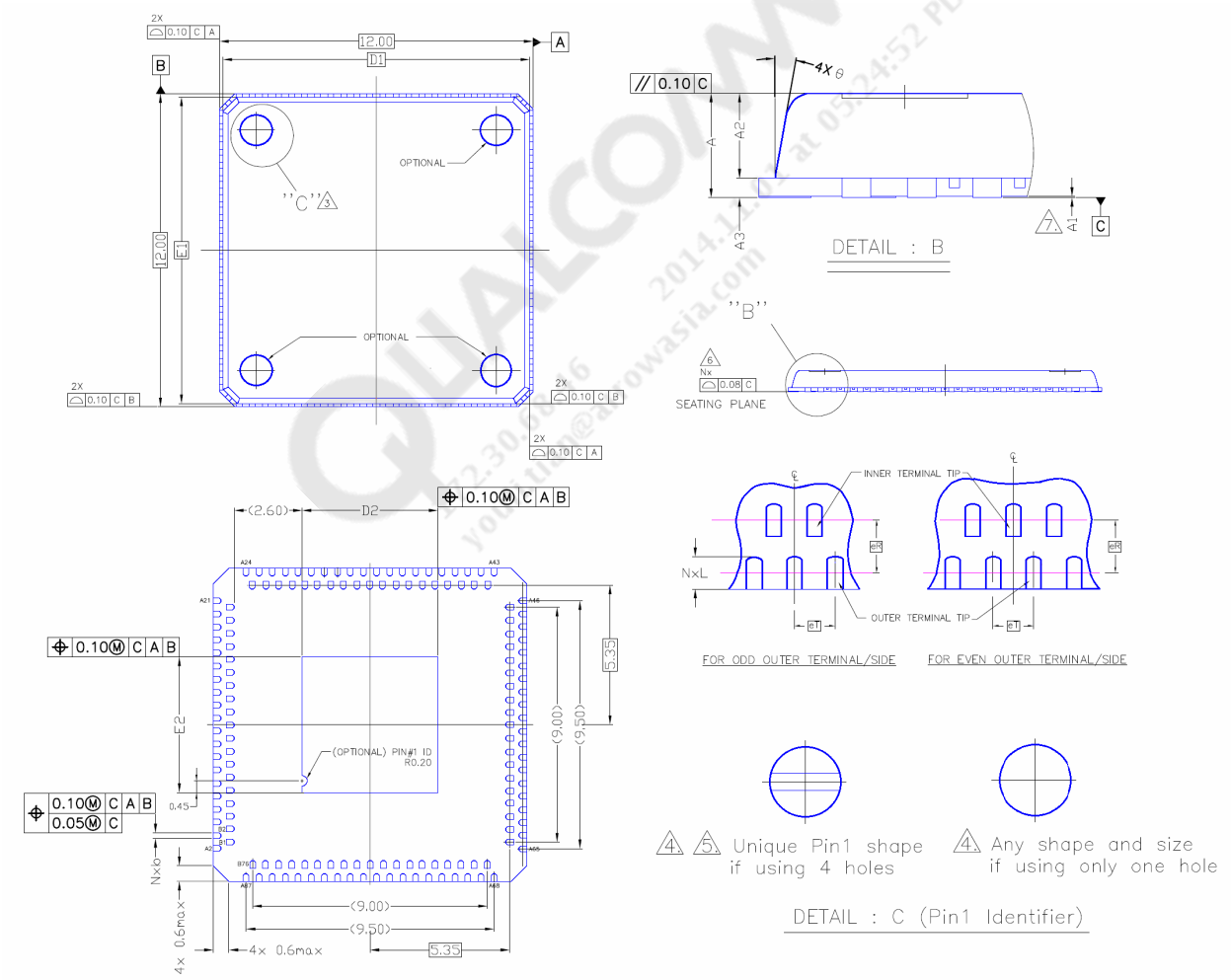


Figure 11-1 QCA9531 Package Drawing

Table 11-1 Package Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	0.90	mm	—	—	0.035	inches
A1	0.00	0.01	0.05	mm	0.00	0.0004	0.002	inches
A2	0.55	—	0.75	mm	0.022	0.024	0.030	inches
A3	0.15/0.25 REF			mm	0.006/0.010 REF			inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
L	0.20	0.30	0.40	nn	0.008	0.012	0.016	inches
D1/E1	11.73 - 11.75			mm	0.462/0.463			inches
D2/E2	5.10	5.20	5.30	mm	0.201	0.205	0.209	inches
eR	0.50 BSC			mm	0.020 BSC			inches
eT	0.50 BSC			mm	0.020 BSC			inches
La/Lb	0.20	0.30	0.40	mm	0.008	0.012	0.016	inches
θ	5-15			°	5-15			°

Notes:

1. Controlling dimension: millimeter
2. Reference Document: NT90-Y5244-1

12 Ordering Information

The order number QCA9531-BL3A specifies a lead-free standard-temperature version of the QCA9531.

The order number QCA9531-BL3A-R specifies a lead-free standard-temperature tape-and-reel version of the QCA9531.