

VUT BRNO

NXP LPC55S6X

NOV 2023
TOMAS VODA



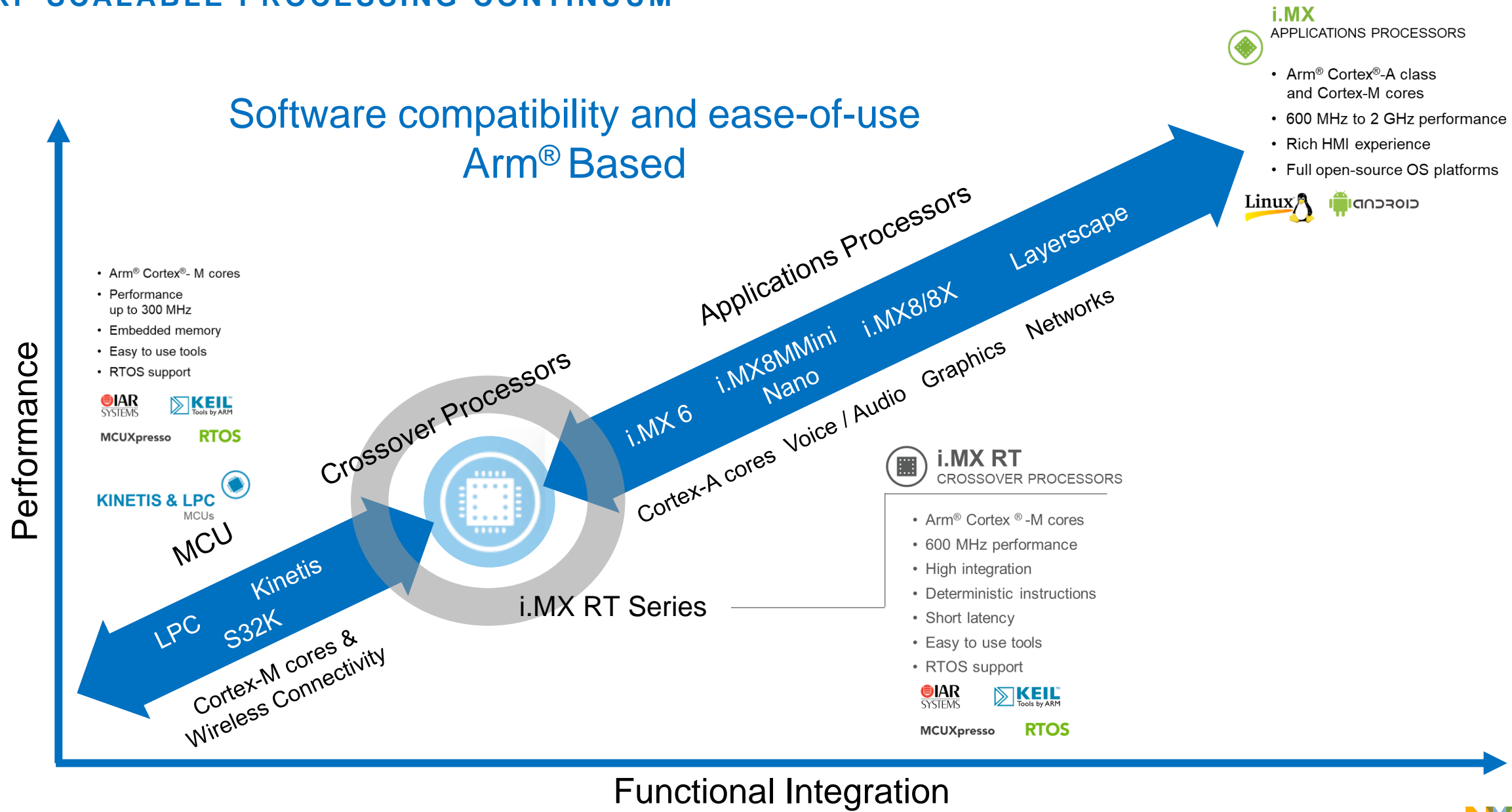
SECURE CONNECTIONS
FOR A SMARTER WORLD

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NXP SCALABLE PROCESSING CONTINUUM



i.MX APPLICATIONS PROCESSORS

- Arm® Cortex®-A class and Cortex-M cores
- 600 MHz to 2 GHz performance
- Rich HMI experience
- Full open-source OS platforms



i.MX RT CROSSOVER PROCESSORS

- Arm® Cortex®-M cores
- 600 MHz performance
- High integration
- Deterministic instructions
- Short latency
- Easy to use tools
- RTOS support



LPC55Sxx



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LPC5500 MCU SERIES

Key Features and Comparisons

- Nearly 20% performance improvement over Cortex-M4 based MCUs (over 50% vs Cortex-M23) with redesigned pipeline - up to two instructions per clock cycle

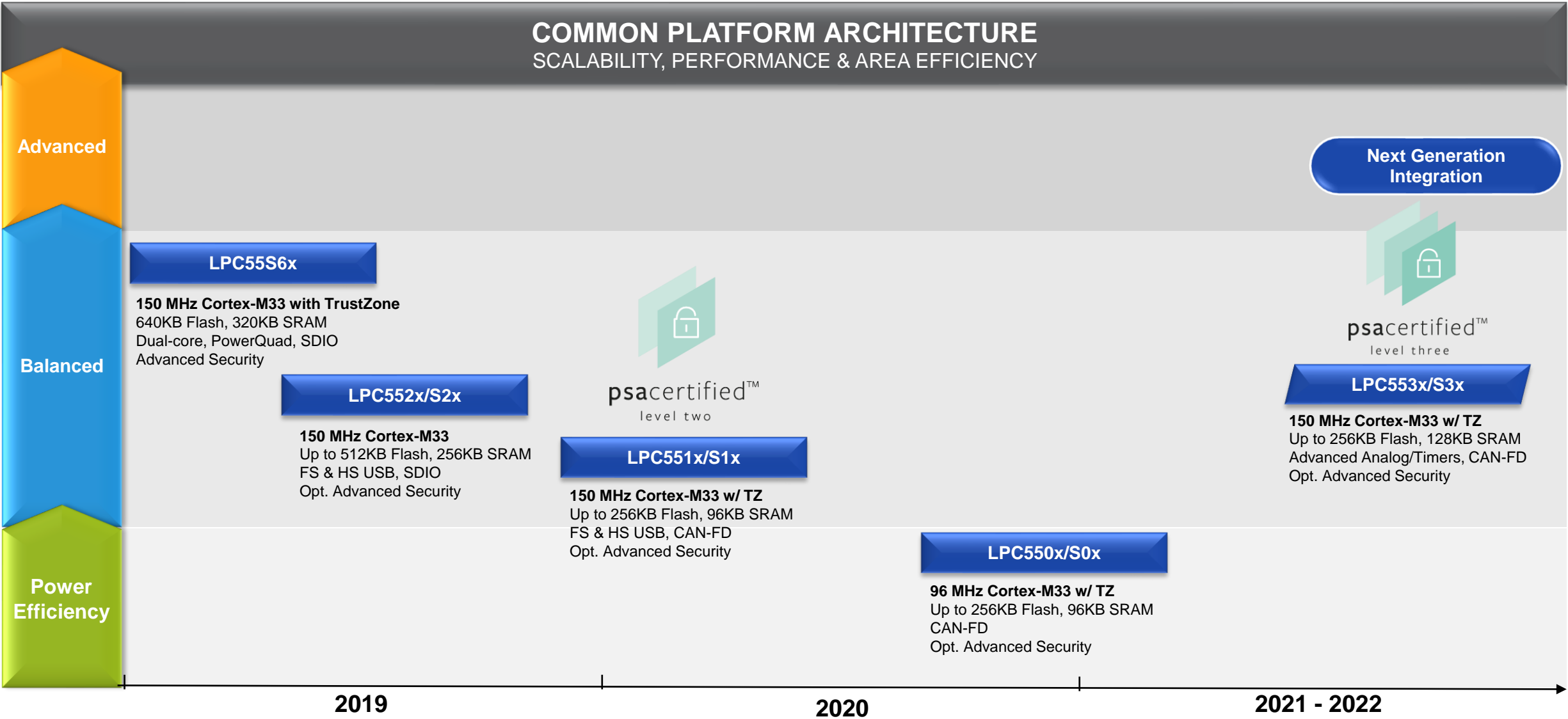
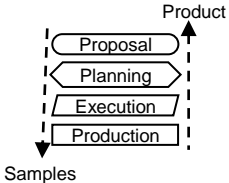
	Cortex-M0+	Cortex-M23	Cortex-M3	Cortex-M4	Cortex-M33
DMIPS/MHz	0.95	0.98	1.25	1.25	1.50
CoreMark®/MHz	2.46	2.50	3.32	3.40	4.02

- Tightly coupled accelerators with coprocessor interface & extensions (Arm’s single precision FPU along with NXP accelerators)
- TrustZone for system-wide, secure resource isolation enabling trusted runtime execution and physical protection in embedded MCU applications

Cortex-M4	Cortex-M33
ETM	TrustZone
NVIC (max 240 IRQs)	Stack limit checking
MPU (PMSAv7)	Co-processor interface
AHB Lite	Enhanced debug
FPU	MTB
SIMD/ DSP	ETM
WIC	NVIC (max 480 IRQs)
Serial wire / JTAG	MPU (PMSAv8)
ARMv7-M	AHB5
	FPU
	SIMD/ DSP
	WIC
	Serial wire / JTAG
	ARMv8-M mainline
	New or updated

LPC5500 MCU SERIES ROADMAP

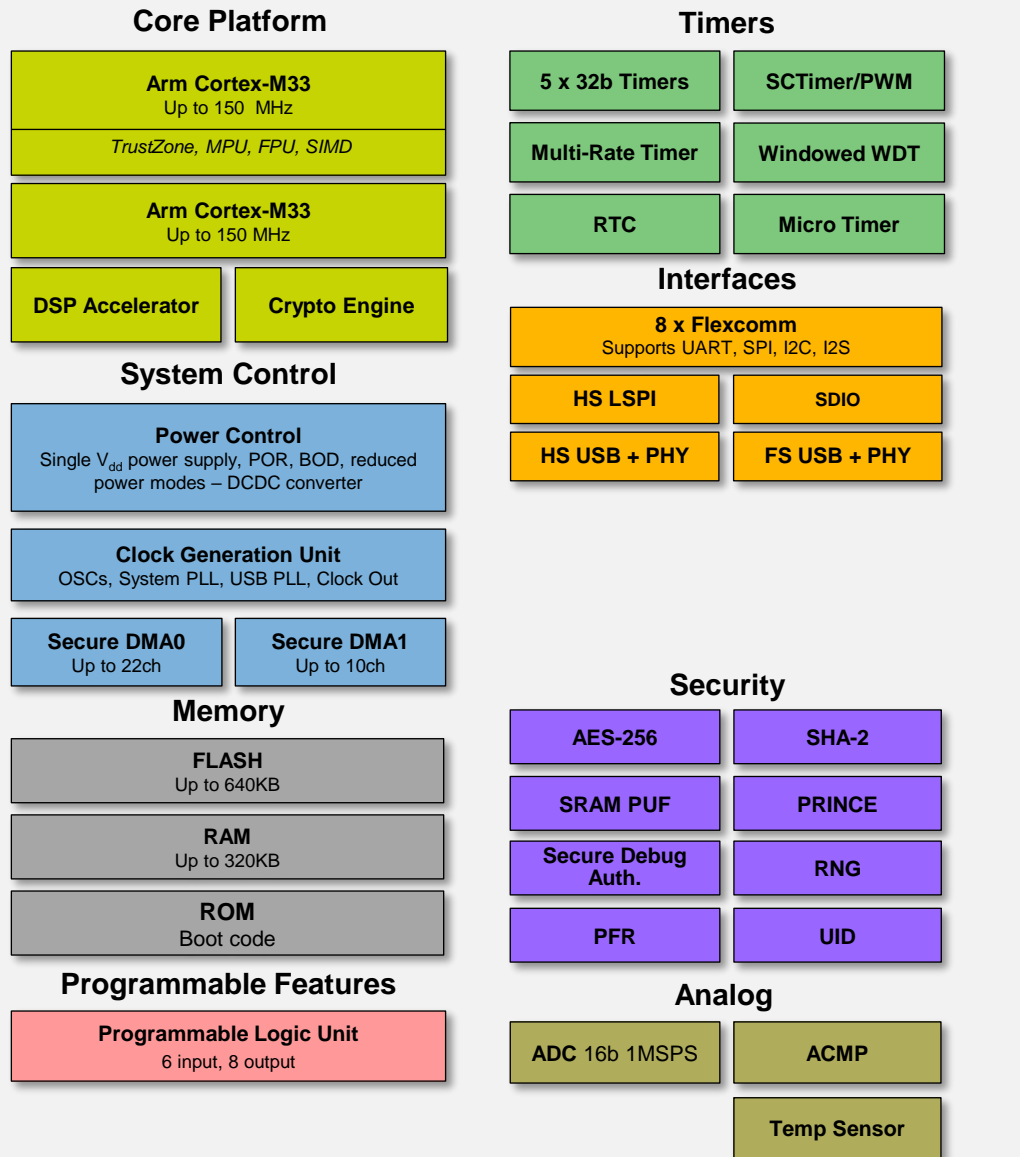
Arm CM7 Arm CM33 Arm CM4



LPC5500 MCU SERIES OVERVIEW

	LPC550x/S0x	LPC551x/S1x	LPC552x/S2x	LPC553x/S3x	LPC55S6x
Cortex-M33 Max Frequency	Up to 96MHz	Up to 150MHz	Up to 150MHz	Up to 150MHz & 8KB Cache	Up to 150MHz (w 2 nd M33)
Accelerators/ Co-processors	Crypto Accelerator	Crypto Accelerator	Crypto Accelerator	PowerQuad DSP, PKC	PowerQuad DSP, Crypto Accelerator
Flash	Up to 256 KB	Up to 256 KB	Up to 512KB	Up to 256KB	Up to 640KB
SRAM	Up to 96KB	Up to 96KB	Up to 256KB	Up to 112kB w Parity + 16kB ECC	Up to 320 KB
Security	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	CSS, TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR
CoreMarks	384	600	600	625	1150+ (Dual-core)
Serial Interfaces	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI
USB	-	USB FS w/PHY	USB FS w/PHY, USB HS w/PHY	USB FS w/PHY	USB FS w/PHY, USB HS w/PHY
SDIO	-	-	SDIO/SD/MMC	-	SDIO/SD/MMC
FlexSPI				Support 2 SPI Flash or 1 Flash + 1 PSRAM	
CAN	CAN FD/ CAN 2.0	CAN FD/CAN 2.0	-	CAN FD/CAN 2.0	-
ADC	2x 16b 2 Msps	2x 16b 2 Msps	2x 16b 1 Msps	4x 16b 2 Msps (4x12b 3.13Msps)	2x 16b 1 Msps
GPIO	Up to 45	Up to 64	Up to 64	Up to 66	Up to 64
Active Power Consumption	32uA/MHz	32uA/MHz	32uA/MHz	57uA/MHz	32uA/MHz
Packages	HTQFP64, HVQFN48	HTQFP64, HLQFP100, VFBGA98	HTQFP64, HLQFP100, VFBGA98	HTQFP64, HLQFP100, QFN48	HTQFP64, HLQFP100, VFBGA98

LPC55S6X BLOCK DIAGRAM



Core Platform

- Dual core Up to 150MHz Cortex-M33
 - Core 0: TrustZone, MPU, FPU, SIMD, DSP
 - Core 1: co-processor w/o extensions
- DSP Accelerator (PowerQUAD, w CP intf)
- CASPER crypto co-processor
- Secure Multilayer Bus Matrix

Memory

- Up to 640KB FLASH bank
- Up to 320KB RAM
- ROM

Timers

- 5 x 32b Timers
- SCTimer/PWM
- Multi-Rate Timer
- Windowed Watchdog Timer
- RTC
- Micro Timer
- OS Event Timer

Analog

- 16b ADC up to 10 ch
- Temperature Sensor
- Analog Comparator

Packages

- VFBGA98, HLQFP64, HLQFP100

Advanced Security

- AES-256 encryption/decryption engine
- SHA-2
- RNG
- mbedTLS library HW accelerated
- SRAM PUF for Key Generation support
- PRINCE real-time Encrypt/Decrypt for flash
- Debug authentication
- Protected Flash Region (PFR)
- Secure GPIO

Interfaces

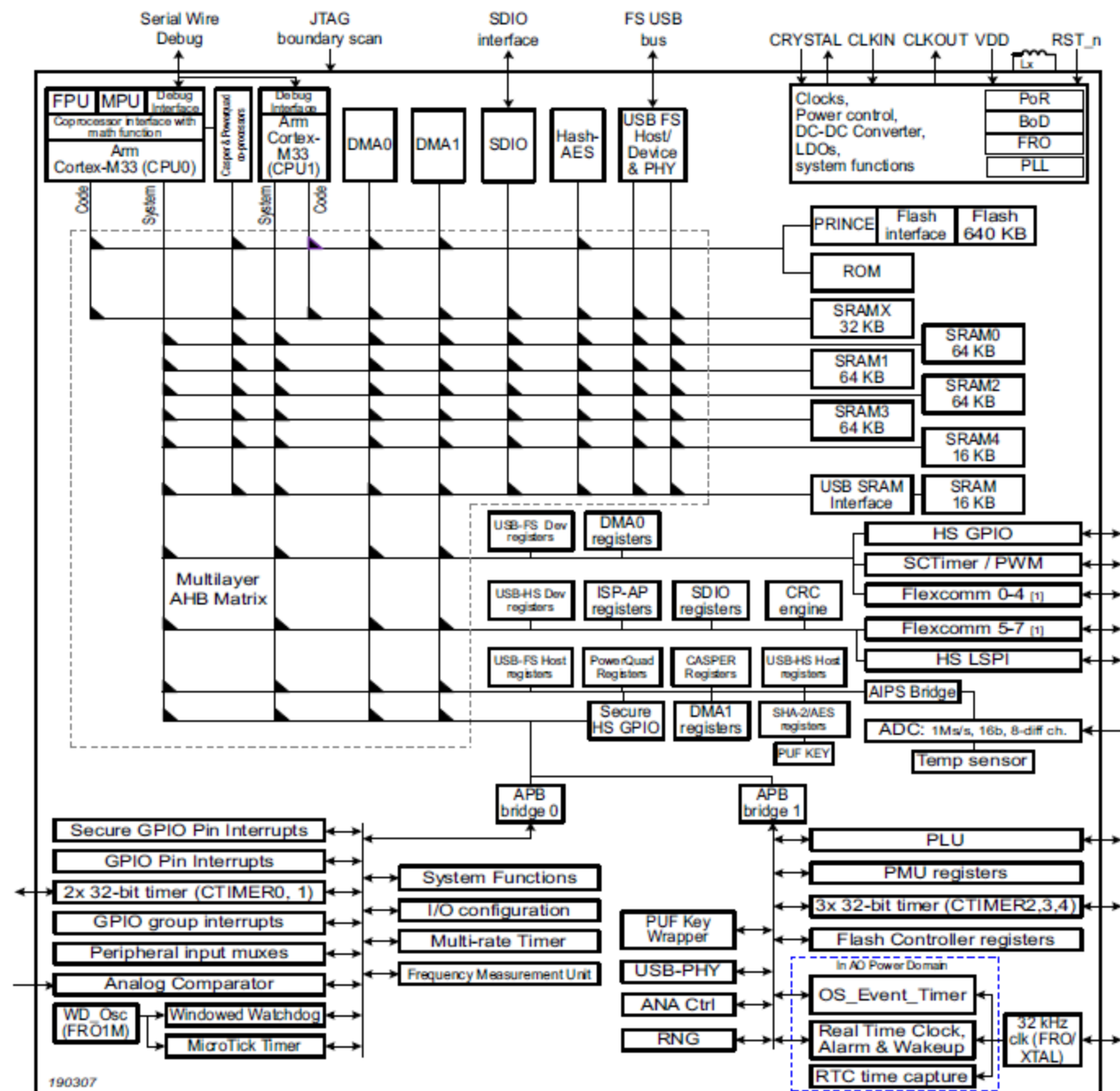
- USB High-speed, on-chip PHY
- USB Full-speed (H/D), Crystal-less, on-chip PHY
- 1 x High-Speed SPI up to 50MHz (HS SPI)
- 8 x Flexcomms each supports SPI, I2C, UART, I²S

Clock generation

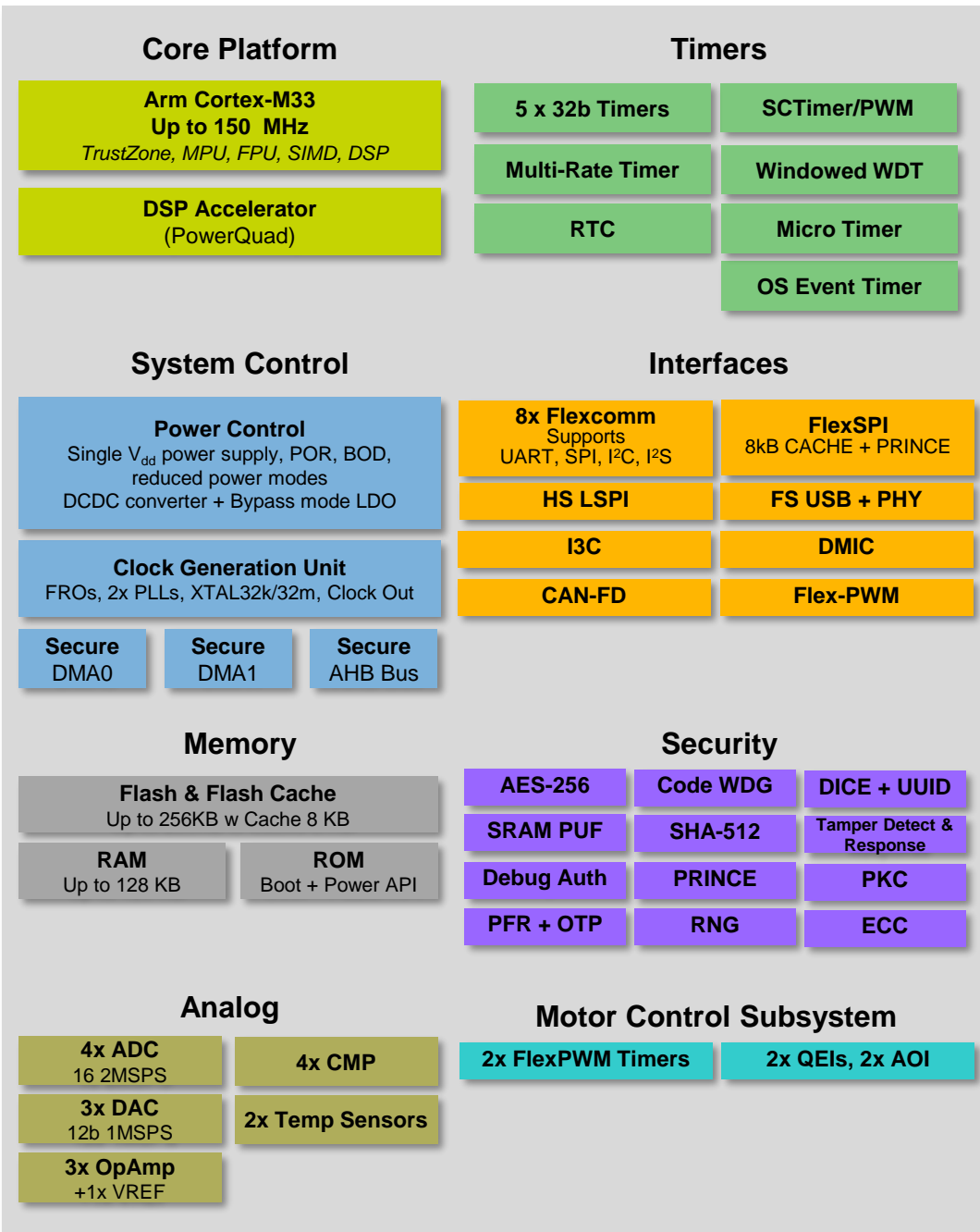
- FRO 96/12MHz - trimmed to +/- 1% accuracy
- FRO 32kHz - trimmed to +/- 1% accuracy
- FRO 1MHz
- XTAL input 1-25MHz
- XTAL input 32 768 Hz
- PLL0/PLL1

Other

- Buck DC-DC
- Operating voltage: 1.8 to 3.6V
- Temperature range: -40 to 105 °C



LPC553X / LPC55S3X BLOCK DIAGRAM



Core Platform

- Up to 150MHz Cortex-M33
 - TrustZone, MPU, FPU, SIMD, DSP
- DSP Accelerator (PowerQUAD, w CP intf)
- Secure Multilayer Bus Matrix

Memory

- Up to 256KB FLASH bank
 - 8kB Low Power Cache
- Up to 128KB RAM
 - 112KB with parity check
 - 16KB ECC RAM
- ROM

Timers

- 5 x 32b Timers
- SCTimer/PWM
- Multi-Rate Timer
- Windowed Watchdog Timer
- RTC with Calendar function
- Micro Timer
- OS Event Timer

Analog

- 4x 16b ADC (Single ended) up to 23 ch
 - 2M sps 16bit
 - 3.3M sps 12bit
 - Up to 8 Differential/ 16 Single Ended channels
- Temperature Sensor
- 3x Analog Comparator
- 3x 12b 1MSPS DAC
- 3x OpAmp

Packages

- HVQFN48, HLQFP64, HLQFP100
 - VFBGA98 and CSP upon request

Advanced Security

- AES-256, SHA-2, RNG
- ECC-256 (ECDSA, ECDH)
- PKC (Math accelerator)
- SRAM PUF for Key Generation support
- PRINCE real-time Encrypt/Decrypt for SPI flash
- Debug authentication
- Protected Flash Region (PFR)
- DICE and UID
- Code Watchdog IP (CodeWDG)
- Anti-tampering and Glitch Detector

Interfaces

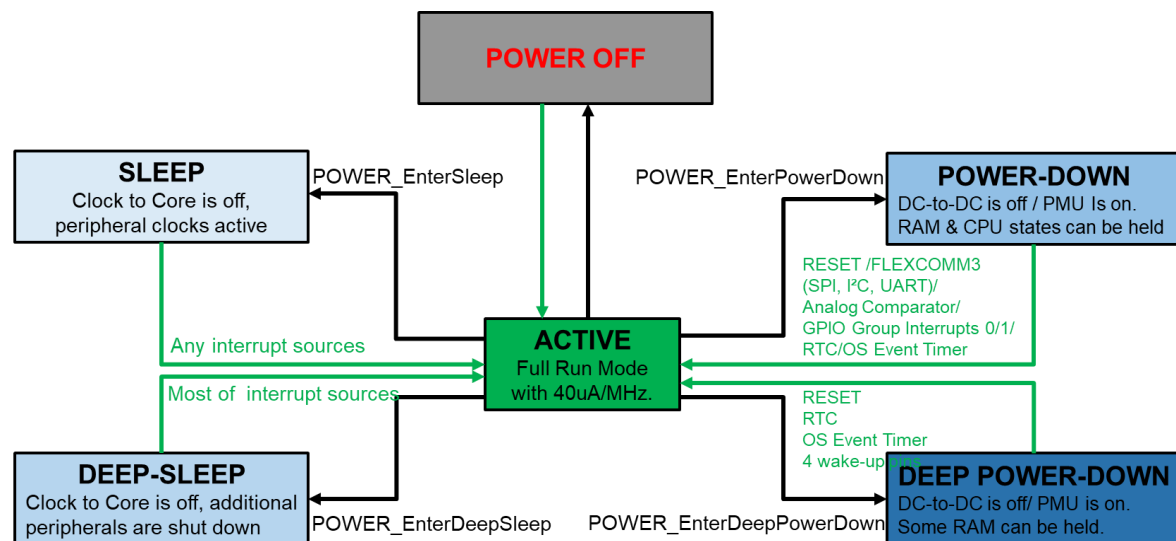
- USB Full-speed (H/D), Crystal-less
- 1 x High-Speed SPI up to 50MHz (HS SPI)
- 8 x Flexcomms each supports SPI, I2C, UART, I2S
 - I2S Pin-sharing
- External SPI -FlexSPI Interface support XIP
 - Octal/Quad Flash
 - with 8kCache
 - PRINCE to encrypt & decrypt on the fly
- 1x CAN-FD
- 1x I3C
- 1x DMIC 2 ch
- 2x FlexPWM with 4 sub-modules, providing 12 PWM outputs
- 2x Quadrature Encoder/Decoder (QEI)

Other

- Buck DC-DC
- Operating voltage: 1.8 to 3.6V
- Two Main IO supplies (VDDIO_1: 1.8 V to 3.6 V, VDDIO_2: 1.08 v to 3.6 V).
- Temperature range: -40 to 105 °C

NXP LPC5500 MCU SERIES

POWER MODES



Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
ARM Cortex-M33 (CPU0) in active mode; ARM Cortex-M33 (CPU1) in sleep mode						
I _{DD}	supply current	CoreMark code executed from SRAMX; flash powered down				
		CCLK = 12 MHz	[2][3][3]	0.9	-	mA
		CCLK = 48 MHz	[2][3][3]	2.1	-	mA
		CCLK = 60 MHz	[2][3][3]	2.3	-	mA
		CCLK = 96 MHz	[2][3][3]	3.4	-	mA
		CCLK = 100 MHz	[3][3][4]	3.5	-	mA
		CCLK = 150 MHz	[3][3][4]	6.2	-	mA

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
ARM Cortex-M33 (CPU0) in sleep mode; ARM Cortex-M33 (CPU1) OFF (in reset, clock disabled)						
I _{DD}	supply current	CCLK = 12 MHz, PLL disabled	[1][2]	0.7	-	mA
		CCLK = 96 MHz, PLL disabled	[2][3]	2.7	-	mA

Symbol	Parameter	Conditions	Min	Typ ^{[1][2]}	Max ^[3]	Unit
I _{DD}	supply current	Deep-sleep mode; all SRAM on	[2]			
		T _{amb} = 25 °C, VBAT_DCDC = 3.0 v	-	110	135	μA
		T _{amb} = 25 °C, VBAT_DCDC = 1.8 v	[2]	148	191	μA
		T _{amb} = 105 °C, VBAT_DCDC = 3.0 v	-	-	<tbd>	μA
		Power-down mode.	[2]			
		SRAM_X2 (4 KB) powered				
		T _{amb} = 25 °C, VBAT_DCDC = 3.0 v	-	3.9	4.5	μA
		SRAM_X2 (4 KB) powered				
		T _{amb} = 105 °C, VBAT_DCDC = 3.0 v	-	-	<tbd>	μA
		SRAM_X2 and SRAM_X3 (8 KB) powered				
		T _{amb} = 25 °C, VBAT_DCDC = 3.0 v	-	4.0	-	μA
		320 KB full retention				
		T _{amb} = 25 °C, VBAT_DCDC = 3.0 v	-	13	15	μA
		320 KB full retention				
		T _{amb} = 105 °C, VBAT_DCDC = 3.0 v	-	-	<tbd>	μA
		Deep power-down mode;	[2]			
		RTC oscillator input grounded (RTC oscillator disabled, 4 KB SRAM powered)				
		T _{amb} = 25 °C. VBAT_DCDC = 3.0 v	-	590	750	nA
		T _{amb} = 105 °C, VBAT_DCDC = 3.0 v	-	-	<tbd>	μA
		RTC oscillator running with external crystal (4 KB SRAM powered)	-	790	-	nA

SDK & Ecosystem



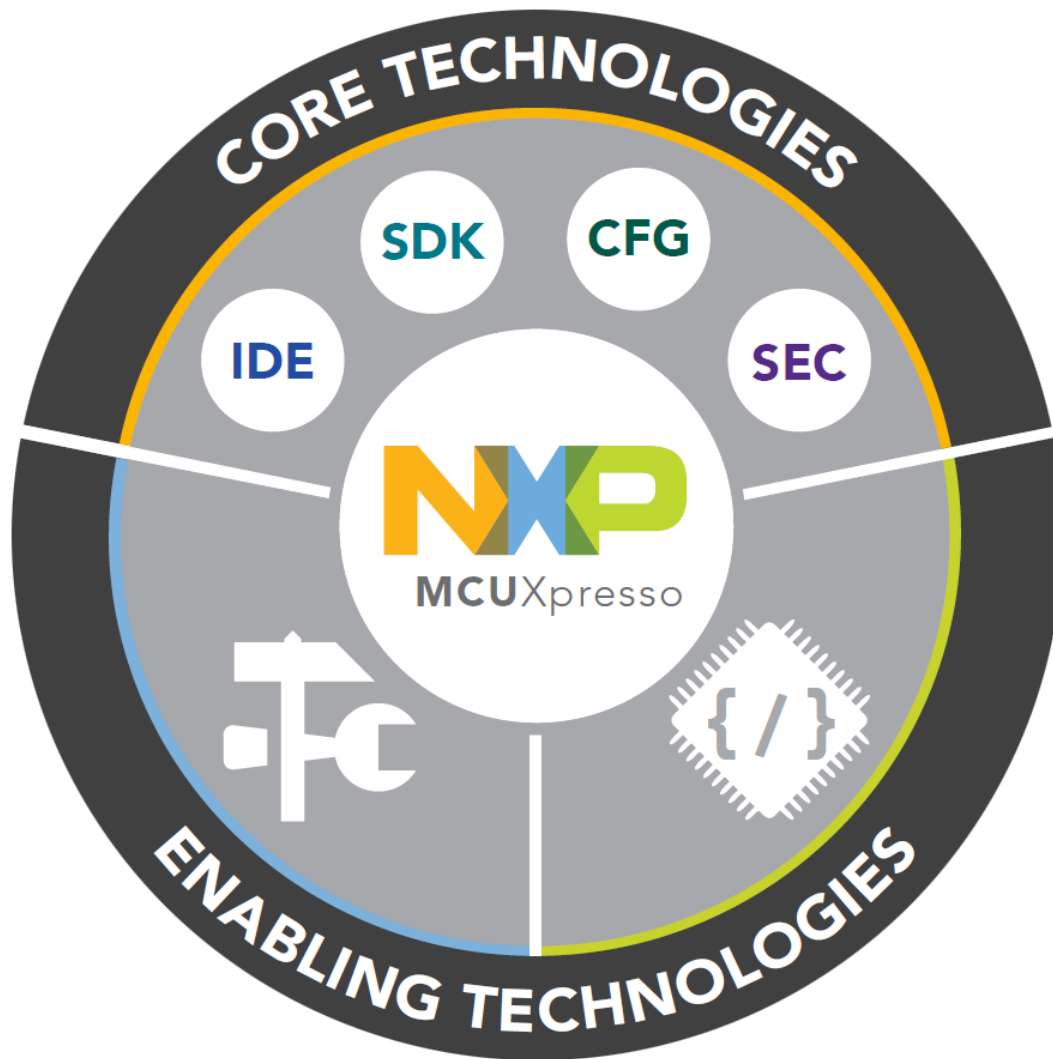
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THE MCUXPRESSO ECOSYSTEM



> Core Technologies from NXP

- MCUXpresso SDK
- MCUXpresso Config Tools
- For Arm® Cortex-M®
 - MCUXpresso IDE
 - MCUXpresso Secure Provisioning Tool

> Enabling Software Technologies

- Run time software libraries and middleware
- Enable customers to focus on differentiation
- From NXP and partners

> Enabling Tools Technologies

- Partner IDEs
- Debug Probes
- Development Boards
- From NXP and partners

MCUXpresso Software and Tools

UNIFIED SUITE OF
TOOLS FOR EASY
DEVELOPMENT
WITH NXP MCUs



LEARN MORE >



MCUXpresso Software and Tools

for General Purpose MCUs and Crossover processors



MCUXpresso IDE

Edit, compile, debug and optimize in an intuitive and powerful IDE



MCUXpresso SDK

Runtime software including peripheral drivers, middleware, RTOS, demos and more



MCUXpresso Config Tools

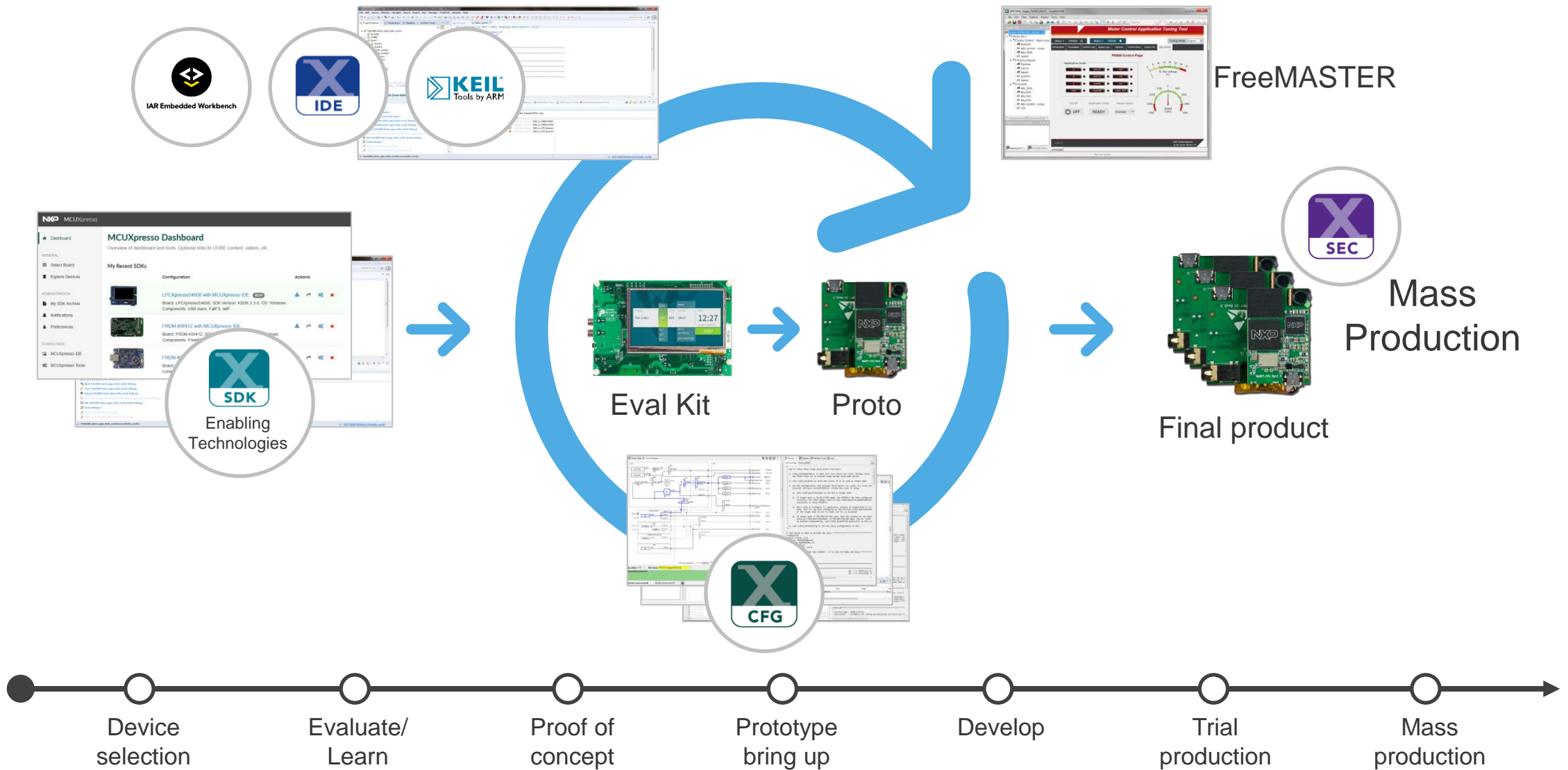
Online and desktop tool suite for system configuration and optimization



MCUXpresso Secure Provisioning Tool

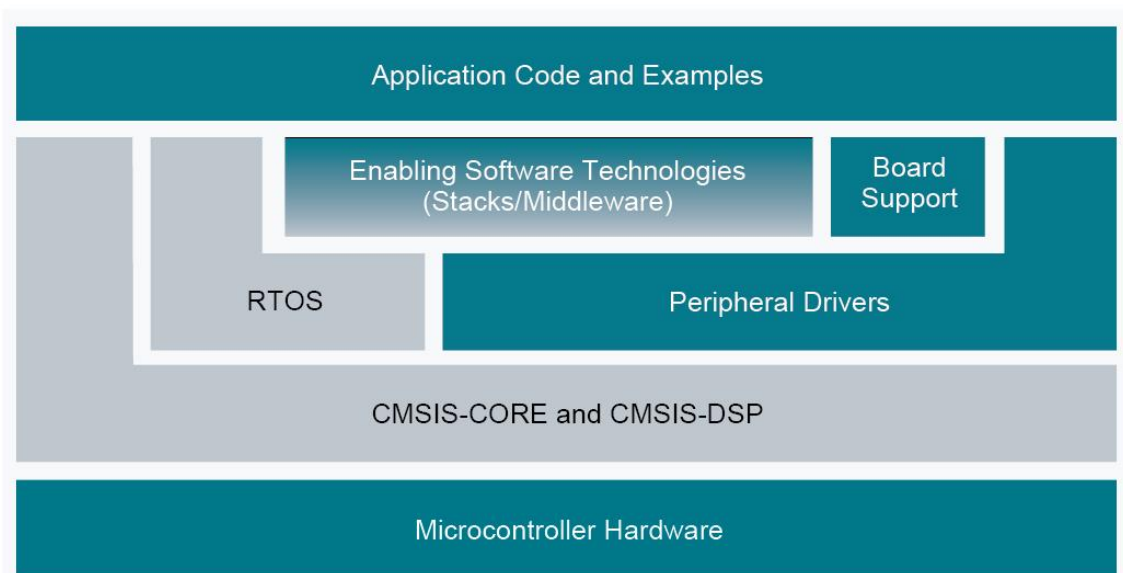
Graphical and command line tool for securely provisioning and programming MCUs with secure boot

STREAMLINED MCUXPRESSO DEVELOPMENT FLOW



MCUXPRESSO SDK

SOFTWARE FRAMEWORK AND DRIVERS



Architecture:

- CMSIS-CORE compatible
- Single driver for each peripheral
- Transactional APIs w/ optional DMA support for communication peripherals

Integrated RTOS options:

- Azure RTOS ThreadX
- FreeRTOS
- RTOS-native driver wrappers

Enabling SW Technologies:

- Connectivity (wired/wireless)
- HMI (Graphics, Voice, Touch)
- Audio
- Motor Control
- eIQ Machine Learning
- Cloud connectivity
- Accelerators and specialized peripherals
- Safety
- Security
- Storage

Reference Software:

- Peripheral driver usage examples
- Application demos
- Azure RTOS and FreeRTOS usage demos
- IoT connectivity examples

License:

- BSD 3-clause for startup, drivers, USB stack
- All code Black Duck scanned

Download options:

- Custom SDK web builder for optimized download size
- Direct download within MCUXpresso
- GitHub repository leveraging community engagement
- CMSIS Packs for supported toolchains

Toolchains:

- MCUXpresso IDE
- IAR®, ARM® Keil®, GCC w/ Cmake

Quality:

- Production-grade software
- Consistent API architecture across all releases
- MISRA 2012 compliance
- Checked with Coverity® static analysis tools
- Extensive Continuous Integration testing across range of compatible development boards, supported toolchains, and debug probes

MCUXpresso Tools Install



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MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- Install MCUXpresso IDE

www.nxp.com/mcuxpresso

MCUXpresso Integrated Development Environment (IDE)

MCUXpresso-IDE [Receive alerts](#)

[Overview](#) [Software Details](#) [Documentation](#) [Design Resources](#) [Training](#) [Support](#)

DOWNLOADS

Core Technologies

MCUXpresso SDK

Software development kit (SDK)

An open source software development kit (SDK) built

MCUXpresso IDE

Integrated development environment (IDE)

An easy-to-use integrated development environment (IDE) for creating, building, debugging and optimizing your application.

MCUXpresso Config Tools

System configuration tools

A comprehensive suite of system configuration tools, including pins, clocks, peripherals and more.

MCUXpresso Secure Provisioning Tool

Secure Provisioning

A tool designed for secure provisioning, generation and management of keys, signatures and certificates.

“MCUXpresso IDE includes Config Tools and SDK download Option inside”

- Install MCUXpresso Config Tools stand Alone (Optional)

MCUXpresso Config Tools - Pins, Clocks, Peripherals

MCUXpresso-Config-Tools [Receive alerts](#)

[Overview](#) [Software Details](#) [Documentation](#) [Design Resources](#) [Training](#) [Support](#)

DOWNLOADS

- Download MCUXpresso SDK (Optional)

MCUXpresso Software Development Kit (SDK)

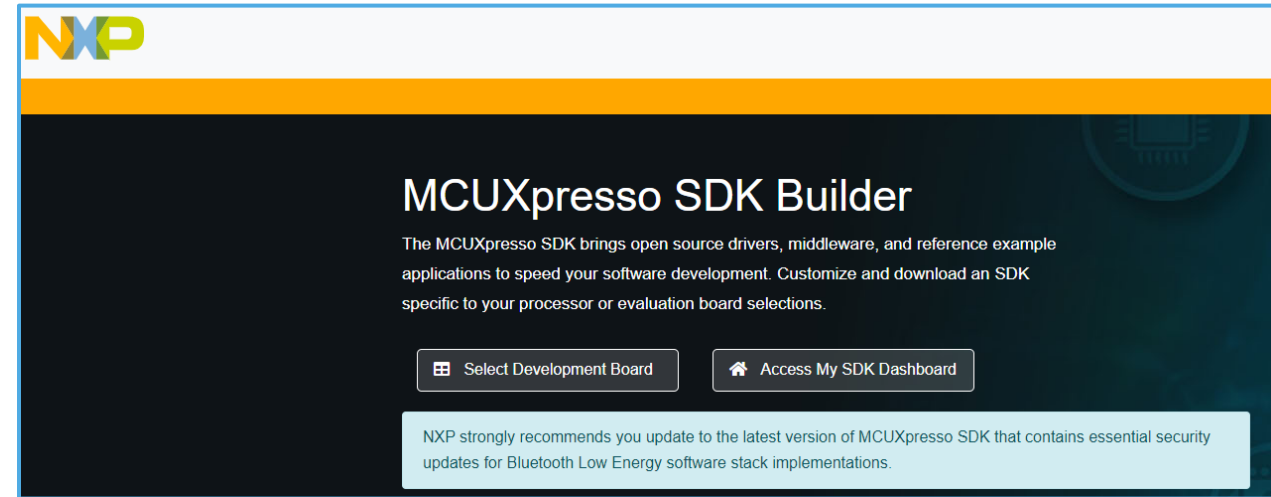
MCUXpresso-SDK [Receive alerts](#)

[Overview](#) [Software Details](#) [Documentation](#) [Design Resources](#) [Training](#) [Support](#)

DOWNLOADS

MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- MCUXpresso SDK Builder
- <https://mcuxpresso.nxp.com/en/welcome>



Select Development Board

Search for your board or kit to get started.

Search for Hardware

lpc55s6



Select a Board, Kit, or Processor

LPCXpresso55S69 (LPC55S69)

Selection Details



LPCXpresso55S69



LPCXpresso Development Board for LPC55S6x family of MCUs

Build MCUXpresso SDK

v2.12.0

Board Configuration

MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- Download SDK

Build SDK for LPCXpresso55S69

Generate a downloadable SDK archive for use with desktop MCUXpresso Tools.

Developer Environment Settings

Selections here (operating host system, toolchain or middleware) will impact files and examples projects included in the SDK and Generated Projects

Host OS



Toolchain / IDE



SDK Version

2.12.0 (released 2022-07-14)

SDK Tag

REL_2.12.0_MAJOR_RFP



Search...



SELECT ALL


UNSELECT ALL

	Name	Category	Description	Dependencies
<input checked="" type="checkbox"/>	multicore	Middleware	Multicore Software Development Kit	
<input checked="" type="checkbox"/>	SDMMC Stack	Middleware	Stack supporting SD, MMC, SDIO	
<input checked="" type="checkbox"/>	CMSIS DSP Library	CMSIS DSP Lib	CMSIS DSP Software Library	
<input checked="" type="checkbox"/>	Embedded Wizard GUI	Middleware	Embedded Wizard GUI from TARA Systems	
<input checked="" type="checkbox"/>	emWin	Middleware	emWin graphics library	
<input checked="" type="checkbox"/>	Essential Audio Processing Library	Middleware	Essential Audio Processing Library (EAP) provides audio proc... (more)	
<input checked="" type="checkbox"/>	Fatfs	Middleware	FAT File System stack	
<input checked="" type="checkbox"/>	Azure RTOS (7 selected)		Azure RTOS	
<input checked="" type="checkbox"/>	FreeRTOS (2 selected)		Real-time operating system for microcontrollers from Amazon	

DOWNLOAD SDK

MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

• Download SDK



SDK_2.12.0_LPCXpresso55S69

2022-11-14

Remove SDK

Rebuild SDK

Config Tools

Share SDK

Download SDK

Windows

All Toolchains

2.12.0

NXP.com

LPCXpresso55S69

REL_2.12.0_MAJOR_RFP

CMSIS DSP Library, USB Type-C PD Stack, USB Host, Device, OTG Stack, SDMMC Stack, multicore, MCUboot, mbedTLS, Maestro Audio Framework for MCU, LVGL, FreeRTOS, Fatfs, emWin, Embedded Wizard GUI, Essential Audio Processing Library, AWS IoT Core, FreeMASTER, Nxp iot sensing sdk, Azure RTOS, Azure RTOS ThreadX, Azure RTOS FileX, Azure RTOS GUIX, Azure RTOS LevelX, Azure RTOS NetX Duo, Azure RTOS USBX, Azure RTOS IoT, Motor Control Software, Secure Element Host Library, MW320 Wi-Fi co-processor support, TF-M, PSA Test Suite, Mbed Crypto, NTAG I2C

Downloads

MCUXpresso SDK

[Download SDK Archive \(127 MB\)](#)

[Download SDK Documentation](#)

[Download Standalone Example Project](#)

Additional Tools

Download additional tools from NXP or its partners to create new projects and modify example projects using the associated software components included in this SDK.

[MCUXpresso SDK for Motor Control](#)

Online Documentation

[View SDK API Reference Manual](#)

MCUXpresso Config Tools

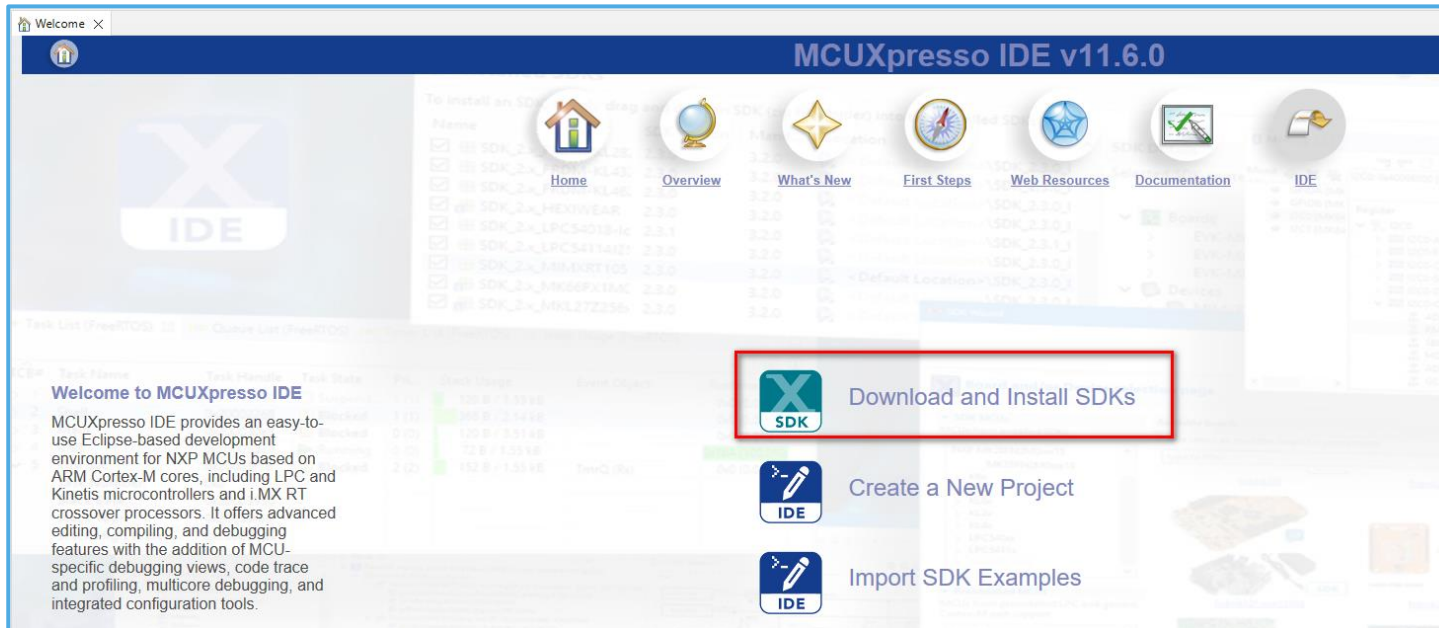
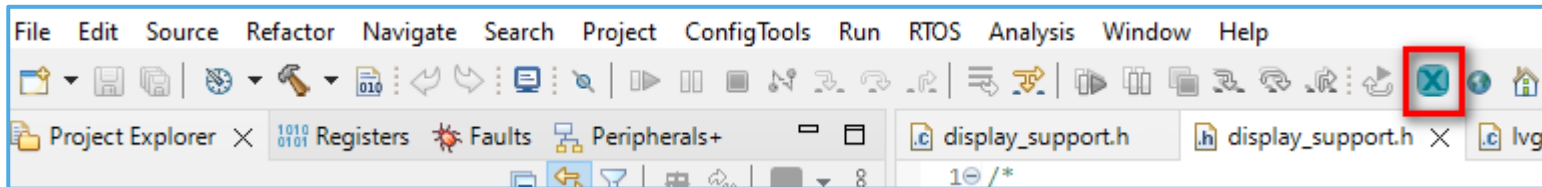
[Download Config Tools Data](#)

Name

- boards
- CMSIS
- components
- devices
- docs
- middleware
- rtos
- tools
- COPYING-BSD-3
- LA_OPT_NXP_Software_License RTAudio.txt
- LPCXpresso55S36_manifest_v3_8.xml
- SW-Content-Register.txt




MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- Install SDK inside the IDE



MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- Filter: “55s6”
- Select the Board

Board	SDK	Version	Package	Flash	RAM	Status
 lpcpresso55s69	SDK_2.x_LPCXpresso5...	2.12.0	LPC55S69JBD100	630	304	
 lpcpresso55s69_om13790dock	SDK_2.x_LPCXpresso5...	2.12.0	LPC55S69JBD100	630	304	
 lpcpresso55s69_om13790host	SDK_2.x_LPCXpresso5...	2.12.0	LPC55S69JBD100	630	304	

Filter: 55s6

☐ Hide Installed ☒ Show latest ☐ Hide board images

Min Flash (KB): 0
Max Flash (KB): 4096

Min RAM (KB): 0
Max RAM (KB): 5120

☐ External Flash

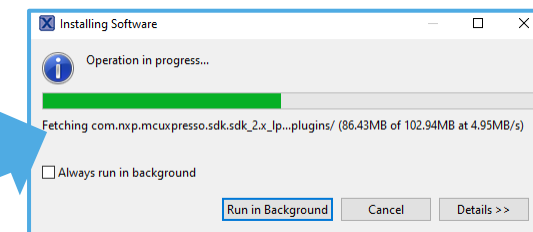
Cores

☐ Multicore

☒ All Cores ☐ Cortex-M0+ ☐ Cortex-M33
☐ Cortex-M4 ☐ Cortex-M7

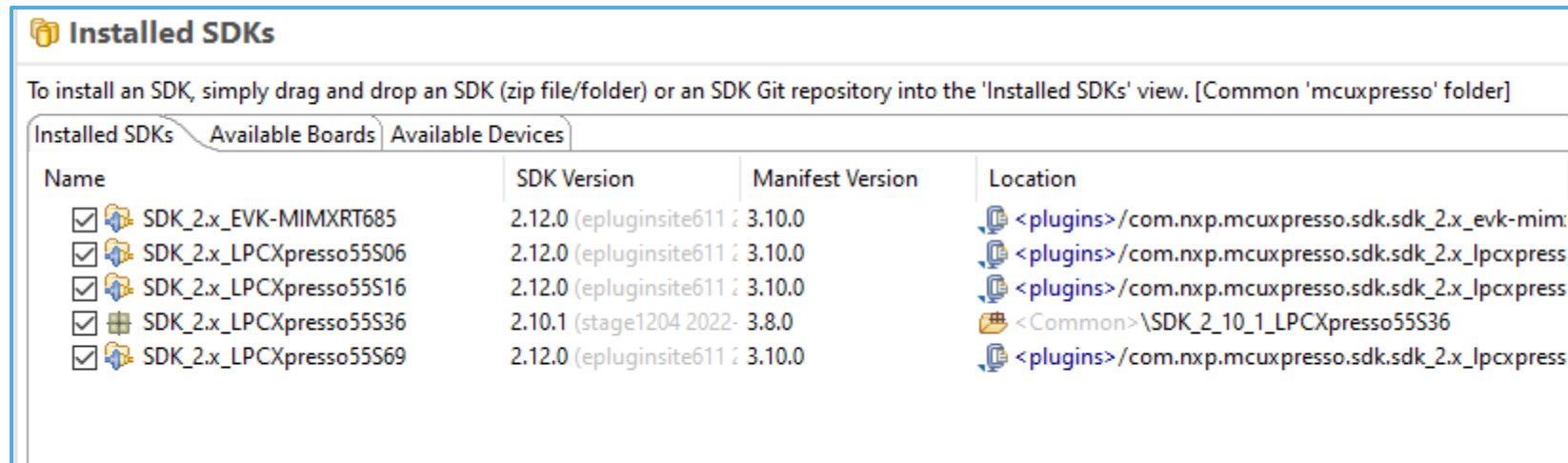
- Install

Install and Create Project Install and Import Examples **Install** Uninstall Cancel



MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

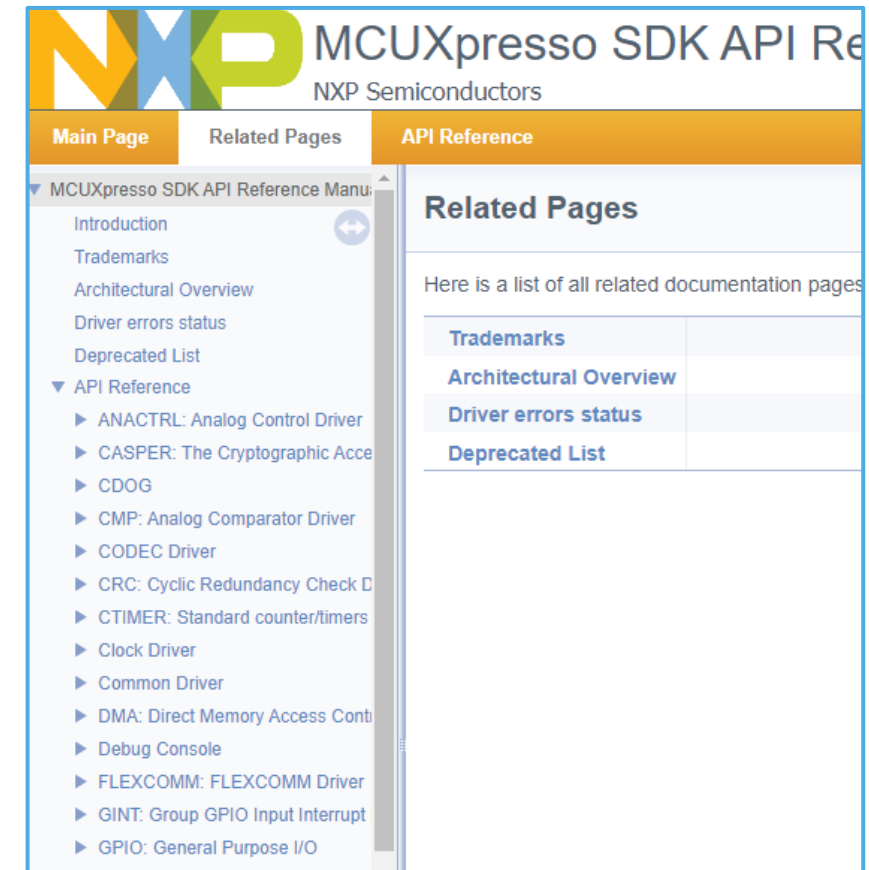
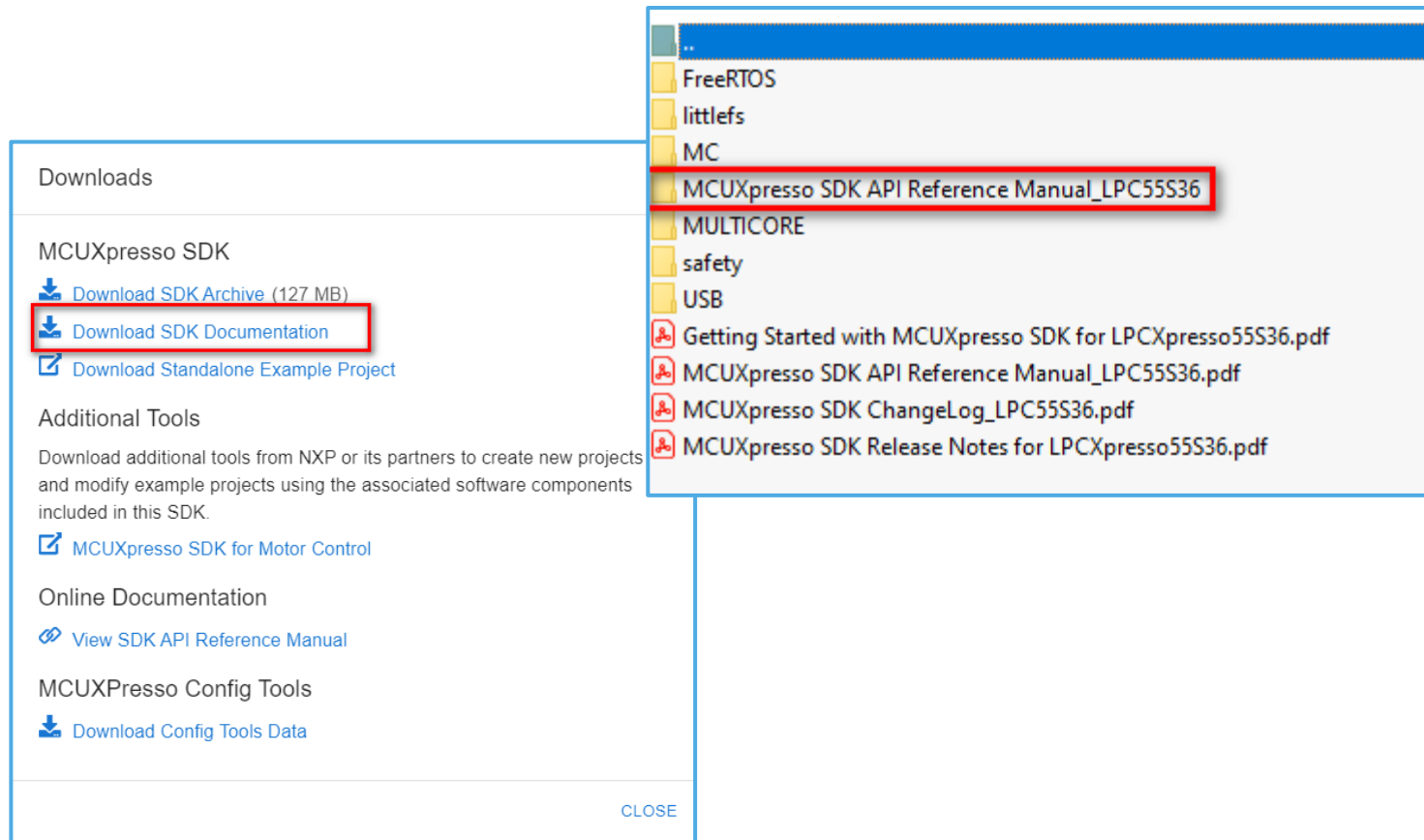
- Installed SDKs View



Name	SDK Version	Manifest Version	Location
<input checked="" type="checkbox"/> SDK_2.x_EVK-MIMXRT685	2.12.0 (epluginsite611 ↗ 3.10.0		<plugins>/com.nxp.mcuxpresso.sdk.sdk_2.x_evk-mim:
<input checked="" type="checkbox"/> SDK_2.x_LPCXpresso55S06	2.12.0 (epluginsite611 ↗ 3.10.0		<plugins>/com.nxp.mcuxpresso.sdk.sdk_2.x_lpcxpress
<input checked="" type="checkbox"/> SDK_2.x_LPCXpresso55S16	2.12.0 (epluginsite611 ↗ 3.10.0		<plugins>/com.nxp.mcuxpresso.sdk.sdk_2.x_lpcxpress
<input checked="" type="checkbox"/> SDK_2.x_LPCXpresso55S36	2.10.1 (stage1204 2022- 3.8.0		<Common>\SDK_2_10_1_LPCXpresso55S36
<input checked="" type="checkbox"/> SDK_2.x_LPCXpresso55S69	2.12.0 (epluginsite611 ↗ 3.10.0		<plugins>/com.nxp.mcuxpresso.sdk.sdk_2.x_lpcxpress

MCUXPRESSO SDK API

- Importing Demo code drivers will help to understand how to use API drivers.
- Download SDK Documentation



Project Import



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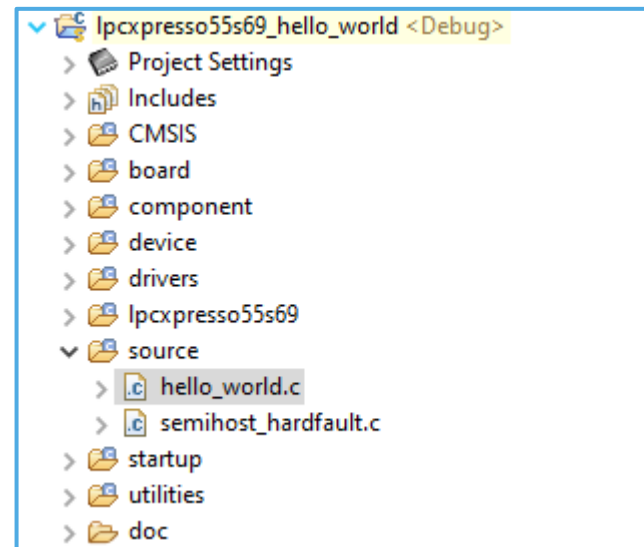
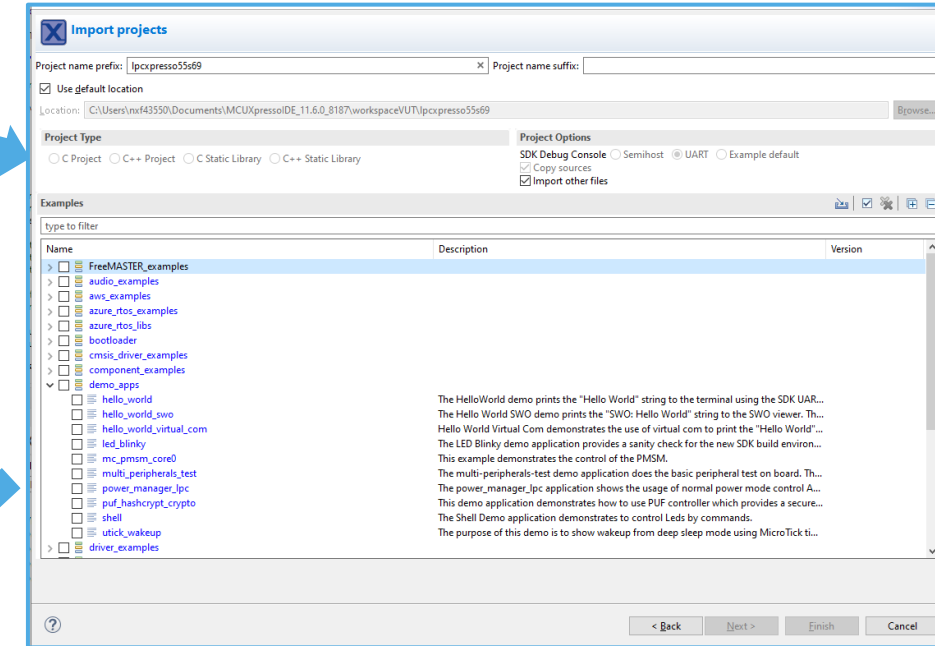
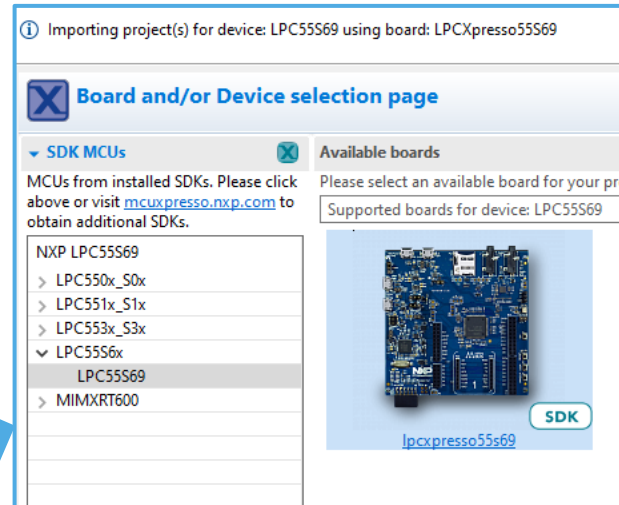
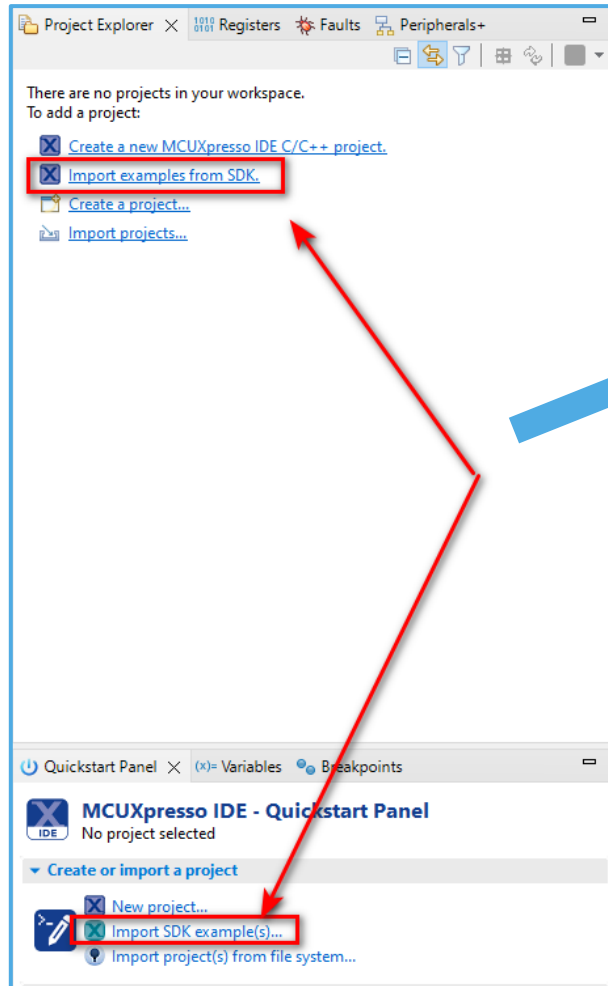
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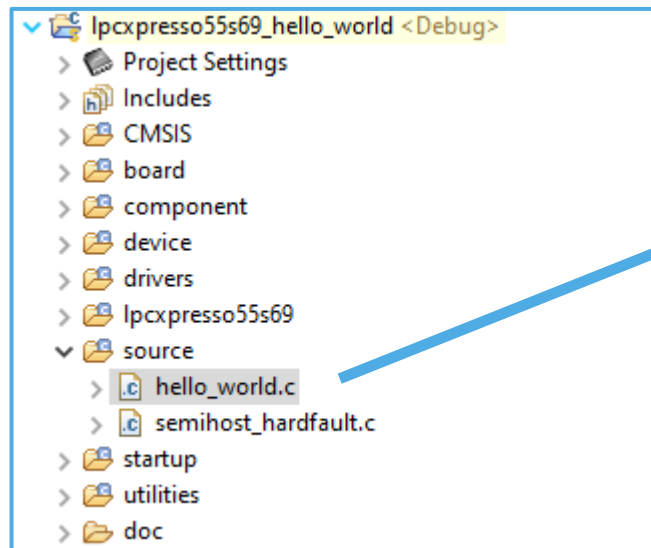
MCUXPRESSO PROJECT IMPORT

• Import Example from SDK



MCUXPRESSO PROJECT IMPORT

- Basic Baremetal Project



```
int main(void)
{
    char ch;

    /* Init board hardware. */
    /* set BOD VBAT level to 1.65V */
    POWER_SetBodVbatLevel(kPOWER_BodVbatLevel1650mv, kPOWER_BodHystLevel50mv, false);
    /* attach main clock divide to FLEXCOMM0 (debug console) */
    CLOCK_AttachClk(BOARD_DEBUG_UART_CLK_ATTACH);

    BOARD_InitBootPins();
    BOARD_InitBootClocks();
    BOARD_InitDebugConsole();
    #if !defined(DONT_ENABLE_FLASH_PREFETCH)
    /* enable flash prefetch for better performance */
    SYSCON->FMCCR |= SYSCON_FMCCR_PREFEN_MASK;
    #endif

    PRINTF("hello world.\r\n");

    while (1)
    {
        ch = GETCHAR();
        PUTCHAR(ch);
    }
}
```

Project Main Settings review



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PROJECT SETTINGS

- Expand Project Settings in the Project Folder

Project Settings

- Associated SDK
 - name = 'SDK_2.x_LPCXpresso55S69'
 - version = '2.12.0'
- Libraries (and semihosting)
 - Library (C) = 'Redlib (nohost-nf)'
- MCU
 - chip = 'LPC55S69'
 - core = 'cm33_core0_LPC55S69'
 - package = 'LPC55S69JBD100'
 - processor = 'cm33'
- Memory
 - Flash name='PROGRAM_FLASH' type='Flash' address='0x0' size='0x9d800' LPC55xx.cfx
 - RAM2 name='SRAMX' type='RAM' address='0x4000000' size='0x8000'
 - RAM3 name='USB_RAM' type='RAM' address='0x40100000' size='0x4000'
 - RAM4 name='SRAM4' type='RAM' address='0x20040000' size='0x4000'
 - RAM name='SRAM' type='RAM' address='0x20000000' size='0x40000'
- Options
 - Defined symbols (-D) (C) = ['_REDLIB_', CPU_LPC55S69JBD100, CPU_LPC55S69JBD100_cm33, CPU_LPC55S69JBD100_cm33_core0, MCUXPRESSO_SDK, SDK_DEBUGCONSOLE=1, CR_INTEGER_PRINTF, PRINTF_FLOAT_ENABLE=0, __MCUXPRESSO, __USE_CMSIS, DEBUG']

MCUXpresso IDE

Memory configuration editor

Edit configuration for LPC55S69

Memory configuration

Default LinkServer Flash Driver Browse...

Type	Name	Alias	Location	Size	Driver
Flash	PROGRA...	Flash	0x0	0x9d800	LPC55xx.cfx
RAM	SRAM	RAM	0x20000000	0x40000	
RAM	SRAMX	RAM2	0x4000000	0x8000	
RAM	USB_RAM	RAM3	0x40100000	0x4000	
RAM	SRAM4	RAM4	0x20040000	0x4000	

Add Flash Add RAM Split Join Delete Import... Merge... Export... Generate...

OK Cancel

PROJECT SETTINGS

- Managed Linker Script

Properties for lpcxpresso55s36_hello_world

type filter text

- > Resource
- Builders
- > C/C++ Build
 - Build Variables
 - Environment
 - Logging
 - MCU settings
 - Settings
 - Tool Chain Editor
- > C/C++ General
- MCUXpresso Config Tools
- Project Natures
- Project References
- > Run/Debug Settings
- Task Tags
- > Validation

Settings

Configuration: Debug [Active] Manage Configurations...

Tool Settings | Build steps | Build Artifact | Binary Parsers | Error Parsers

- > MCU C Compiler
 - Dialect
 - Preprocessor
 - Includes
 - Optimization
 - Debugging
 - Warnings
 - Miscellaneous
 - Architecture
 - TrustZone
- > MCU Assembler
 - General
 - Architecture & Headers
- > MCU Linker
 - General
 - Libraries
 - Miscellaneous
 - Shared Library Settings
 - Architecture
 - Managed Linker Script
 - Multicore
 - TrustZone
- > MCU Debugger
 - Debug
 - Miscellaneous

☒ Manage linker script

Linker script: lpcxpresso55s36_hello_world_Debug.ld

Script path:

Library: Redlib (nohost-nf)

☐ Enable printf float

☐ Enable scanf float

☐ Link application to RAM

☐ Plain load image: SRAM

Heap and Stack placement: MCUXpresso Style

Stack offset: 0

	Region	Location	Size
Heap	Default	Post Data	Default
Stack	Default	End	Default

Global data placement: Default

Extra linker script input sections + x

Input section description	Region	Section Type

Restore Defaults Apply

Apply and Close Cancel

Project SDK Components



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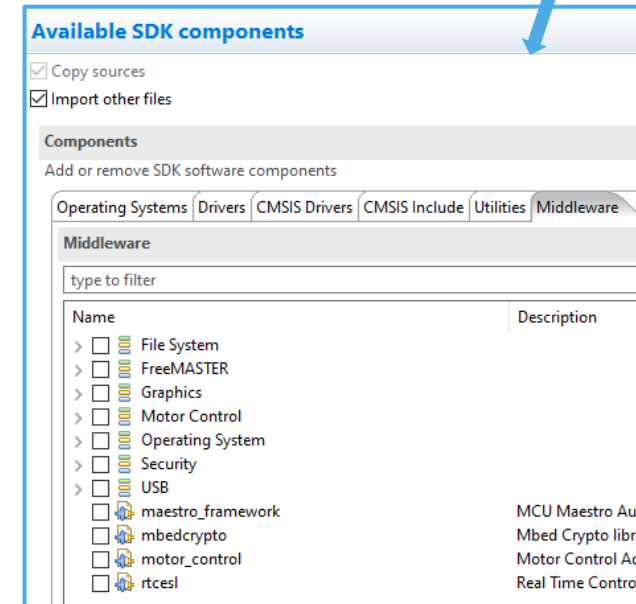
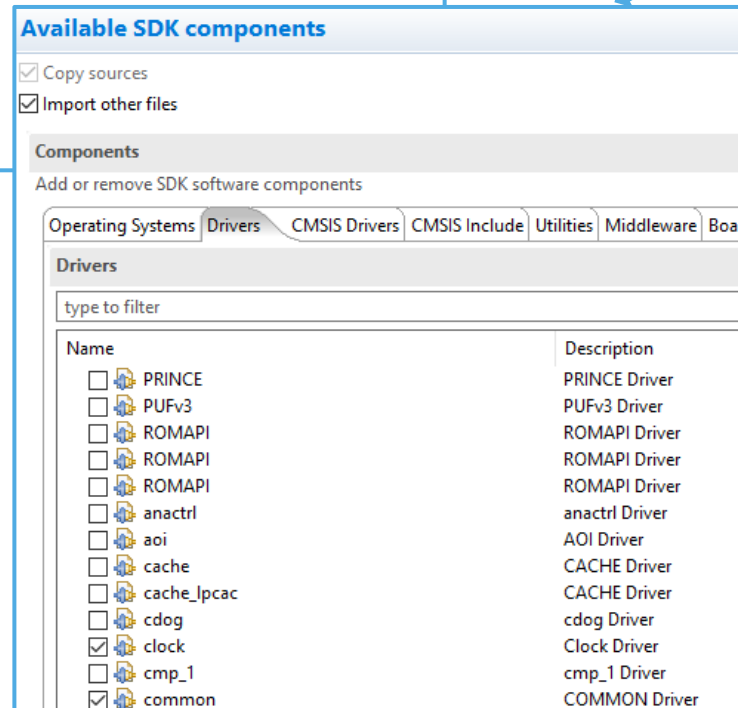
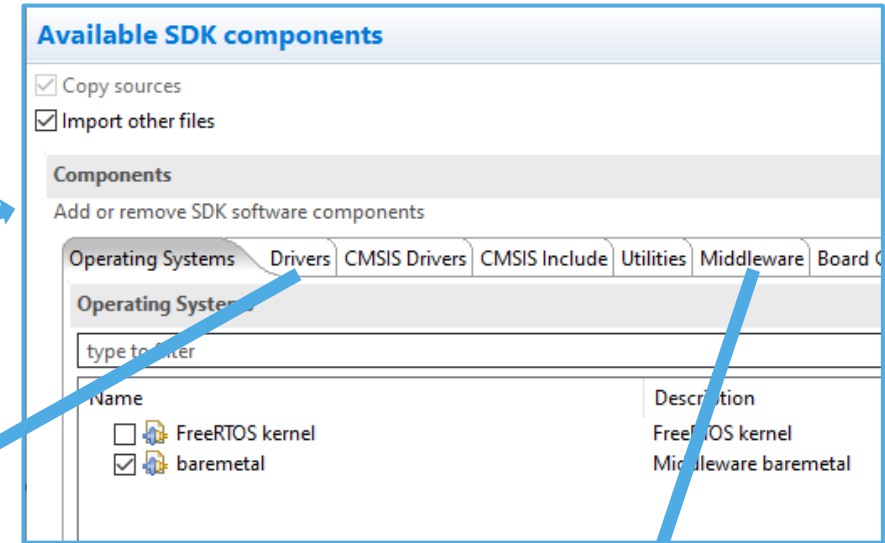
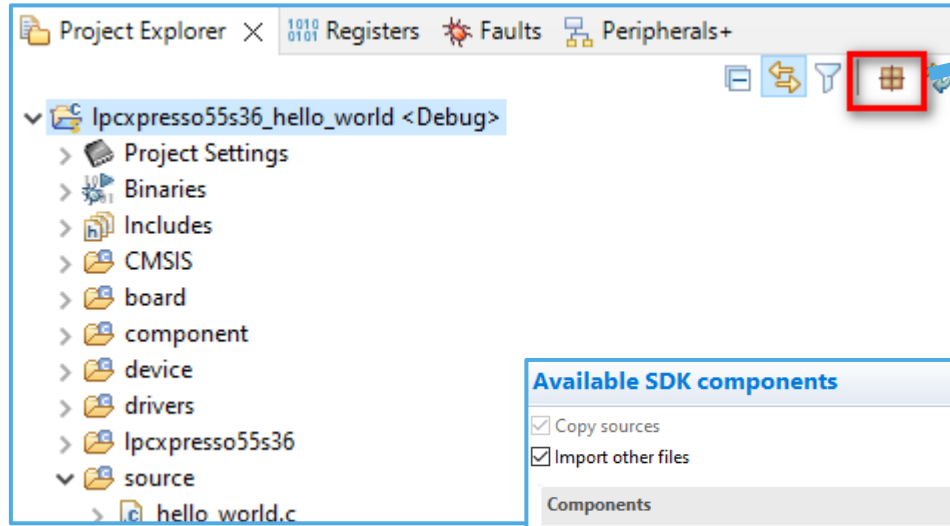
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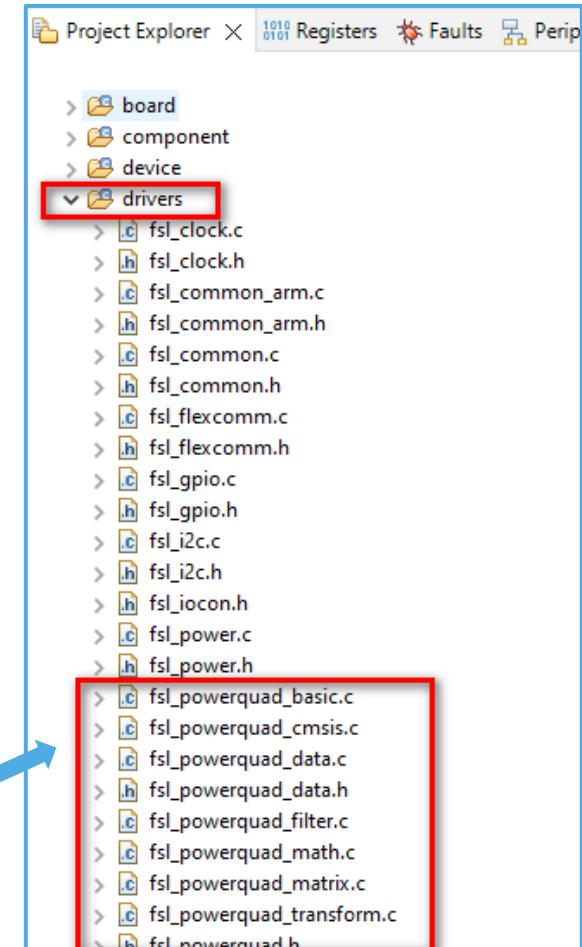
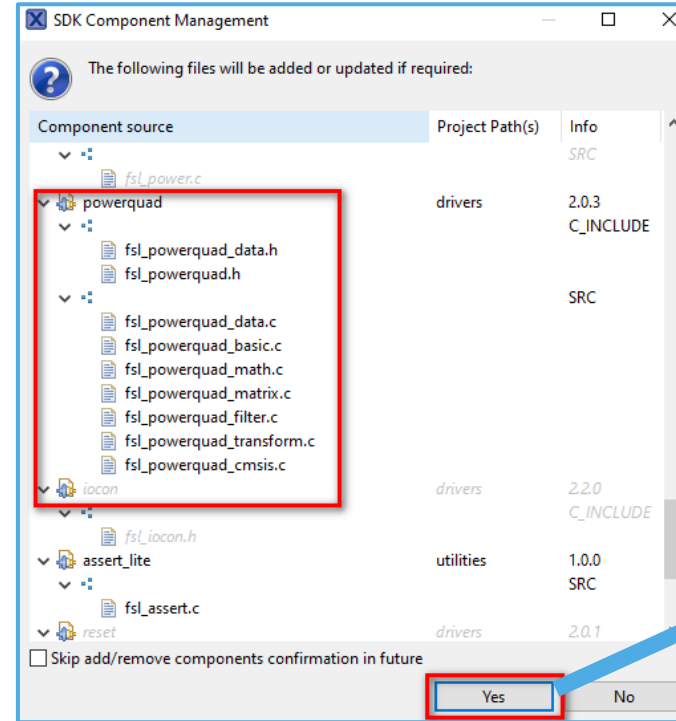
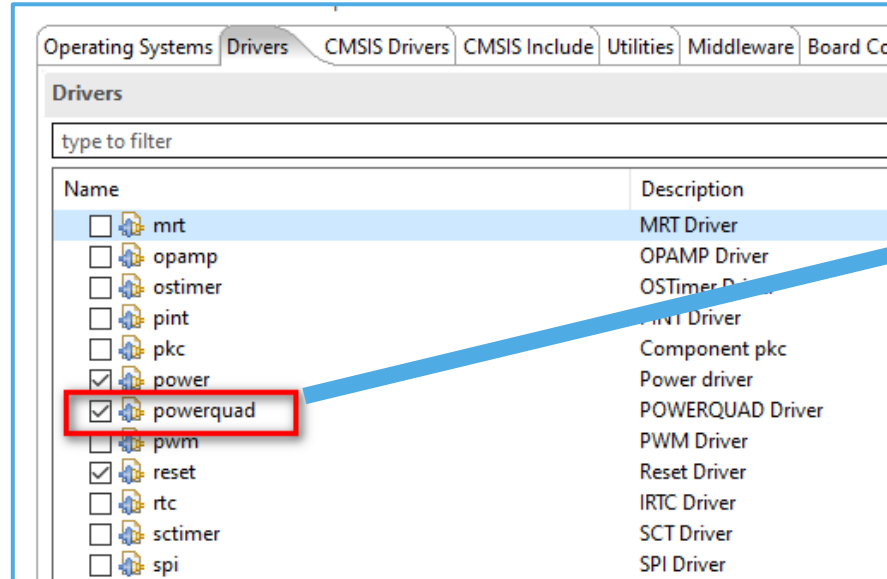
SDK COMPONENTS

- Click on “Managed SDK Components” icon



SDK COMPONENTS

- Selecting a new component, relevant files are added to project



Project SDK DEFINITIONS



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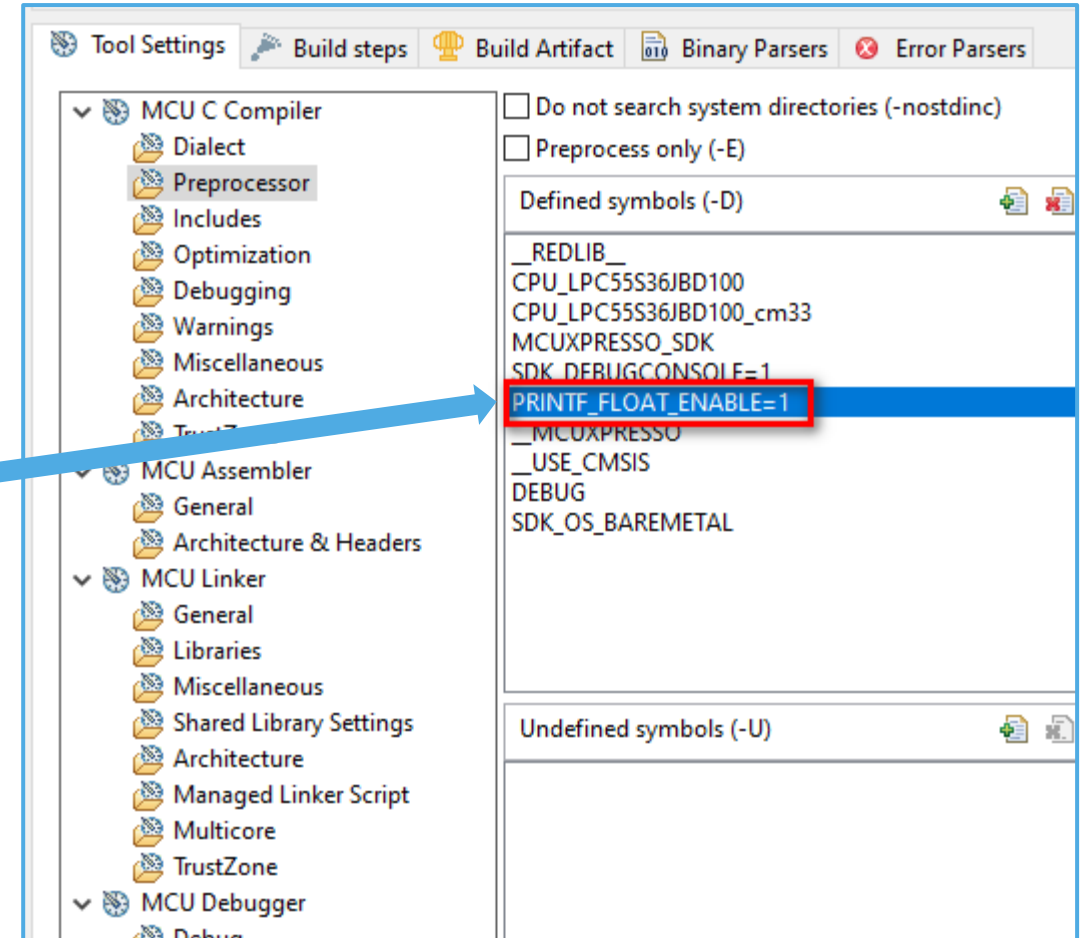
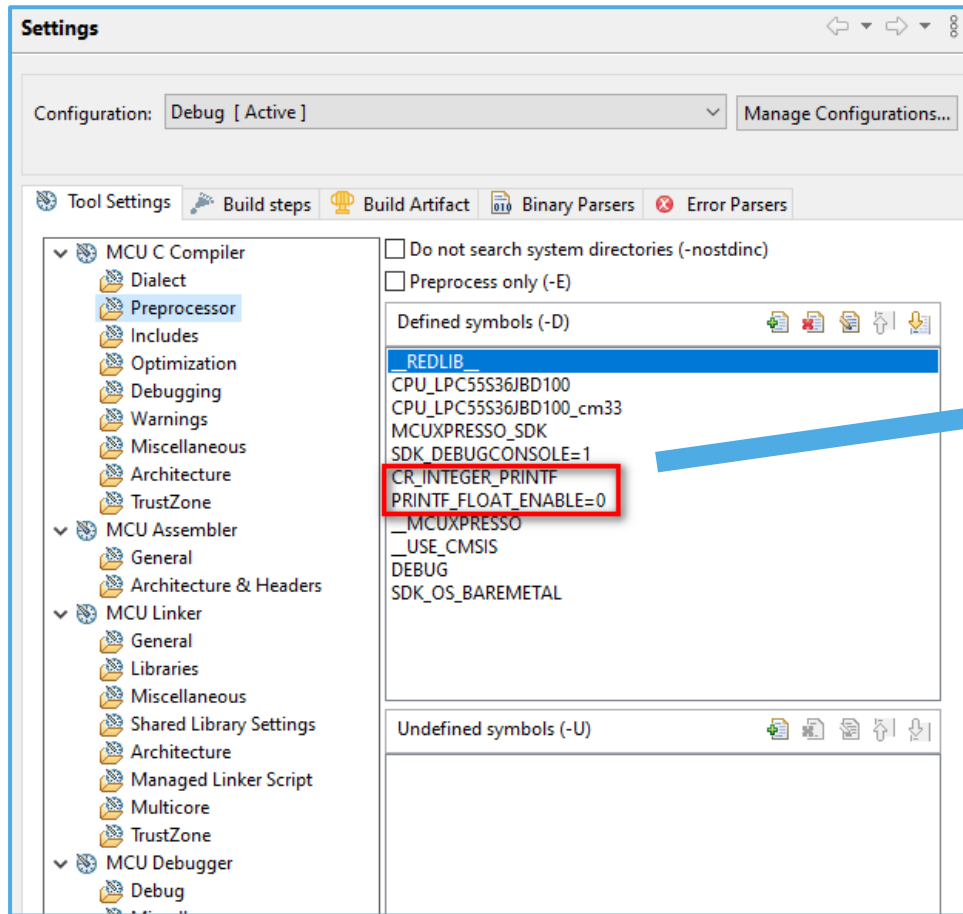
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SDK DEFINITIONS

- Enable float support for PRINTF



Project Build and Debug



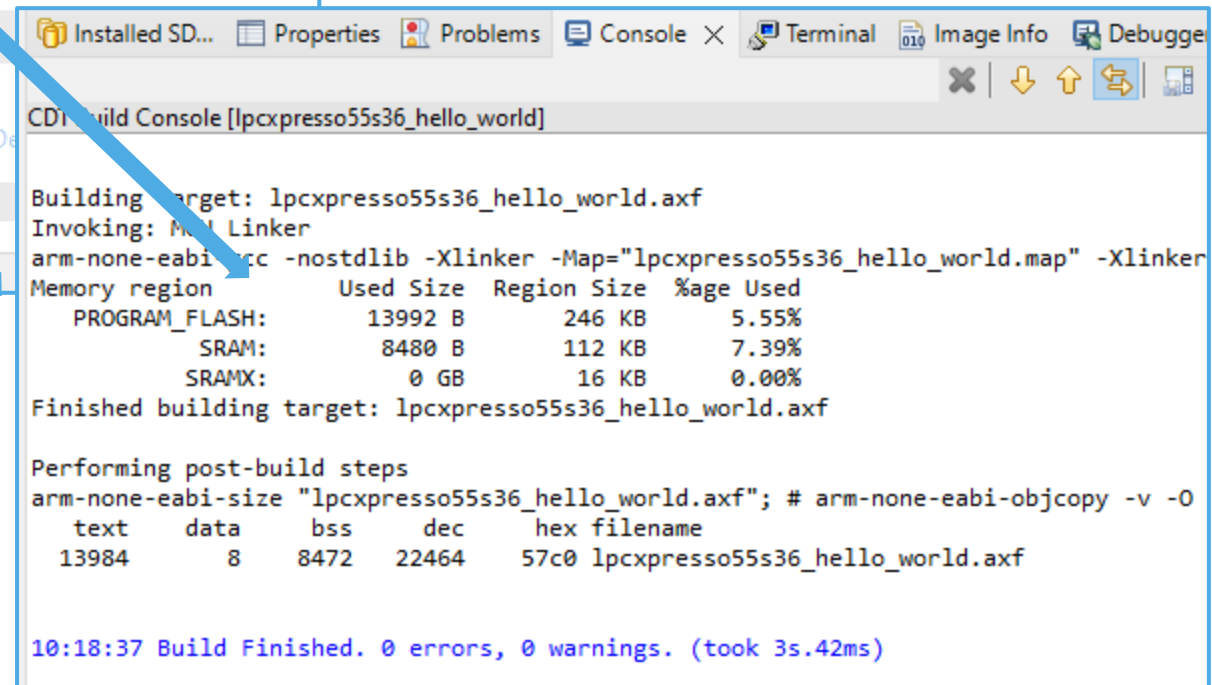
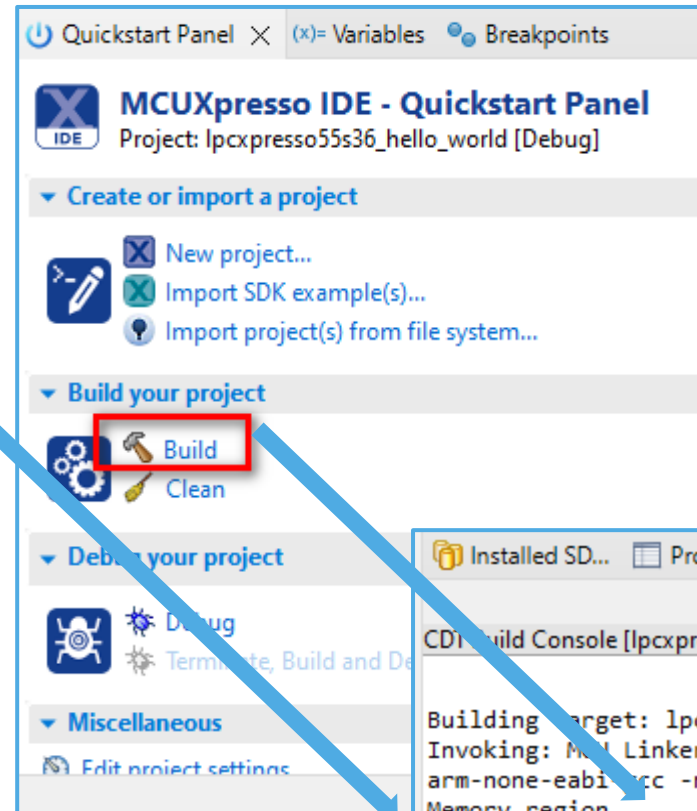
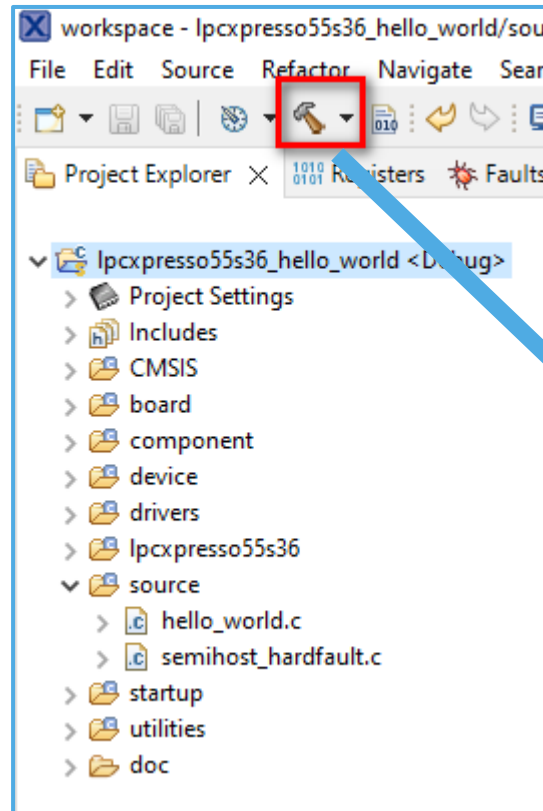
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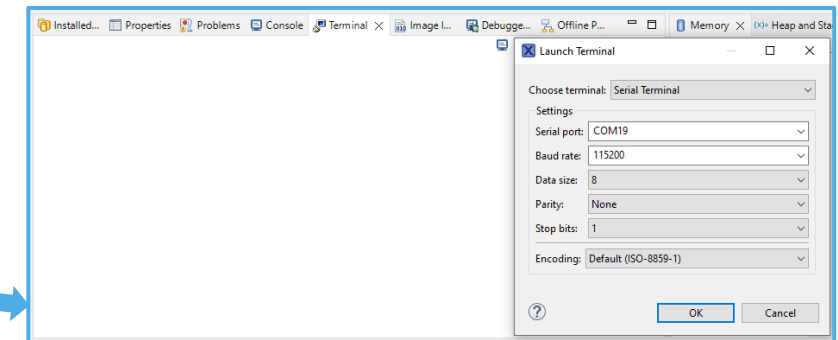
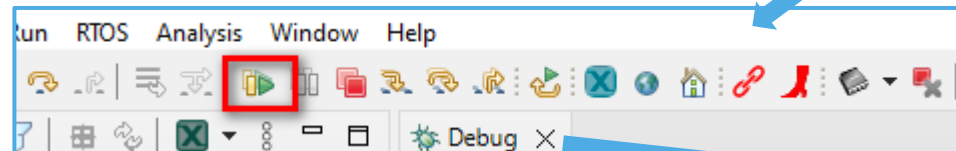
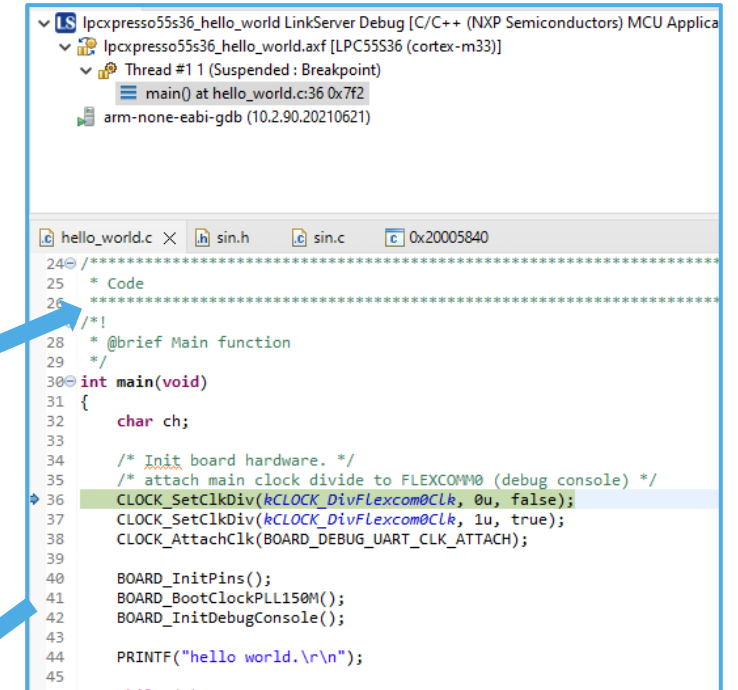
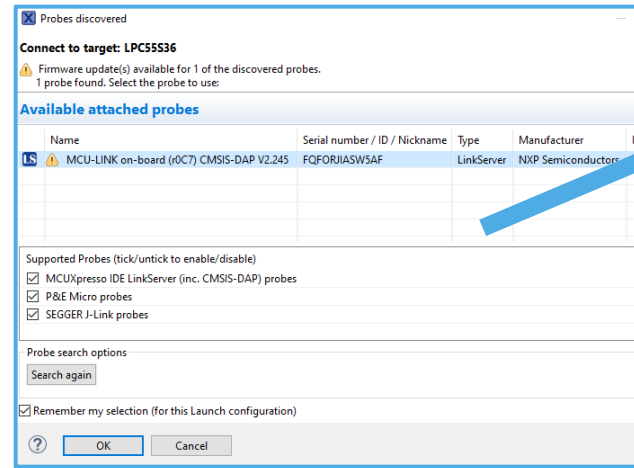
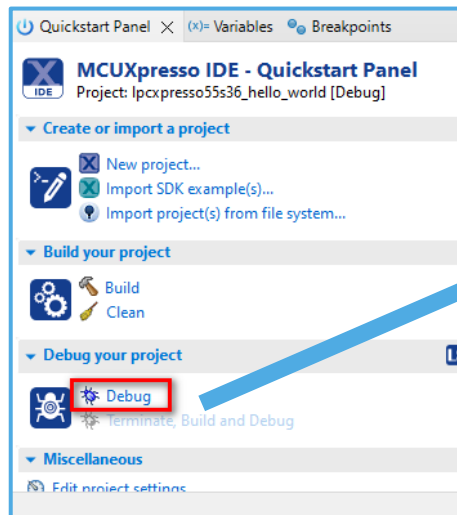
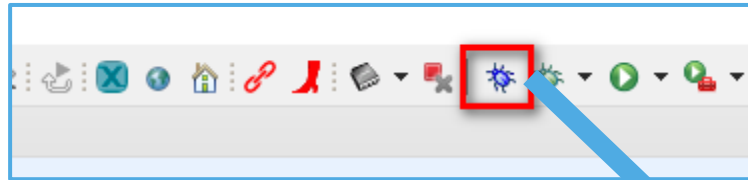
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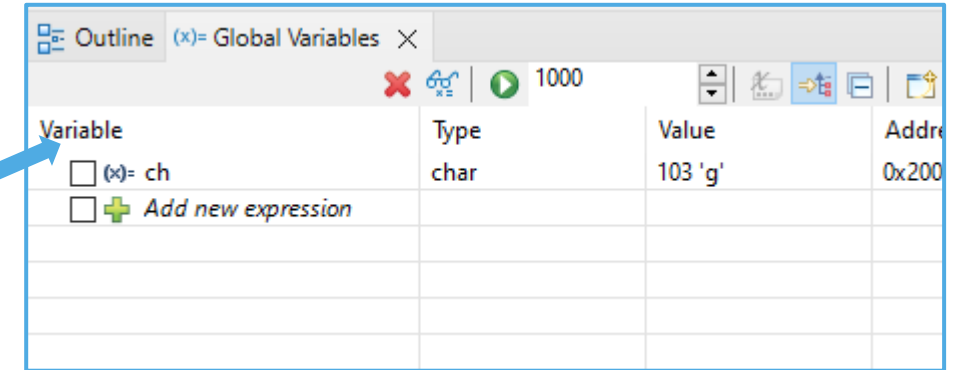
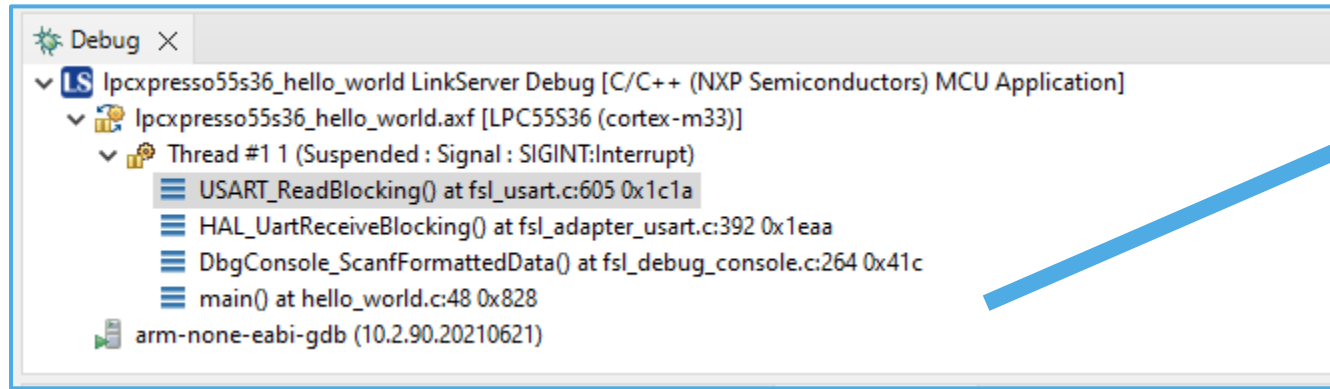
MCUXPRESSO PROJECT BUILD



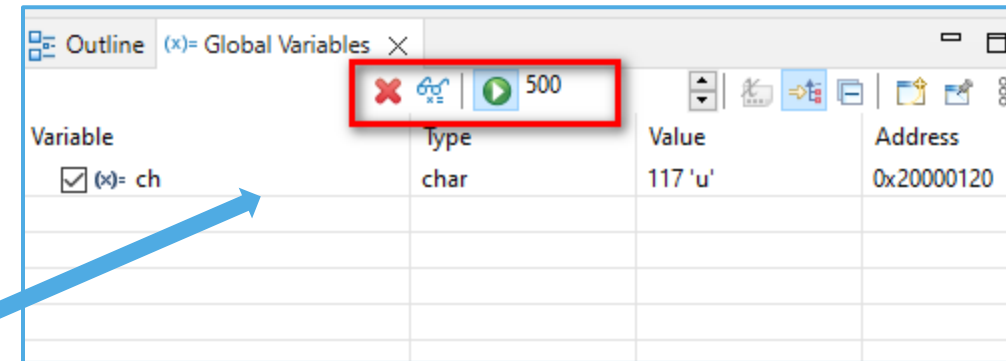
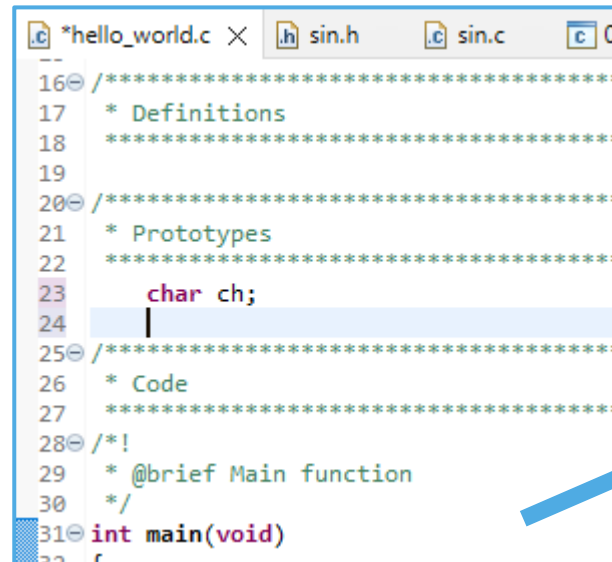
MCUXPRESSO PROJECT DEBUG



• Debugger: Variables



• Live View



Config Tools (Pins)



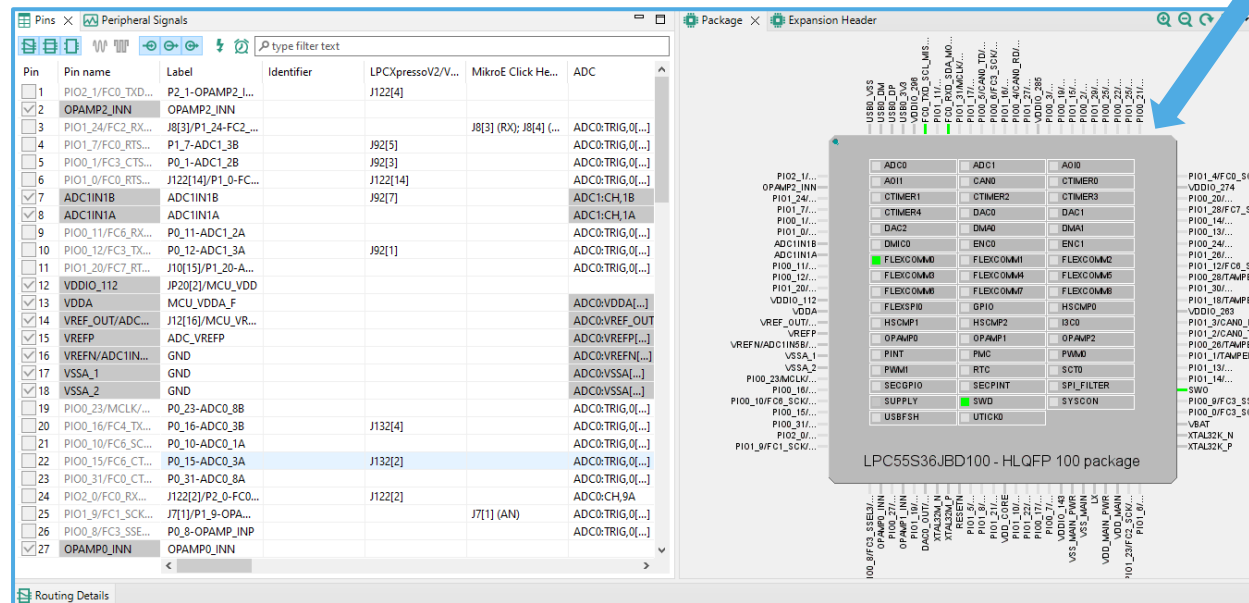
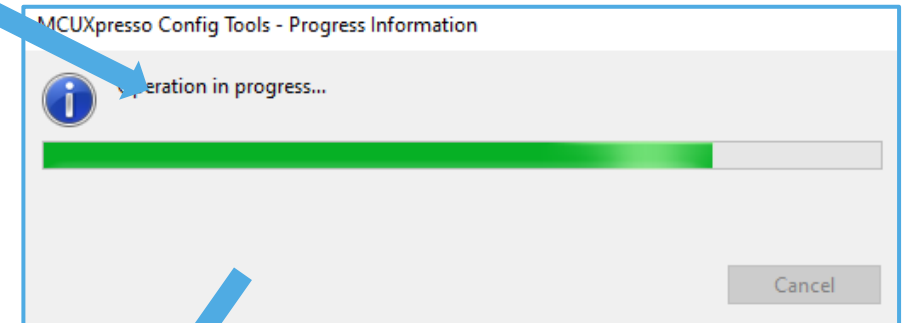
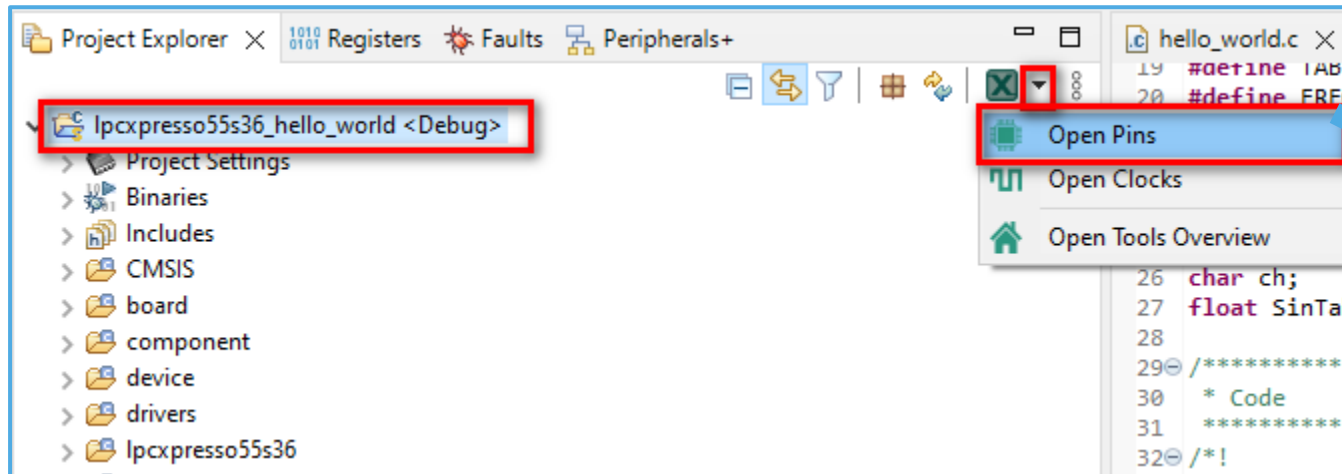
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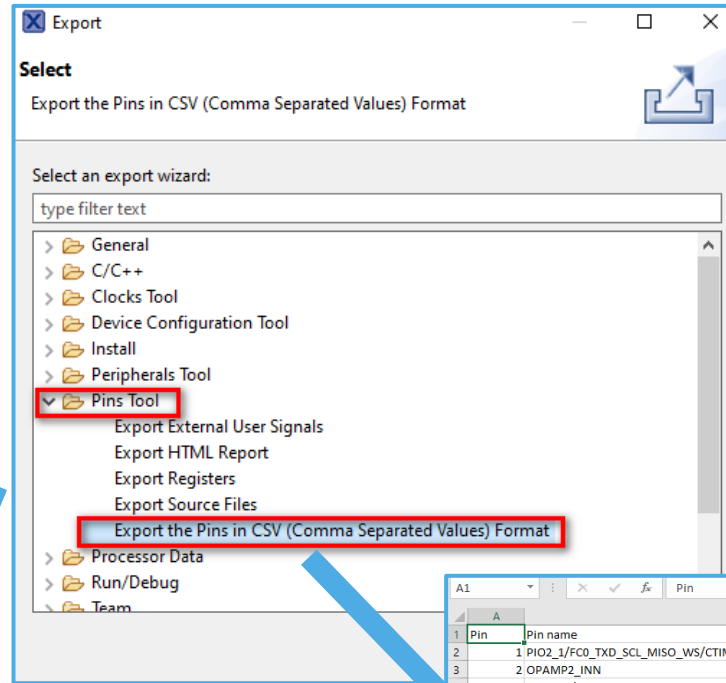
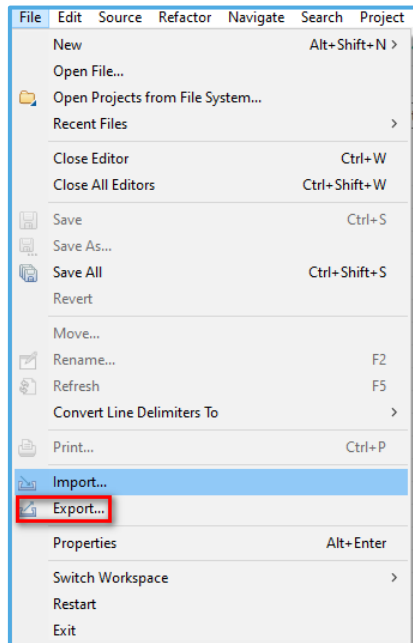


MCUXPRESSO CONFIG TOOLS: PINS



MCUXPRESSO CONFIG TOOLS: PINS

- Export Pins to Excel

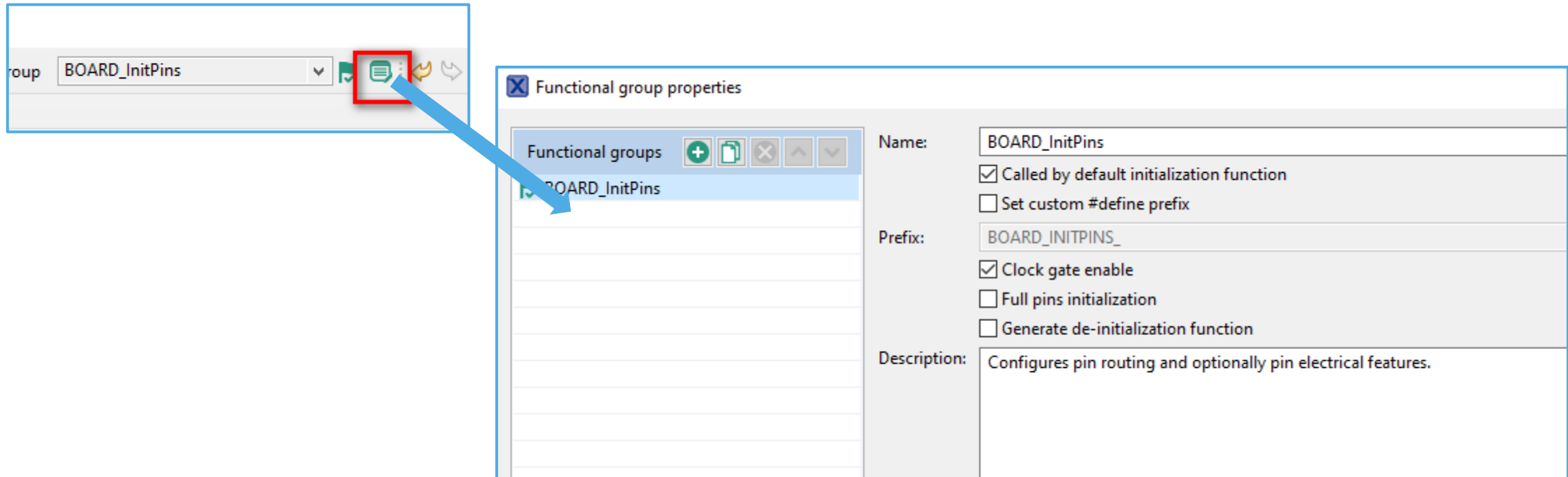


A screenshot of an Excel spreadsheet showing pin configuration data. The spreadsheet has columns A through K. The data is organized into rows, with the first row (A1) containing headers: Pin, Pin name, Label, Identifier, ADC, DAC, GPIO, HSCMP, DMA, PINT, and FLEXCOM. The subsequent rows contain detailed pin configuration information, including pin numbers, names, labels, identifiers, and various peripheral functions.

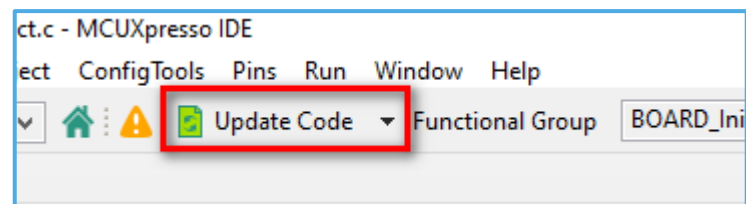
Pin	Pin name	Label	Identifier	ADC	DAC	GPIO	HSCMP	DMA	PINT	FLEXCOM
1	PIO2_1/FC0_TXD_SCL_MISO_WS/CTIMER1_MAT0/I3C0_SDA/AOI0_OUT2/OPAMP2_INP	P2_1-OPAMP2_INP-FC0_TXD_WS				GPIO:PIO2,1(PIO2_1)				FLEXCOM
2	OPAMP2_INN	OPAMP2_INN								
3	PIO1_24/FC2_RXD_SDA_MOSI_DATA/CTIO0_OUT1/FC3_SSEL3/AOI0_OUT2/ADC1_8B	J8[3]/P1_24-FC2_RXI	ADC0:TRIC DAC0:TRIC GPIO:PIO1 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
4	PIO1_7/FC0_RTS_SCL_SSEL1/CTIMER2_MAT2/SCT_GPI4/AOI1_OUT3/ADC1_3B	P1_7-ADC1_3B	ADC0:TRIC DAC0:TRIC GPIO:PIO1 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
5	PIO0_1/FC3_CTS_SDA_SSEL0/CT_INP0/SCT_GPI1/PDM_CLK0/CMP0_OUT/SECURE_GPIO0_1/AOI0_OUT1/ADC1_2B	P0_1-ADC1_2B	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
6	PIO1_0/FC0_RTS_SCL_SSEL1/CT_INP2/SCT_GPI4/AOI1_OUT0/ADC1_0B	J122[14]/P1_0-FC0_	ADC0:TRIC DAC0:TRIC GPIO:PIO1 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
7	ADC1IN1B	ADC1IN1B	ADC1:CH,1B(ADC1IN1B)							
8	ADC1IN1A	ADC1IN1A	ADC1:CH,1A(ADC1IN1A)							
9	PIO0_11/FC6_RXD_SDA_MOSI_DATA/CTIMER2_MAT2/FREQME_GPIO_CLK_A/SECURE_GPIO0_11/AOI1_OUT2/ADC1_2A	P0_11-ADC1_2A	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
10	PIO0_12/FC3_TXD_SCL_MISO_WS/FREQME_GPIO_CLK_B/SCT_GPI7/FC6_TXD_SCL_MISO_WS/SECURE_GPIO0_12/AOI1_OUT1/ADC1_3A	P0_12-ADC1_3A	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
11	PIO1_20/FC7_RTS_SCL_SSEL1/CT_INP14/FC4_TXD_SCL_MISO_WS/PWM0_A0/AOI0_OUT1/ADC1_8A	J10[15]/P1_20-ADC1	ADC0:TRIC DAC0:TRIC GPIO:PIO1 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
12	VDDIO_112	JP20[2]/MCU_VDD								
13	VDDA	MCU_VDDA_F	ADC0:VDC DAC0:REF_0(VDDA)/DAC1:REF_0(VDDA)/DAC2:REF_0(VDDA)							
14	VREF_OUT/ADC1IN5A/ADCOIN5A	J12[16]/MCU_VREF	ADC0:VRE DAC0:REF_1(VREF_OUT)/DAC1:REF_1(VREF_OUT)/DAC2:REF_1(VREF_OUT)							
15	VREFP	ADC_VREFP	ADC0:VRE DAC0:REF_2(VREFP)/DAC1:REF_2(VREFP)/DAC2:REF_2(VREFP)							
16	VREFN/ADC1IN5B/ADCOIN5B	GND	ADC0:VREFN(VREFN)/ADC1:VREFN(VREFN)/ADC1:CH,5B(ADC1IN5B)/AD							
17	VSSA_1	GND	ADC0:VSSA(VSSA_1)/ADC1:VSSA(VSSA_1)							
18	VSSA_2	GND	ADC0:VSSA(VSSA_2)/ADC1:VSSA(VSSA_2)							
19	PIO0_23/MCLK/CTIMER1_MAT2/CTIMER3_MAT3/SCT0_OUT4/FC0_CTS_SDA_SSEL0/SECURE_GPIO0_23/ADC0_8B	P0_23-ADC0_8B	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
20	PIO0_16/FC4_TXD_SCL_MISO_WS/CLKOUT/CT_INP4/SECURE_GPIO0_16/AOI0_OUT3/ADC0_3B	P0_16-ADC0_3B	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
21	PIO0_10/FC6_SCK/CT_INP10/CTIMER2_MAT0/FC1_TXD_SCL_MISO_WS/SEC0_OUT2/SECURE_GPIO0_10/ADC0_1A	P0_10-ADC0_1A	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
22	PIO0_15/FC6_CTS_SDA_SSEL0/UTICK_CAP2/CT_INP16/SCT0_OUT2/SECURE_GPIO0_15/ADC0_3A	P0_15-ADC0_3A	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
23	PIO0_31/FC0_CTS_SDA_SSEL0/CTIMER0_MAT1/SCT0_OUT3/SECURE_GPIO0_31/AOI0_OUT0/ADC0_8A	P0_31-ADC0_8A	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
24	PIO2_0/FC0_RXD_SDA_MOSI_DATA/CT_INP4/I3C0_PUR/AOI0_OUT0/ADC0_9A	J122[2]/P2_0-FC0_R	ADC0:CH,9A(ADC0_9 GPIO:PIO2,0(PIO2_0)							FLEXCOM
25	PIO1_9/FC1_SCK/CT_INP4/SCT0_OUT2/FC4_CTS_SDA_SSEL0/AOI1_OUT3/ADC0_0A/OPAMP0_OUT/HSCMP0_IN4	J7[1]/P1_9-OPAMP0	ADC0:TRIC DAC0:TRIC GPIO:PIO1 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							
26	PIO0_8/FC3_SSEL3/FC5_RXD_SDA_MOSI_DATA/SW0/PDM_DATA1/SECURE_GPIO0_8/OPAMP0_INP	P0_8-OPAMP_INP	ADC0:TRIC DAC0:TRIC GPIO:PIO0 HSCMP0:S DMA0:TRI PINT:PINT FLEXCOM							

MCUXPRESSO CONFIG TOOLS: PINS

- PINS FUNCTIONAL GROUPS



- CODE UPDATE



Config Tools (Clock)



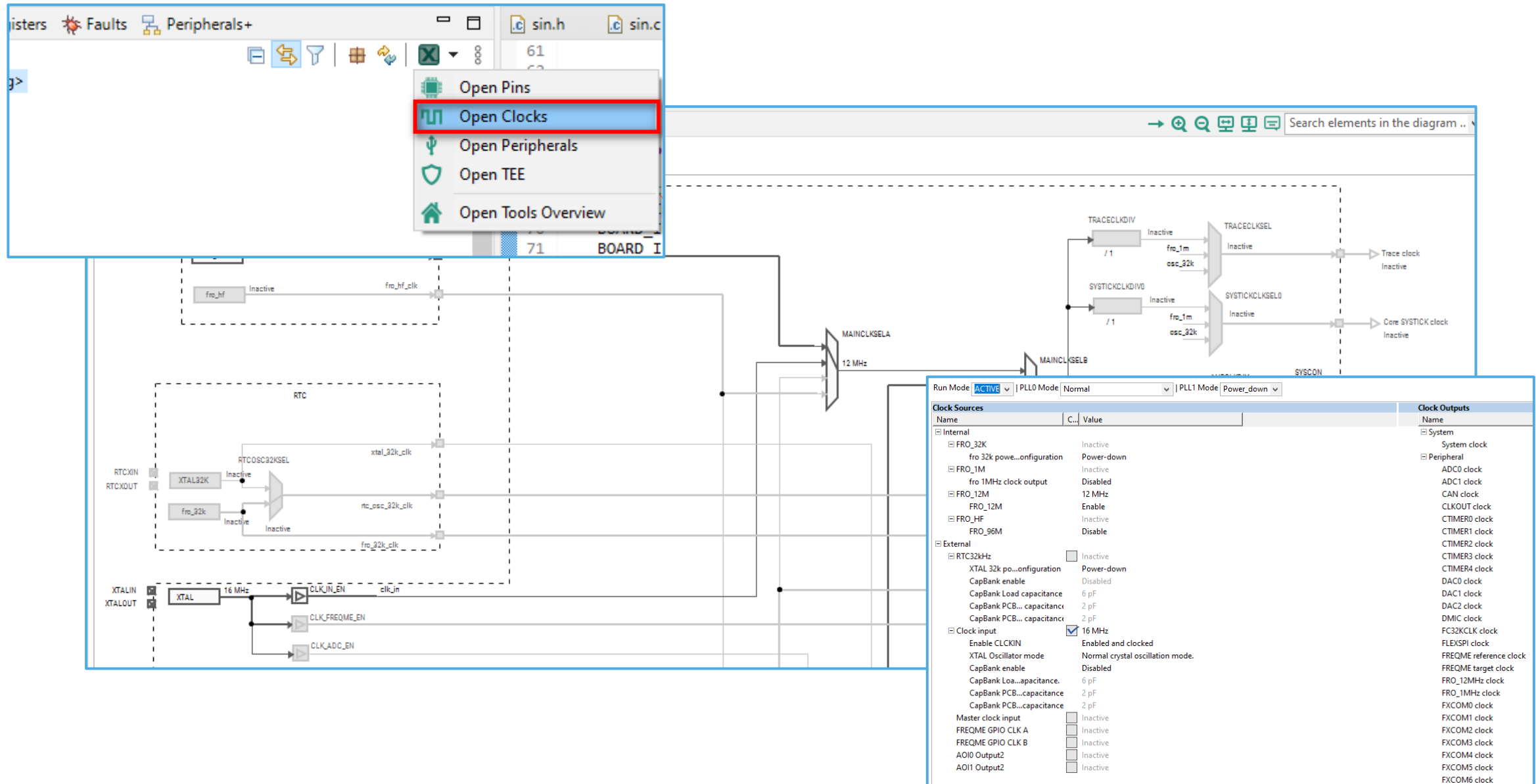
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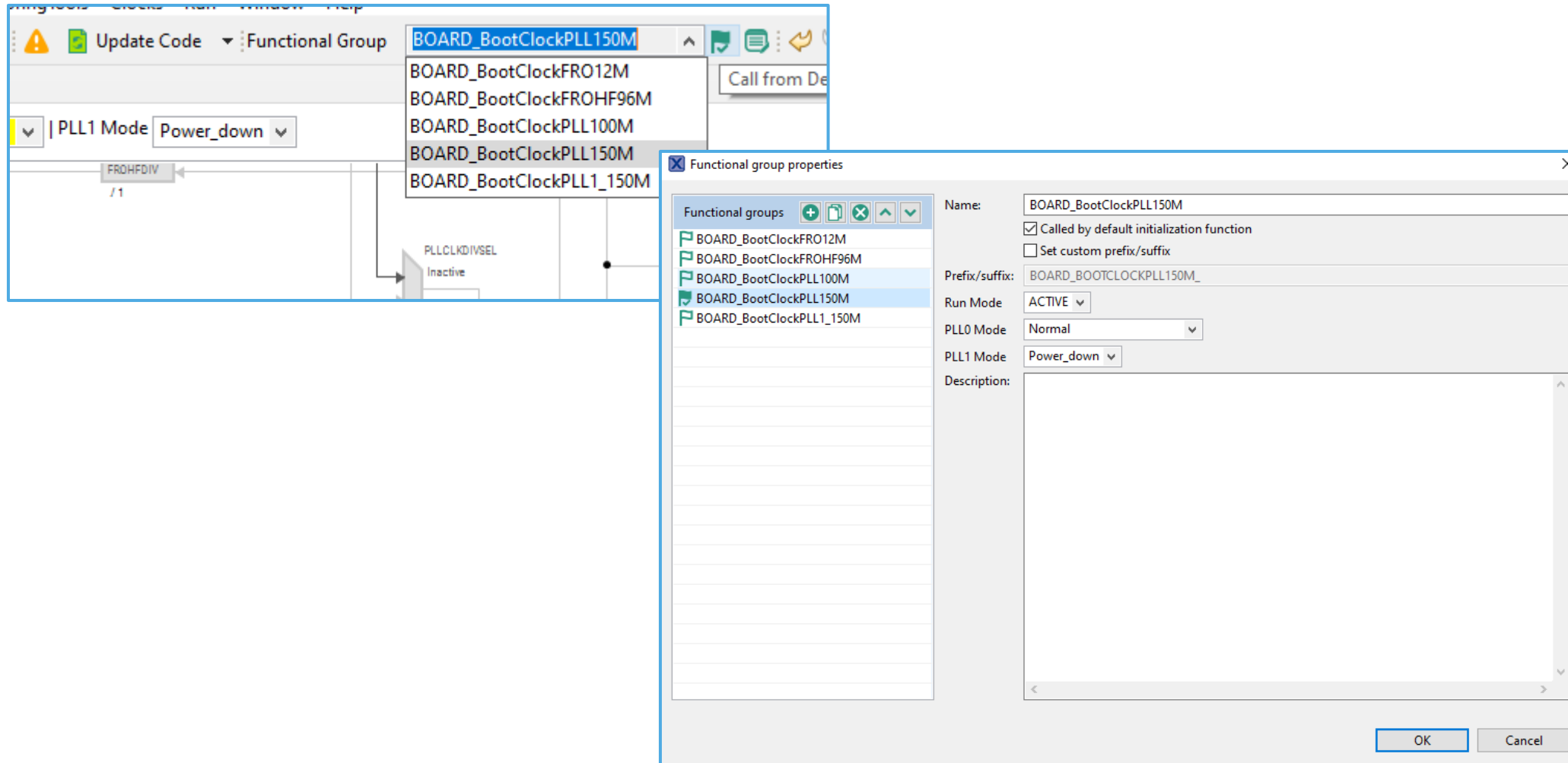


MCUXPRESSO CONFIG TOOLS: CLOCKS



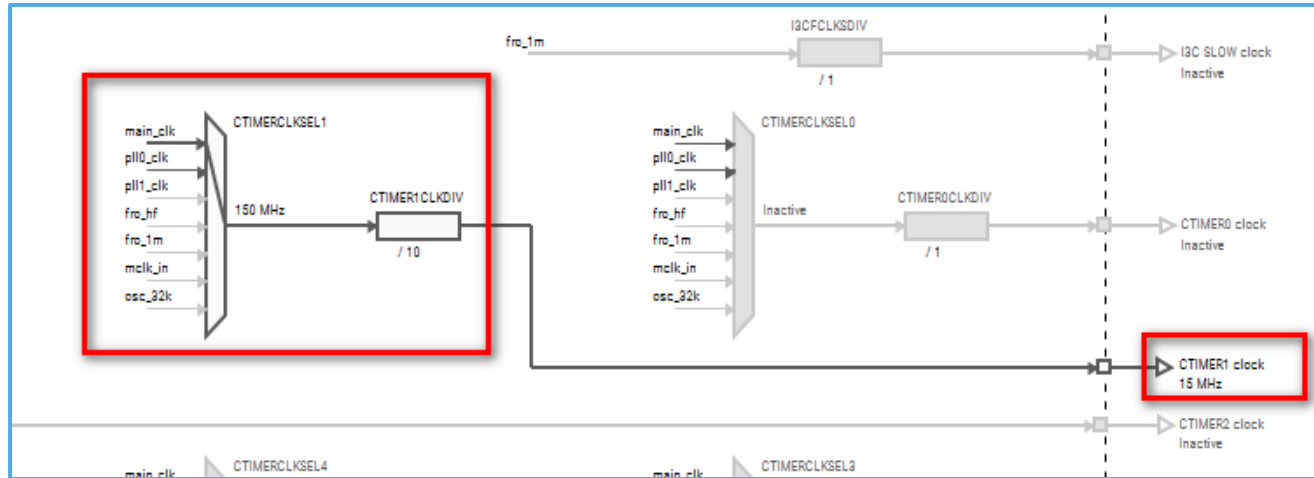
MCUXPRESSO CONFIG TOOLS: CLOCKS

- CLOCK CONFIGURATIONS (FUNCTIONAL GROUPS)



MCUXPRESSO CONFIG TOOLS: CLOCKS

- CTIMER CLOCK ENABLE



Config Tools (Peripherals)



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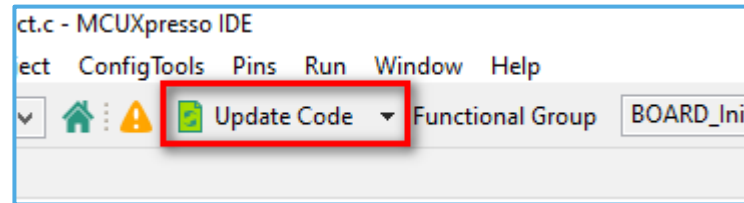
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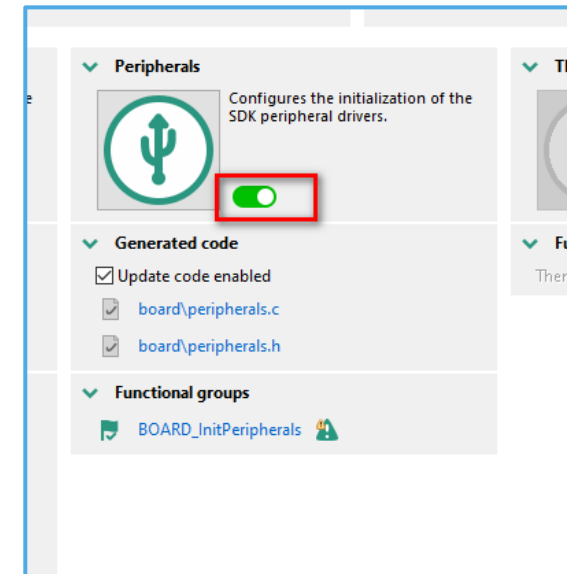
MCUXPRESSO CONFIG TOOLS: PERIPHERALS

- In some projects Peripherals Tool is disable, Enable it
- Update Code



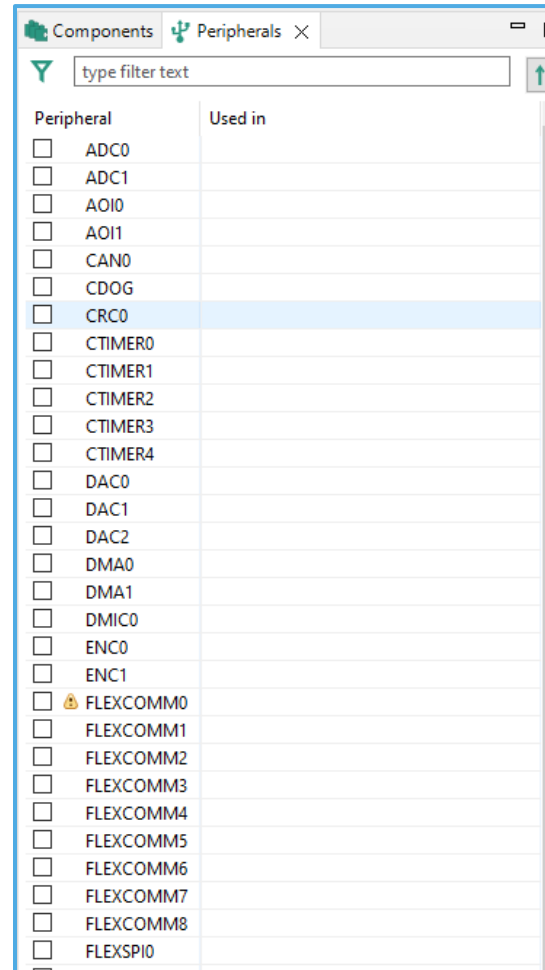
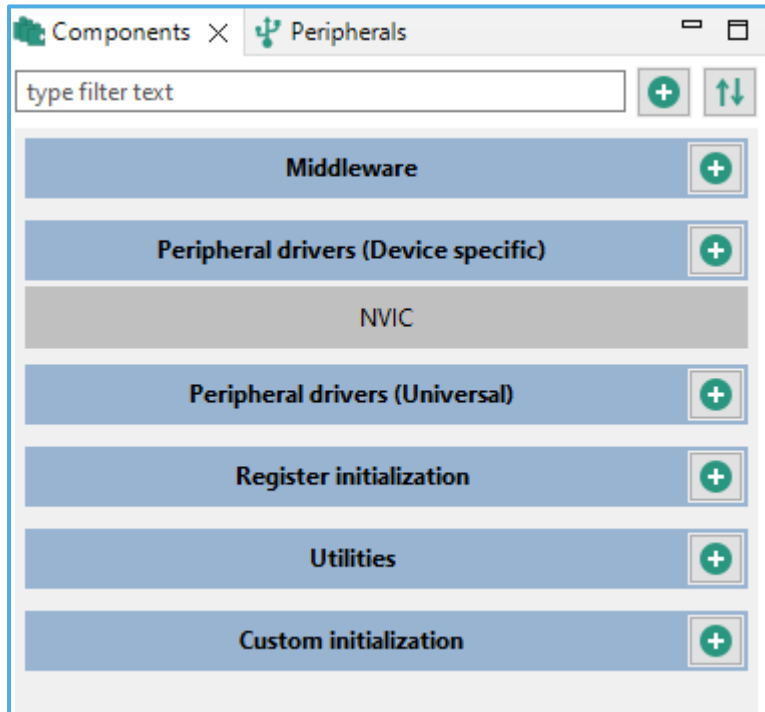
- Call Init Peripherals function

```
66 int main(void) {  
67  
68     /* Init board hardware. */  
69     BOARD_InitBootPins();  
70     BOARD_InitBootClocks();  
71     BOARD_InitBootPeripherals();
```



MCUXPRESSO CONFIG TOOLS: PERIPHERALS

- Components and Peripherals



CTIMER



SECURE CONNECTIONS
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MCUXPRESSO CONFIG TOOLS: CTIMER

Mode: Input Capture/Match Peripheral: CTIMER0

Timer/counter general configuration Preset: Custom...

Timer counter configuration

Timer mode: Timer (bus clock source)

Bus clock source: CTIMER0 clock - BOARD_BootClockFRO12M: Inactive, BOARD_BootClockFROHF96M: Inactive, BOARD_BootClockPLL100M: Inactive, BOARD_BootClockPLL150M: Active

Clock source frequency: 150 MHz (BOARD_BootClockPLL150M)

Timer input frequency/prescaler: 1000Hz

Calculated prescaler: 150000

Calculated timer input frequency: 1 kHz; 1 ms

Timer counter period: 100 ms

Start timer in initialization code: ☐

Match channels + x

Match_0

Channel ID: Match_0

Match channel: Match channel 0

Channel frequency/period/offset: 10Hz

Channel period [ticks]: 100

Calculated match frequency/period/offset: 10 Hz; 100 ms

Enable counter reset on match: ☒

Enable counter stop on match: ☐

Output control: No action is taken

Initial output value: Low

Enable match interrupt request: ☒

Capture channels + x

Add item by clicking on plus button

Interrupt and callback settings

Configuration enabled (a match/capture/pwm channel interrupt is enabled)

Interrupt

Interrupt: CTIMER0_IRQn

Enable priority initialization: ☐

Priority: 0

Callback mode: Single callback

Shared callback function: TimerIRQ

- Ctimer peripheral input clock
 - Common clock for match0-3 and capture0-3

- Match0 settings

MCUXPRESSO CONFIG TOOLS: CTIMER

Add item by clicking on plus button

✓ **Interrupt and callback settings**

Configuration enabled (a match/capture/pwm channel interrupt is enabled)

✓ **Interrupt**

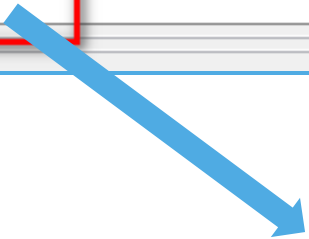
Interrupt CTIMER1_IRQn

Enable priority initialization ☐

Priority 0

Callback mode Single callback

Shared callback function TimerIRQ



```
55
56 void TimerIRQ(uint32_t flags)
57 {
58
59
60 }
61
```

MCUXPRESSO CONFIG TOOLS: CTIMER

- API Information

Deprecated List

▼ API Reference

- ▶ ANACTRL: Analog Control Driver
- ▶ CASPER: The Cryptographic Acc
- ▶ CDOG
- ▶ CMP: Analog Comparator Driver
- ▶ CODEC Driver
- ▶ CRC: Cyclic Redundancy Check D
- ▶ CTIMER: Standard counter/timers
- ▶ Clock Driver
- ▶ Common Driver
- ▶ DMA: Direct Memory Access Conti
- ▶ Debug Console
- ▶ FLEXCOMM: FLEXCOMM Driver
- ▶ GINT: Group GPIO Input Interrupt
- ▶ GPIO: General Purpose I/O
- ▶ Hashcrypt: The Cryptographic Acc
- ▶ Hashcrypt_driver
- ▶ I2C FreeRTOS Driver
- ▶ I2C: Inter-Integrated Circuit Driver
- ▶ I2S: I2S Driver
 - I2c_cmsis_driver
- ▶ I2c_dma_driver
- ▶ I2s_dma_driver
- ▶ INPUTMUX: Input Multiplexing Dri
- ▶ IOCON: I/O pin configuration
- ▶ LPADC: 12-bit SAR Analog-to-Digi
- ▶ MCAN: Controller Area Network D
- ▶ MRT: Multi-Rate Timer
- ▶ Notification Framework

PWM setup operations

status_t

CTIMER_SetupPwmPeriod (CTIMER_Type *base, const ctimer_r

Configures the PWM signal parameters. [More...](#)

status_t

CTIMER_SetupPwm (CTIMER_Type *base, const ctimer_match_

Configures the PWM signal parameters. [More...](#)

static void

CTIMER_UpdatePwmPulsePeriod (CTIMER_Type *base, ctimer_

Updates the pulse period of an active PWM signal. [More...](#)

void

CTIMER_UpdatePwmDutycycle (CTIMER_Type *base, const ctin

Updates the duty cycle of an active PWM signal. [More...](#)

Interrupt Interface

static void

CTIMER_EnableInterrupts (CTIMER_Type *base, uint32_t ma

Enables the selected Timer interrupts. [More...](#)

static void

CTIMER_DisableInterrupts (CTIMER_Type *base, uint32_t ma

Disables the selected Timer interrupts. [More...](#)

static uint32_t

CTIMER_GetEnabledInterrupts (CTIMER_Type *base)

Gets the enabled Timer interrupts. [More...](#)

Status Interface

static uint32_t

CTIMER_GetStatusFlags (CTIMER_Type *base)

Gets the Timer status flags. [More...](#)

static void

CTIMER_ClearStatusFlags (CTIMER_Type *base, uint32_t ma

Clears the Timer status flags. [More...](#)

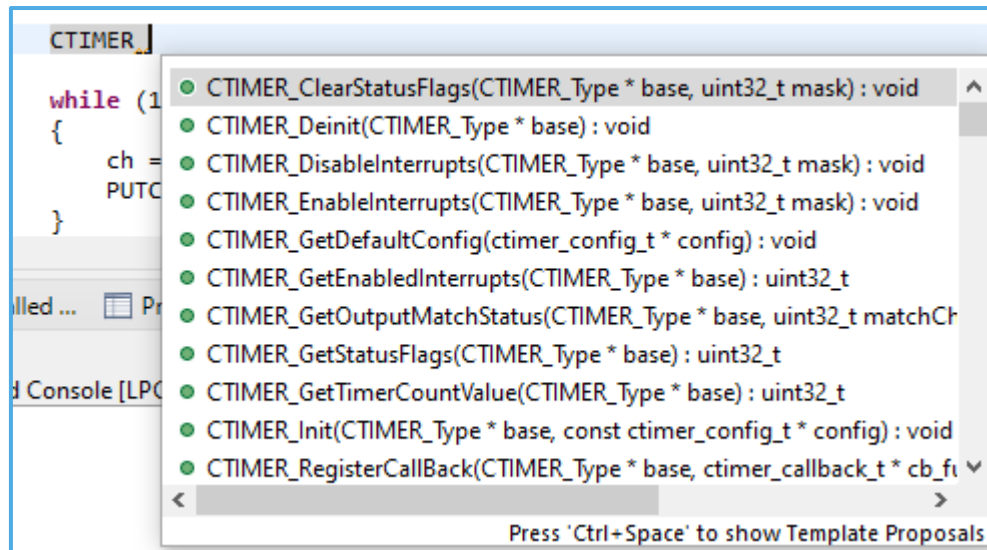
Counter Start and Stop

static void

CTIMER_StartTimer (CTIMER_Type *base)

MCUXPRESSO CONFIG TOOLS: CTIMER

- Code Modification
- Write “CTIMER_” and CTRL + SPACE



```
8
9 #include "fsl_device_registers.h"
10 #include "fsl_debug_console.h"
11 #include "pin_mux.h"
12 #include "clock_config.h"
13 #include "board.h"
14 #include "peripherals.h"
15
```

```
27 void TimerIRQ(uint32_t flags)
28 {
29
30 }
31
32
33
34 * Code
35
36
37 * @brief Main function
38
39 int main(void)
40 {
41     char ch;
42
43     /* Init board hardware. */
44     /* attach main clock divide to FLEXCOMM0 (debug console) */
45     CLOCK_SetClkDiv(kCLOCK_DivFlexcom0Clk, 0u, false);
46     CLOCK_SetClkDiv(kCLOCK_DivFlexcom0Clk, 1u, true);
47     CLOCK_AttachClk(BOARD_DEBUG_UART_CLK_ATTACH);
48
49     BOARD_InitPins();
50     BOARD_BootClockPLL150M();
51     BOARD_InitDebugConsole();
52     BOARD_InitPeripherals();
53
54     PRINTF("hello world.\r\n");
55
56     CTIMER_StartTimer(CTIMER1_PERIPHERAL);
57
58     while (1)
59     {
60         ch = GETCHAR();
61         PUTCHAR(ch);
62     }
63 }
64
```

MCUXPRESSO CONFIG TOOLS: SIN WAVE

- Add “sin wave” generation

```
void Generate_sin_table_float(float *table, uint32_t length, float amplitude,
float frequency)
{
    uint32_t index;
    float theta, sample_time;
    sample_time=1.0f/(frequency * (float)length);
    for(index=0;index < length;index++)
    {
        theta= 2.0f * PI * frequency * sample_time * (float)index;
        table[index]=amplitude * sin(theta);
    }
}
```

MCUXPRESSO CONFIG TOOLS: SIN WAVE

“sin wave” generation (PowerQuad Version)

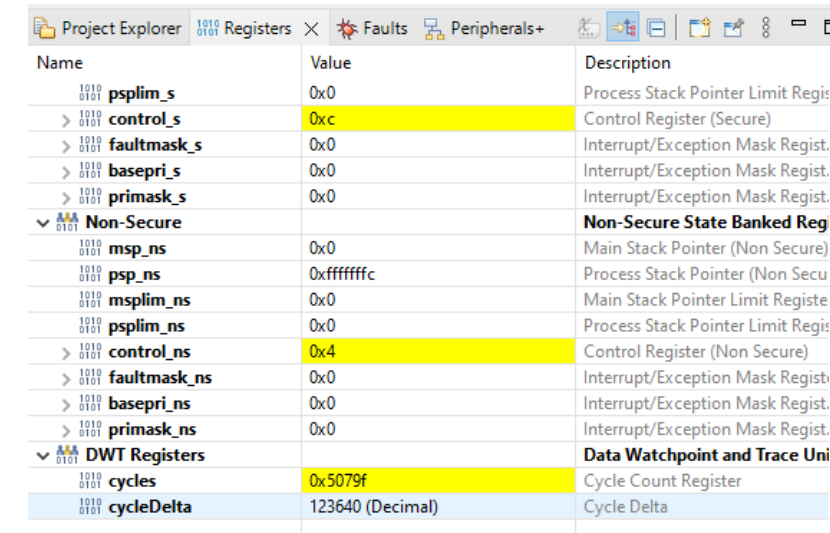
```
#include "fsl_powerquad.h"
```

```
BOARD_InitPins();  
BOARD_BootClockPLL150M();  
BOARD_InitDebugConsole();  
BOARD_InitPeripherals();  
PQ_Init(POWERQUAD);
```

```
void Generate_sin_table_float(float *table, uint32_t length, float amplitude, float frequency)  
{  
    uint32_t index;  
    float theta, sample_time, result;  
    sample_time=1.0f/(frequency * (float)length);  
    for(index=0;index < length;index++)  
    {  
        theta= 2.0f * PI * frequency * sample_time * (float)index;  
        #if USE_POWERQUAD  
            PQ_SinF32(&theta, &result);  
        table[index]=amplitude * result;  
        #else  
            table[index]=amplitude * sin(theta);  
        #endif  
    }  
}
```

MCUXPRESSO CONFIG TOOLS: SIN WAVE (SW VS POWERQUAD)

Execution comparative



Name	Value	Description
psplim_s	0x0	Process Stack Pointer Limit Register (Secure)
control_s	0xc	Control Register (Secure)
faultmask_s	0x0	Interrupt/Exception Mask Register (Secure)
basepri_s	0x0	Interrupt/Exception Mask Register (Secure)
primask_s	0x0	Interrupt/Exception Mask Register (Secure)
Non-Secure		Non-Secure State Banked Registers
mnp_ns	0x0	Main Stack Pointer (Non Secure)
psp_ns	0xffffffffc	Process Stack Pointer (Non Secure)
msplim_ns	0x0	Main Stack Pointer Limit Register (Non Secure)
psplim_ns	0x0	Process Stack Pointer Limit Register (Non Secure)
control_ns	0x4	Control Register (Non Secure)
faultmask_ns	0x0	Interrupt/Exception Mask Register (Non Secure)
basepri_ns	0x0	Interrupt/Exception Mask Register (Non Secure)
primask_ns	0x0	Interrupt/Exception Mask Register (Non Secure)
DWT Registers		Data Watchpoint and Trace Unit Registers
cycles	0x5079f	Cycle Count Register
cycleDelta	123640 (Decimal)	Cycle Delta

```
CPU cycles: 810985 -- Exec.Time(us): 5406.566895  
Set Frequency at 1.000000 Hz  
hello world.  
CPU cycles: 19506 -- Exec.Time(us): 130.040009  
Set Frequency at 1.000000 Hz
```

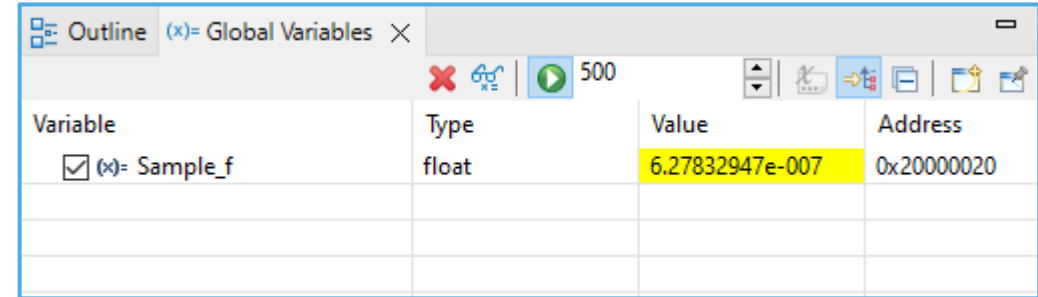
← `#define USE_POWERQUAD 0`

← `#define USE_POWERQUAD 1`

MCUXPRESSO CONFIG TOOLS: SIN WAVE

“sin wave” generation (Visualization) - Live View

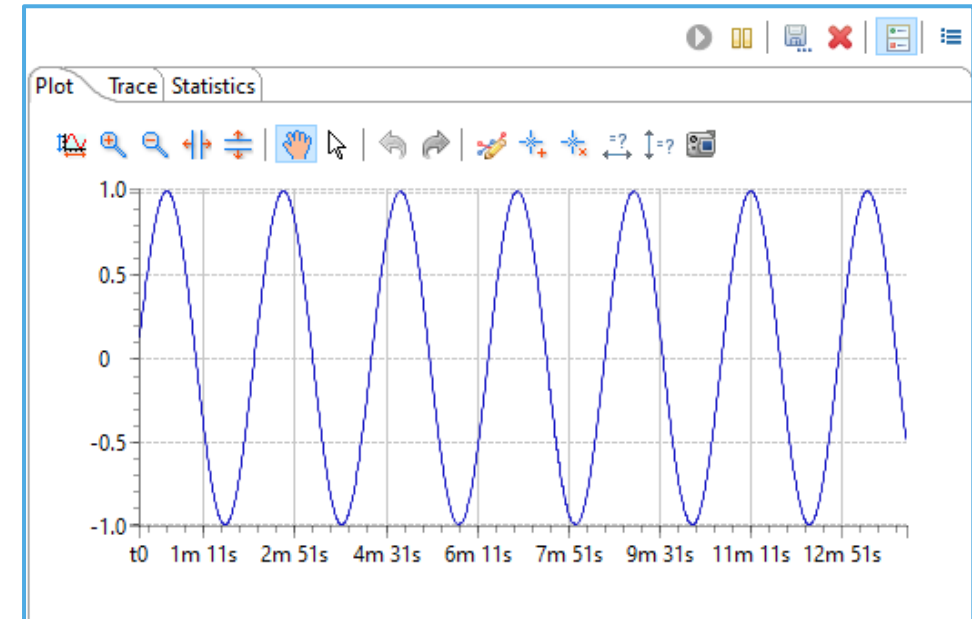
```
float Sample_f;  
uint32_t index=0;  
  
float SinTable_f[TABLE_LENGTH];
```



Variable	Type	Value	Address
<input checked="" type="checkbox"/> (x)= Sample_f	float	6.27832947e-007	0x20000020

```
Generate_sin_table_float(&SinTable_f[0],TABLE_LENGTH,1.0f, 1.0f);
```

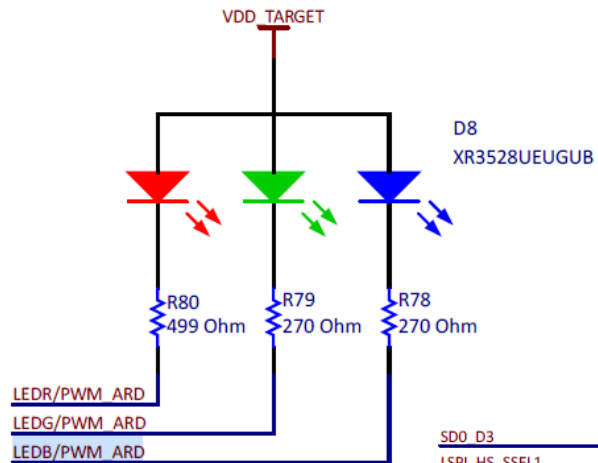
```
/*  
 * IRQ  
 */  
*****/  
void TimerIRQ(uint32_t flags)  
{  
    Sample_f=SinTable_f[index];  
    index++;  
    if(index==TABLE_LENGTH)index=0;  
}
```



CTIMER2

Pin	Pin name		FLEXCOMM	CTIMER	SCT	SDIF	SYSCON
✓ 1	CTIMER2_MAT1	T,0[...]	FLEXCOMM0:SCK	CTIMER2:MATC...	SCT0:OUT,0	SDIF:SD0_D,0	SYSCON:FREQM...

- EVK Schematic
 - Led blue at PIO1_4



LEDR/PWM_ARD	11	PIO1_0
LEDG/PWM_ARD	59	PIO1_1
LEDB/PWM_ARD	61	PIO1_2
	62	PIO1_3
LEDB/PWM_ARD	1	PIO1_4
PIO1_5 GPIO_ARD	31	PIO1_5
LEDR/PWM_ARD	5	PIO1_6
LEDG/PWM_ARD	9	PIO1_7
PIO1_8 GPIO_ARD	24	PIO1_8

Name: CTIMER2
Custom name: ☐

Mode: Input Capture/Match
Peripheral: CTIMER2
Preset: Custom...

Timer/counter general configuration

Timer counter configuration

Timer mode: Timer (bus clock source)
Bus clock source: CTIMER2 clock - BOARD_BootClockFRO12M: Inactive, BOARD_BootClockFROHF96M: Inactive, BOARD_BootClockPLL100M: Inactive, BOARD_...
Clock source frequency: 150 MHz (BOARD_BootClockPLL150M)
Timer input frequency/prescaler: 50MHz
Calculated prescaler: 3
Calculated timer input frequency: 50 MHz; 20 ns
Timer counter period: 1 s
Start timer in initialization code: ☒

Match channels

Match 0

Channel ID: Match_0
Match channel: Match channel 1
Channel frequency/period/offset: 1Hz
Channel period [ticks]: 50000000
Calculated match frequency/period/offset: 1 Hz; 1 s
Enable counter reset on match: ☒
Enable counter stop on match: ☐
Output control: Toggle bit/output
Initial output value: Low
Enable match interrupt request: ☐



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