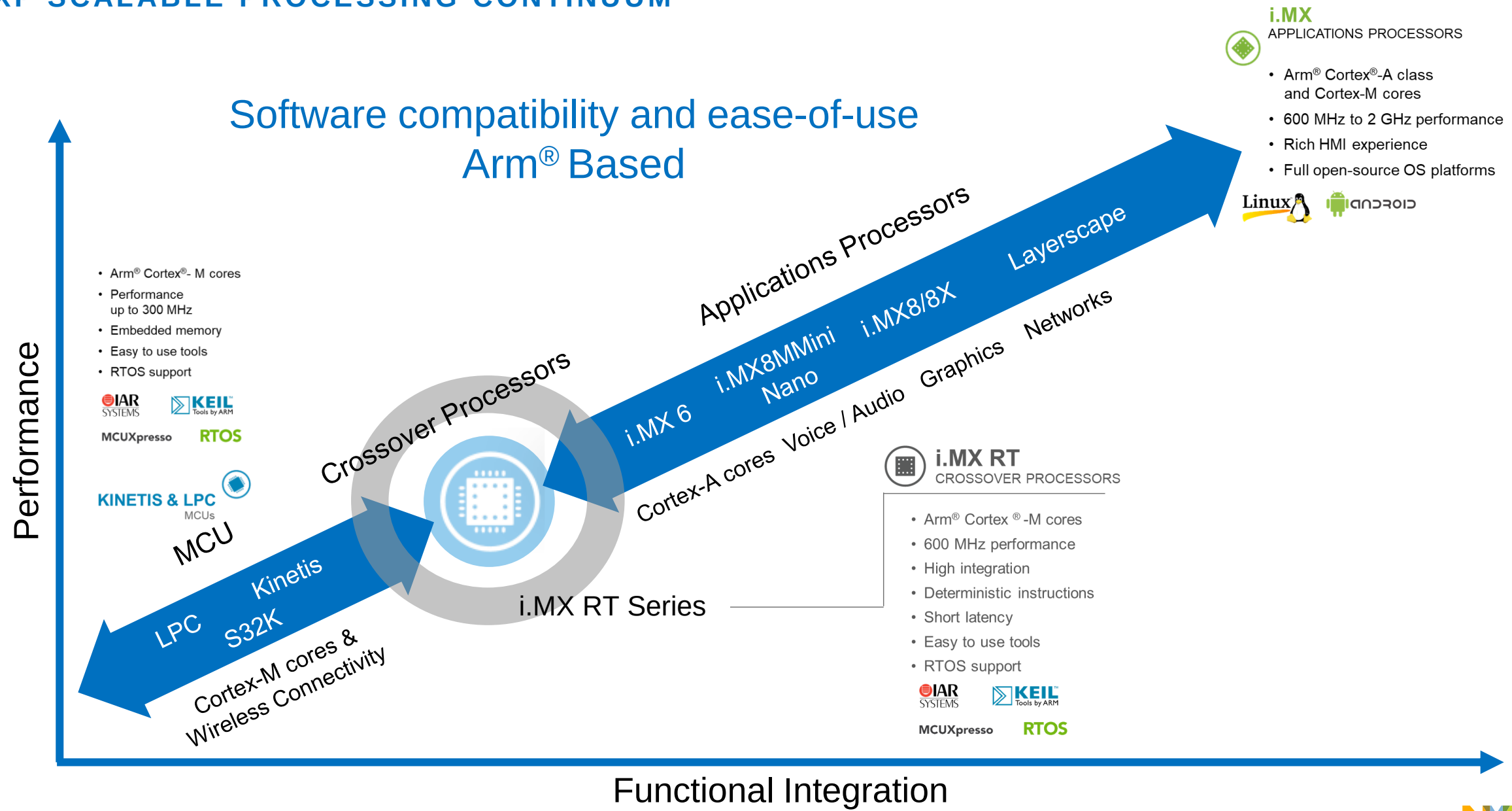
VUT BRNO
NXP LPC55S6X

NOV 2023
TOMAS VODA

SECURE CONNECTIONS
FOR A SMARTER WORLD

PUBLIC

NXP SCALABLE PROCESSING CONTINUUM



LPC55Sxx

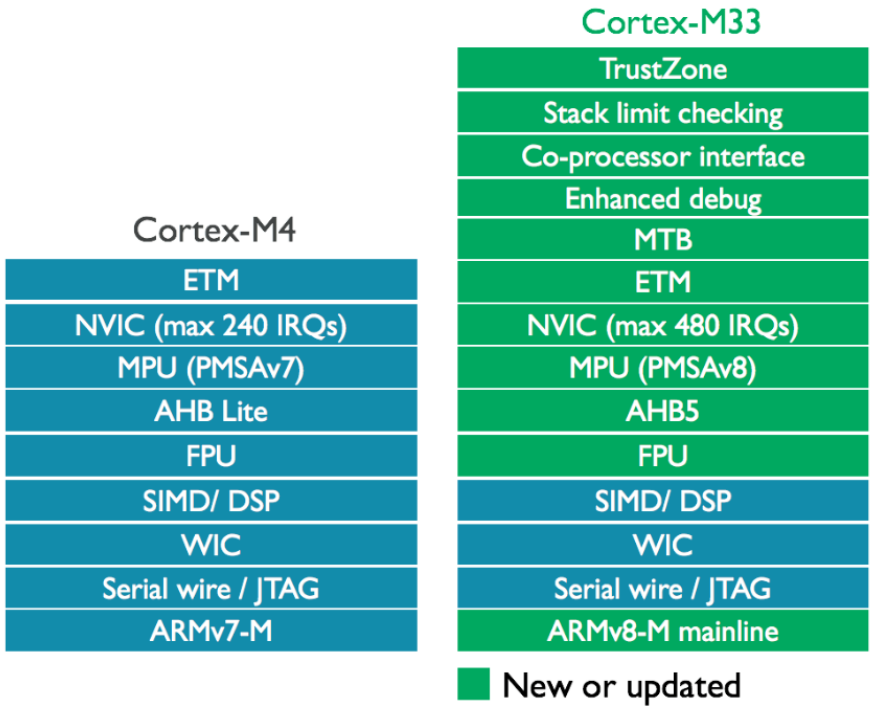
SECURE CONNECTIONS
FOR A SMARTER WORLD

Key Features and Comparisons

- Nearly 20% performance improvement over Cortex-M4 based MCUs (over 50% vs Cortex-M23) with redesigned pipeline - up to two instructions per clock cycle

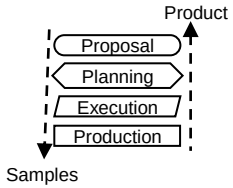
	Cortex-M0+	Cortex-M23	Cortex-M3	Cortex-M4	Cortex-M33
DMIPS/MHz	0.95	0.98	1.25	1.25	1.50
CoreMark®/MHz	2.46	2.50	3.32	3.40	4.02

- Tightly coupled accelerators with coprocessor interface & extensions (Arm's single precision FPU along with NXP accelerators)
- TrustZone for system-wide, secure resource isolation enabling trusted runtime execution and physical protection in embedded MCU applications



LPC5500 MCU SERIES ROADMAP

Arm CM7 | Arm CM33 | Arm CM4



COMMON PLATFORM ARCHITECTURE
SCALABILITY, PERFORMANCE & AREA EFFICIENCY

Advanced

Balanced

Power Efficiency

Next Generation Integration

psacertified™ level three

LPC553x/S3x

150 MHz Cortex-M33 w/ TZ
Up to 256KB Flash, 128KB SRAM
Advanced Analog/Timers, CAN-FD
Opt. Advanced Security

LPC55S6x

150 MHz Cortex-M33 with TrustZone
640KB Flash, 320KB SRAM
Dual-core, PowerQuad, SDIO
Advanced Security

LPC552x/S2x

150 MHz Cortex-M33
Up to 512KB Flash, 256KB SRAM
FS & HS USB, SDIO
Opt. Advanced Security

psacertified™ level two

LPC551x/S1x

150 MHz Cortex-M33 w/ TZ
Up to 256KB Flash, 96KB SRAM
FS & HS USB, CAN-FD
Opt. Advanced Security

LPC550x/S0x

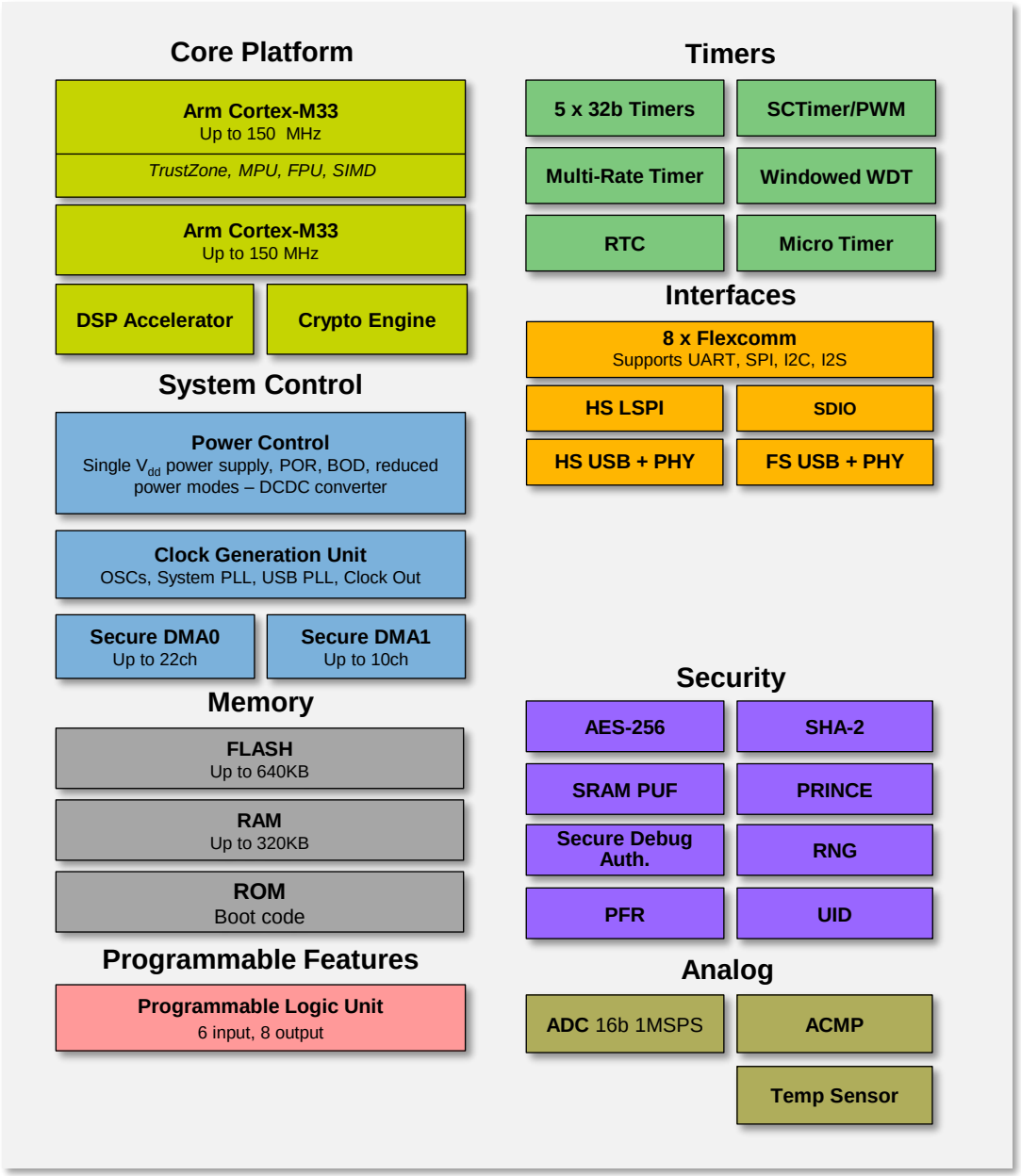
96 MHz Cortex-M33 w/ TZ
Up to 256KB Flash, 96KB SRAM
CAN-FD
Opt. Advanced Security

2019 | 2020 | 2021 - 2022

LPC5500 MCU SERIES OVERVIEW

	LPC550x/S0x	LPC551x/S1x	LPC552x/S2x	LPC553x/S3x	LPC55S6x
Cortex-M33 Max Frequency	Up to 96MHz	Up to 150MHz	Up to 150MHz	Up to 150MHz & 8KB Cache	Up to 150MHz (w 2nd M33)
Accelerators/ Co-proccessors	Crypto Accelerator	Crypto Accelerator	Crypto Accelerator	PowerQuad DSP, PKC	PowerQuad DSP, Crypto Accelerator
Flash	Up to 256 KB	Up to 256 KB	Up to 512KB	Up to 256KB	Up to 640KB
SRAM	Up to 96KB	Up to 96KB	Up to 256KB	Up to 112kB w Parity + 16kB ECC	Up to 320 KB
Security	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	CSS, TrustZone,HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR	TrustZone, HW SRAM PUF, Debug Authentication, real-time encryption/ decryption, TRNG, Secure boot, SHA-2, AES-256, PFR
CoreMarks	384	600	600	625	1150+ (Dual-core)
Serial Interfaces	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI	Up to 8 FlexComm supporting USART, SPI, I2C and I2S. 1x HS LSPI
USB	-	USB FS w/PHY	USB FS w/PHY, USB HS w/PHY	USB FS w/PHY	USB FS w/PHY, USB HS w/PHY
SDIO	-	-	SDIO/SD/MMC	-	SDIO/SD/MMC
FlexSPI				Support 2 SPI Flash or 1 Flash + 1 PSRAM	
CAN	CAN FD/ CAN 2.0	CAN FD/CAN 2.0	-	CAN FD/CAN 2.0	-
ADC	2x 16b 2 Msps	2x 16b 2 Msps	2x 16b 1 Msps	4x 16b 2 Msps (4x12b 3.13Msps)	2x 16b 1 Msps
GPIO	Up to 45	Up to 64	Up to 64	Up to 66	Up to 64
Active Power Consumption	32uA/MHz	32uA/MHz	32uA/MHz	57uA/MHz	32uA/MHz
Packages	HTQFP64, HVQFN48	HTQFP64, HLQFP100, VFBGA98	HTQFP64, HLQFP100, VFBGA98	HTQFP64, HLQFP100, QFN48	HTQFP64, HLQFP100, VFBGA98

LPC55S6X BLOCK DIAGRAM



Core Platform

- Dual core Up to 150MHz Cortex-M33
  - Core 0:TrustZone, MPU, FPU, SIMD, DSP
  - Core 1: co-processor w/o extensions
- DSP Accelerator (PowerQUAD, w CP intf)
- CASPER crypto co-processor
- Secure Multilayer Bus Matrix

Memory

- Up to 640KB FLASH bank
- Up to 320KB RAM
- ROM

Timers

- 5 x 32b Timers
- SCTimer/PWM
- Multi-Rate Timer
- Windowed Watchdog Timer
- RTC
- Micro Timer
- OS Event Timer

Analog

- 16b ADC up to 10 ch
- Temperature Sensor
- Analog Comparator

Packages

- VFBGA98, HLQFP64, HLQFP100

Advanced Security

- AES-256 encryption/decryption engine
- SHA-2
- RNG
- mbedTLS library HW accelerated
- SRAM PUF for Key Generation support
- PRINCE real-time Encrypt/Decrypt for flash
- Debug authentication
- Protected Flash Region (PFR)
- Secure GPIO

Interfaces

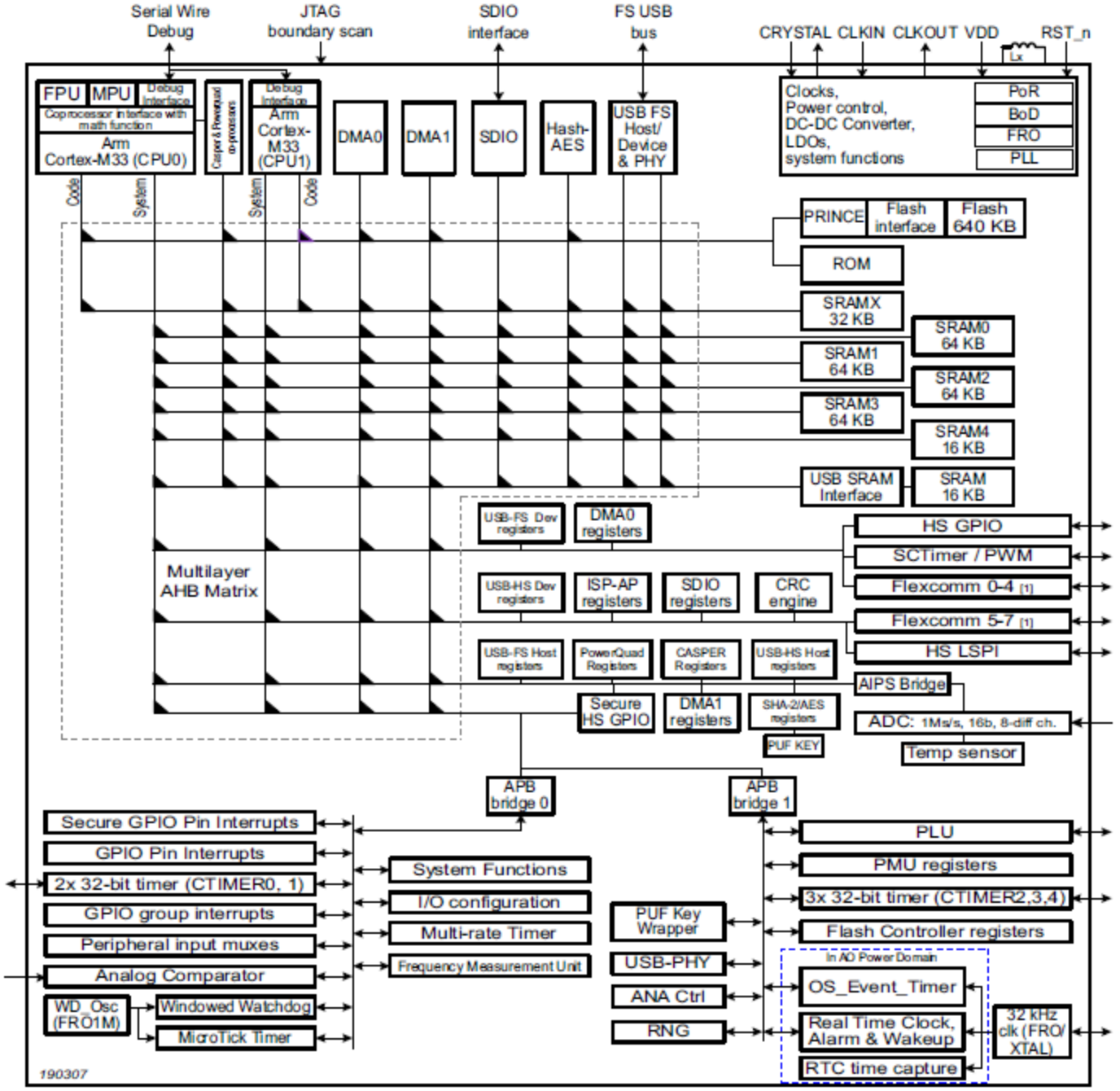
- USB High-speed, on-chip PHY
- USB Full-speed (H/D), Crystal-less, on-chip PHY
- 1 x High-Speed SPI up to 50MHz (HS SPI)
- 8 x Flexcomms each supports SPI, I2C, UART, I^2S

Clock generation

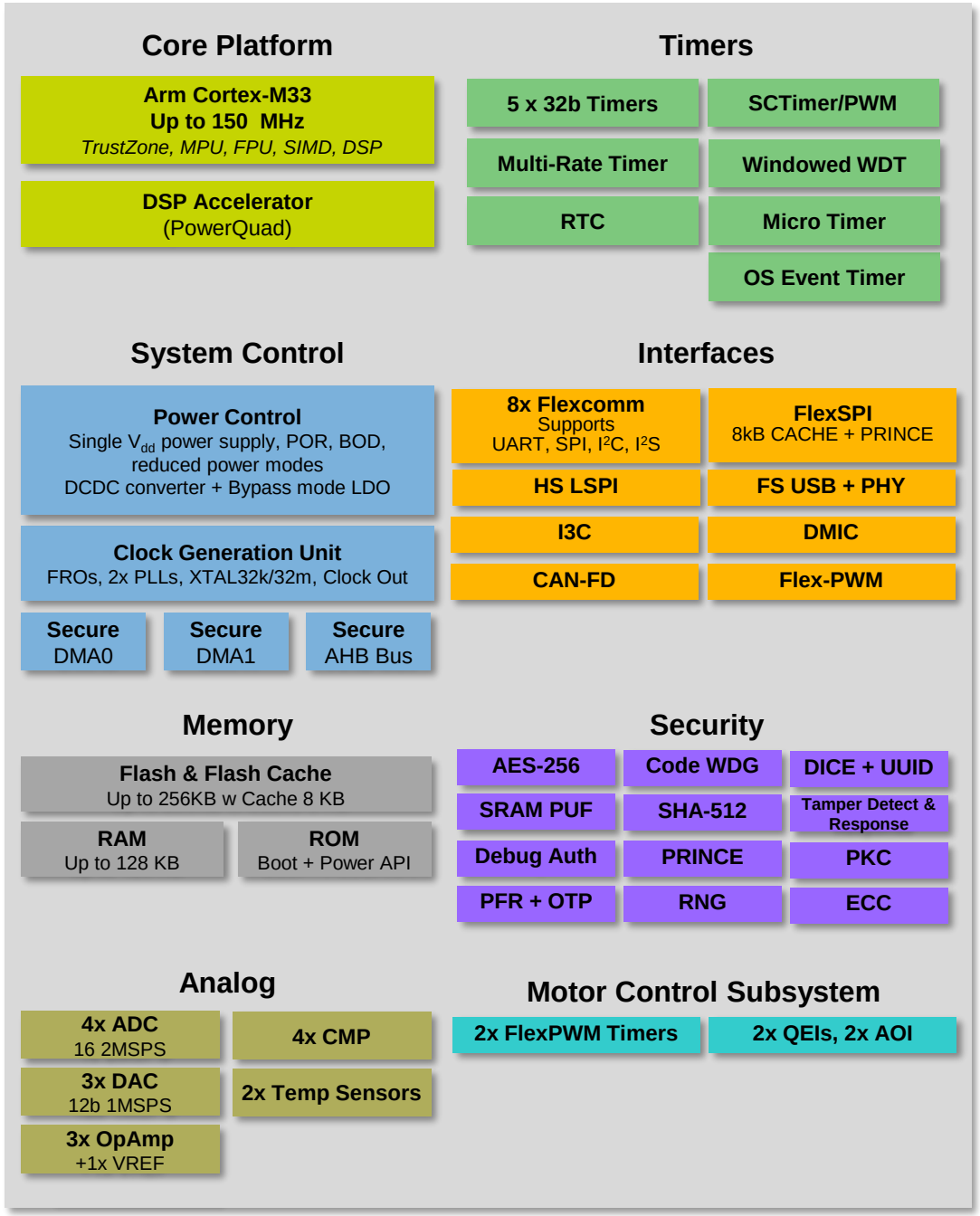
- FRO 96/12MHz - trimmed to +/- 1% accuracy
- FRO 32kHz - trimmed to +/- 1% accuracy
- FRO 1MHz
- XTAL input 1-25MHz
- XTAL input 32 768 Hz
- PLL0/PLL1

Other

- Buck DC-DC
- Operating voltage: 1.8 to 3.6V
- Temperature range: -40 to 105 °C


Serial Wire Debug
JTAG boundary scan
SDIO interface
FS USB bus
CRYSTAL CLKIN CLKOUT VDD RST_n
FPU
MPU
Debug Interface
Coprocessor interface with math function
Arm Cortex-M33 (CPU0)
Casper & Powerquad co-processors
Debug Interface
Arm Cortex-M33 (CPU1)
DMA0
DMA1
SDIO
Hash-AES
USB FS Host/ Device & PHY
Clocks, Power control, DC-DC Converter, LDOs, system functions
PoR
BoD
FRO
PLL
Code
System
System
Code
PRINCE
Flash interface
Flash 640 KB
ROM
SRAMX 32 KB
SRAM0 64 KB
SRAM1 64 KB
SRAM2 64 KB
SRAM3 64 KB
SRAM4 16 KB
USB SRAM Interface
SRAM 16 KB
USB-FS Dev registers
DMA0 registers
HS GPIO
SCTimer / PWM
Flexcomm 0-4 [1]
Flexcomm 5-7 [1]
HS LSPI
AIPS Bridge
ADC: 1Ms/s, 16b, 8-diff ch.
Temp sensor
Multilayer AHB Matrix
USB-HS Dev registers
ISP-AP registers
SDIO registers
CRC engine
USB-FS Host registers
PowerQuad Registers
CASPER Registers
USB-HS Host registers
Secure HS GPIO
DMA1 registers
SHA-2/AES registers
PUF KEY
APB bridge 0
APB bridge 1
Secure GPIO Pin Interrupts
GPIO Pin Interrupts
2x 32-bit timer (CTIMER0, 1)
GPIO group interrupts
Peripheral input muxes
Analog Comparator
WD_Osc (FRO1M)
Windowed Watchdog
MicroTick Timer
System Functions
I/O configuration
Multi-rate Timer
Frequency Measurement Unit
PUF Key Wrapper
USB-PHY
ANA Ctrl
RNG
PLU
PMU registers
3x 32-bit timer (CTIMER2,3,4)
Flash Controller registers
In AO Power Domain
OS_Event_Timer
Real Time Clock, Alarm & Wakeup
RTC time capture
32 kHz clk (FRO/ XTAL)
190307

LPC553X / LPC55S3X BLOCK DIAGRAM



Core Platform

- Up to 150MHz Cortex-M33
  - TrustZone, MPU, FPU, SIMD, DSP
- DSP Accelerator (PowerQUAD, w CP intf)
- Secure Multilayer Bus Matrix

Memory

- Up to 256KB FLASH bank
  - 8kB Low Power Cache
- Up to 128KB RAM
  - 112KB with parity check
  - 16KB ECC RAM
- ROM

Timers

- 5 x 32b Timers
- SCTimer/PWM
- Muiti-Rate Timer
- Windowed Watchdog Timer
- RTC with Calendar function
- Micro Timer
- OS Event Timer

Analog

- 4x 16b ADC (Single ended) up to 23 ch
  - 2M sps 16bit
  - 3.3M sps 12bit
  - Up to 8 Differential/ 16 Single Ended channels
- Temperature Sensor
- 3x Analog Comparator
- 3x 12b 1Msps DAC
- 3x OpAmp

Packages

- HVQFN48, HLQFP64, HLQFP100
  - VFBGA98 and CSP upon request

Advanced Security

- AES-256, SHA-2, RNG
- ECC-256 (ECDSA, ECDH)
- PKC (Math accelerator)
- SRAM PUF for Key Generation support
- PRINCE real-time Encrypt/Decrypt for SPI flash
- Debug authentication
- Protected Flash Region (PFR)
- DICE and UID
- Code Watchdog IP (CodeWDG)
- Anti-tampering and Glitch Detector

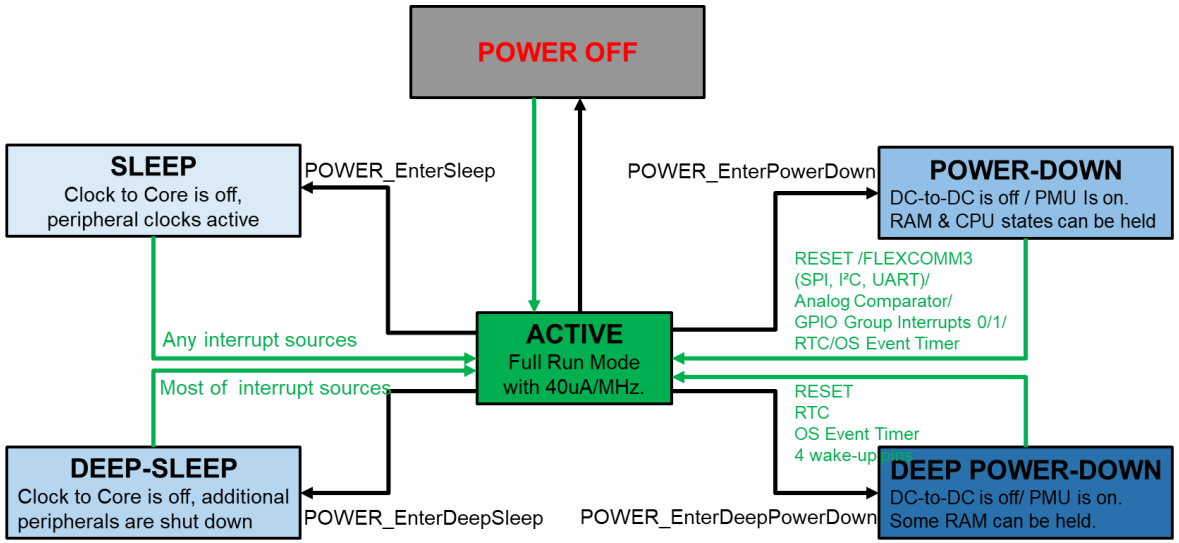
Interfaces

- USB Full-speed (H/D), Crystal-less
- 1 x High-Speed SPI up to 50MHz (HS SPI)
- 8 x Flexcomms each supports SPI, I2C, UART, I2S
  - I2S Pin-sharing
- External SPI -FlexSPI Interface support XIP
  - Octal/Quad Flash
  - with 8kCache
  - PRINCE to encrypt & decrypt on the fly
- 1x CAN-FD
- 1x I3C
- 1x DMIC 2 ch
- 2x FlexPWM with 4 sub-modules, providing 12 PWM outputs
- 2x Quadrature Encoder/Decoder (QEI)

Other

- Buck DC-DC
- Operating voltage: 1.8 to 3.6V
- Two Main IO supplies (VDDIO_1: 1.8 V to 3.6 V, VDDIO_2: 1.08 v to 3.6 V).
- Temperature range: -40 to 105 °C

POWER MODES



Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M33 (CPU0) in active mode; ARM Cortex-M33 (CPU1) in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down					
		CCLK = 12 MHz	[2][3][3]	-	0.9	-	mA
		CCLK = 48 MHz	[2][3][3]	-	2.1	-	mA
		CCLK = 60 MHz	[2][3][3]	-	2.3	-	mA
		CCLK = 96 MHz	[2][3][3]	-	3.4	-	mA
		CCLK = 100 MHz	[3][3][4]	-	3.5	-	mA
		CCLK = 150 MHz	[3][3][4]	-	6.2	-	mA

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M33 (CPU0) in sleep mode; ARM Cortex-M33 (CPU1) OFF (in reset, clock disabled)							
I_{DD}	supply current	CCLK = 12 MHz, PLL disabled	[1][2]	-	0.7	-	mA
		CCLK = 96 MHz, PLL disabled	[2][3]	-	2.7	-	mA

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode; all SRAM on T_{amb} = 25 °C, VBAT_DCDC = 3.0 v	[2]	-	110	135	µA
		T_{amb} = 25 °C, VBAT_DCDC = 1.8 v	[2]	-	148	191	µA
		T_{amb} = 105 °C, VBAT_DCDC = 3.0 v		-	-	<tbd>	µA
		Power-down mode.	[2]				
		SRAM_X2 (4 KB) powered T_{amb} = 25 °C, VBAT_DCDC = 3.0 v		-	3.9	4.5	µA
		SRAM_X2 (4 KB) powered T_{amb} = 105 °C, VBAT_DCDC = 3.0 v		-	-	<tbd>	µA
		SRAM_X2 and SRAM_X3 (8 KB) powered T_{amb} = 25 °C, VBAT_DCDC = 3.0 v		-	4.0	-	µA
		320 KB full retention T_{amb} = 25 °C, VBAT_DCDC = 3.0 v		-	13	15	µA
		320 KB full retention T_{amb} = 25 °C, VBAT_DCDC = 3.6 v		-	14	16	µA
		320 KB full retention T_{amb} = 105 °C, VBAT_DCDC = 3.0 v		-	-	<tbd>	µA
		Deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled, 4 KB SRAM powered) T_{amb} = 25 °C. VBAT_DCDC = 3.0 v	[2]	-	590	750	nA
		T_{amb} = 105 °C, VBAT_DCDC = 3.0 v		-	-	<tbd>	µA
		RTC oscillator running with external crystal (4 KB SRAM powered)		-	790	-	nA

SDK & Ecosystem

SECURE CONNECTIONS
FOR A SMARTER WORLD

THE MCUXPRESSO ECOSYSTEM

Core Technologies from NXP

- MCUXpresso SDK
- MCUXpresso Config Tools
- For Arm® Cortex-M®
  - MCUXpresso IDE
  - MCUXpresso Secure Provisioning Tool

Enabling Software Technologies

- Run time software libraries and middleware
- Enable customers to focus on differentiation
- From NXP and partners

Enabling Tools Technologies

- Partner IDEs
- Debug Probes
- Development Boards
- From NXP and partners

MCUXpresso Software and Tools

for General Purpose MCUs and Crossover processors

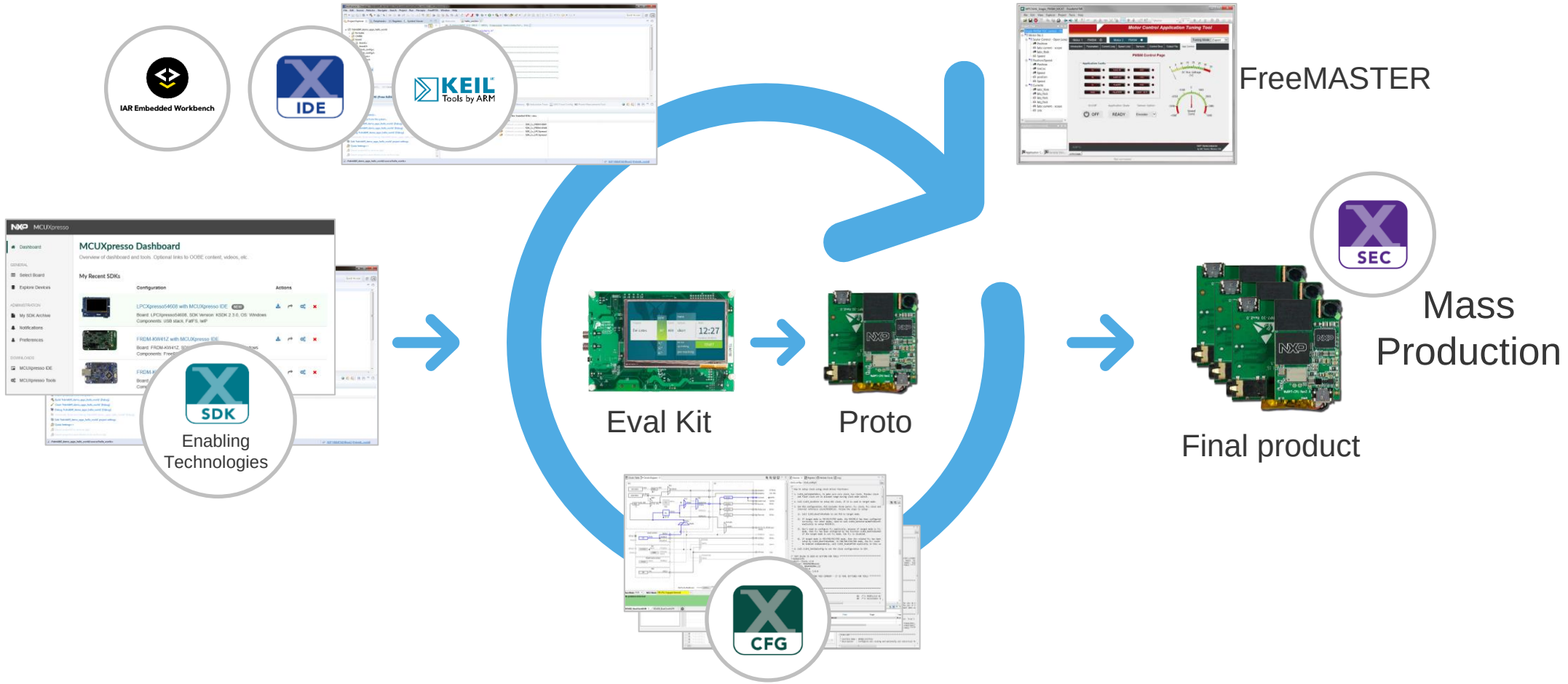
MCUXpresso IDE
Edit, compile, debug and optimize in an intuitive and powerful IDE

MCUXpresso SDK
Runtime software including peripheral drivers, middleware, RTOS, demos and more

MCUXpresso Config Tools
Online and desktop tool suite for system configuration and optimization

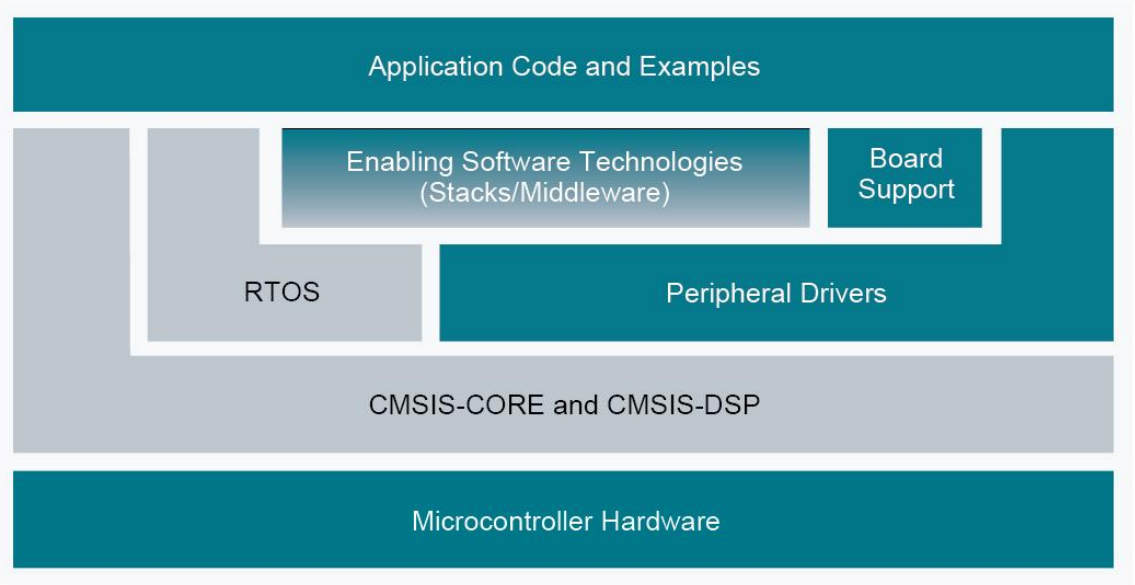
MCUXpresso Secure Provisioning Tool
Graphical and command line tool for securely provisioning and programming MCUs with secure boot

STREAMLINED MCUXPRESSO DEVELOPMENT FLOW



www.nxp.com/mcuxpresso/sdk

MCUXPRESSO SDK
SOFTWARE FRAMEWORK AND DRIVERS



Architecture:
- CMSIS-CORE compatible
- Single driver for each peripheral
- Transactional APIs w/ optional DMA support for communication peripherals

Integrated RTOS options:
- Azure RTOS ThreadX
- FreeRTOS
- RTOS-native driver wrappers

Enabling SW Technologies:
- Connectivity (wired/wireless)
- HMI (Graphics, Voice, Touch)
- Audio
- Motor Control
- eIQ Machine Learning
- Cloud connectivity
- Accelerators and specialized peripherals
- Safety
- Security
- Storage

Reference Software:
- Peripheral driver usage examples
- Application demos
- Azure RTOS and FreeRTOS usage demos
- IoT connectivity examples

License:
- BSD 3-clause for startup, drivers, USB stack
- All code Black Duck scanned

Download options:
- Custom SDK web builder for optimized download size
- Direct download within MCUXpresso
- GitHub repository leveraging community engagement
- CMSIS Packs for supported toolchains

Toolchains:
- MCUXpresso IDE
- IAR®, ARM® Keil®, GCC w/ Cmake

Quality:
- Production-grade software
- Consistent API architecture across all releases
- MISRA 2012 compliance
- Checked with Coverity® static analysis tools
- Extensive Continuous Integration testing across range of compatible development boards, supported toolchains, and debug probes

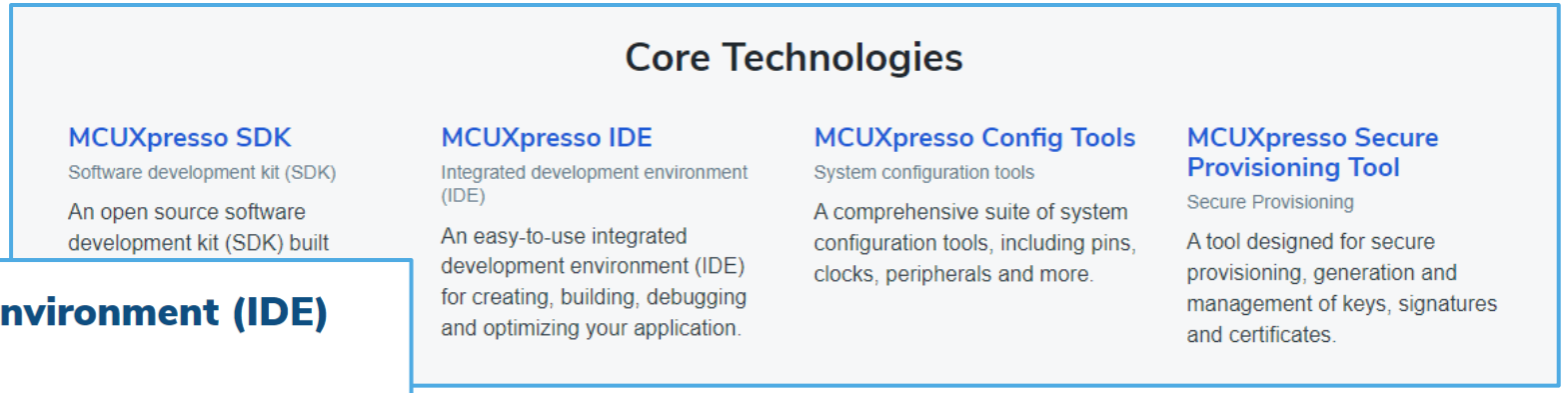
MCUXpresso Tools Install

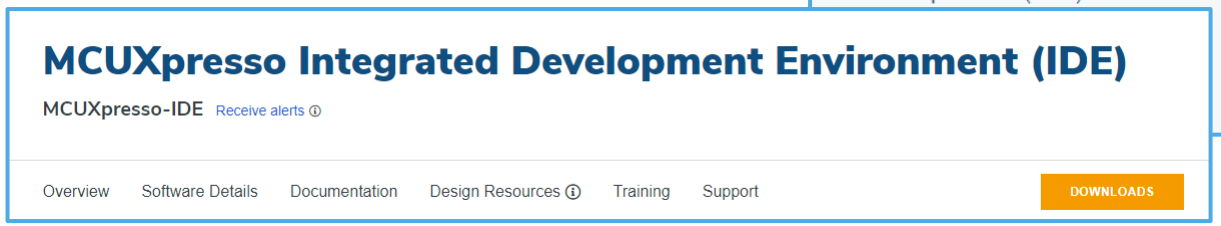
SECURE CONNECTIONS
FOR A SMARTER WORLD

MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- Install MCUXpresso IDE

www.nxp.com/mcuxpresso





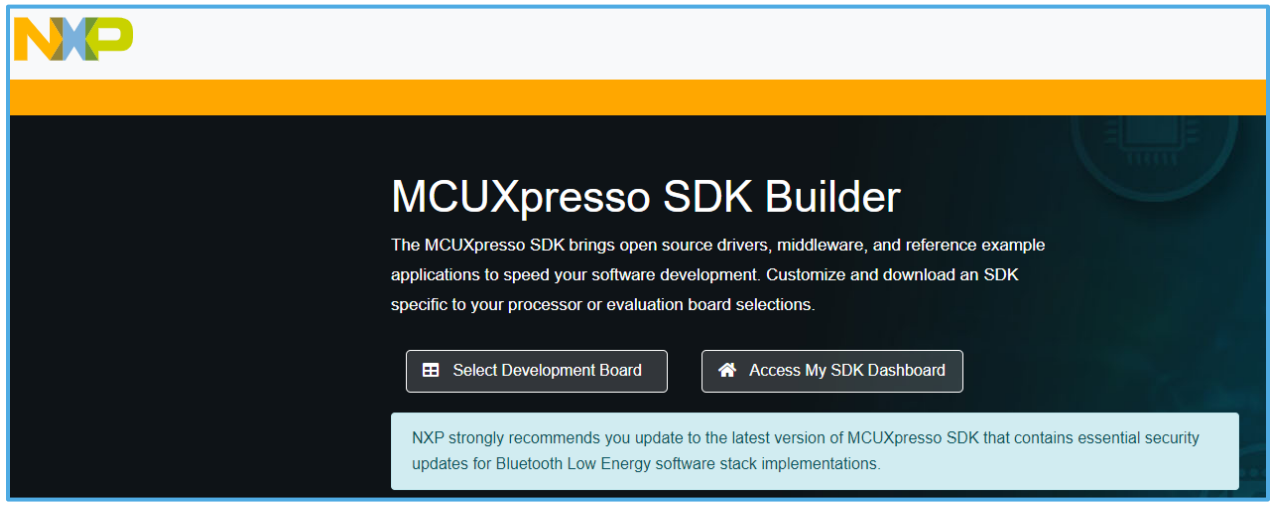
"MCUXpresso IDE includes Config Tools and SDK download Option inside"

- Install MCUXpresso Config Tools stand Alone (Optional)

- Download MCUXpresso SDK (Optional)

MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- MCUXpresso SDK Builder
- https://mcuxpresso.nxp.com/en/welcome



MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- Download SDK

Build SDK for LPCXpresso55S69

Generate a downloadable SDK archive for use with desktop MCUXpresso Tools.

Developer Environment Settings

Selections here (operating host system, toolchain or middleware) will impact files and examples projects included in the SDK and Generated Projects

Host OS

Toolchain / IDE

All

SDK Version 2.12.0 (released 2022-07-14)

SDK Tag REL_2.12.0_MAJOR_RFP

Search...

SELECT ALL

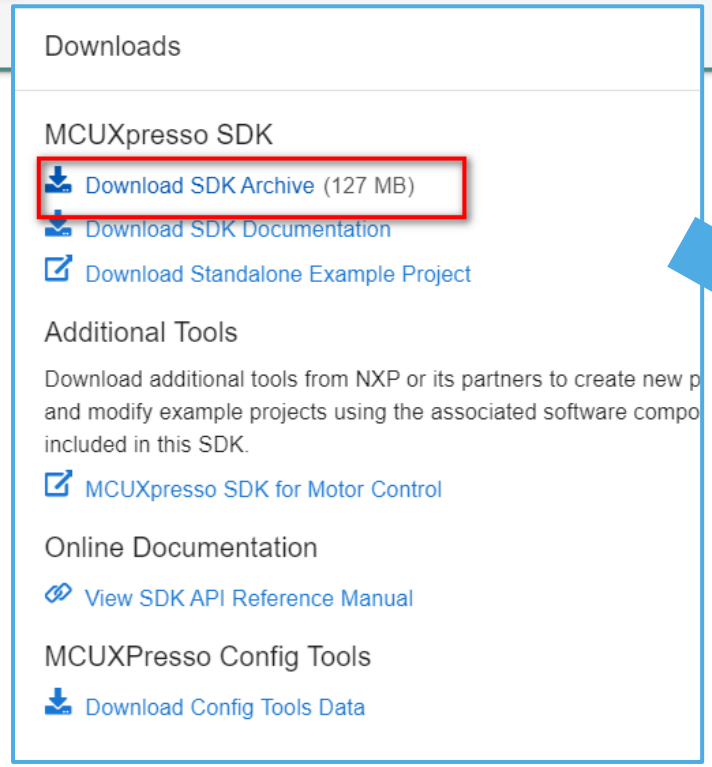
UNSELECT ALL

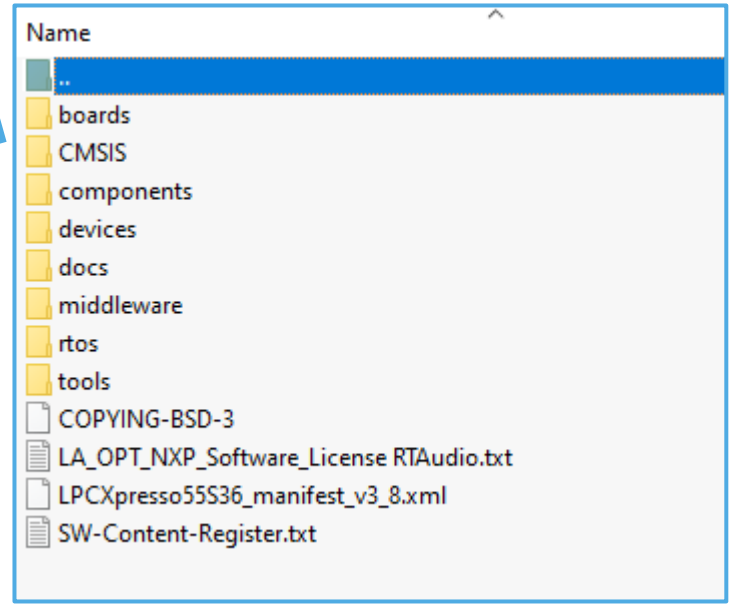
	Name	Category	Description	Dependencies
☑	multicore	Middleware	Multicore Software Development Kit	
☑	SDMMC Stack	Middleware	Stack supporting SD, MMC, SDIO	
☑	CMSIS DSP Library	CMSIS DSP Lib	CMSIS DSP Software Library	
☑	Embedded Wizard GUI	Middleware	Embedded Wizard GUI from TARA Systems	
☑	emWin	Middleware	emWin graphics library	
☑	Essential Audio Processing Library	Middleware	Essential Audio Processing Library (EAP) provides audio proc... (more)	
☑	Fatfs	Middleware	FAT File System stack	
☑	Azure RTOS *(7 selected)*	Azure RTOS		
☑	FreeRTOS *(2 selected)*	Real-time operating system for microcontrollers from Amazon		

DOWNLOAD SDK

MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

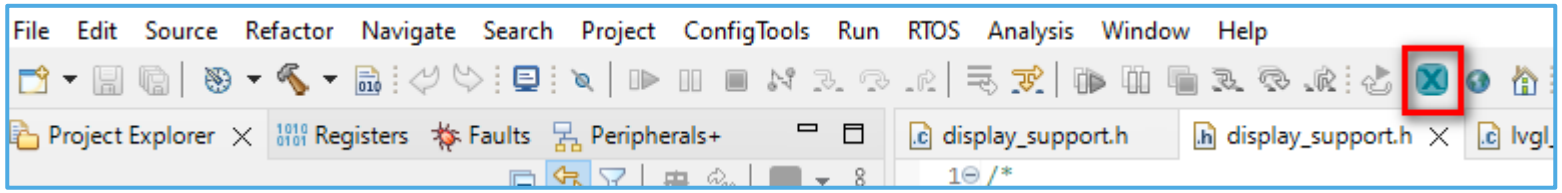
- Download SDK

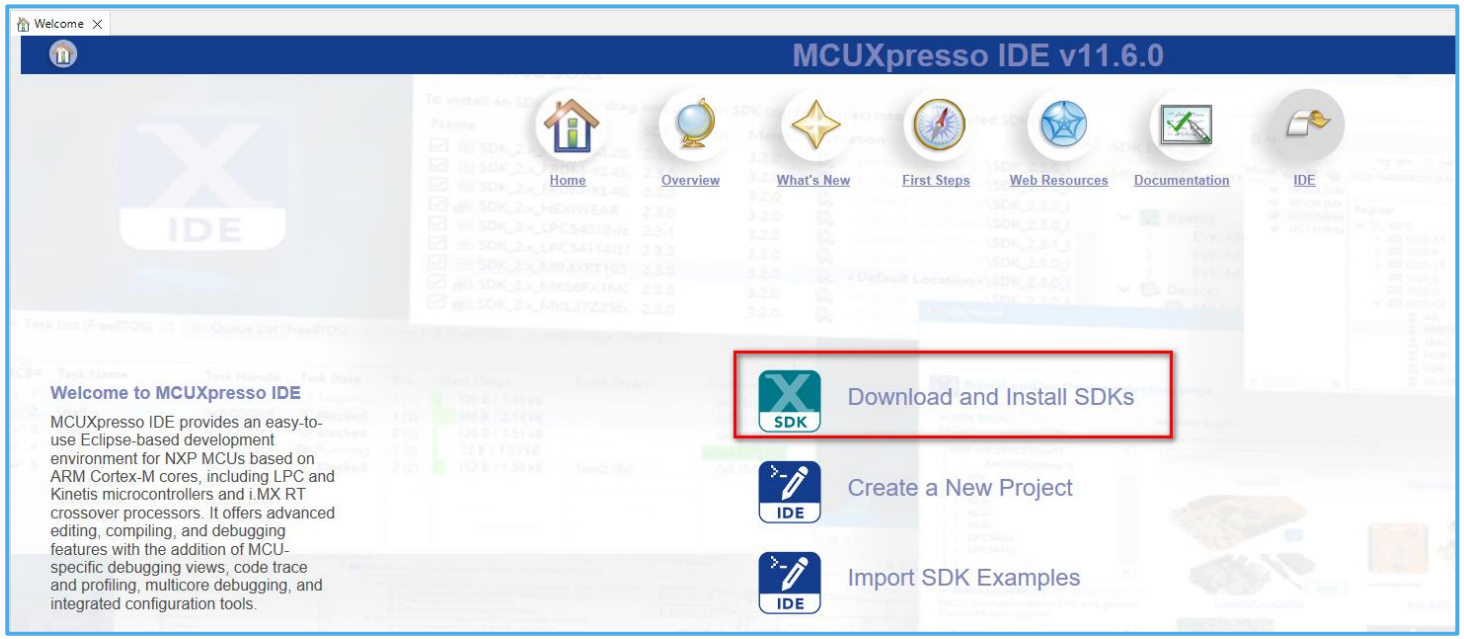




MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

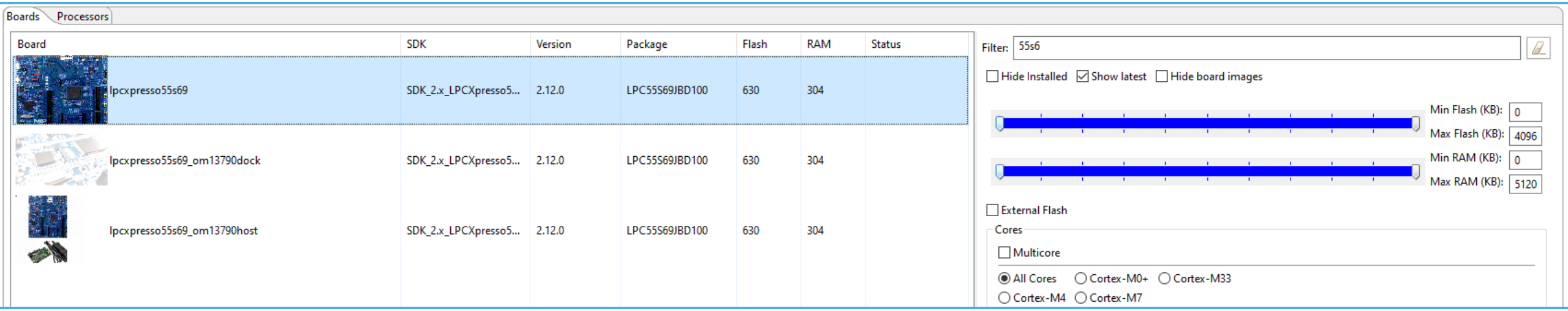
- Install SDK inside the IDE



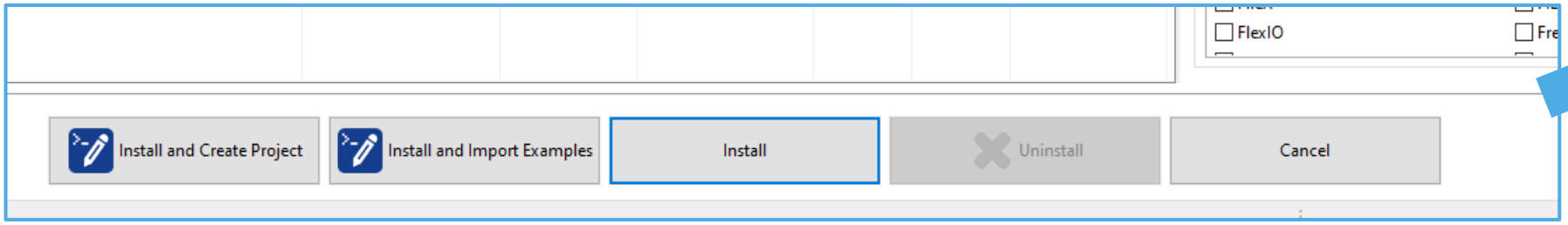


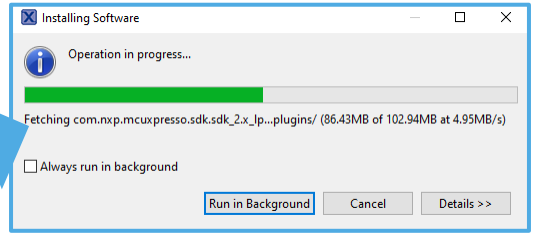
MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

- Filter: “55s6”
- Select the Board



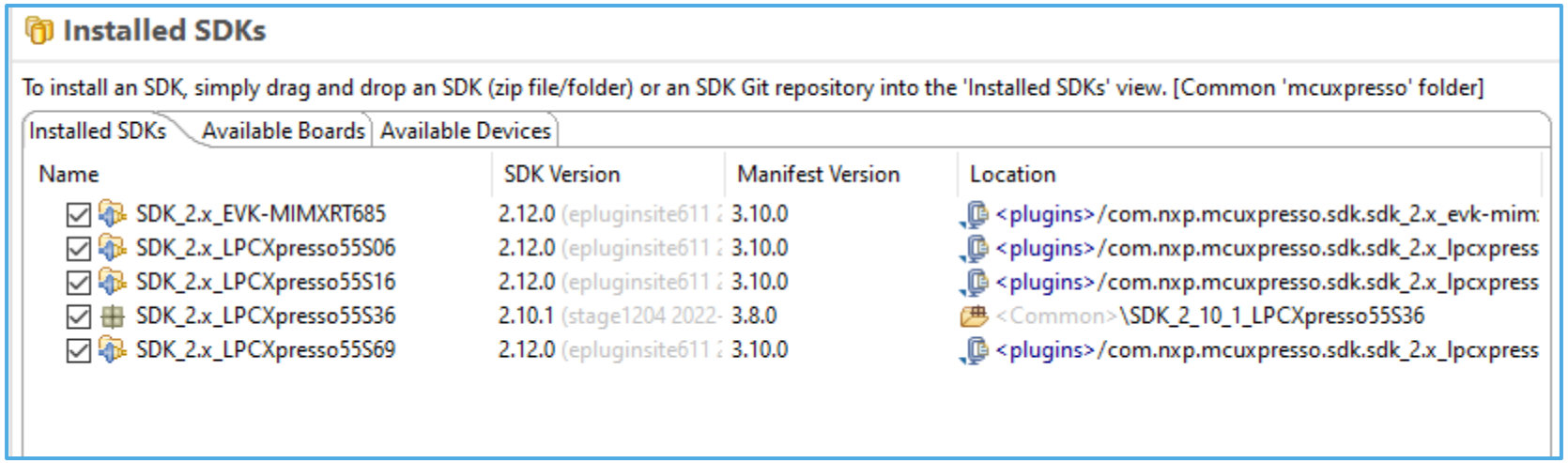
- Install





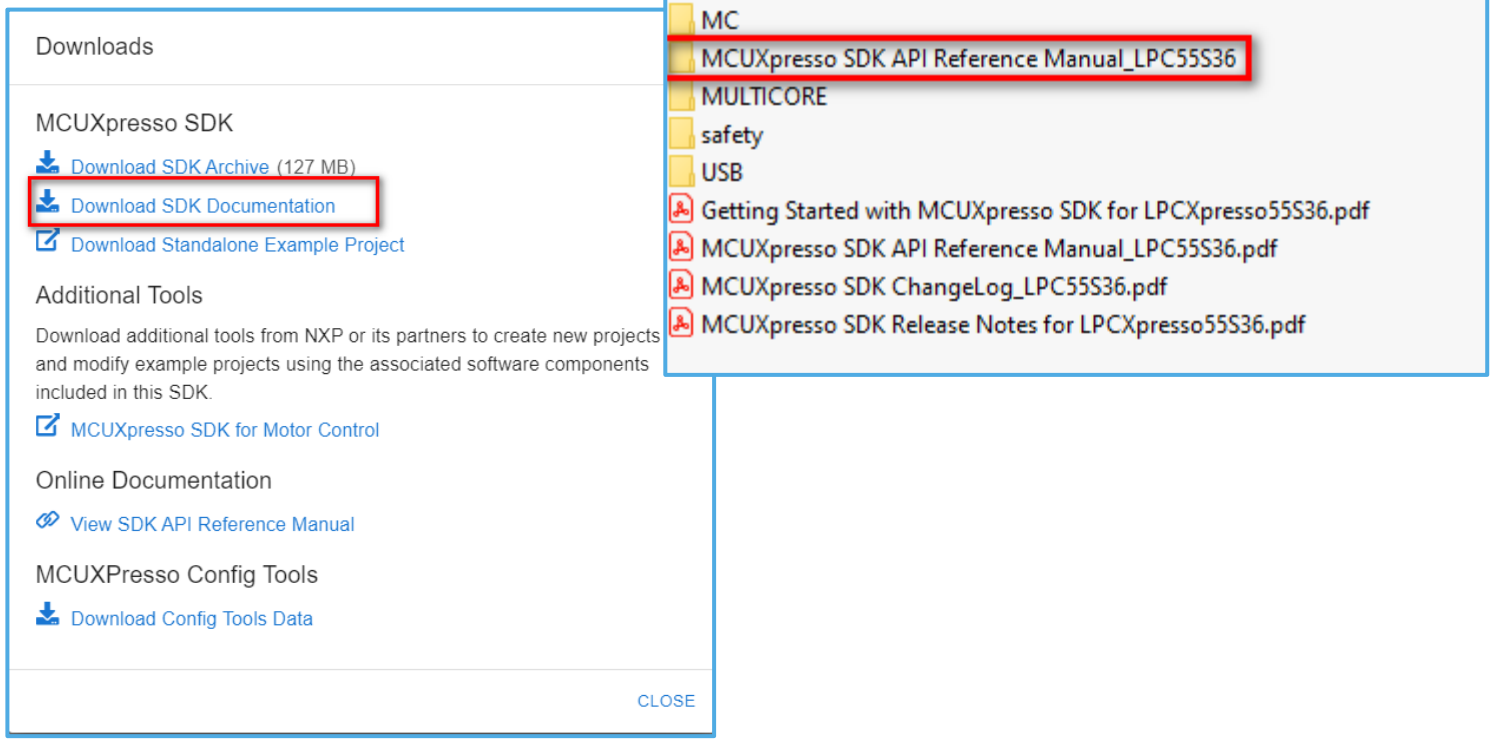
MCUXPRESSO TOOLS DOWNLOAD AND INSTALL

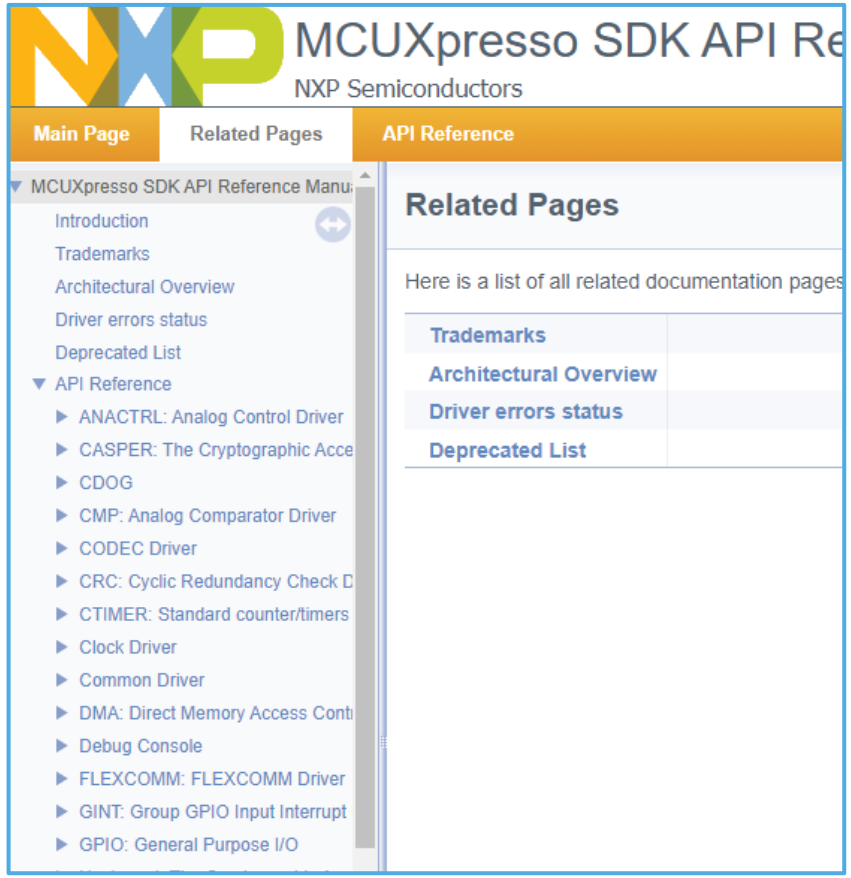
- Installed SDKs View



MCUXPRESSO SDK API

- Importing Demo code drivers will help to understand how to use API drivers.
- Download SDK Documentation



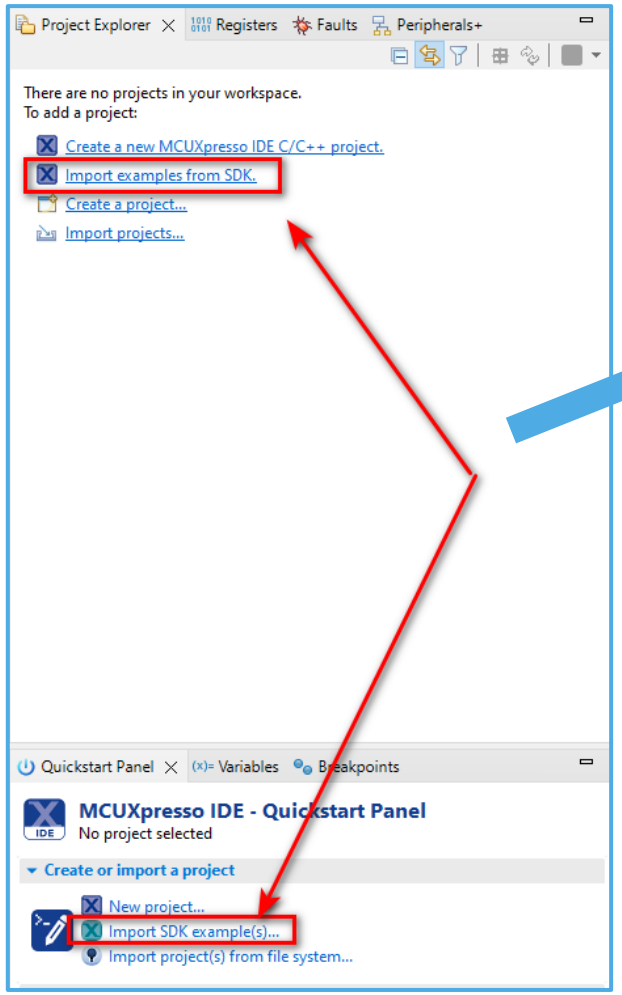


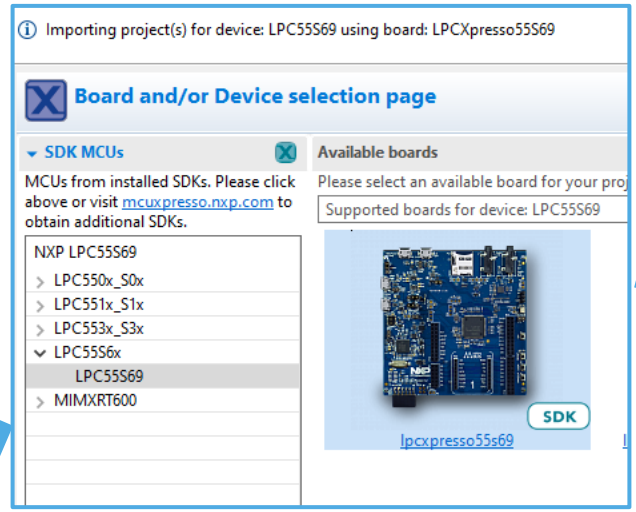
Project Import

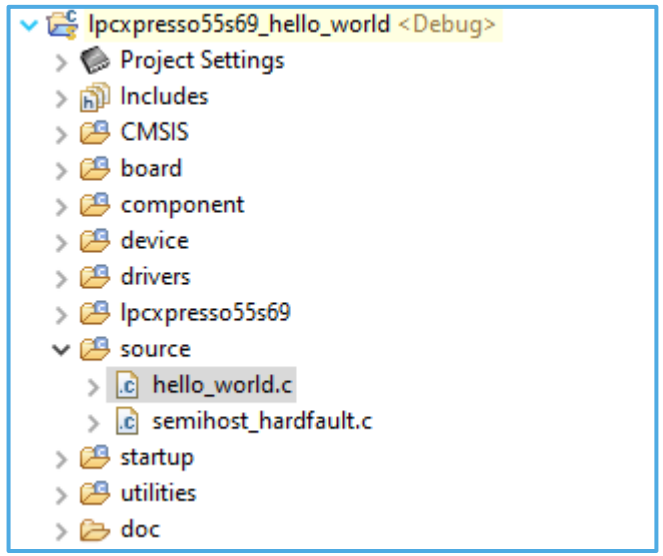
SECURE CONNECTIONS
FOR A SMARTER WORLD

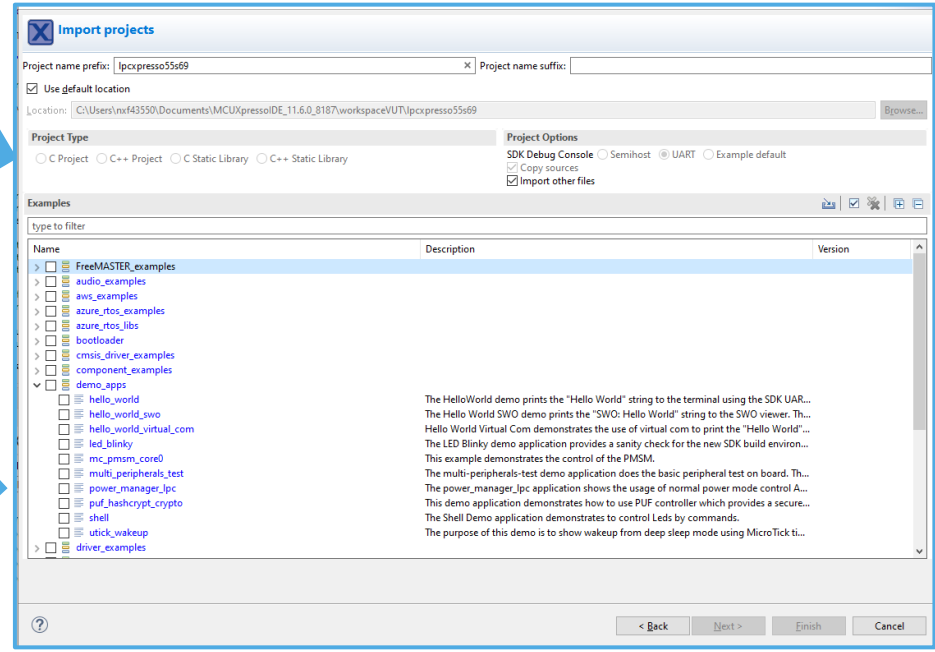
MCUXPRESSO PROJECT IMPORT

- Import Example from SDK



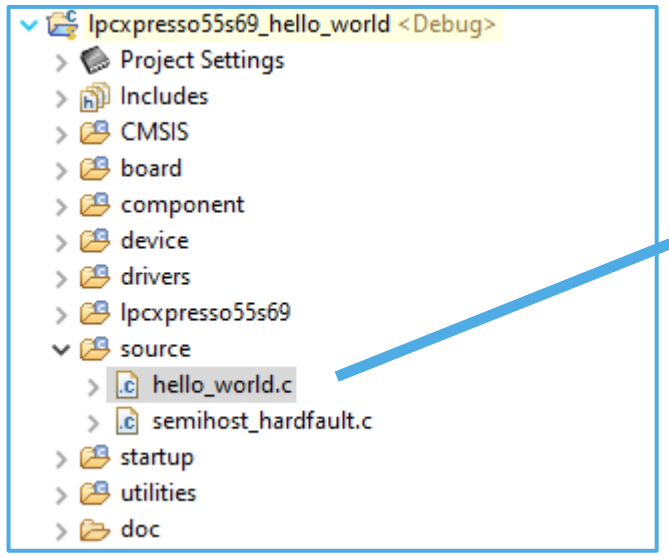






MCUXPRESSO PROJECT IMPORT

- Basic Baremetal Project



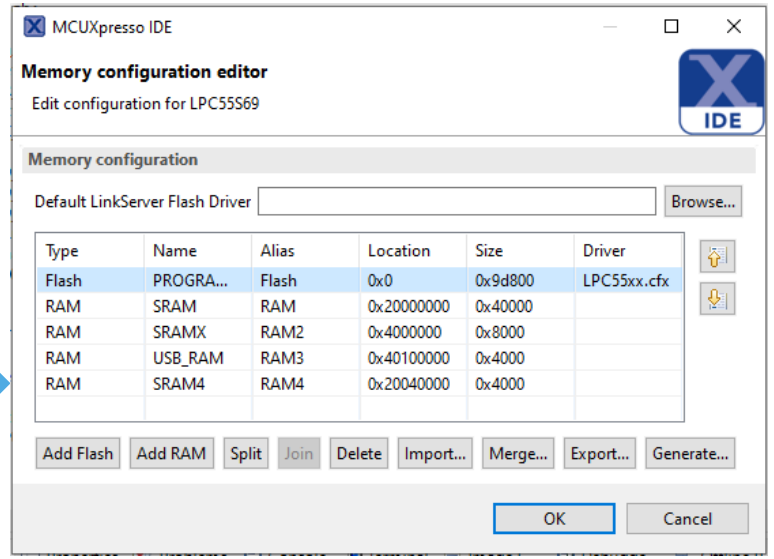

```c
int main(void)
{
    char ch;

    /* Init board hardware. */
    /* set BOD VBAT level to 1.65V */
    POWER_SetBodVbatLevel(kPOWER_BodVbatLevel1650mv, kPOWER_BodHystLevel50mv, false);
    /* attach main clock divide to FLEXCOMM0 (debug console) */
    CLOCK_AttachClk(BOARD_DEBUG_UART_CLK_ATTACH);

    BOARD_InitBootPins();
    BOARD_InitBootClocks();
    BOARD_InitDebugConsole();
#if !defined(DONT_ENABLE_FLASH_PREFETCH)
    /* enable flash prefetch for better performance */
    SYSCON->FMCCR |= SYSCON_FMCCR_PREFEN_MASK;
#endif

    PRINTF("hello world.\r\n");

    while (1)
    {
        ch = GETCHAR();
        PUTCHAR(ch);
    }
}
```

Project Main Settings review

SECURE CONNECTIONS
FOR A SMARTER WORLD

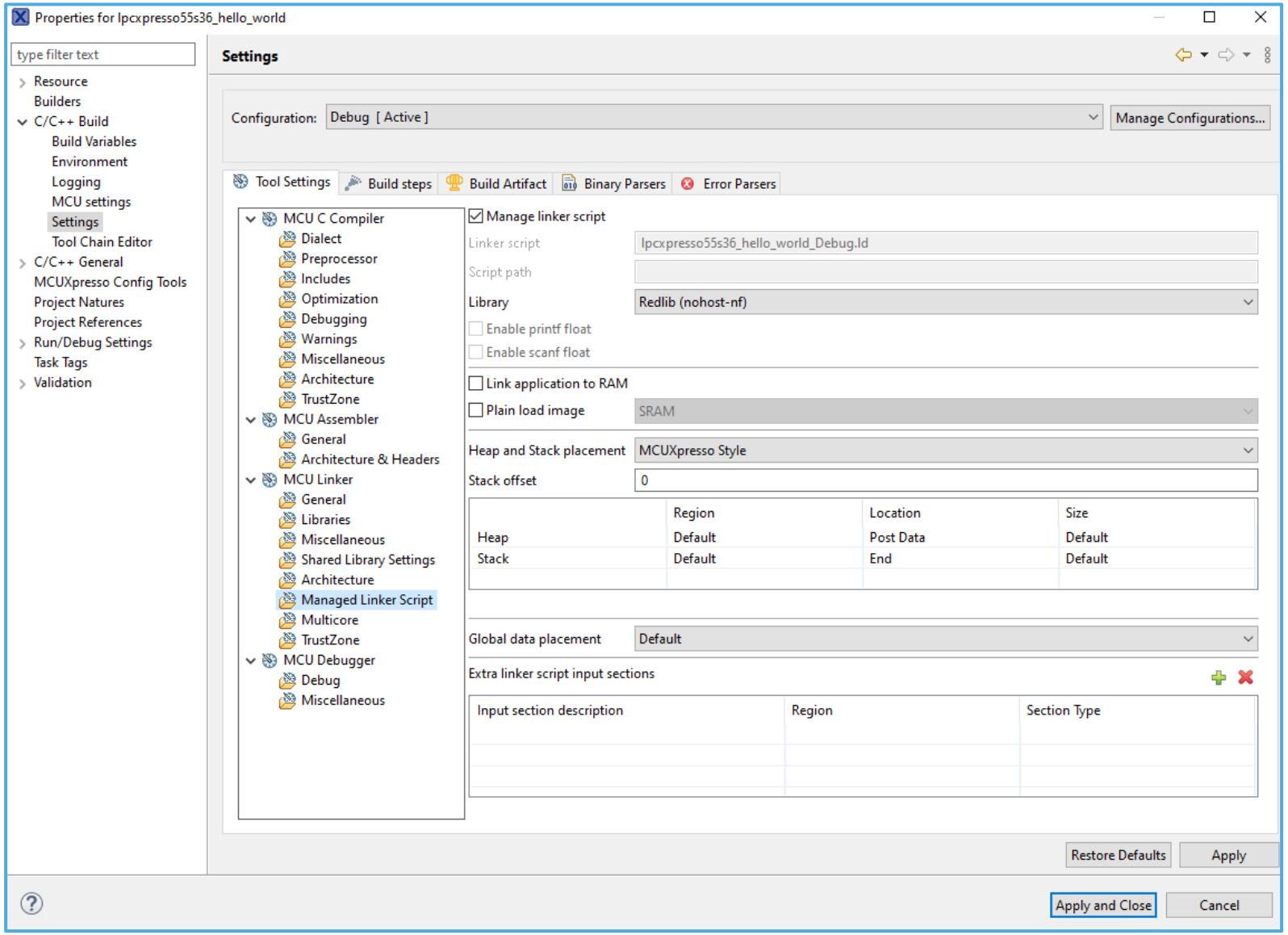
PROJECT SETTINGS

- Expand Project Settings in the Project Folder



PROJECT SETTINGS

- Managed Linker Script

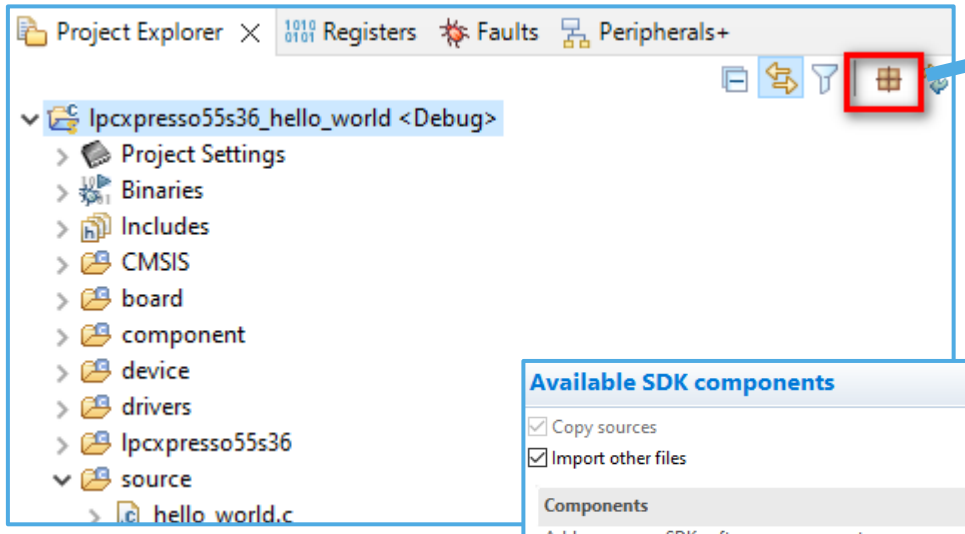


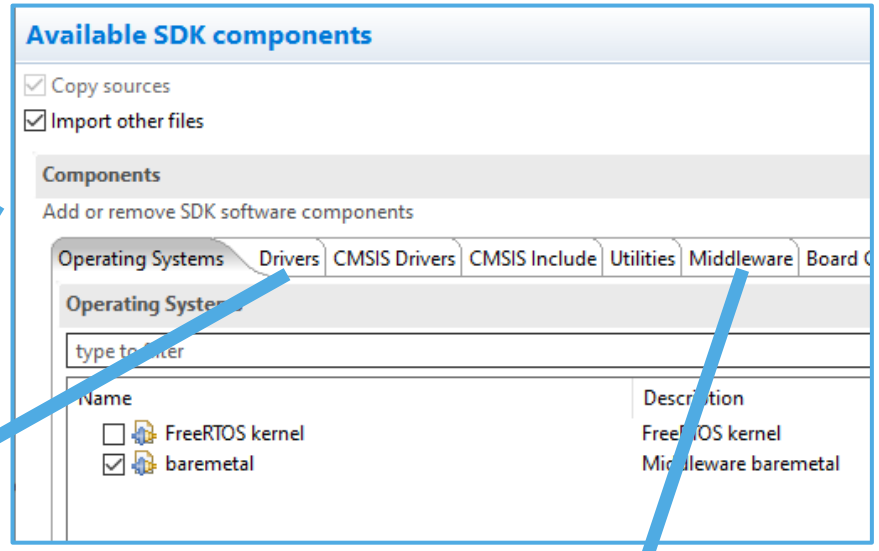
Project SDK Components

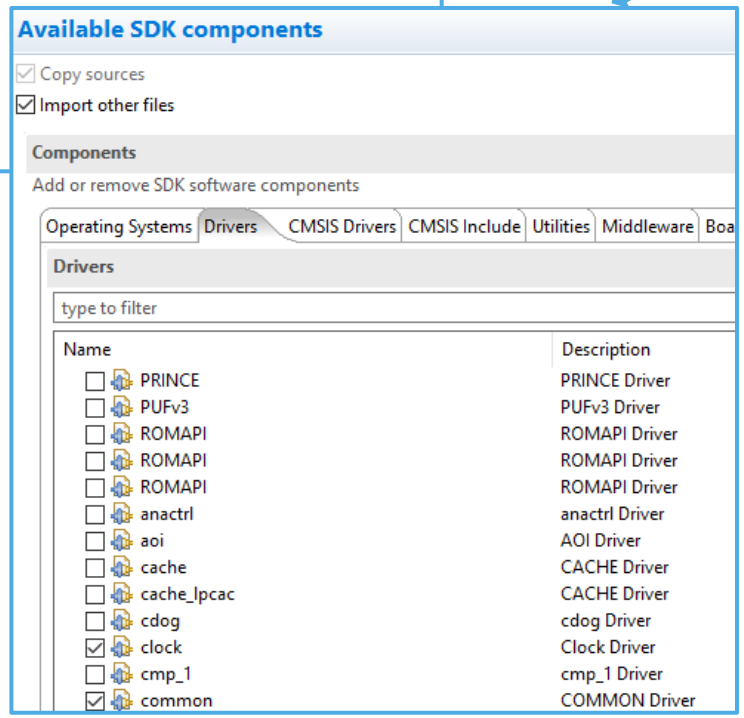
SECURE CONNECTIONS
FOR A SMARTER WORLD

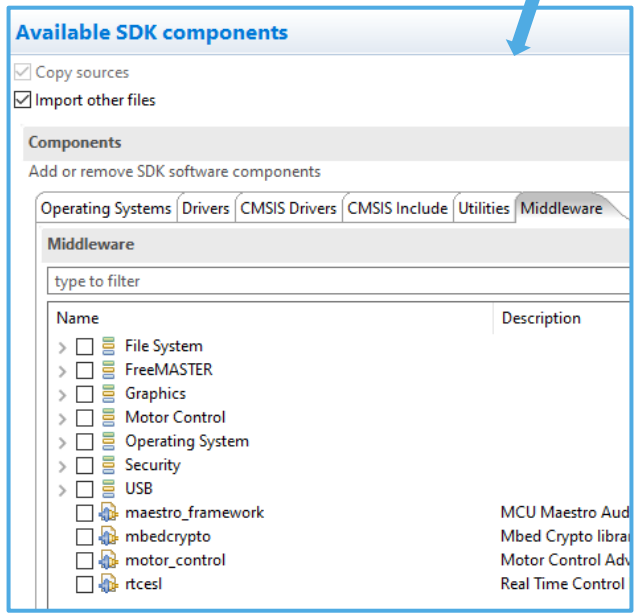
SDK COMPONENTS

- Click on “Managed SDK Components” icon



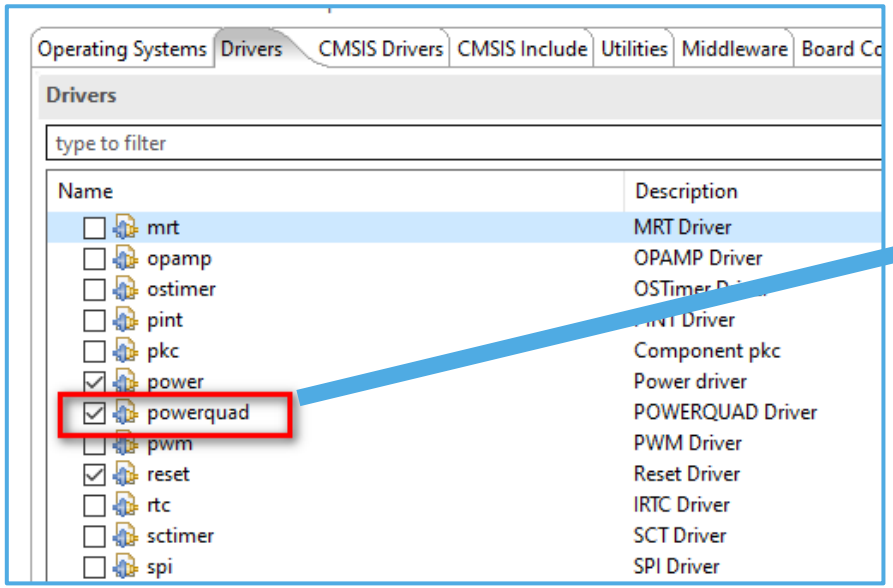


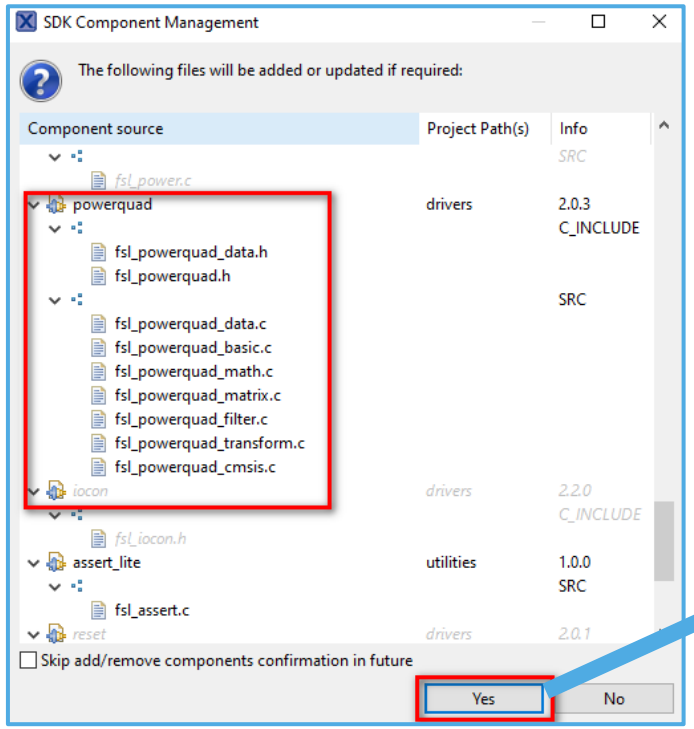


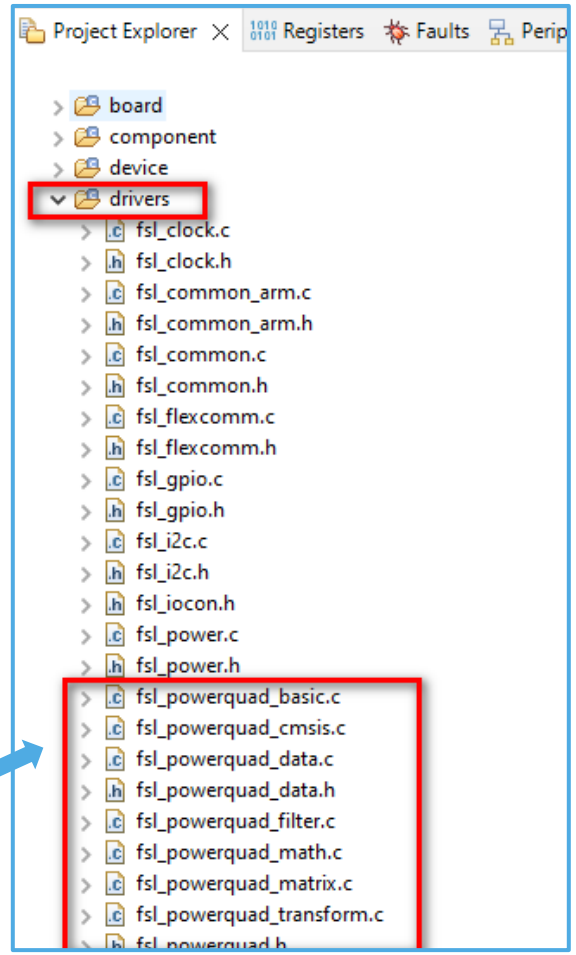


SDK COMPONENTS

- Selecting a new component, relevant files are added to project





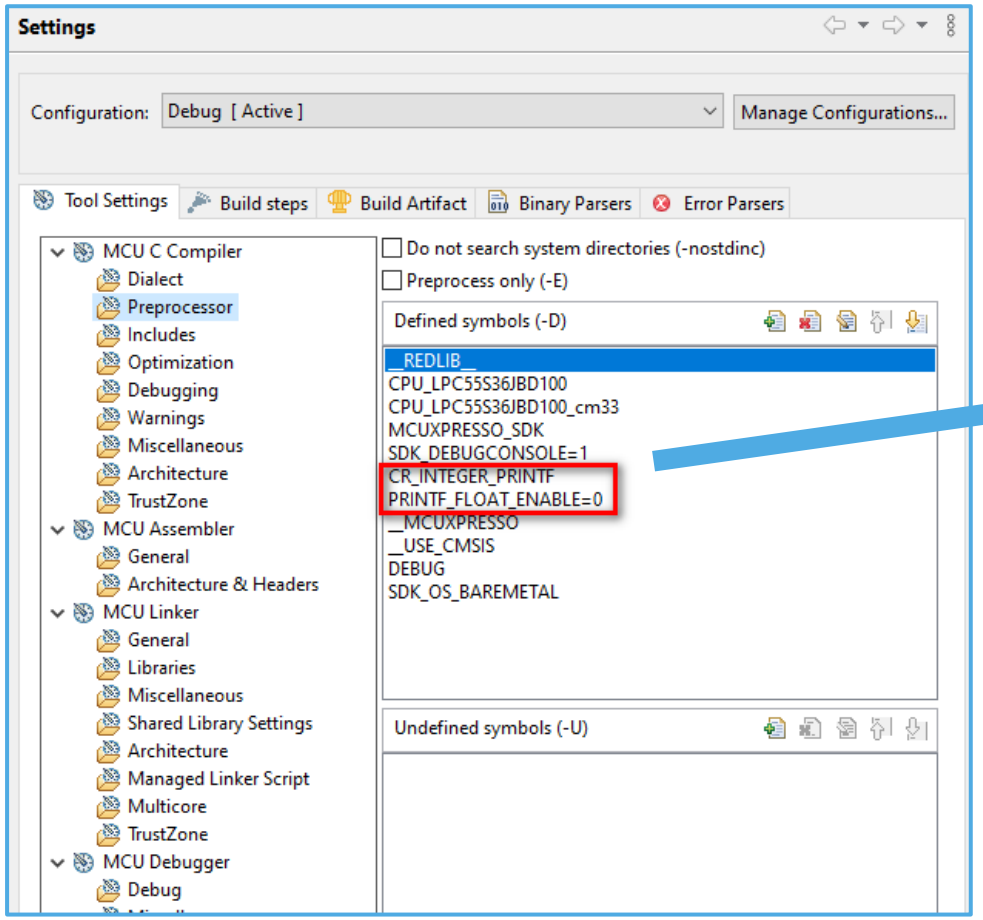


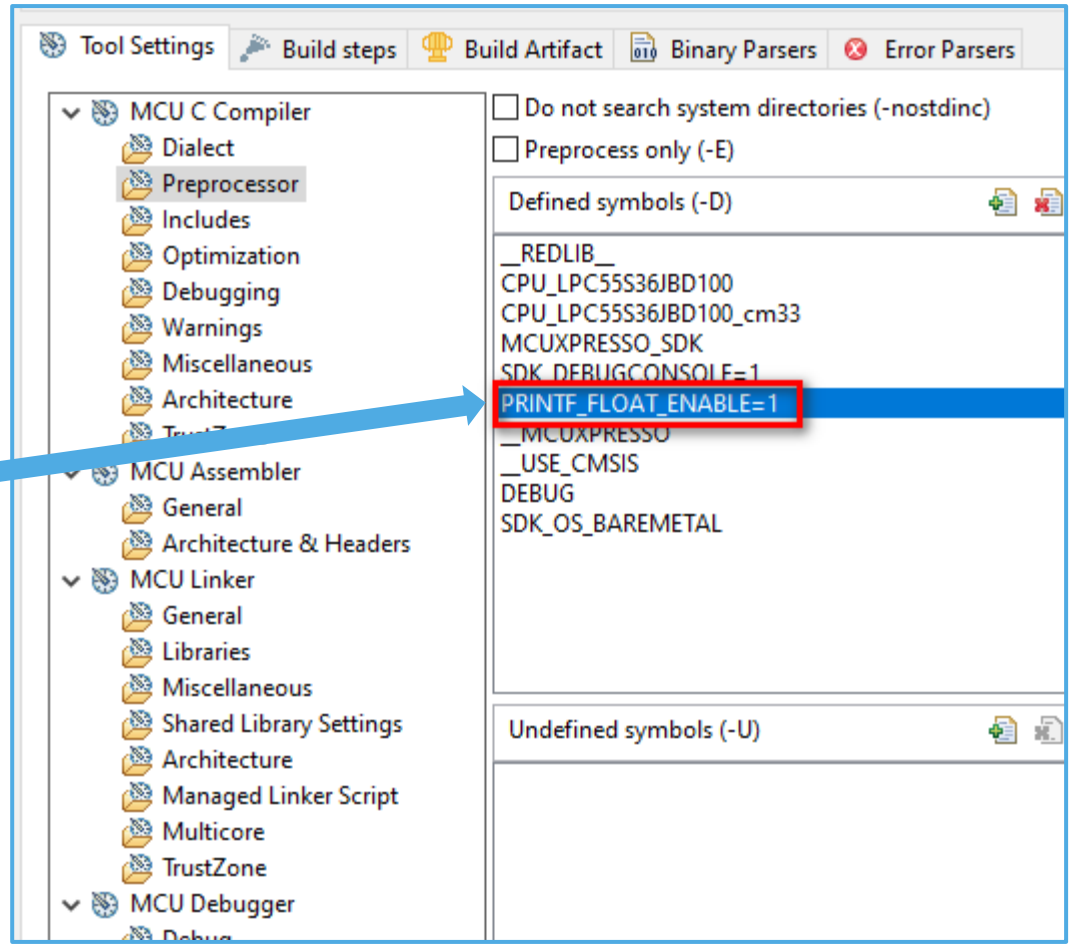
Project SDK DEFINITIONS

SECURE CONNECTIONS
FOR A SMARTER WORLD

SDK DEFINITIONS

- Enable float support for PRINTF

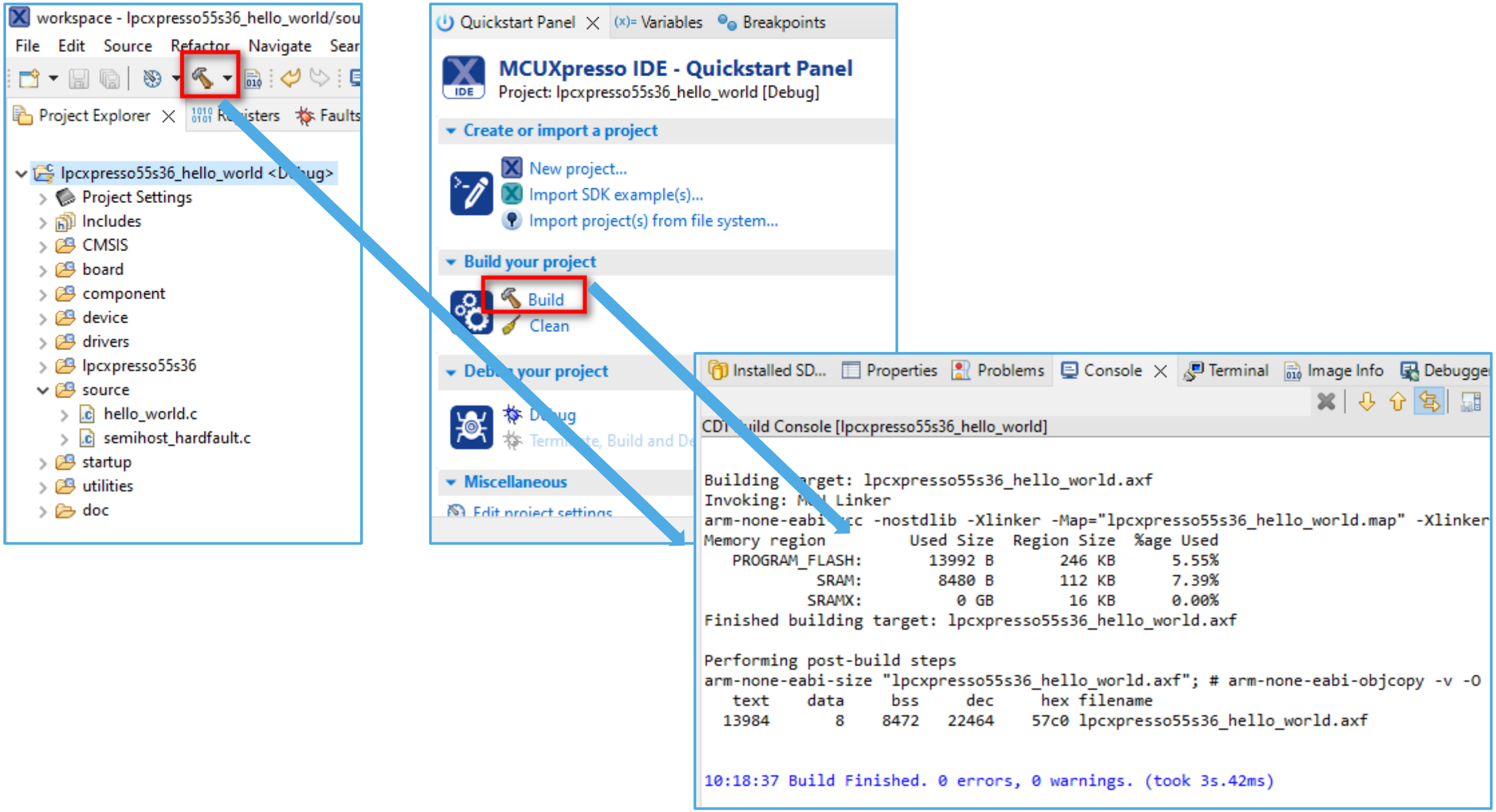




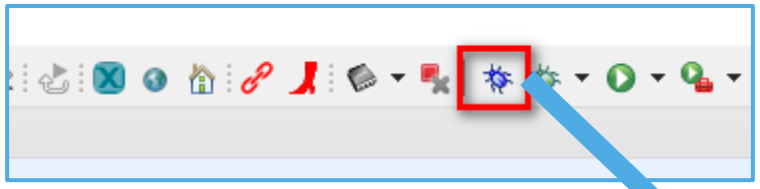
Project Build and Debug

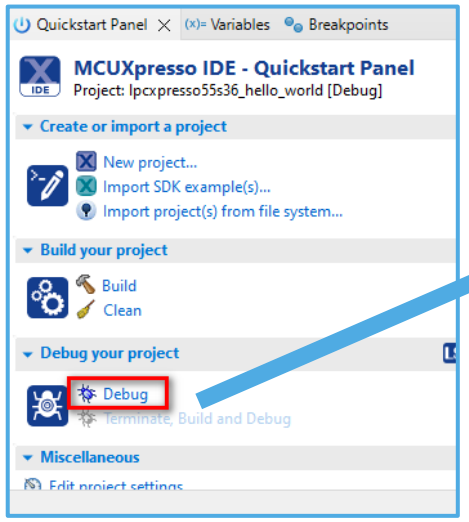
SECURE CONNECTIONS
FOR A SMARTER WORLD

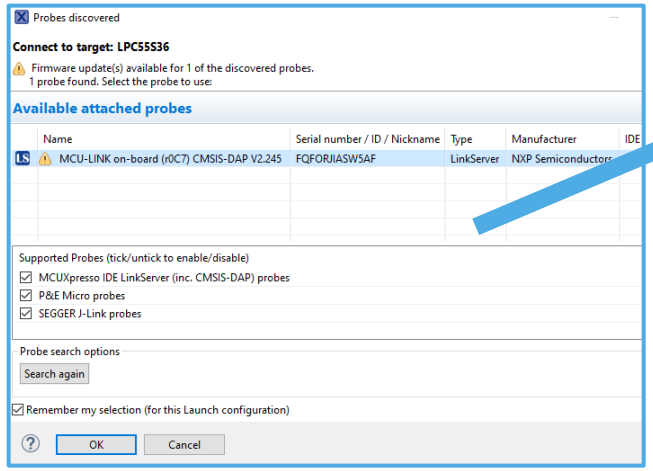
MCUXPRESSO PROJECT BUILD

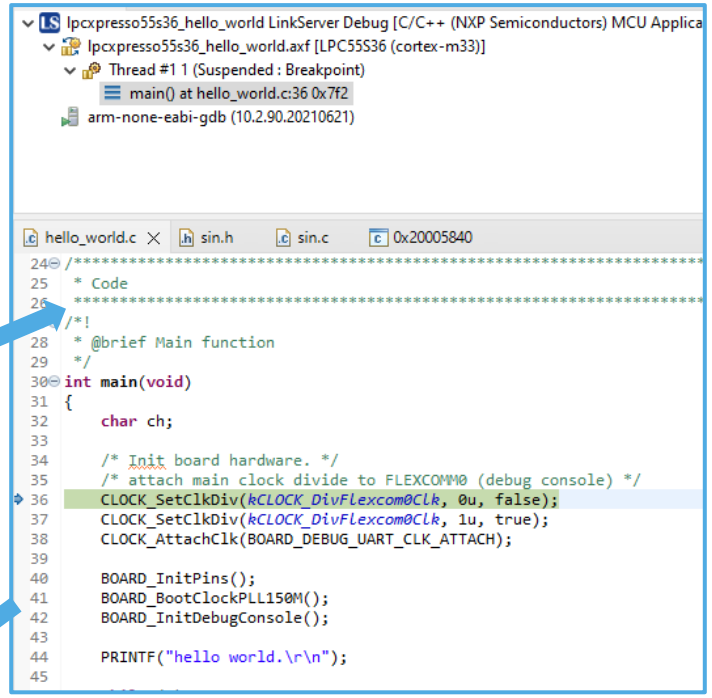


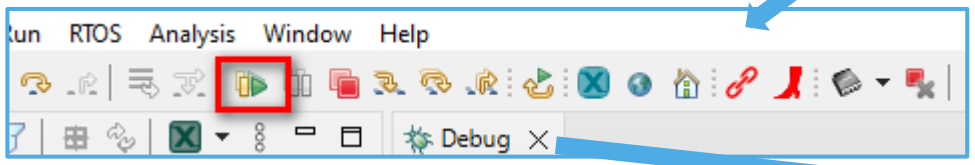
MCUXPRESSO PROJECT DEBUG

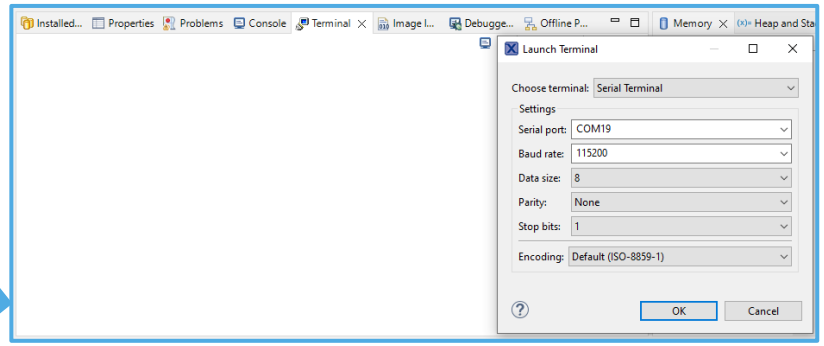




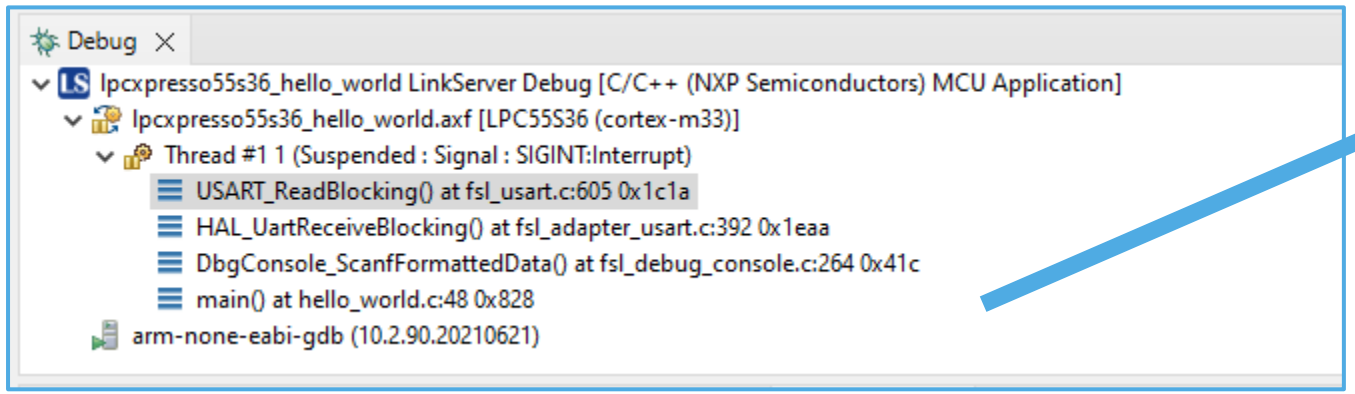


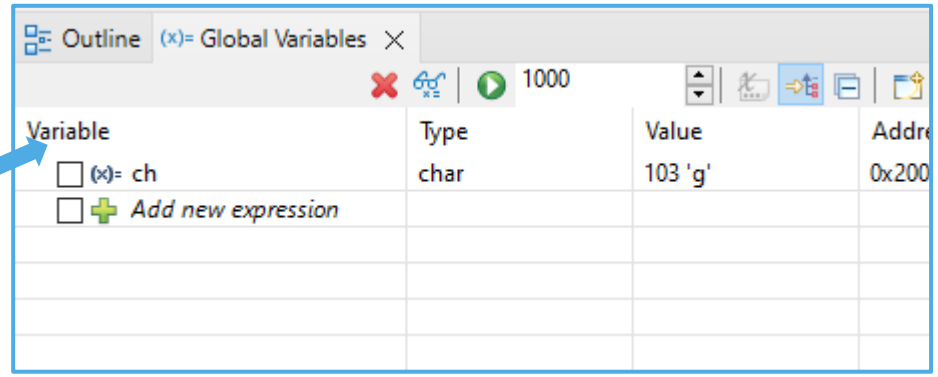




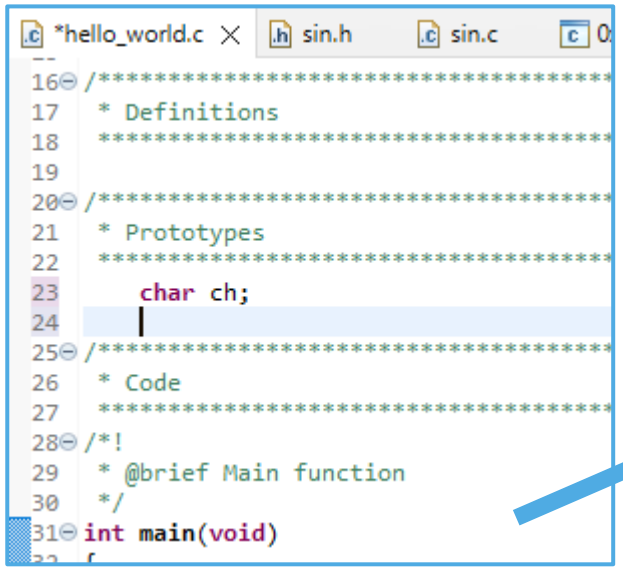


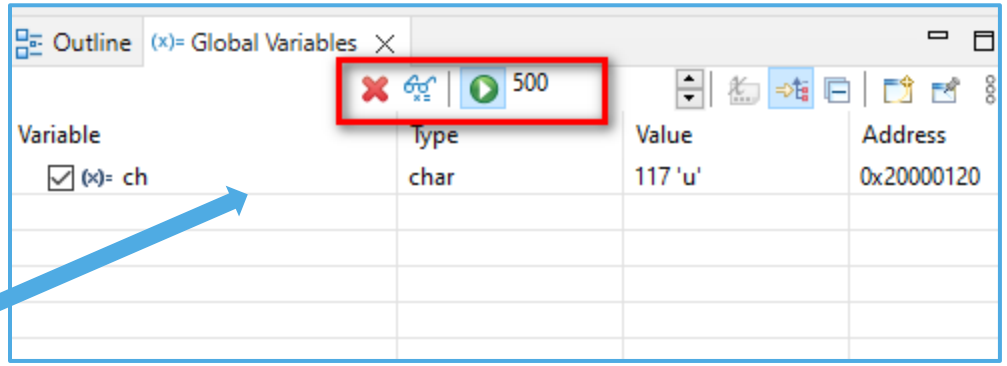
- Debugger: Variables





- Live View

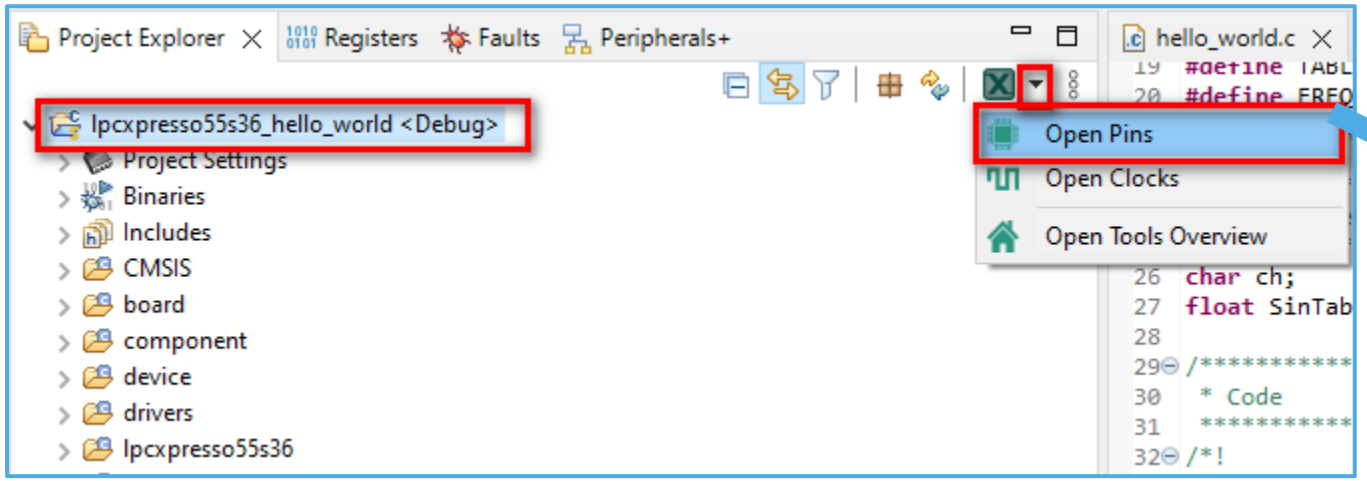


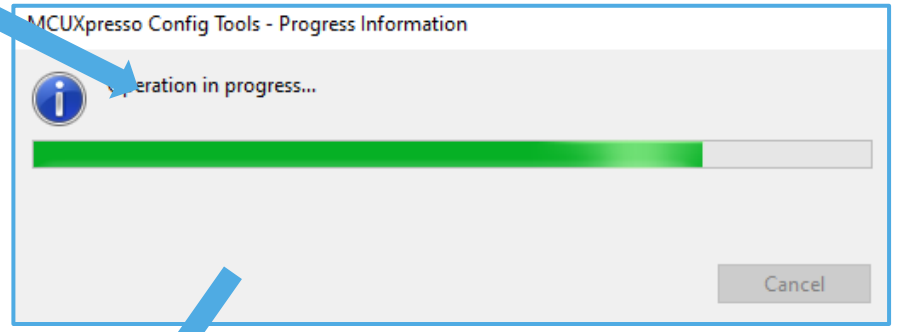


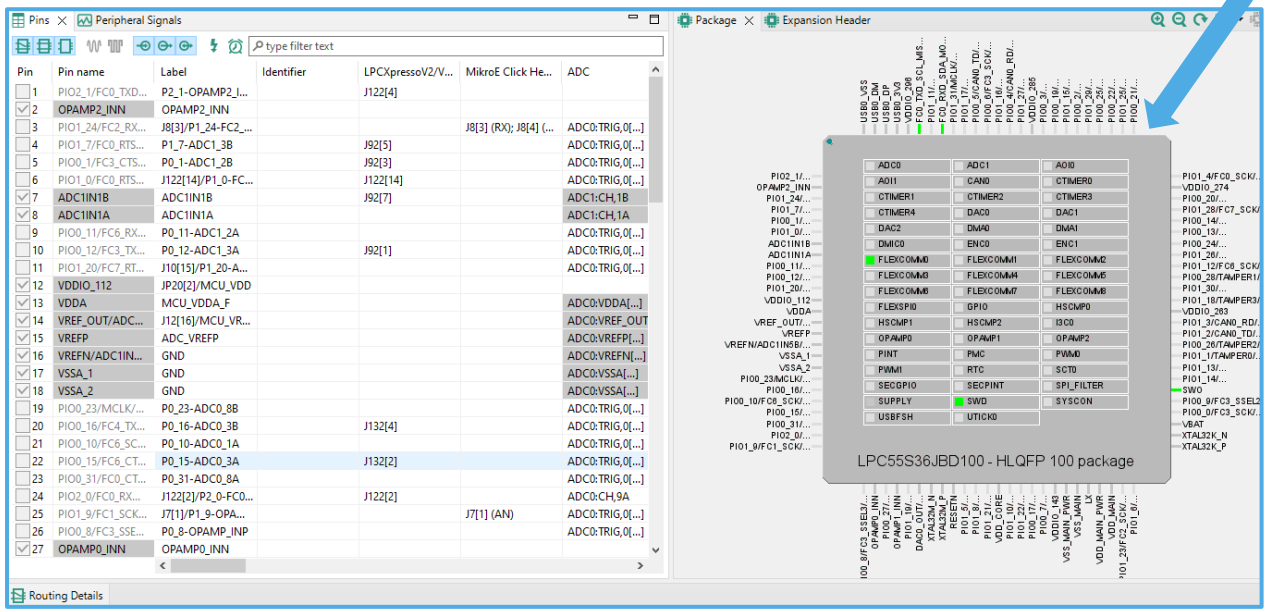
Config Tools (Pins)

SECURE CONNECTIONS
FOR A SMARTER WORLD

MCUXPRESSO CONFIG TOOLS: PINS

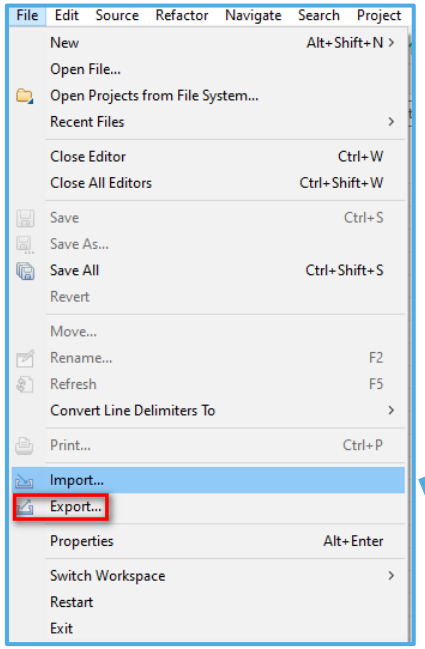


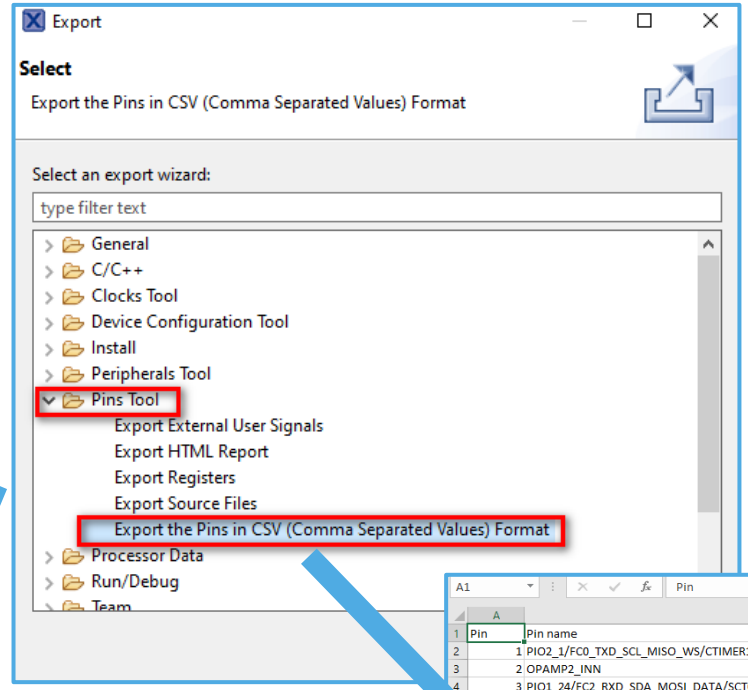


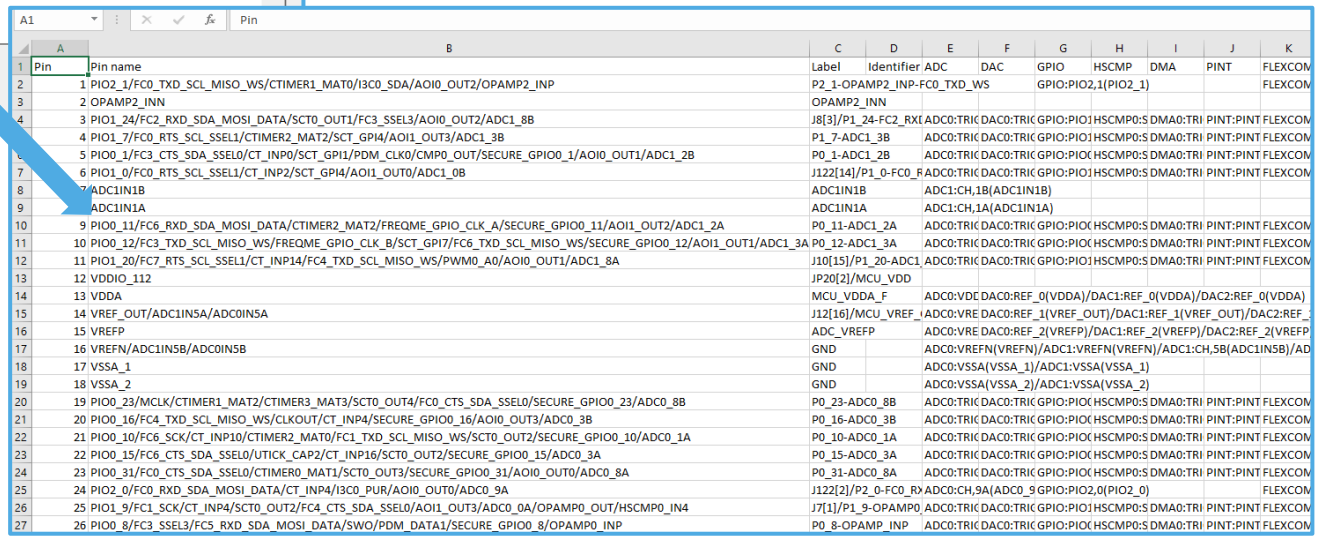


MCUXPRESSO CONFIG TOOLS: PINS

- Export Pins to Excel



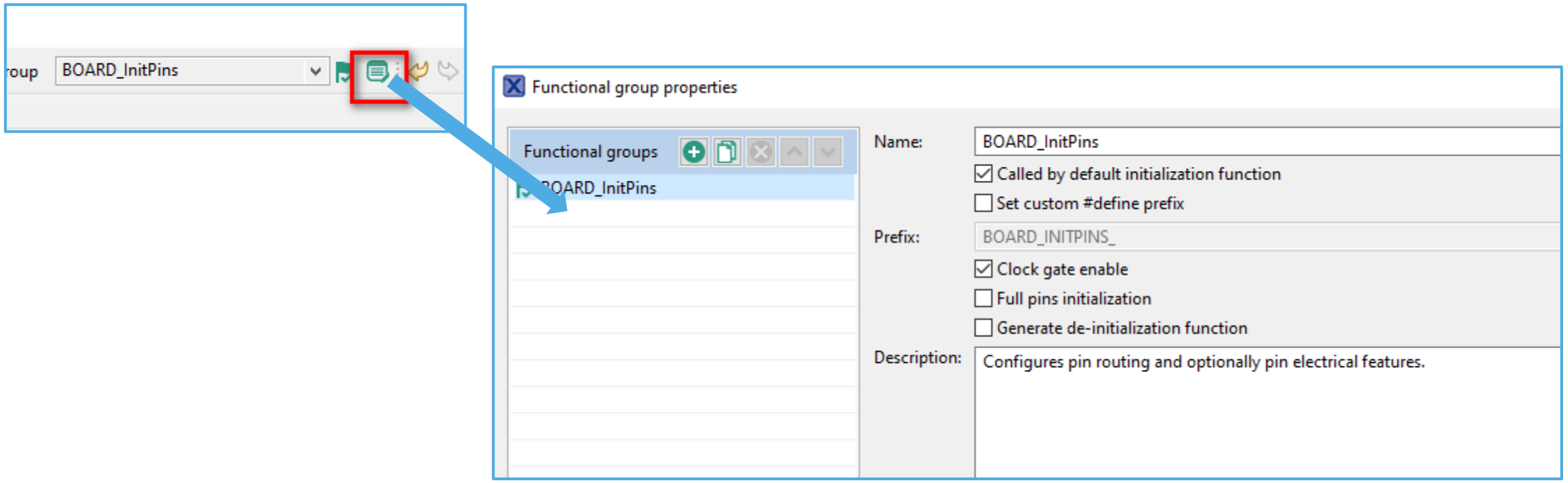




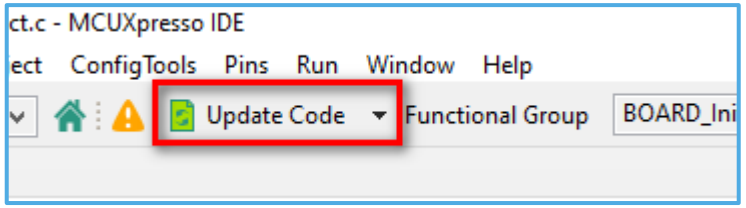
Pin	Pin name	Label	Identifier	ADC	DAC	GPIO	HSCMP	DMA	PINT	FLEXCOM
1	PIO2_1/FC0_TXD_SCL_MISO_WS/CTIMER1_MAT0/I3C0_SDA/AOI0_OUT2/OPAMP2_INP	P2_1-OPAMP2_INP-FC0_TXD_WS				GPIO:PIO2,1(PIO2_1)				FLEXCOM
2	OPAMP2_INN	OPAMP2_INN								
3	PIO1_24/FC2_RXD_SDA_MOSI_DATA/SCT0_OUT1/FC3_SSEL3/AOI0_OUT2/ADC1_8B	J8[3]/P1_24-FC2_RX		ADC0:TRIC	DAC0:TRIC	GPIO:PIO1	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
4	PIO1_7/FC0_RTS_SCL_SSEL1/CTIMER2_MAT2/SCT_GPI4/AOI1_OUT3/ADC1_3B	P1_7-ADC1_3B		ADC0:TRIC	DAC0:TRIC	GPIO:PIO1	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
5	PIO0_1/FC3_CTS_SDA_SSEL0/CT_INP0/SCT_GPI1/PDM_CLK0/CMP0_OUT/SECURE_GPIO0_1/AOI0_OUT1/ADC1_2B	P0_1-ADC1_2B		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
6	PIO1_0/FC0_RTS_SCL_SSEL1/CT_INP2/SCT_GPI4/AOI1_OUT0/ADC1_0B	J122[14]/P1_0-FC0_R		ADC0:TRIC	DAC0:TRIC	GPIO:PIO1	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
7	ADC1IN1B	ADC1IN1B		ADC1:CH,1B(ADC1IN1B)						
8	ADC1IN1A	ADC1IN1A		ADC1:CH,1A(ADC1IN1A)						
9	PIO0_11/FC6_RXD_SDA_MOSI_DATA/CTIMER2_MAT2/FREQME_GPIO_CLK_A/SECURE_GPIO0_11/AOI1_OUT2/ADC1_2A	P0_11-ADC1_2A		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
10	PIO0_12/FC3_TXD_SCL_MISO_WS/FREQME_GPIO_CLK_B/SCT_GPI7/FC6_TXD_SCL_MISO_WS/SECURE_GPIO0_12/AOI1_OUT1/ADC1_3A	P0_12-ADC1_3A		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
11	PIO1_20/FC7_RTS_SCL_SSEL1/CT_INP14/FC4_TXD_SCL_MISO_WS/PWM0_A0/AOI0_OUT1/ADC1_8A	J10[15]/P1_20-ADC1		ADC0:TRIC	DAC0:TRIC	GPIO:PIO1	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
12	VDDIO_112	JP20[2]/MCU_VDD								
13	VDDA	MCU_VDDA_F		ADC0:VDD	DAC0:REF_0(VDDA)/DAC1:REF_0(VDDA)/DAC2:REF_0(VDDA)					
14	VREF_OUT/ADC1IN5A/ADC0IN5A	J12[16]/MCU_VREF_		ADC0:VRE	DAC0:REF_1(VREF_OUT)/DAC1:REF_1(VREF_OUT)/DAC2:REF_					
15	VREFP	ADC_VREFP		ADC0:VRE	DAC0:REF_2(VREFP)/DAC1:REF_2(VREFP)/DAC2:REF_2(VREFP					
16	VREFN/ADC1IN5B/ADC0IN5B	GND		ADC0:VREFN(VREFN)/ADC1:VREFN(VREFN)/ADC1:CH,5B(ADC1IN5B)/AD						
17	VSSA_1	GND		ADC0:VSSA(VSSA_1)/ADC1:VSSA(VSSA_1)						
18	VSSA_2	GND		ADC0:VSSA(VSSA_2)/ADC1:VSSA(VSSA_2)						
19	PIO0_23/MCLK/CTIMER1_MAT2/CTIMER3_MAT3/SCT0_OUT4/FC0_CTS_SDA_SSEL0/SECURE_GPIO0_23/ADC0_8B	P0_23-ADC0_8B		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
20	PIO0_16/FC4_TXD_SCL_MISO_WS/CLKOUT/CT_INP4/SECURE_GPIO0_16/AOI0_OUT3/ADC0_3B	P0_16-ADC0_3B		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
21	PIO0_10/FC6_SCK/CT_INP10/CTIMER2_MAT0/FC1_TXD_SCL_MISO_WS/SCT0_OUT2/SECURE_GPIO0_10/ADC0_1A	P0_10-ADC0_1A		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
22	PIO0_15/FC6_CTS_SDA_SSEL0/UTICK_CAP2/CT_INP16/SCT0_OUT2/SECURE_GPIO0_15/ADC0_3A	P0_15-ADC0_3A		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
23	PIO0_31/FC0_CTS_SDA_SSEL0/CTIMER0_MAT1/SCT0_OUT3/SECURE_GPIO0_31/AOI0_OUT0/ADC0_8A	P0_31-ADC0_8A		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
24	PIO2_0/FC0_RXD_SDA_MOSI_DATA/CT_INP4/I3C0_PUR/AOI0_OUT0/ADC0_9A	J122[2]/P2_0-FC0_RX		ADC0:CH,9A(ADC0_9	GPIO:PIO2,0(PIO2_0)					FLEXCOM
25	PIO1_9/FC1_SCK/CT_INP4/SCT0_OUT2/FC4_CTS_SDA_SSEL0/AOI1_OUT3/ADC0_0A/OPAMP0_OUT/HSCMP0_IN4	J7[1]/P1_9-OPAMP0		ADC0:TRIC	DAC0:TRIC	GPIO:PIO1	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM
26	PIO0_8/FC3_SSEL3/FC5_RXD_SDA_MOSI_DATA/SWO/PDM_DATA1/SECURE_GPIO0_8/OPAMP0_INP	P0_8-OPAMP_INP		ADC0:TRIC	DAC0:TRIC	GPIO:PIO(	HSCMP0:S	DMA0:TRI	PINT:PINT	FLEXCOM

MCUXPRESSO CONFIG TOOLS: PINS

- PINS FUNCTIONAL GROUPS



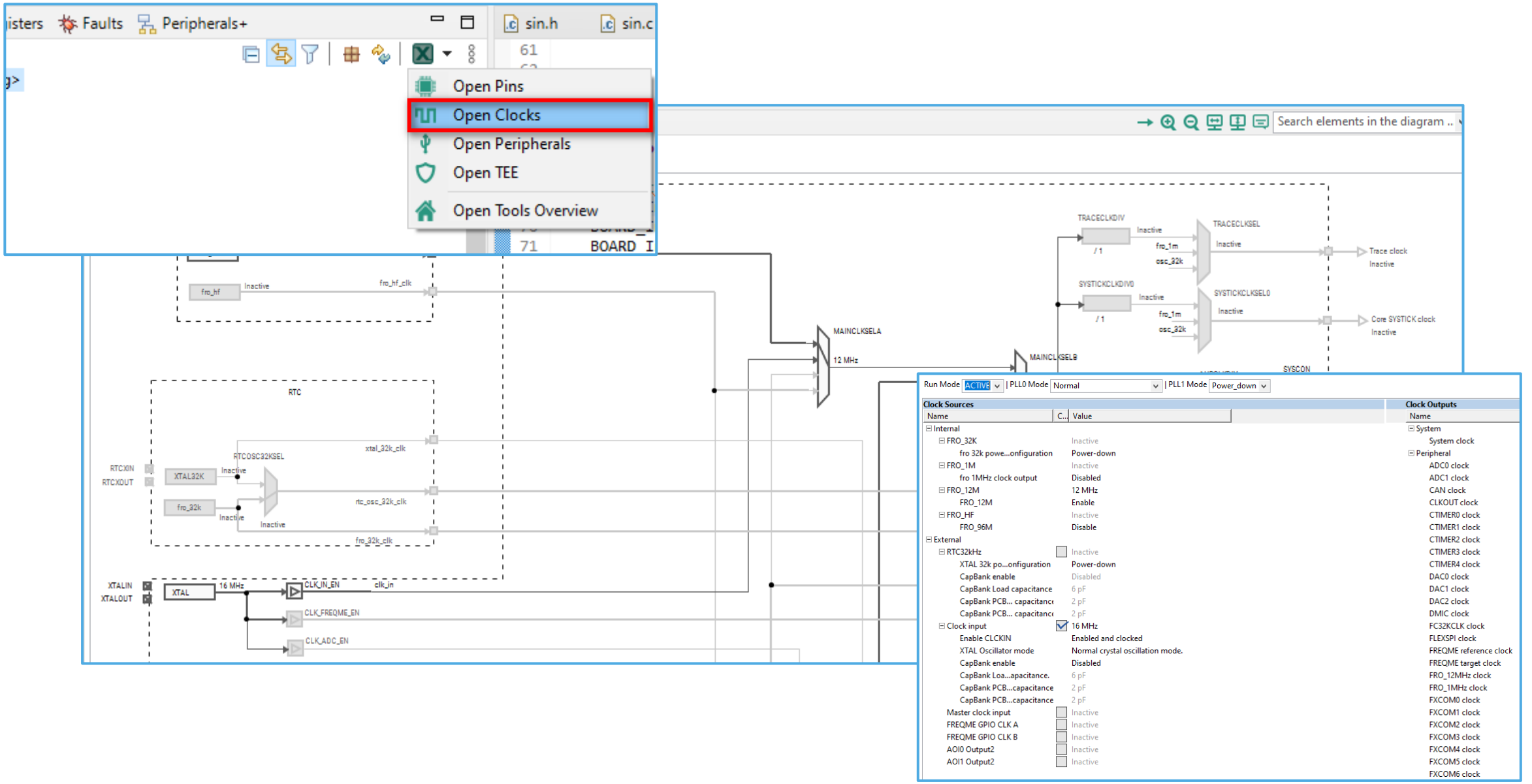
- CODE UPDATE



Config Tools (Clock)

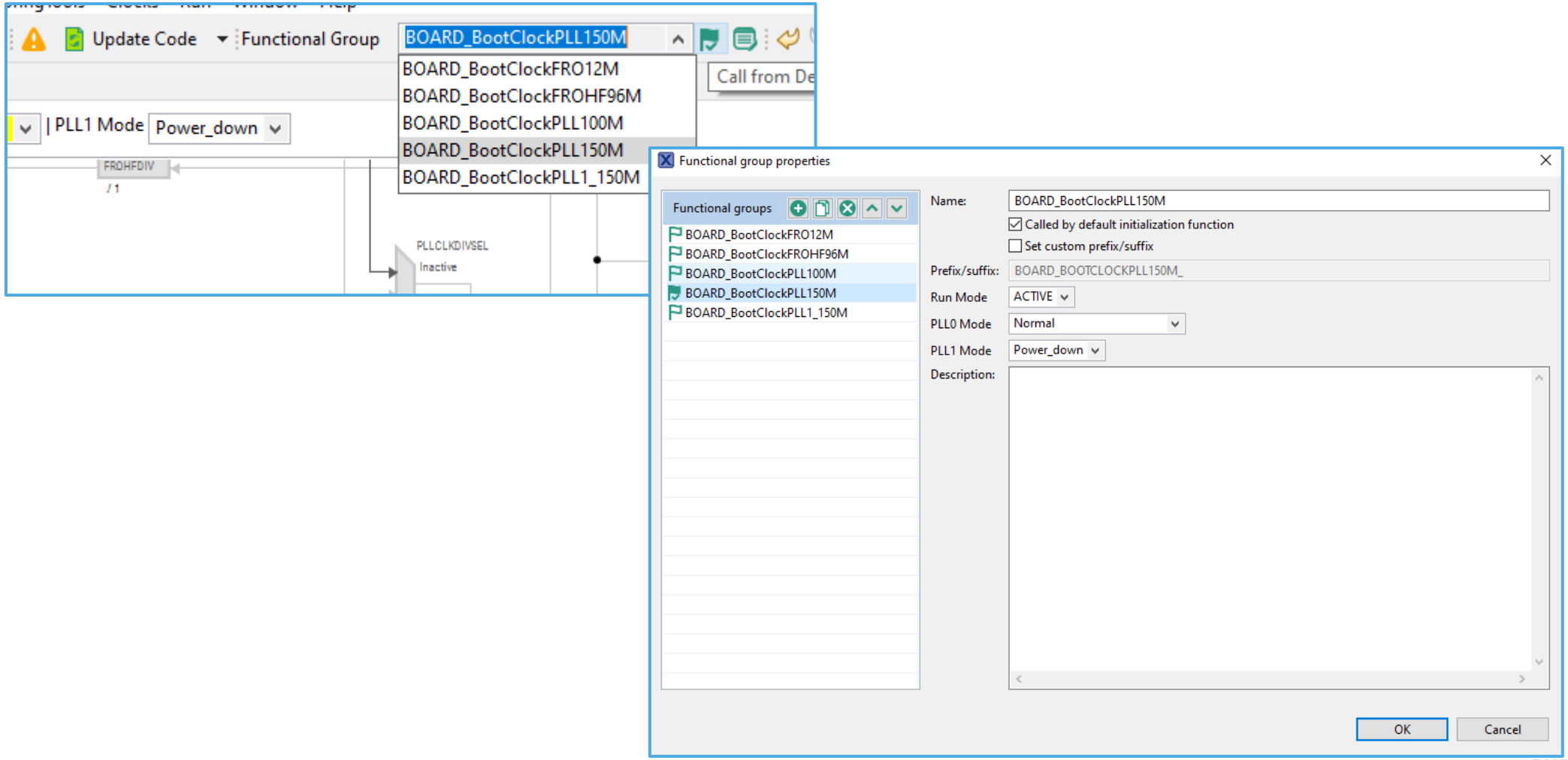
SECURE CONNECTIONS
FOR A SMARTER WORLD

MCUXPRESSO CONFIG TOOLS: CLOCKS



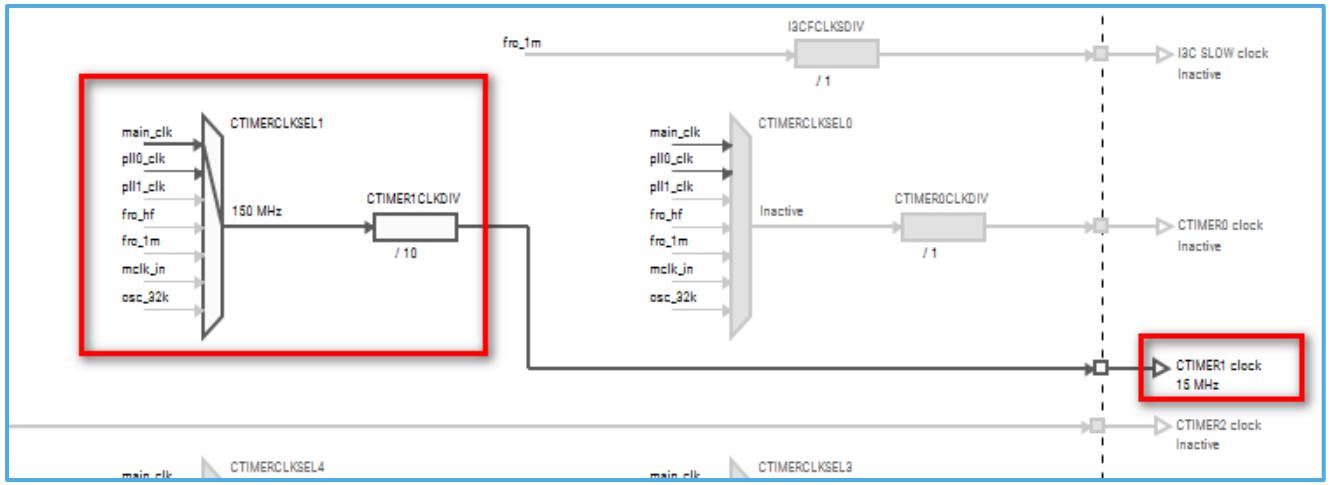
MCUXPRESSO CONFIG TOOLS: CLOCKS

- CLOCK CONFIGURATIONS (FUNCTIONAL GROUPS)



MCUXPRESSO CONFIG TOOLS: CLOCKS

- CTIMER CLOCK ENABLE

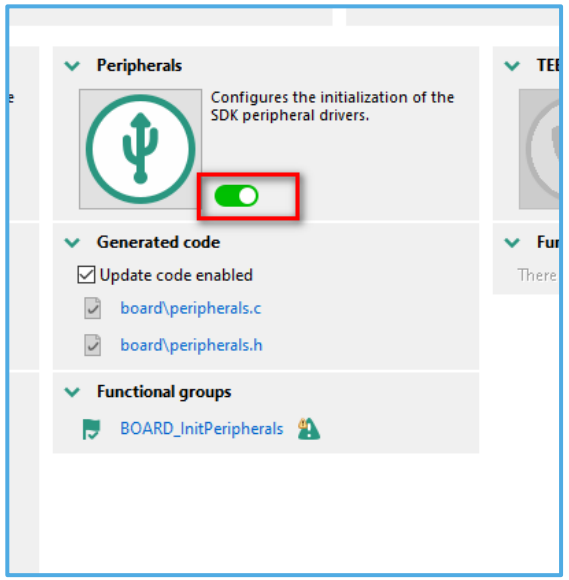


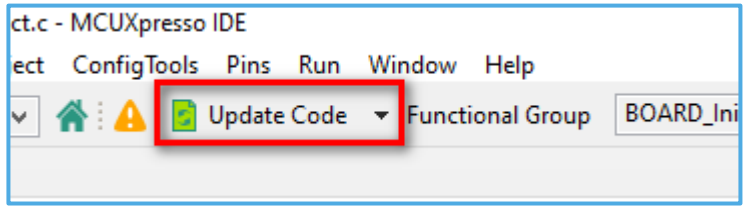
Config Tools (Peripherals)

SECURE CONNECTIONS FOR A SMARTER WORLD

MCUXPRESSO CONFIG TOOLS: PERIPHERALS

- In some projects Peripherals Tool is disable, Enable it
- Update Code



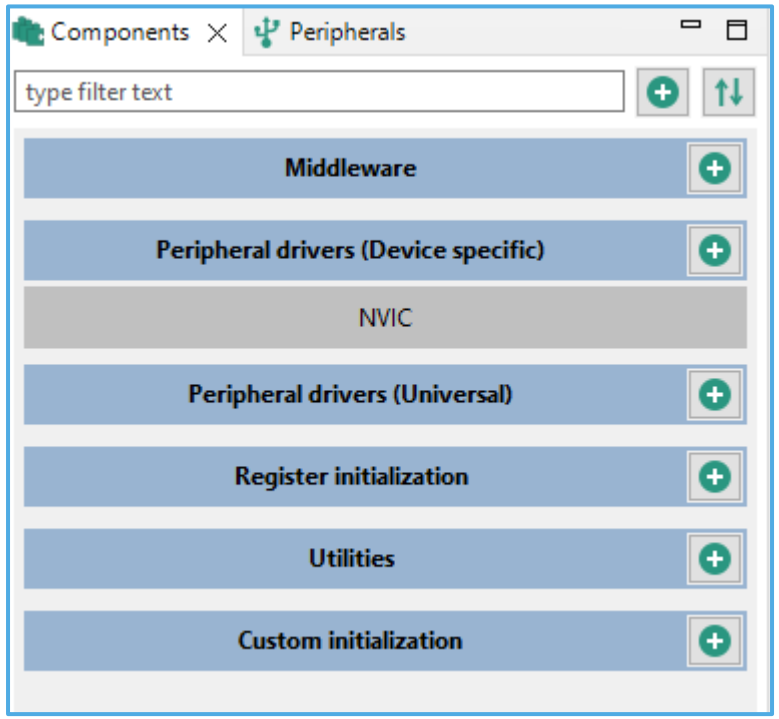


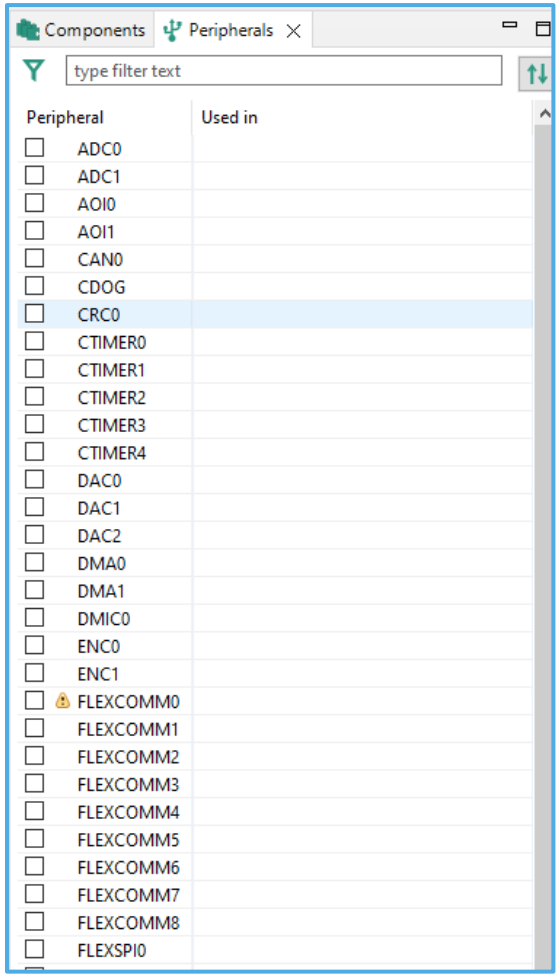
- Call Init Peripherals function

```
66  int main(void) {
67
68      /* Init board hardware. */
69      BOARD_InitBootPins();
70      BOARD_InitBootClocks();
71      BOARD_InitBootPeripherals();
```

MCUXPRESSO CONFIG TOOLS: PERIPHERALS

- Components and Peripherals

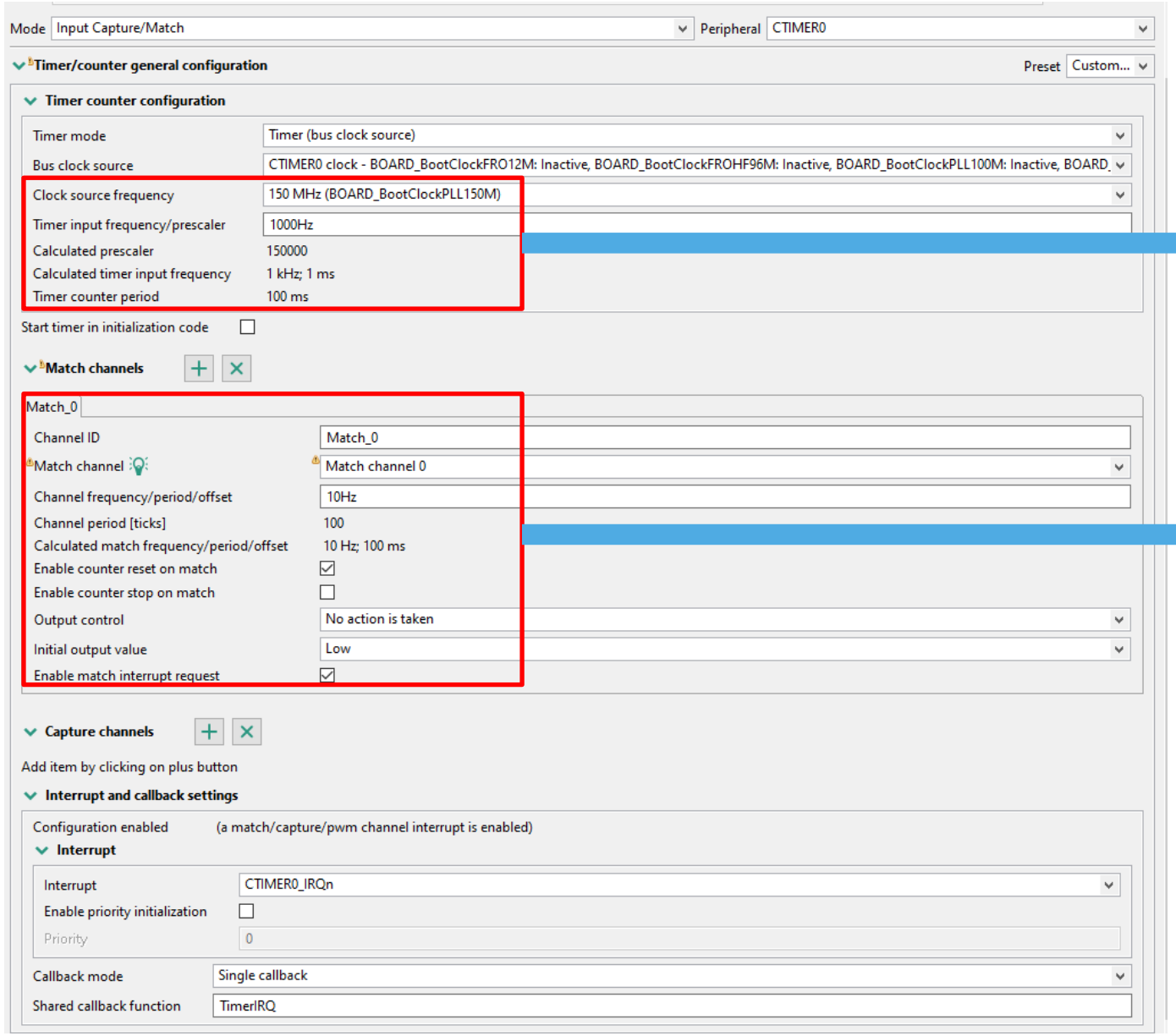




CTIMER

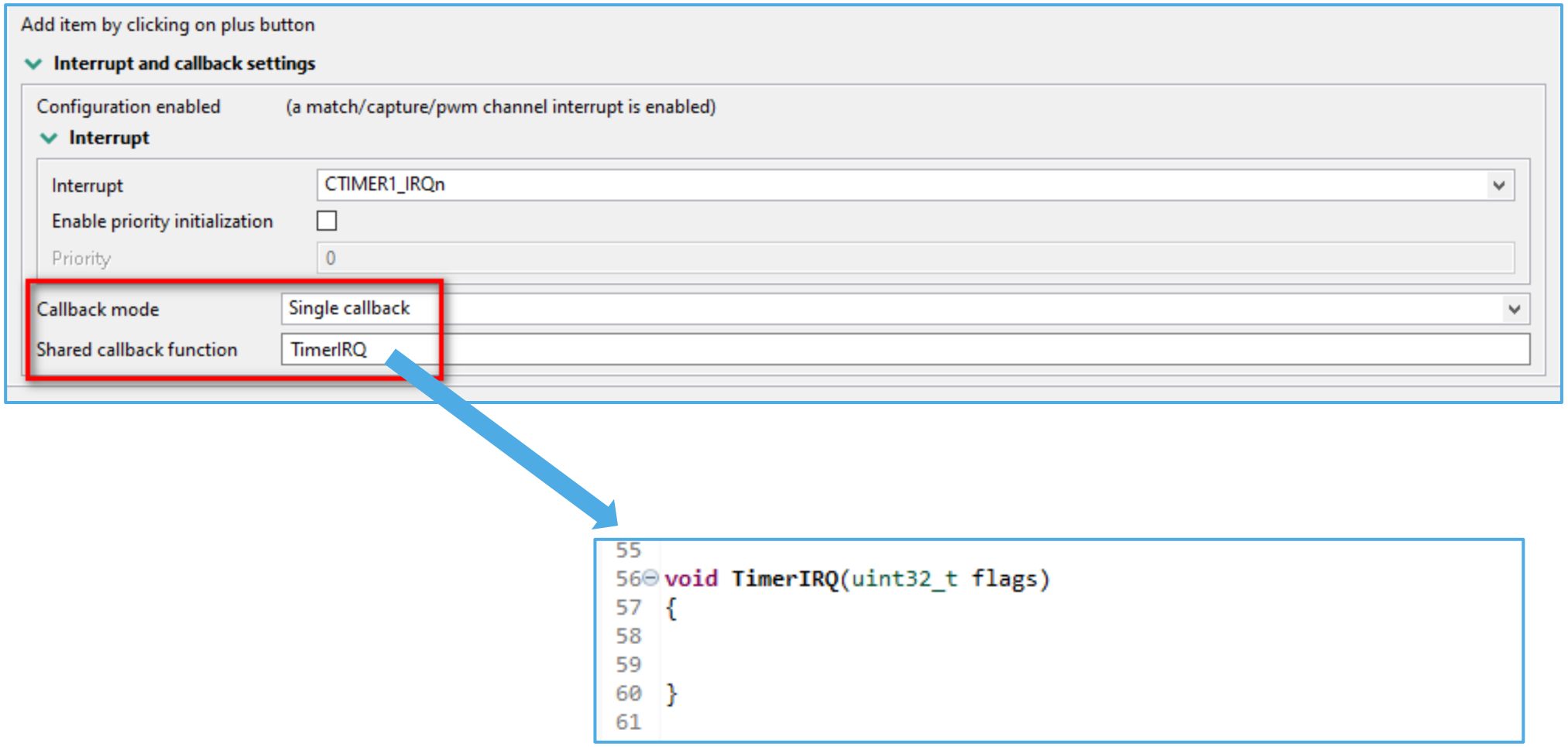
SECURE CONNECTIONS
FOR A SMARTER WORLD

MCUXPRESSO CONFIG TOOLS: CTIMER



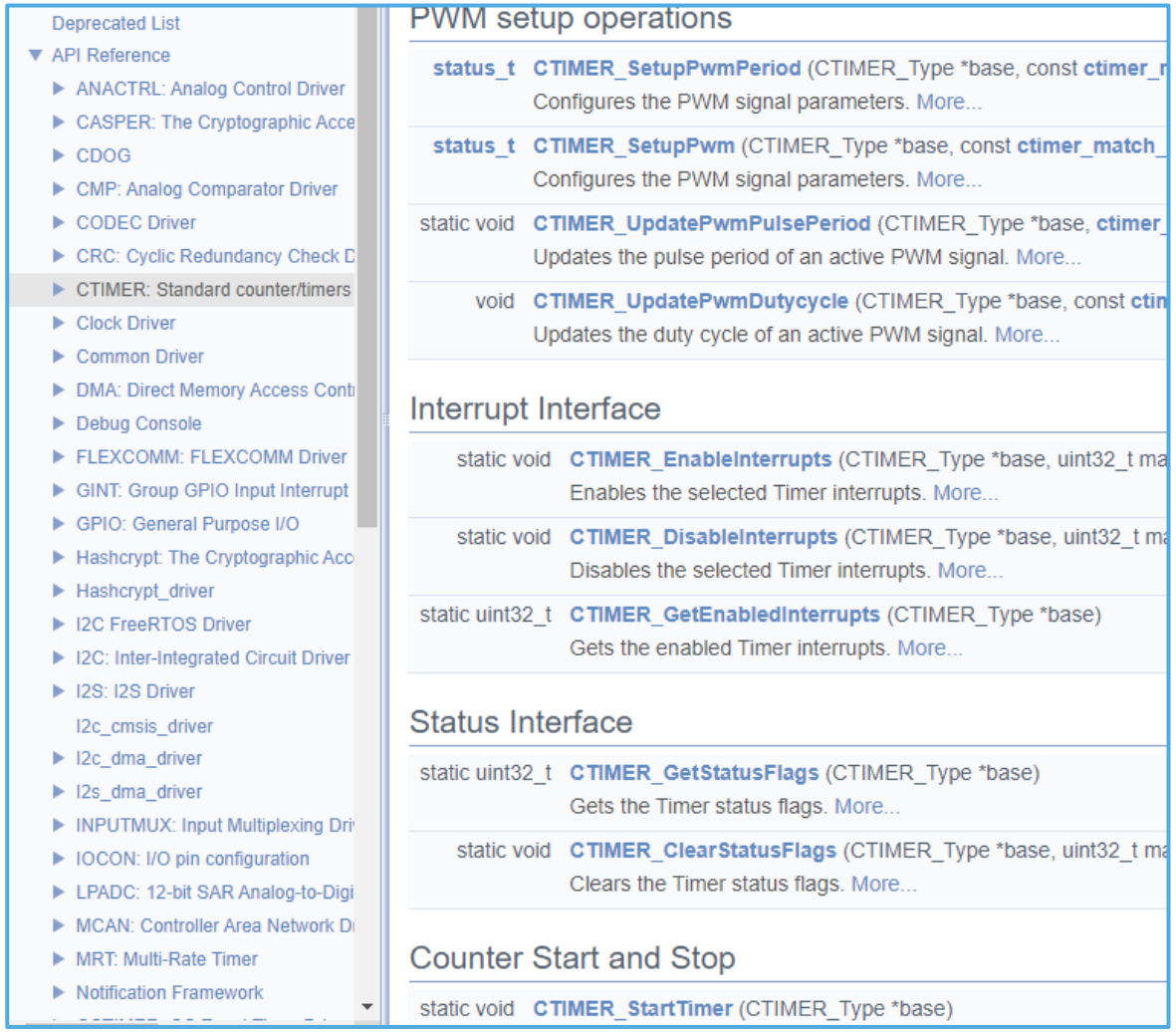
- Ctimer peripheral input clock
  - Common clock for match0-3 and capture0-3
- Match0 settings

MCUXPRESSO CONFIG TOOLS: CTIMER



MCUXPRESSO CONFIG TOOLS: CTIMER

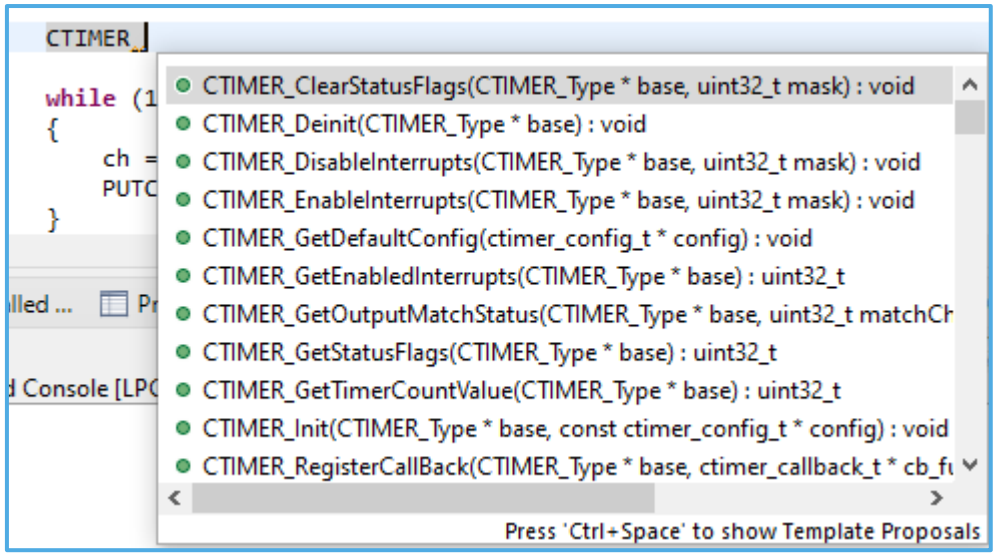
- API Information



MCUXPRESSO CONFIG TOOLS: CTIMER

- Code Modification

- Write “CTIMER_” and CTRL + SPACE




```
#include "fsl_device_registers.h"
#include "fsl_debug_console.h"
#include "pin_mux.h"
#include "clock_config.h"
#include "board.h"
#include "peripherals.h"
```

```
void TimerIRQ(uint32_t flags)
{


}
/*******************************************************************************
 * Code
 ******************************************************************************/
/*!
 * @brief Main function
 */
int main(void)
{
    char ch;

    /* Init board hardware. */
    /* attach main clock divide to FLEXCOMM0 (debug console) */
    CLOCK_SetClkDiv(kCLOCK_DivFlexcom0Clk, 0u, false);
    CLOCK_SetClkDiv(kCLOCK_DivFlexcom0Clk, 1u, true);
    CLOCK_AttachClk(BOARD_DEBUG_UART_CLK_ATTACH);

    BOARD_InitPins();
    BOARD_BootClockPLL150M();
    BOARD_InitDebugConsole();
    BOARD_InitPeripherals();

    PRINTF("hello world.\r\n");

    CTIMER_StartTimer(CTIMER1_PERIPHERAL);

    while (1)
    {
        ch = GETCHAR();
        PUTCHAR(ch);
    }
}
```

MCUXPRESSO CONFIG TOOLS: SIN WAVE

- Add “sin wave” generation

```
void Generate_sin_table_float(float *table, uint32_t length,float amplitude,
float frequency)
{

uint32_t index;
float theta, sample_time;
sample_time=1.0f/(frequency * (float)length);
for(index=0;index < length;index++)
{
theta= 2.0f * PI * frequency * sample_time * (float)index;
table[index]=amplitude * sin(theta);
}
```

MCUXPRESSO CONFIG TOOLS: SIN WAVE

“sin wave” generation (PowerQuad Version)

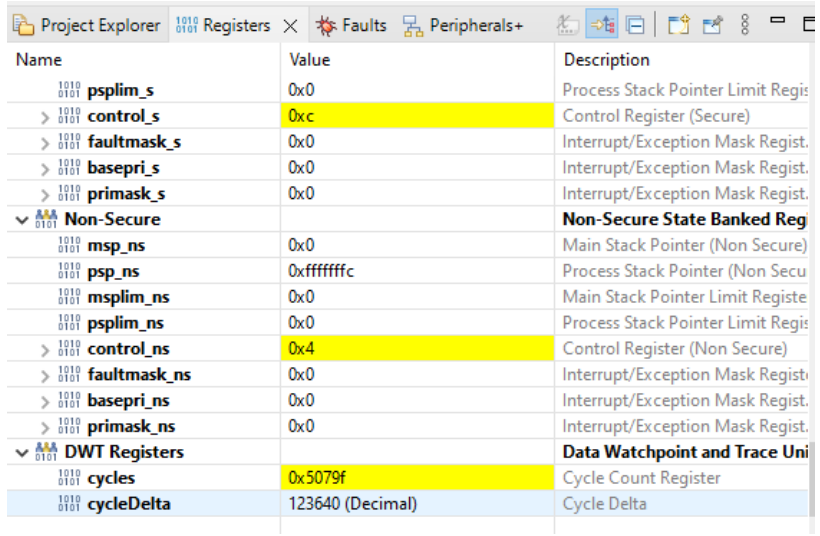
```
#include "fsl_powerquad.h"
```

```
 BOARD_InitPins();
 BOARD_BootClockPLL150M();
 BOARD_InitDebugConsole();
 BOARD_InitPeripherals();
 PQ_Init(POWERQUAD);
```

```
void Generate_sin_table_float(float *table, uint32_t length,float amplitude, float frequency)
{

uint32_t index;
float theta, sample_time, result;
sample_time=1.0f/(frequency * (float)length);
for(index=0;index < length;index++)
 {
 theta= 2.0f * PI * frequency * sample_time * (float)index;
 #if USE_POWERQUAD
 PQ_SinF32(&theta, &result);
 table[index]=amplitude * result;
 #else
 table[index]=amplitude * sin(theta);
 #endif
}
```

MCUXPRESSO CONFIG TOOLS: SIN WAVE (SW VS POWERQUAD)

Execution comparative




```
CPU cycles: 810985 -- Exec.Time(us): 5406.566895
Set Frequency at 1.000000 Hz
hello world.
CPU cycles: 19506 -- Exec.Time(us): 130.040009
Set Frequency at 1.000000 Hz
```

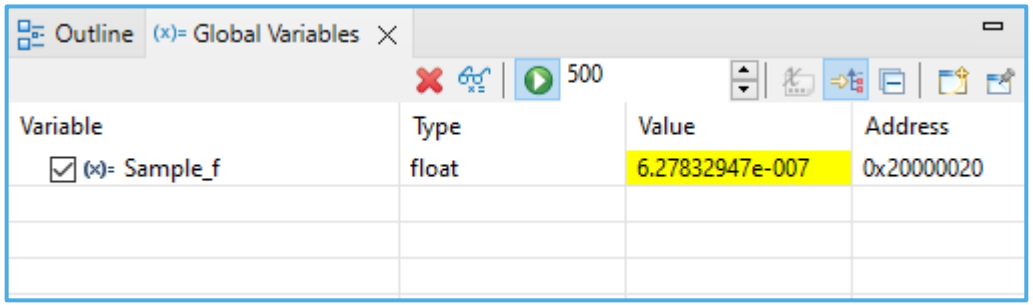
```
#define USE_POWERQUAD 0
```

```
#define USE_POWERQUAD 1
```

MCUXPRESSO CONFIG TOOLS: SIN WAVE

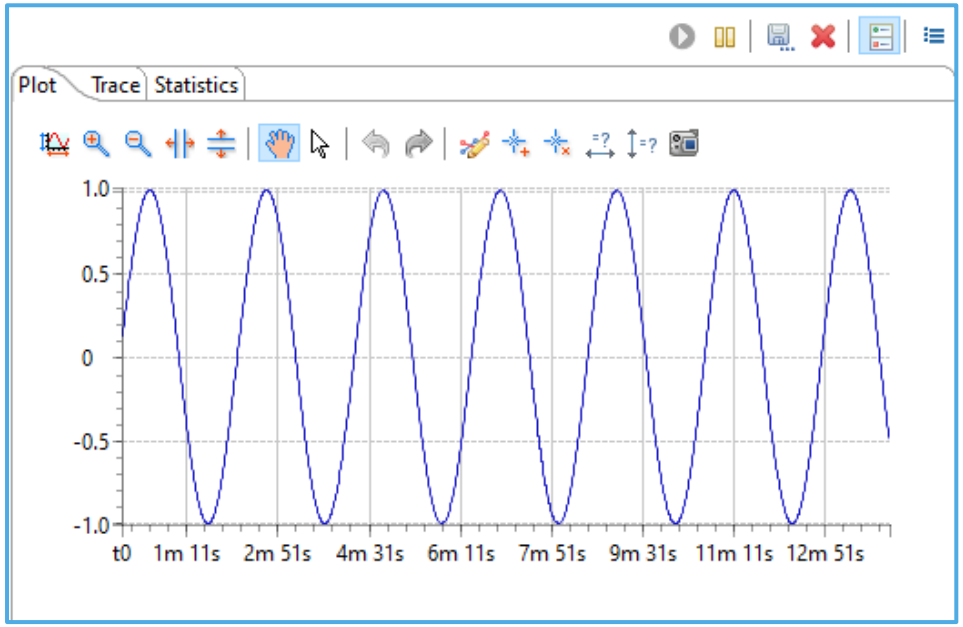
"sin wave" generation (Visualization) - Live View

```
float Sample_f;
uint32_t index=0;

float SinTable_f[TABLE_LENGHT];
```




```
Generate_sin_table_float(&SinTable_f[0],TABLE_LENGHT,1.0f, 1.0f);
```

```
/*************************************************************************
 * IRQ

*************************************************************************/
void TimerIRQ(uint32_t flags)
{
Sample_f=SinTable_f[index];
index++;
if(index==TABLE_LENGHT)index=0;
}
```



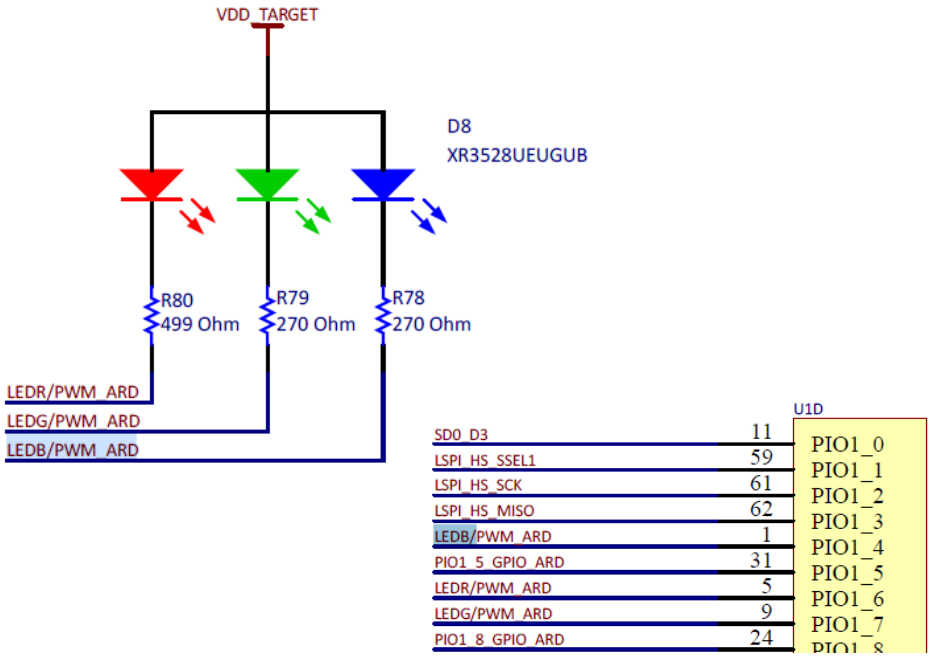
CTIMER2

Pins | Peripheral Signals

PIO1_4

Pin	Pin name		FLEXCOMM	CTIMER	SCT	SDIF	SYSCON
1	CTIMER2_MAT1	T,0[...]	FLEXCOMM0:SCK	CTIMER2:MATC...	SCT0:OUT,0	SDIF:SD0_D,0	SYSCON:FREQM...

- EVK Schematic
  - Led blue at PIO1_4



Name CTIMER2 Custom name

Mode Input Capture/Match Peripheral CTIMER2

Timer/counter general configuration Preset Custom...

Timer counter configuration

Timer mode	Timer (bus clock source)
Bus clock source	CTIMER2 clock - BOARD_BootClockFRO12M: Inactive, BOARD_BootClockFROHF96M: Inactive, BOARD_BootClockPLL100M: Inactive, BOARD_
Clock source frequency	150 MHz (BOARD_BootClockPLL150M)
Timer input frequency/prescaler	50MHz
Calculated prescaler	3
Calculated timer input frequency	50 MHz; 20 ns
Timer counter period	1 s

Start timer in initialization code ☑

Match channels + ×

Match_0

Channel ID	Match_0
Match channel	Match channel 1
Channel frequency/period/offset	1Hz
Channel period [ticks]	50000000
Calculated match frequency/period/offset	1 Hz; 1 s
Enable counter reset on match	☑
Enable counter stop on match	☐
Output control	Toggle bit/output
Initial output value	Low
Enable match interrupt request	☐

SECURE CONNECTIONS
FOR A SMARTER WORLD