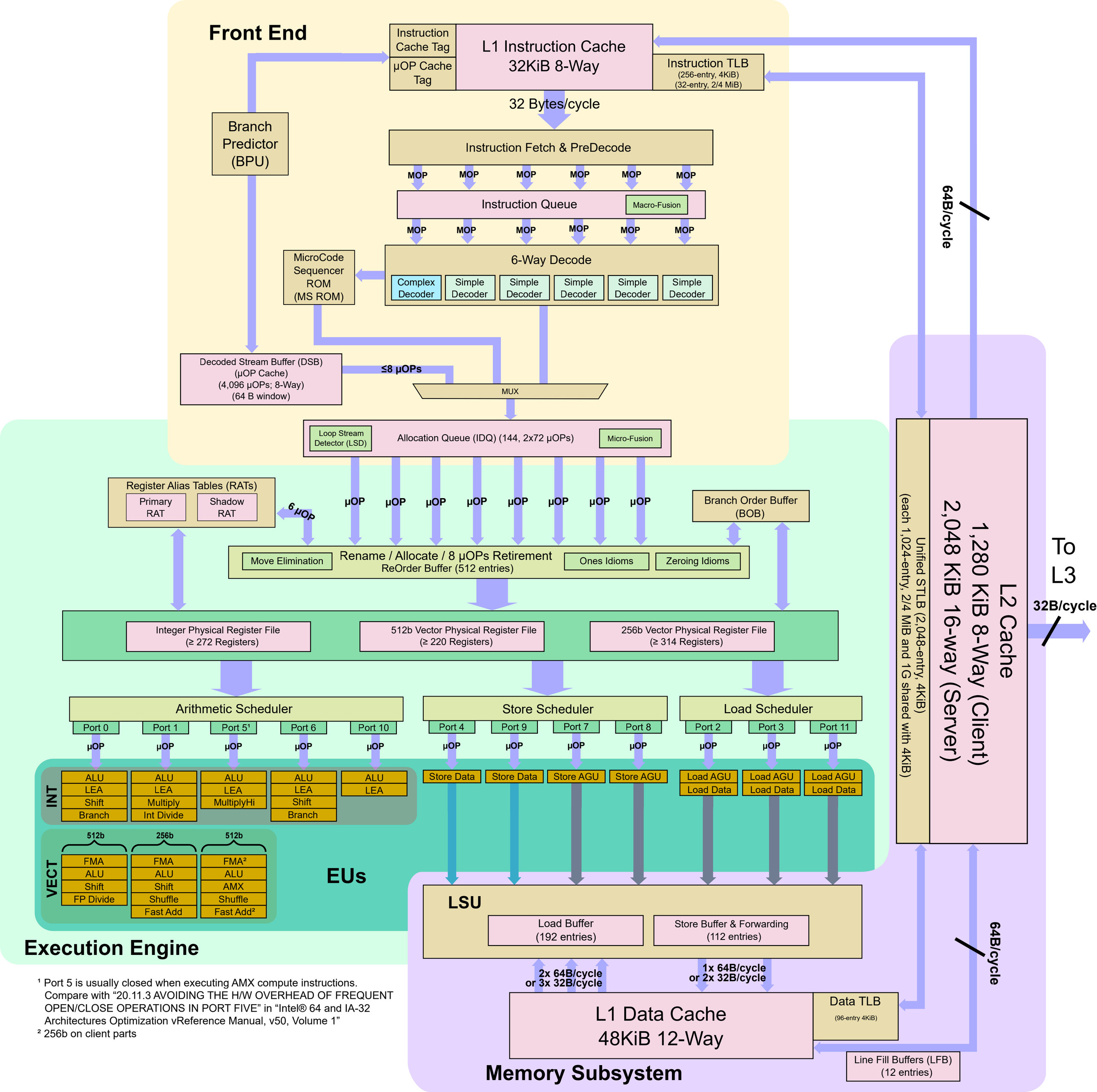

[1] Port 5 is usually closed when executing AMX compute instructions. Compare with "20.11.3 AVOIDING THE H/W OVERHEAD OF FREQUENT OPEN/CLOSE OPERATIONS IN PORT FIVE" in "Intel® 64 and IA-32 Architectures Optimization vReference Manual, v50, Volume 1"

[2] 256b on client parts