Review Test Submission: Midterm

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Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Midterm
Started	3/1/21 1:01 PM
Submitted	3/1/21 3:03 PM LATE
Due Date	3/1/21 3:00 PM
Status	Completed
Attempt Score	55 out of 98 points
Time Elapsed	2 hours, 2 minutes

Instructions

Regarding the Questions

Please read each question carefully before answering. We will be unable to accommodate answers that do not follow the expected format.

Color Guide for Questions to ease understanding of emphasis:

- Main Task is written in **RED Boldface**
- Key points are written in **Black Boldface**
- Advisory notes are prefixed with "Note" and written in *Blue Italics.*

Please be sure to read the advisory notes for "fill-in-the-blank" questions very carefully. These questions are auto-graded so it is important to adhere to the stated advisory for entering answers.

Regarding the Timing

A 5 minute buffer will be added at the end of the exam to accommodate any administrative overhead related to submission. Late submissions beyond the 5-minute buffer will incur 1 point penalty for every minute past the

deadline. Submissions turned in 10 minutes past the buffer (total 15 minutes past the completion time) will NOT be accepted.

Advisory: ***Please do NOT wait to submit the exam at the last minute as it places you at jeopardy of missing the deadline for online submission. As a guide, start turnin preparation BEFORE the deadline to be safe.***

Results Displayed: All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

On my honor, as an Aggie, I promise to abide by the Academic Code of Conduct specified in the course syllabus and will follow the honor code policies stated in the exam preparation guide.

Selected Answer: True

Answers: True
False

Question 2

0 out of 5 points

Minimize the following Boolean equation. Write the steps you took to get to the final answer.

F = xz + x'y + z'y

Note: You do NOT need to write the Boolean laws/theorems that were used in the minimization process. We are ONLY looking for your stepwise approach to minimization.

Selected Answer: F = XZ+Y

Correct Answer:

Note: Partial credits were given for (a) correct answers that were missing the steps or (b) incorrect answers that showed some correct steps

F = xz + x'y + z'y
F = xz + y(x'+z') --> associative
F = xz + y(xz)' --> deMorgan's
F = (xz+y)(xz+(xz)') --> distributive
F = (xz+y)

Response Feedback: No steps shown, talk to Tyagi

Question 3

5 out of 5 points

The well known Binary, Decimal, and Hexadecimal number systems use the bases of 2, 10, and 16 respectively. Suppose we have a *DECA* number system that uses the **base of 20 system**. In this system we use the numbers **0 to 9 and the capital letters A to J** to represent its Binary or Decimal number equivalent, starting with the least significant digit at the right hand side. **The decimal number 1537 in the DECA number system is ____**

Note: Only write the number as expressed in DECA digits in the box.

Selected Answer: 3GH

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	3GH	
Exact Match	03GH	

Response Feedback: 1537_{10} can be evaluated as follows in DECA number system :

First we write the weight of the digits in this number system

position: . 3 2 1 0

weight: 20^3 20^2 20^1 20^0

DECA digit: 0. 3 G H

MULT 0 + $3*20^2$ + $16*20^1$ + $17*20^0$

= $1200+320+17=1537_{10}$

Question 4

4 out of 4 points

A game has **38 possible outcomes**. **The minimum number of bits required to uniquely encode the 38 outcomes in binary number system is _____**

Note: Only write the numerical value of the number of bits in the box.

Selected Answer: 6

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	6	
Exact Match	six	
Exact Match	floor(log38)+1	

Response Feedback: Minimum number of bits to uniquely encode 38 is floor($\log_2 38$)+1

Question 5

0 out of 5 points

We are given a Boolean expression **F = ab + a'c + bc.**

If you could **minimize the above expression** and then implement it using **NAND gates ONLY**, the **number of NAND gates you will need to implement it is**

Selected Answer: A. 3

Answers:
A. 3
B. 4
C. 5
D. 6

Response Feedback:

F = ab + a'c + bc

F = ab + a'c + bc (a+a')

F = ab + a'c + abc + a'bc

F = ab(1+c) + a'c(1+b)

F = ab + a'c

To write it for NAND friendly form:

F = (ab)" + (a'c)" = (a'+b')' + (a"+c')' = P' + Q' or P **NAND** Q, where P = a'+b' and Q = a+c'

P = a **NAND** b and Q = a' **NAND** c

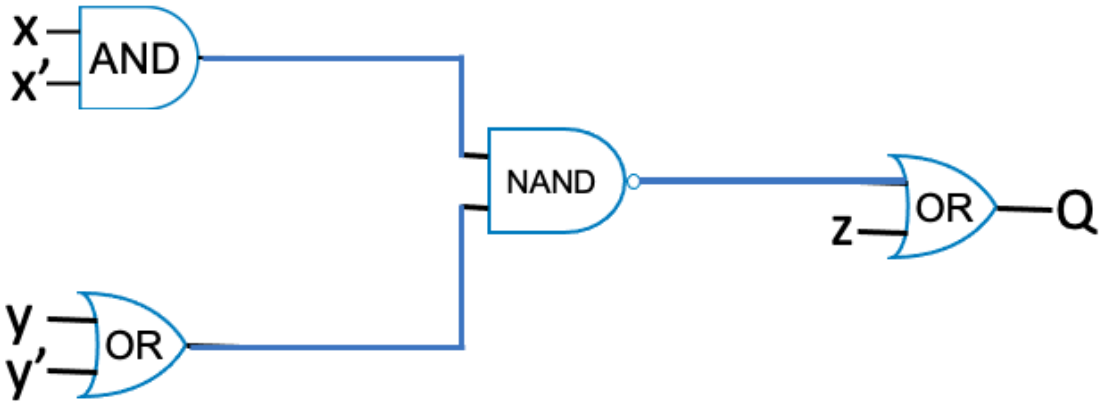
a' = a **NAND** a

Therefore we will need 4 NAND gates to implement the minimized function with NAND only.

Question 6

4 out of 4 points

The **minimized logic expression for the function Q** shown in the logic gate diagram below is



Selected Answer: d. 1

Answers:
a. (xx')' + (y+y')' + z
b. 0
c. x + x' + yy' + z
d. 1

Response Feedback: x.x' will result in 0. This goes as one of the inputs of the NAND gate which is sensitive to 0, and therefore will deliver a 1 on its output. If any input of the OR gate is a 1, its output will be a 1.

Question 7

4 out of 4 points

The logic expression **P = x'yz +xy'z + xyz' + x'y'z' is equivalent to**

Selected Answer: d. x XOR (y XNOR z)

Answers:
a. x OR (y OR z)
b. x XOR (y XOR Z)
c. x XNOR (y XNOR z)
d. x XOR (y XNOR z)

Response Feedback:

P = x'yz +xy'z + xyz' + x'y'z'

P= x'yz+x'y'z' + xy'z+xyz'

P = x'(yz+y'z') + x(y'z+yz')

P = x'(y xnor z) + x(y xor z)

P = x'(y xnor z) + x (y xnor z)'

P = x xor (y xnor z)

Question 8

4 out of 4 points

Which of the logic gates below can be **directly** *(Note: without any other additional gates)* used to **detect if two 8-bit binary numbers are identical**

Selected Answer: b. 2 input 8-bit XNOR gate

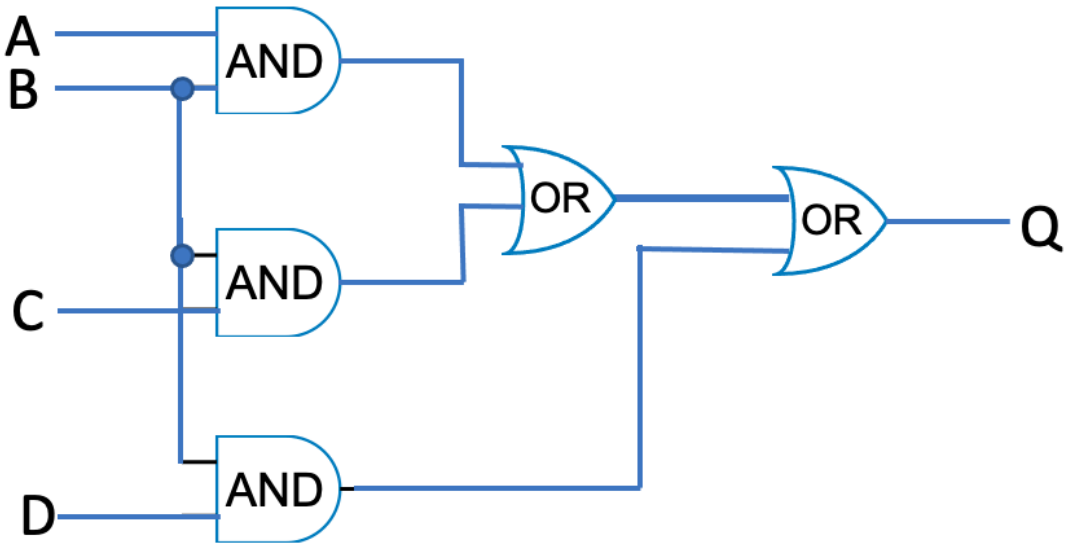
Answers:
a. 2 input 8-bit NAND gate
b. 2 input 8-bit XNOR gate
c. 2 input 8-bit OR gate
d. 2 input 8-bit NOR gate

Response Feedback: For any two inputs A and B, the XNOR operation outputs a 1 if A and B match. The other choices do not work because an OR gate is sensitive to a 1, a NAND gate is sensitive to a 0, and a NAND gate is sensitive to a 0 on either of their inputs regardless of the value of their other input.

Question 9

0 out of 6 points

In the logic gate diagram below, assume that inputs **A, C, and D arrive at the time t=0 and input B arrives at t=3**. Also assume that **all gate delays are 1 ns**.



The length in time of the critical path to the output Q without any modification to the logic is [A] ns.
Now, explore how you can minimize the length of the critical path. There is no restriction on the number of inputs to logic gates (i.e. 2-Way, 3-way, 4-way, ...gates are allowed).
The length in time of the minimized critical path to the output Q is [B] ns.

Note: Just write the numerical values in the boxes.

Specified Answer for: A 3

Specified Answer for: B 2

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	6	
Contains	six	
Correct Answers for: B		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	4	
Contains	four	

Response Feedback: For the first part, the critical path can be either of the two and in both cases it will be 3+1+1+1 = 6ns.

Since the logic function implemented is AB + BC + BD, we can rewrite it as B((A+C)+D). This allows B to be brought as an input in the last stage where it AND's with the partial SOP (A+C)+D. The length of the optimized critical path is 3+1 = 4ns.

Question 10

0 out of 4 points

The total number of MUX2Way chips needed to construct a MUX16Way chip is

Selected Answer: d. None of the above

Answers:
a. 12
b. 14
c. 15
d. None of the above

Response Feedback: To build a MUX16Way chip using Mux2Way chip, we work our way forwards. In the first stage we will need 16/2 = 8 MUX2Way chips to accept all 16 inputs. This stage will generate 8 outputs which will now need 8/2 = 4 MUX2Way chips in the second stage which in turn will generate 4 outputs which will now need 2 MUX2Way chips. Finally we will need 1 Mux2Way to select between the last two outputs. Therefore the number of Mux2Way chips is 8+4+2+1 = 15

Question 11

3 out of 6 points

Suppose there is a **sequence of 5 bits** represented by Boolean variables "**a b c d e**". **Write the logic Boolean expression for a chip that outputs Q=1 if TWO consecutive 0's are detected in the sequence.**

Note: You do NOT need to write HDL, simply a Boolean expression for Q as a function of {a,b,c,d,e}. You do not need to minimize the expression.

Selected Answer:	Q = ab + bc + cd + de
Correct Answer:	for a sequence abcde, two consecutive zeros can be detected by checking two at a time to see if they are both zeros. In other words Q is 1 if a is 0 && b is 0 OR b is 0 && c is 0 OR c is 0 && d is 0 OR d is 0 && e is 0. Therefore **Q = a'b' + b'c' + c'd' + d'e'**
Response Feedback:	Should test if 2 consecutive 0s, not 1s

Question 12

6 out of 6 points

Design a system "MULTOF4" with combinational logic to detect if a 4-bit number N is a multiple of 4. In other words, Q = 1 if N = k * 4 where k >= 0.

Note:

Full points will only be awarded for optimal design that translates to fewest gates. There is no restriction on the type of gate you may use, or the number of gate inputs (i.e. 2-way, 3-way, 4-way,....gates are allowed).

You do NOT need to write HDL. You may typewrite the function Q = f(N) in the form of a logic operation. There is no strict format for your answer, just as long as we can understand howyou generate Q as a function of the input signal N.

Selected Answer:

Suppose there is a **sequence of 4 bits** represented by Boolean variables "**a b c d**" (that define this number N)
because we know that the max value for a 4 bit number in decimal is 15 (binary 1111 = decimal 15)
we know that there can be a total of 4 multiples in the range (ceiling(15/4)). This can be shown in the truth table below :

decimal	a b c d	Q
0	0 0 0 0	1
1	0 0 0 1	0
2	0 0 1 0	0
3	0 0 1 1	0
4	0 1 0 0	1
5	0 1 0 1	0
6	0 1 1 0	0
7	0 1 1 1	0
8	1 0 0 0	1
9	1 0 0 1	0
10	1 0 1 0	0
11	1 0 1 1	0
12	1 1 0 0	1
13	1 1 0 1	0
14	1 1 1 0	0
15	1 1 1 1	0

we see that Q is true 4 times in the truth table . we use these logical values to form the logical expression for Q.
Q = a'b'c'd'+a'bc'd' + ab'c'd'+ a'b'cd = c'd' = (Demorgans law) c nor d
Therefore Q = c NOR d

Correct Answer: For a multiple of 4 we need to have 0 in the last two bits of the number N (0000, 0100, 1000, 1100)
Therefore **Q = N[1] NOR N[0]**

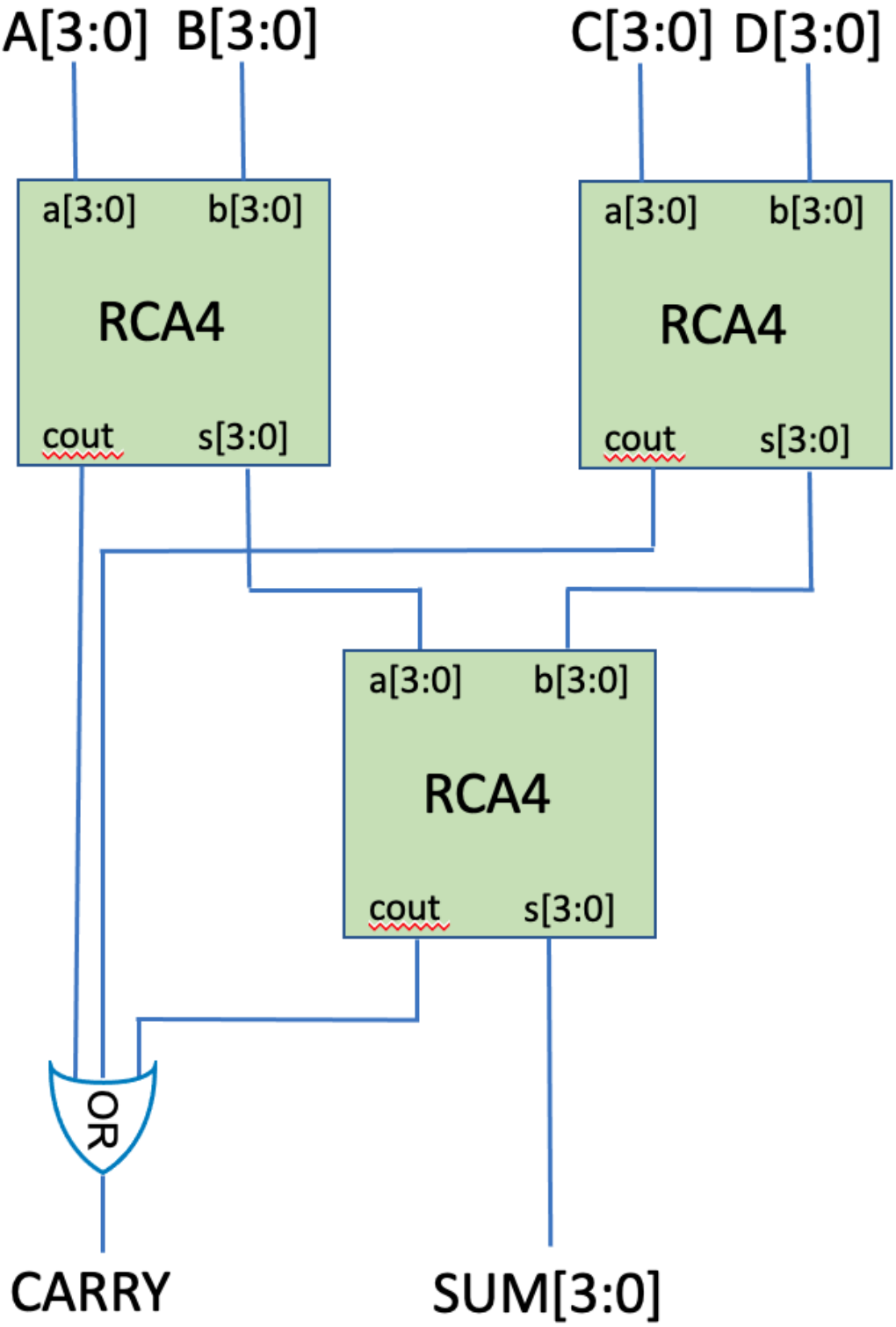
Response Feedback: [None Given]

Question 13 0 out of 6 points

An Adder capable of adding FOUR 4-bit inputs A[3:0], B[3:0], C[3:0], and D[3:0] is shown below. The adder uses 3 RCA4 adders to accomplish the addition.

Here are the assumptions:

- **The RCA4 adders are implemented with 1HA and 3 FA.**
- **AND and OR gate delays are 1 ns, XOR delay is 3 ns**
- **All inputs A[3:0], B[3:0}, C[3:0], and D[3:0] arrive at the same time t=0.**
- **There is no restriction on the number of inputs in logic gates. For example, 2-way, 3-way, 4-way... gates are allowed.**



Calculate the delay of the above adder and write its numerical value in the box _____

Note: As an example, say, the delay is 15ns, just write 15 in the box.

Selected Answer: 24

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity

Exact Match	11
Exact Match	11ns
Exact Match	11 ns
Exact Match	17
Exact Match	17ns
Exact Match	17 ns

Response Feedback: The output of the first stage RCA4 is as follows: Sum bits arrive at 3, 4, 6, 8 and the carryout at 7.

The output of the second stage RCA4 is as follows: Sum bits arrive at 6, 7, 9, 11 and the carryout at 10.

The CARRY will add 1 to the stage 2 carryout and equal to 11.

Both SUM[3] and CARRY will arrive at 11 ns.

If an assumption is made about XOR3 being two stage XOR2, the delays will be incremented by 6ns and hence longest delay will be in SUM path and will be 17ns. This is also deemed as acceptable answer.

Question 14

2 out of 4 points

The range of **8-bit binary numbers represented in 2s complement format** is from **[A]** to **[B]**. **Write the range as integer decimal numbers.**

Note: For example if the range is from -X to Y then you would write the number -X in the first blank space and the number Y in the second blank space.

Specified Answer for: A ✗ -127

Specified Answer for: B ✓ 127

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	-128	
Exact Match	- 128	
Correct Answers for: B		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	+127	
Exact Match	+ 127	
Exact Match	127	

Response Feedback: Range of an n-bit 2's complement is -2^{n-1} to $2^{n-1}-1$

if n==8 then range is -2^7 to 2^7-1 = -128 to 127

Question 15

4 out of 4 points

The number of 16-bit Registers needed to make a 16-bit RAM16 chip is

Selected Answer: 16

Answers: 16

64

128

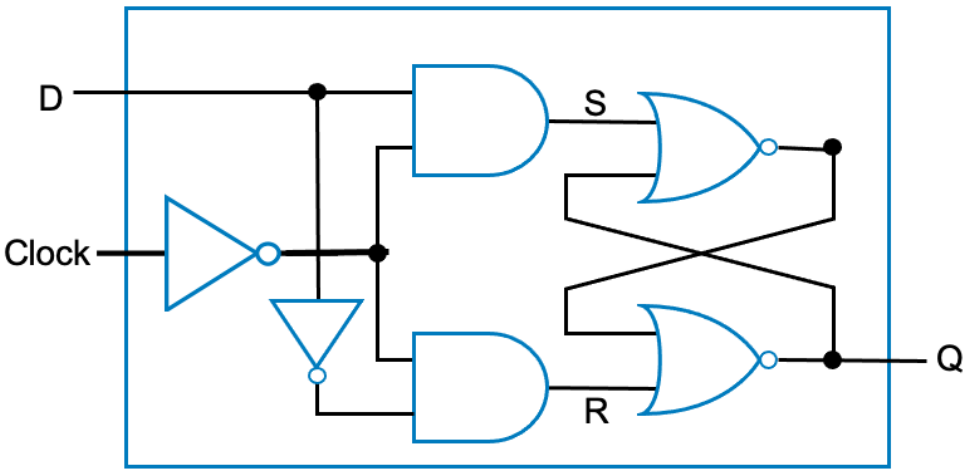
256

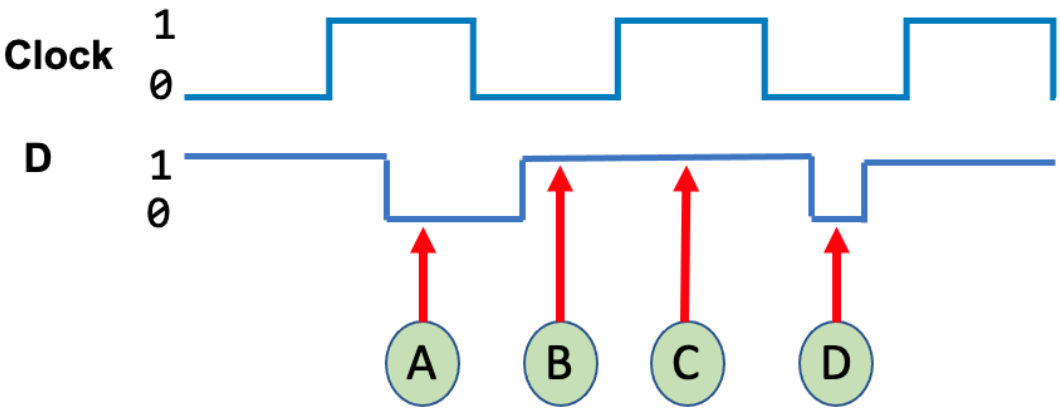
Response Feedback: RAM16 is composed of 16 Registers.

Question 16

2 out of 8 points

A clocked D-Latch is shown in the picture below along with its *clock* and *D* input timing waveforms. Fill in the blanks for the value of its output *Q* (1 or 0) at time marked with symbols A, B, C, and D.





The value of Q at time marked with symbol A is **[A]**

The value of Q at time marked with symbol B is **[B]**

The value of Q at time marked with symbol C is **[C]**

The value of Q at time marked with symbol D is **[D]**

Specified Answer for: A ✗ 0

Specified Answer for: B ✗ 0

Specified Answer for: C ✓ 1

Specified Answer for: D ✗ 1

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	1	
✓ *Exact Match*	ONE	
Correct Answers for: B		

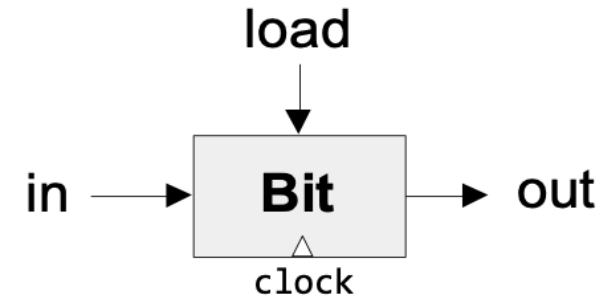
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	1	
Exact Match	ONE	
Correct Answers for: C		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	1	
Exact Match	ONE	
Correct Answers for: D		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	0	
Exact Match	ZERO	

Response Feedback: Since inverted Clock goes to the AND gates, the D-Latch allows D input changes to reflect on the output only during Clock==0 phases. In other words, the latch is "closed" when Clock == 1 so no D input changes during Clock ==1 are registered to the latch output.

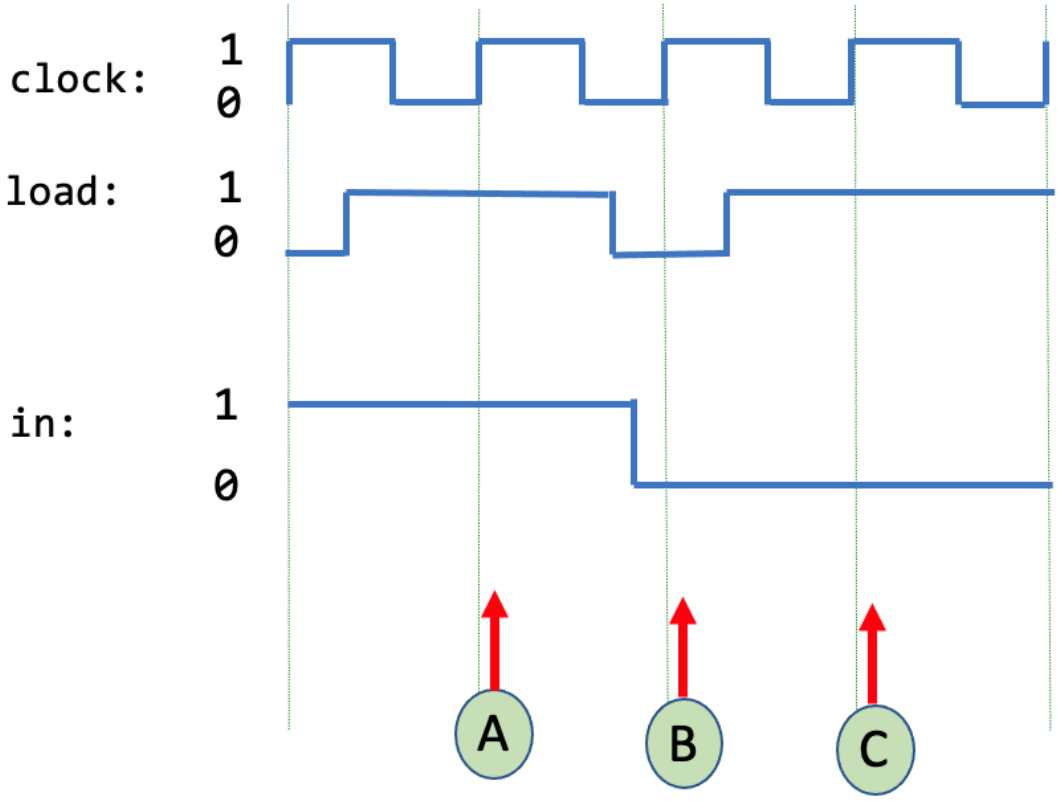
Question 17

6 out of 6 points

A clocked 1-bit register is shown in the picture below along with its *clock, load, and in* timing waveforms. Fill in the blanks for the value of its output *out* (1 or 0) at time marked with symbols A, B, and C.



if load(t) then out($t+1$) = in(t)
else out($t+1$) = out(t)



The value of *out* at time marked with symbol *A* is **[A]**

The value of *out* at time marked with symbol *B* is **[B]**

The value of *out* at time marked with symbol *C* is **[C]**

Specified Answer for: A ✓ 1

Specified Answer for: B ✓ 1

Specified Answer for: C ✓ 0

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	1	

Exact Match	ONE	
Correct Answers for: B		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	1	
Exact Match	ONE	
Correct Answers for: C		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	0	
Exact Match	ZERO	

Response Feedback: When load is inactive, input changes are not registered.

Question 18

4 out of 4 points

Consider a **RAM chip consisting of 256 registers, each 32-bits wide. The minimal width in number of bits of the address input of this RAM chip is**

Selected Answer: C. 8

Answers:
A. 32
B. 16
C. 8
D. 5
E. None of the above

Response Feedback: address bits = $\log_2 256 = 8$

Question 19

4 out of 4 points

The number of DFF's needed to make a 16-bit RAM16 chip is

Selected Answer: D. 256

Answers:
A. 16
B. 64
C. 128
D. 256
E. None of the above

Response Feedback: 16 bit RAM16 chip will have 16 x 16 BITs. Each BIT is made of 1 DFF. Therefore total number of DFFs is 256.

Question 20

2 out of 8 points

BONUS QUESTION for EXTRA CREDITS

In this problem, you are expected to design a soft drink vending machine controller that is specified as follows:

1. A drink costs 10 cents (10c).
2. Assume that the only valid coin denomination is 10c.
3. Machine initial deposit state is 0c. No coin inserted is treated as 0c.
4. The machine dispenses a drink only when deposit = 10c AND the input button “P” is pressed.
5. The machine dispenses a drink by turning the output signal Q=1.
6. The machine is reset to 0c deposit state when a drink is dispensed.
7. Any extra change is not returned and also does not change the deposit state.

Your task:

- **Draw the state diagram (2 points).**
- **Choose encoding for states and inputs and write the truth table (3 points).**
- **Write the minimized logic equations for output and next state (3 points).**

You may draw and handwrite your answer on a piece of paper and upload a camera picture of your answer, or use a Word Processor to document your answer and upload a PDF. Be sure to state any assumptions you make.

Note: The points reflect the share of the grade for the sub-parts of the question. For each sub-part, the scoring will be on a binary scale to ease grading: Full marks for correct answer and Zero marks for wrong answer. Benefit of doubt will be given for "90%" correct answer.

Selected Answer: unnamed.jpg

Response Feedback: [None Given]

Tuesday, May 11, 2021 11:35:17 AM CDT

← OK