Review Test Submission: Q13

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q13
Started	3/4/21 9:40 PM
Submitted	3/4/21 9:42 PM
Due Date	3/4/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	1 minute
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

Machine Language instructions are constituted of 1s and 0s in a format specific to a given Computing Machine

Selected Answer: True
Answers: True
False

Response Feedback: While it is true that high level programs are written in English like language, the language that a (digital) computer understands is constituted of 1s and 0s.

Question 2

1 out of 1 points

The von Neumann architecture of a stored program computer models separate program and data memories.

Selected Answer: False
Answers: True
False

Response Feedback: von Neumann model requires unified program and data memory

Question 3

1 out of 1 points

The Harvard architecture of a stored program computer models separate program and data memories.

Selected Answer: True
Answers: True
False

Question 4

1 out of 1 points

A Programmer's traditional view of a computer as far as programming interface is concerned comprises of Memory (address and content), CPU (operations), and Registers (quick access data).

Selected Answer: True
Answers: True
False

Question 5

1 out of 1 points

As computer scientists, we care to understand and learn machine (assembly) language as it is a useful skill for when code performance is critical.

Selected Answer: True
Answers: True
False

Response At the level of machine(assembly) language, a programmer has direct access to a machine instruction and all its programmer visible resources

Feedback: whereas with traditional high-level programming, one is left to trust the effectiveness of compilers to produce optimal code for performance.

Monday, May 3, 2021 9:58:30 AM CDT

← OK

Review Test Submission: Q14

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q14
Started	3/9/21 9:54 AM
Submitted	3/9/21 9:10 PM
Due Date	3/9/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	11 hours, 16 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

A typical operation "x=x+4" expressed in a high level language constitutes which class (categories) of machine language instructions?

Selected Answer: b. Arithmetic and Memory Instructions

Answers:
a. Arithmetic Instructions
b. Arithmetic and Memory Instructions
c. Memory Instructions
d. None of the above

Response Feedback: x=x+4 involves an arithmetic addition operation and also a memory access operation for variable x

Question 2

1 out of 1 points

A high level operation "if x==4 then y=5" generates a **conditional instruction** in machine language

Selected Answer: True

Answers:
True
False

Response It is a conditional instruction because the outcome of the test determines

Feedback: the outcome

Question 3

1 out of 1 points

In a memory hierarchy that employs a spectrum of memory ranging from Registers on one end and SSD/Disk on the other end, the only two components of the hierarchy that are visible to a programmer are Cache Memory and SSD/Disk.

Selected Answer: False

Answers: True
False

Response Feedback: Registers and Main Memory are made programmer visible through a machine instruction set

Question 4

1 out of 1 points

A machine language instruction "Load R1, M[A]" is an example of which class of machine language addressing modes?

Selected Answer: a. Indirect

Answers: a. Indirect
b. Direct
c. Immediate
d. Register

Response Feedback: A machine language instruction "Load R1, M[A]" is an example of indirect addressing mode since the memory address is indirectly specified through a pointer that resides in Address Register A.

Question 5

1 out of 1 points

A machine language instruction "Sub R1, 1" is an example of which class of machine language addressing modes?

Selected Answer: b. Immediate

Answers: a. Direct
b. Immediate
c. None of the above
d. Indirect

Response Feedback: A machine language instruction "Sub R1, 1" is an example of immediate addressing mode.

Monday, May 3, 2021 10:00:58 AM CDT

← OK

Review Test Submission: Q15

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q15
Started	3/11/21 7:50 PM
Submitted	3/11/21 8:03 PM
Due Date	3/11/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	12 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

2 out of 2 points

Which of the following sets of Hack commands will effect the operation RAM[17]=2? Mark all correct answers.

NOTE: The instructions are separated by a comma to conserve space.

Selected Answers:
- a. `@2, D=A, @17, M=D`
- b. `@17, M=1, M=M+1`

Answers:
- a. `@2, D=A, @17, M=D`
- b. `@17, M=1, M=M+1`
- c. `@17, M=2`
- d. (a), (b), and (c)
- e. All answers are wrong

Response Feedback: `@2, D=A, @17, M=D` and `@17, M=1, M=M+1` are both correct.

Question 2

1 out of 1 points

The A register can be used to store data and also to address the memory (RAM and ROM)

Selected Answer: True

Answers: True
False

Response Feedback: @21 puts 21 in the A register.

Example usages:

Use of A as data: D=A //D=21

Use of A as RAM address: D=M //D = RAM[21]

Use of A as ROM address: D;JLE //Jump to location 21 in the ROM is D is less than or equal to 0

Question 3

2 out of 2 points

Which of these instructions translates to the binary instruction 1111010101101100?

Symbolic syntax: *dest* = *comp* ; *jump*

Binary syntax: 1 1 1 a c1 c2 c3 c4 c5 c6 d1 d2 d3 j1 j2 j3

comp		c1	c2	c3	c4	c5	c6
0		1	0	1	0	1	0
1		1	1	1	1	1	1
-1		1	1	1	0	1	0
D		0	0	1	1	0	0
A	M	1	1	0	0	0	0
!D		0	0	1	1	0	1
!A	!M	1	1	0	0	0	1
-D		0	0	1	1	1	1
-A	-M	1	1	0	0	1	1
D+1		0	1	1	1	1	1
A+1	M+1	1	1	0	1	1	1
D-1		0	0	1	1	1	0
A-1	M-1	1	1	0	0	1	0
D+A	D+M	0	0	0	0	1	0
D-A	D-M	0	1	0	0	1	1
A-D	M-D	0	0	0	1	1	1
D&A	D&M	0	0	0	0	0	0
D|A	D|M	0	1	0	1	0	1
a=0	a=1						

dest	d1	d2	d3	effect: the value is stored in:
null	0	0	0	The value is not stored
M	0	0	1	RAM[A]
D	0	1	0	D register
MD	0	1	1	RAM[A] and D register
A	1	0	0	A register
AM	1	0	1	A register and RAM[A]
AD	1	1	0	A register and D register
AMD	1	1	1	A register, RAM[A], and D register

jump	j1	j2	j3	effect:
null	0	0	0	no jump
JGT	0	0	1	if out > 0 jump
JEQ	0	1	0	if out = 0 jump
JGE	0	1	1	if out ≥ 0 jump
JLT	1	0	0	if out < 0 jump
JNE	1	0	1	if out ≠ 0 jump
JLE	1	1	0	if out ≤ 0 jump
JMP	1	1	1	Unconditional jump

Selected Answer: a. AM=D|M;JLT

Answers: a. AM=D|M;JLT

b. AM=D&M;JLT

c. AM = D|A; JLT

d. D|M; JNE

e. AM=D|M;JLE

Response Feedback:

Refer to the table:

MSB=1 means it is a C instruction

Now bits [2:0] are the jump bits and they are '100 which shows as JLT in the JUMP table

bits [5:3] are the dest bits and they are '101 which shows as AM in the DEST table

Finally, bits [12:6] are the comp bits of which bit 12 is a and bits 11:6 are c bits

a bit [12] is 1 so we look in the a=1 column of the COMP table

c bits [11:6] are 010101 which is D|M in the COMP table

Monday, May 3, 2021 10:03:07 AM CDT

← OK

Review Test Submission: Q16

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q16
Started	3/16/21 5:05 PM
Submitted	3/16/21 5:41 PM
Due Date	3/16/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	36 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

Which of the following lines completes the HACK program so that RAM[11]=10?

@10

D=A

A=D+1

Selected Answer: d. M=D

Answers:
a. M=A
b. D=A
c. D=M
d. M=D

Response Feedback:

@10 //A=10

D=A //D = 10

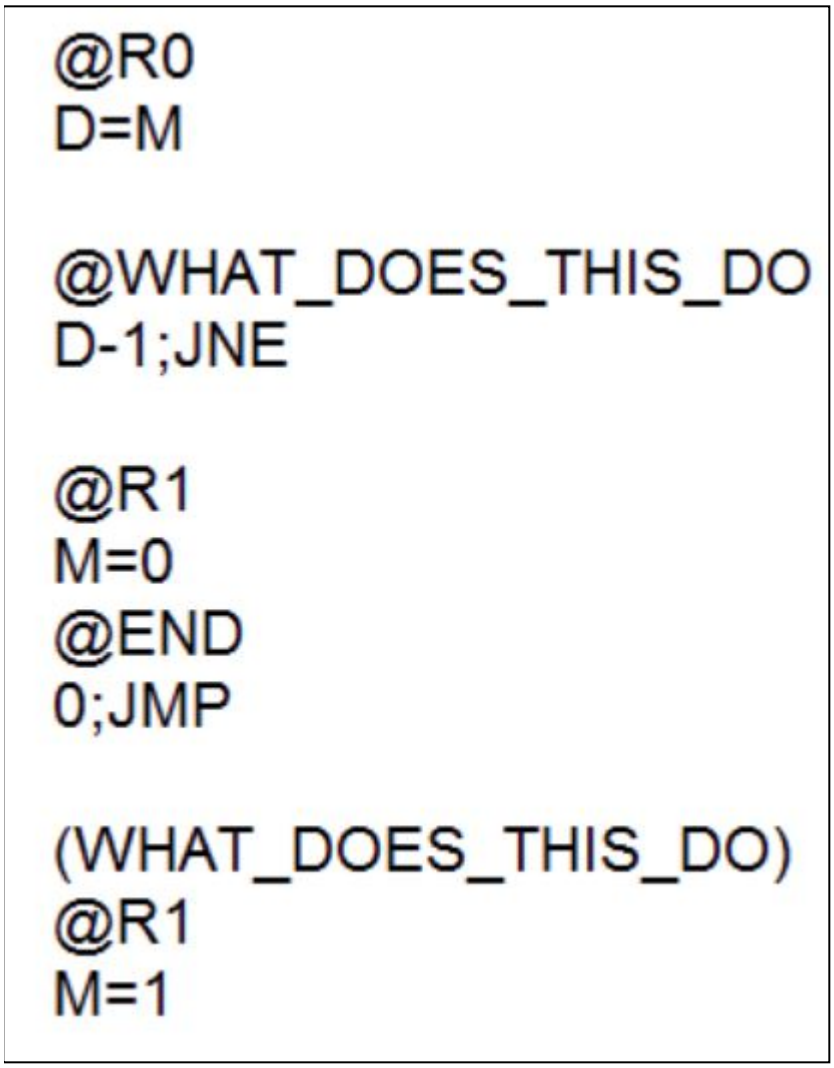
A=D+1 //A=10+1=11

therefore M=D would be M[11] = D = 10

Question 2

1 out of 1 points

What label would be the most descriptive replacement for the label symbol "WHAT_DOES_THIS_DO"?



Selected Answer: NOT_EQUAL_TO_1

Answers:
- NOT_EQUAL_TO_0
- NEGATIVE
- SMALLER_THAN_1
- NOT_EQUAL_TO_1
- GREATER_THAN_1

Response Feedback: D-1;JNE results in D-1 operation and jumping to ROM location in A if D-1 <> 0 or D<>1

Question 3

1 out of 1 points

Accessing a pointer usually involves:

Selected Answer: a. Assigning the address register A to a value retrieved from memory.

Answers:
a. Assigning the address register A to a value retrieved from memory.
b. Assigning a memory register to the value of the address register.
c. Changing a memory register using another memory register.
d. Combining the values of the A register and the D register.

Response Feedback: A pointer is a memory location containing an address. Therefore we first load A register with the pointer and then use A to reference the memory.

Question 4

2 out of 2 points

What would be the value in memory location holding the variable foo if R0 contained the value 5 and the following HACK program is executed?

```
        @R0
        D=M
        @foo
        M=0

(LOOP)
        @END
        D;JEQ
        @foo
        M=M+D
        D=D-1
        @LOOP
        0;JMP

(END)
        @END
        0;JMP
```

Selected Answer: d. 15

Answers:
a. 20
b. 10
c. 30

d. 15

e. 25

Response Feedback: The loop will start with D=5, then every iteration D reduces by 1 and adds to the sum resulting in 5+4+3+2+1 = 15

Monday, May 3, 2021 11:21:25 AM CDT

← OK

Review Test Submission: Q17

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q17
Started	3/18/21 2:06 PM
Submitted	3/18/21 11:13 PM
Due Date	3/18/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	9 hours, 6 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

The number of 16-bit registers needed to map the screen display on RAM of our HACK computer is

Selected Answer: a. 8K

Answers: a. 8K

b. 4K

c. 2K

d. 16K

Response Feedback: Total 8K 16 bit registers are dedicated to memory mapped IO for display (screen) ranging from 16384 to 24575 (both inclusive)

Question 2

1 out of 1 points

The number of 16-bit registers needed to map the keyboard on RAM of our HACK computer is

Selected Answer: b. 1

Answers: a. 16

b. 1

c. 16384

d. 24576

Response Feedback: The keyboard is mapped to single memory location address 24576, so only 1 register is mapped to the keyboard.

Question 3

2 out of 2 points

The base RAM address for Screen memory map is 16384. Setting pixel (row, column) = (150, 275) black on the display is achieved by setting bit 3 of which RAM address (register) to a 1?

Selected Answer: a. 21201

Answers: a. 21201

b. 20000

c. 21000

d. 20021

Response Feedback:

The register selected for Row 150 Column 275 is calculated as follows:

Rows start with index 0.

Screen base address is Register #16384.

Each row has 32 16-bit registers.

Total registers in 150 rows (0..149) is equal to 150 * 32 = 4800 leading to address 16384+4800 = 21,184

Remaining registers can be calculated using column information. Each column is single bit. Hence, register selected in Row 150 will be floor integer of 275/16 = 17. We add this to 21, 184 to result in Register address 21201.

Now, to find which bit of this register needs to be written with a 1, all you need to do is to do col mod 16 which in this case will be 275 mod 16 i.e. 3.

So it is bit 3 of register # 21201.

To summarize, to set pixel (row,col) on/off:
(1) word = RAM[16384 + 32*row + col/16]
(2) Set the (col % 16)th bit of word to 0 or 1
(3) RAM[i] = word

Question 4

1 out of 1 points

To construct HACK MEMORY, one needs to create a 16K RAM with 14 address bits, and use built-in versions of 8K screen chip with 13 address bits and 1 word keyboard chip with address matched to 0x6000.

Selected Answer: True

Answers: True

False

Monday, May 3, 2021 11:39:55 AM CDT

← OK

Review Test Submission: Q18

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q18
Started	3/23/21 3:17 PM
Submitted	3/23/21 5:43 PM
Due Date	3/23/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	2 hours, 26 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

The *program counter*

Selected Answer: c. Contains the address of the next instruction that should be fetched from the instruction memory

Answers:

a. Counts the number of iterations in the current loop

b. Counts the number of functions that were called thus far in the program

c. Contains the address of the next instruction that should be fetched from the instruction memory

d. Keeps track of how many cycles the program has been running so far

Response Feedback: The program counter has the provision of being loaded with a value from the A-register depending on unconditional jump or a true conditional jump instruction. The next instruction will be selected from this loaded address.

Question 2

1 out of 1 points

In the Hack hardware platform, the logic that decides which instruction to fetch next

Selected Answer: d. Is based on bits that come from the instruction and from the ALU

Answers:
a. Is in charge for handling low-level operating system calls
b. Must be implemented using a separate control chip
c. Is solely implemented inside the ALU
d. Is based on bits that come from the instruction and from the ALU

Response Feedback: The next instruction address is present in the A-register. The jump bits come from the instruction bits Instruction[2:0]. The jump conditions zr and ng are calculated by the ALU based on the comp performed by the ALU.

Question 3

1 out of 1 points

The destination of computation performed by an Instruction is determined

Selected Answer: a. Solely by the Instruction[5:3] bits that serve as destination of computation. Note that the instruction is a 16 bit field noted as Instruction[15:0].

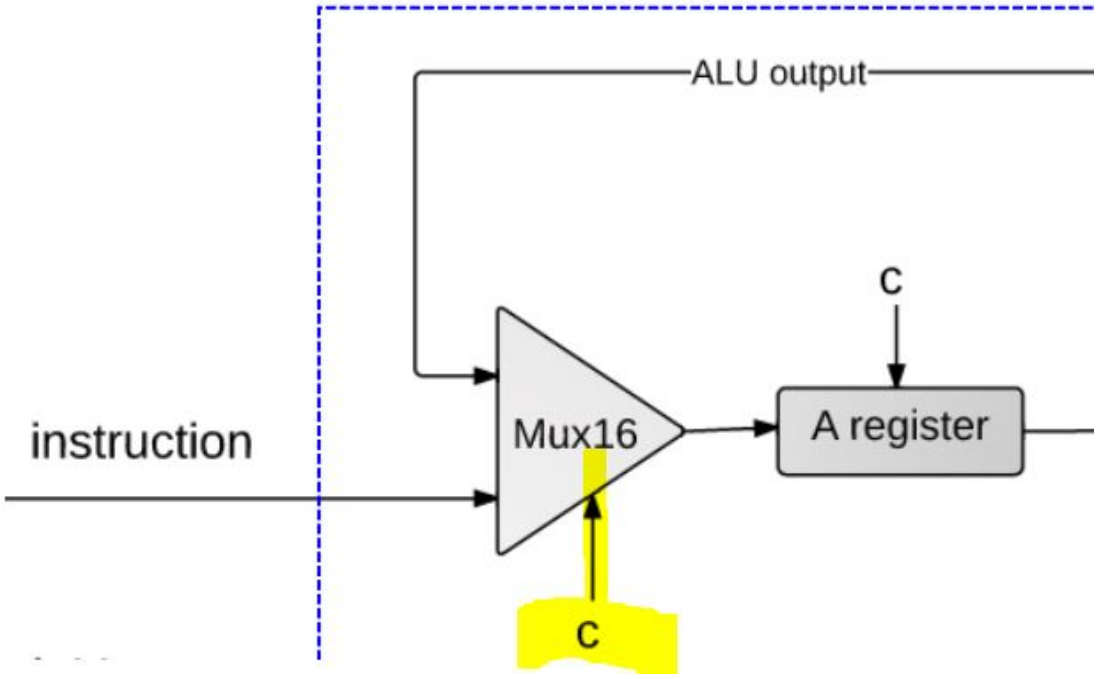
Answers:
a. Solely by the Instruction[5:3] bits that serve as destination of computation. Note that the instruction is a 16 bit field noted as Instruction[15:0].
b. based on the result of the computation performed by the ALU
c. Solely by the Instruction[2:0] bits that serve as destination of computation. Note that the instruction is a 16 bit field noted as Instruction[15:0].
d. Together by the content of the A-register and the Instruction[5:3] bits. Note that the instruction is a 16 bit field noted as Instruction[15:0].

Response Feedback: In a 16-bit instruction denoted as Instruction[15:0], Instruction[5:3] bits indeed serve as destination of computation.

Question 4

1 out of 1 points

Which bit of the instruction Instruction[15:0] will be instrumental in acting as the **select signal** (in yellow highlight) of the MUX that feeds into the A-register in the following picture?



Selected Answer: d. Bit 15 of Instruction[15:0] i.e. Instruction[15]

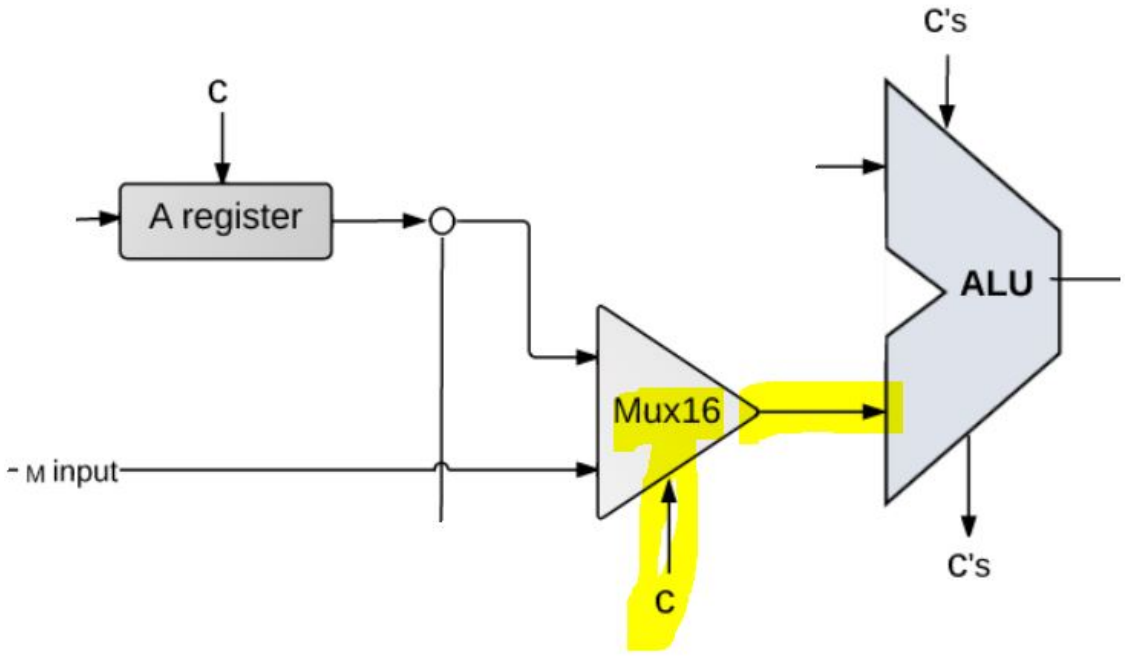
Answers:
a. Bit 0 of Instruction[15:0] i.e. Instruction[0]
b. Bit 1 of Instruction[15:0] i.e. Instruction[1]
c. Bit 14 of Instruction[15:0] i.e. Instruction[14]
d. Bit 15 of Instruction[15:0] i.e. Instruction[15]

Response Feedback: Instruction[15] is a 0 is it is an A-instruction and a 1 if it is a C-Instruction. Clearly, the MUX into A should be controlled by Instruction[15] bit.

Question 5

1 out of 1 points

Which bit of the instruction Instruction[15:0] will be instrumental in acting as the **select signal** (in yellow highlight) of the MUX that feeds into the second input of the ALU in the following picture?



Selected Answer: b. Bit 12 of Instruction[15:0] i.e. Instruction[12]

Answers:
a. Bit 15 of Instruction[15:0] i.e. Instruction[15]
b. Bit 12 of Instruction[15:0] i.e. Instruction[12]
c. Bit 0 of Instruction[15:0] i.e. Instruction[0]
d. Bit 5 of Instruction[15:0] i.e. Instruction[5]

Response Feedback: Instruction[12] is the "a" bit which in the COMP table selects whether we have the second source as A or M. Notice that the a=0 column only shows A as the second source (D being the other). Then a=1 column shows M as the second source (D being the other).

Monday, May 3, 2021 11:44:37 AM CDT

← OK

Review Test Submission: Q19

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q19
Started	3/25/21 3:14 PM
Submitted	3/25/21 3:32 PM
Due Date	3/25/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	17 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

Assembler is a software created to convert code written in assembly (mnemonic) language to machine (1s and 0s) language

Selected Answer: True

Answers: True

False

Question 2

1 out of 1 points

The HACK instruction M=D translates to the bit pattern -

Selected Answer: c. 1110001100001000

Answers: 1110001100000000

a. 0110001100000000

b. 1110001100001000

c. 1000001100001000

d.

Response Feedback: Refer to the HACK C instruction table and carefully look at the opcode, COMP, DEST, and JUMP bits

Question 3

1 out of 1 points

The HACK machine code: 1111000010010000 corresponds to which HACK assembly instruction?

Selected Answer: D = D + M

Answers:
- M = D
- D = M; JLE
- D = D + M
- D = D|M

Response Feedback: The MSB is 1 so it is a C instruction. Refer to the HACK C instruction table and carefully look at the opcode, COMP, DEST, and JUMP bits. For an 16 bit instruction these are -

1 11 a c1 c2 c3 c4 c5 c6 d1 d2 d3 j1 j2 j3

Map the given bits to the above pattern and then look at the tables to realize the correct instruction.

Question 4

1 out of 1 points

The HACK assembler software starts parsing from the 1st line of HACK assembly code and only converts lines with valid A and C instructions into corresponding HACK machine code. In this process it ignores empty lines and comment lines.

Selected Answer: True

Answers:
- True
- False

Question 5

1 out of 1 points

The HACK Machine code 0000000000000101 translates to which valid HACK assembly instruction?

Selected Answer:	d. @5
Answers:	a. M=D
	b. D = A
	c. A = 5
	d. @5
Response Feedback:	The MSB = 0 implies it is an A instruction. The magnitude of this number is 5 in decimal.

Monday, May 3, 2021 11:48:52 AM CDT

← OK

Review Test Submission: Q20

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q20
Started	3/30/21 8:10 PM
Submitted	3/30/21 8:49 PM
Due Date	3/30/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	39 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

In the *symbol table* used by the assembler, each row resolves (gives meaning) to a

Selected Answer: c. Either a variable or a label

Answers:
a. Variable
b. Label
c. Either a variable or a label
d. None of the above

Response Feedback: A symbol table consists of symbol and their assigned values on each row. These symbols can be labels or regular and predefined symbols that are used as variables.

Question 2

1 out of 1 points

In the *first pass* of our two-pass assembly process, the assembler handles only

Selected Answer: e. Labels

Answers:
a. A-instructions (addressing instructions)

C-instructions (compute instructions)

b.

c. A-instructions that contain symbols

d. C-instructions that contain symbols

e. Labels

Response Feedback: Among the choices given, the most appropriate answer is Labels since in the first pass, the assembler goes from top to bottom and keeps a line # count where as soon as it encounters a LABEL it assigns the line number to that LABEL in the symbol table. The second pass of the code uses this information for flow control references.

Question 3

1 out of 1 points

When translating `D+M` into binary code, the assembler

Selected Answer: Generates the binary equivalent of the `D+M` mnemonic

Answers:

Evaluates `D`, evaluates `M`, and emits binary code that adds them up

Evaluates `D+M` and stores the result in a temporary variable

Generates the binary equivalent of the `D+M` mnemonic

Generates a command that pops `D` and `M` from the stack and computes their sum

Response Feedback: D+M is comp mnemonic for which the binary encoding exists in the comp table of the C Instruction.

Question 4

1 out of 1 points

Suppose that during the second pass of the assembly process, the command `@x` is encountered, and `x` does not appear in the symbol table. What should the assembler do?

Selected Answer: c. Allocate `x` to some address in the RAM, say *n* and add `(x,n)` to the symbol table, where *n* is an integer

Answers:

a. Issue an error message

b. Allocate `x` to some address in the ROM, say *n*

c. Allocate `x` to some address in the RAM, say *n* and add `(x,n)` to the symbol table, where *n* is an integer

d. Exit the main routine

Response Feedback: When the assembler encounters an A instruction that calls a variable, the assembler looks in the symbol table to see if that variable already exists in the symbol table. If it does NOT, then the assembler assigns a memory location to the variable, and then creates an entry in the symbol table with the variable and corresponding memory address assigned to the variable.

Question 5

1 out of 1 points

If two symbols have identical values in the Symbol Table, it likely means that one symbol is a variable symbol pointing to an address in the RAM and the other is a label symbol pointing to an address in the ROM.

Selected Answer: True

Answers: True

False

Monday, May 3, 2021 11:53:25 AM CDT

← OK

Review Test Submission: Q21

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q21
Started	4/1/21 8:17 PM
Submitted	4/1/21 8:18 PM
Due Date	4/2/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	1 minute
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

How many bytes are in 32 GB of memory?

Selected Answer: ✓ b. 2^{35}

Answers:
a. $\log_2 2^{32}$
✓ b. 2^{35}
c. 2^{32}
d. $\log_2 32$

Response Feedback: 32 GB = 32 * 2^{30} Bytes = 2^5*2^{30} Bytes = 2^{35} Bytes

Question 2

1.25 out of 1.25 points

How many address bits will be needed to address 17 GB of memory?

Selected Answer: ✓ d. 35

Answers:
a. 34
b. 25

c. 24

d. 35

Response Feedback: To address 17 GB we will need (ceiling($\log_2 17$) + $\log_2 2^{30}$) bits = 5+30 = 35 bits

Question 3

0.75 out of 0.75 points

Solid State Drive (SSD) memory is an example of non-volatile memory

Selected Answer: True

Answers: True

False

Question 4

2 out of 2 points

A 16 GB memory organized in words of 4 Bytes each will have how many bits dedicated to identifying a word?

Selected Answer: 32

Answers: 30

32

34

36

Response Feedback: A 16 GB memory organized in words of 4 Bytes each will have total $\log_2(16*2^{30})$ bit address. This ends up being 34 bit address. Of this, $\log_2 4$ (=2) will be the number of bits dedicated to Byte Offset (i.e. to id one out of 4 Bytes in a given selected word). Hence you will need 34-2 = **32 bits** for determining the entry (word) address.

Monday, May 3, 2021 12:01:36 PM CDT

← OK

Review Test Submission: Q22

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q22
Started	4/8/21 8:36 PM
Submitted	4/8/21 8:43 PM
Due Date	4/8/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	6 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

If the physical memory size is doubled without changing any of its other parameters, the **number of bits in each entry of the page table**

Selected Answer: d. Increases by 1 bit

Answers:
a. Halves
b. Reduces by 1
c. Remains unchanged
d. Increases by 1 bit
e. Doubles

Response Feedback: Assuming the frame size remains the same, there are now twice as many physical pages, so the physical page number needs to expand by 1 bit.

Question 2

1 out of 1 points

If the physical memory size is doubled without changing any of its other parameters, the number of entries in the page table

Selected Answer: c. Remains unchanged

Answers:
a. Increases by 1 bit

b. Reduces by 1 bit

c. Remains unchanged

d. Doubles

e. Halves

Response Feedback: No change. The number of entries in the page table is determined by the size of the virtual address (page number) and the size of a page. It's not affected by the size of physical memory.

Question 3

1 out of 1 points

In a byte addressable virtual memory with 8-bit virtual memory addresses, 8 pages of virtual memory, and 4 frames of physical memory, the frame size is

Selected Answer: a. 32 bytes

Answers:
a. 32 bytes

b. 64 Bytes

c. 256 Bytes

d. None of the above

Response Feedback: In a byte addressable virtual memory with 8-bit virtual memory addresses and 8 pages of virtual memory, the page size is 2^8/2^3 = 2^5 = 32 Bytes. Frame size in memory is the same as page size, hence frame size is 32 Bytes as well.

Question 4

1 out of 1 points

The number of bits representing the Virtual Page Number in a virtual memory system with 8 GB Physical Memory, 256 GB Virtual Memory, and 4 KB Page Size is

Selected Answer: c. 26 bits

Answers:
a. 24 bits

b. 28 bits

c. 26 bits

d. 38 bits

Response Feedback: The number of bits representing the Virtual Page Number in a virtual memory system with 8 GB Physical Memory, 256 GB Virtual Memory, and 4 KB Page Size is calculated as follows:

256GB of Virtual memory translates to $\log_2 256*2^{30}$ bits = 38 bits of Virtual Address. Of this, the page (frame) offset is 12 bits since page (frame) size is 4KB. Therefore the Virtual Page Number is 38-12 = 26 bits.

Question 5

1 out of 1 points

In a virtual memory system, each process must have its own page table.

Selected Answer: True

Answers: True

False

Monday, May 3, 2021 12:07:52 PM CDT

← OK

Review Test Submission: Q22

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q22
Started	4/8/21 8:36 PM
Submitted	4/8/21 8:43 PM
Due Date	4/8/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	6 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

If the physical memory size is doubled without changing any of its other parameters, the **number of bits in each entry of the page table**

Selected Answer: d. Increases by 1 bit

Answers:
a. Halves
b. Reduces by 1
c. Remains unchanged
d. Increases by 1 bit
e. Doubles

Response Feedback: Assuming the frame size remains the same, there are now twice as many physical pages, so the physical page number needs to expand by 1 bit.

Question 2

1 out of 1 points

If the physical memory size is doubled without changing any of its other parameters, the number of entries in the page table

Selected Answer: c. Remains unchanged

Answers:
a. Increases by 1 bit

b. Reduces by 1 bit

c. Remains unchanged

d. Doubles

e. Halves

Response Feedback: No change. The number of entries in the page table is determined by the size of the virtual address (page number) and the size of a page. It's not affected by the size of physical memory.

Question 3

1 out of 1 points

In a byte addressable virtual memory with 8-bit virtual memory addresses, 8 pages of virtual memory, and 4 frames of physical memory, the frame size is

Selected Answer: a. 32 bytes

Answers:
a. 32 bytes

b. 64 Bytes

c. 256 Bytes

d. None of the above

Response Feedback: In a byte addressable virtual memory with 8-bit virtual memory addresses and 8 pages of virtual memory, the page size is 2^8/2^3 = 2^5 = 32 Bytes. Frame size in memory is the same as page size, hence frame size is 32 Bytes as well.

Question 4

1 out of 1 points

The number of bits representing the Virtual Page Number in a virtual memory system with 8 GB Physical Memory, 256 GB Virtual Memory, and 4 KB Page Size is

Selected Answer: c. 26 bits

Answers:
a. 24 bits

b. 28 bits

c. 26 bits

d. 38 bits

Response Feedback: The number of bits representing the Virtual Page Number in a virtual memory system with 8 GB Physical Memory, 256 GB Virtual Memory, and 4 KB Page Size is calculated as follows:

256GB of Virtual memory translates to $\log_2 256*2^{30}$ bits = 38 bits of Virtual Address. Of this, the page (frame) offset is 12 bits since page (frame) size is 4KB. Therefore the Virtual Page Number is 38-12 = 26 bits.

Question 5

1 out of 1 points

In a virtual memory system, each process must have its own page table.

Selected Answer: True

Answers: True

False

Monday, May 3, 2021 12:12:51 PM CDT

← OK

Review Test Submission: Q23

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q23
Started	4/13/21 10:31 AM
Submitted	4/13/21 10:36 AM
Due Date	4/13/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	4 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

Cache memory addresses the central issue of performance-capacity gap in the memory hierarchy that exists between the fast CPU and its limited register space on one side and the slower but larger memory on the other side.

Selected Answer: True

Answers: True

False

Response Feedback: For detailed guidance, please look at introductory notes in N23 and also narration in V23 part1

Question 2

1 out of 1 points

In a set associative cache memory, if the number of ways (lines) in a set is doubled while keeping the cache size and line size unchanged, the number of set index bits

Selected Answer: a. Reduces by 1

Answers: a. Reduces by 1

b. Halves

c. Doubles

d. Increases by 1

Response Feedback: In a set associative cache memory, if the number of ways (lines) in a set is doubled while keeping the cache size and line size unchanged, the number of set index bits will reduce by 1 because the number of sets is cut in half.

Question 3

1 out of 1 points

The principle of spatial locality suggests that a memory location accessed at time t has a high probability of being accessed soon again

Selected Answer: False

Answers: True
False

Response Feedback: The principle of spatial locality suggests that a memory location accessed at time t implies that its neighboring address also have a high probability of being accessed in the future.

Question 4

1 out of 1 points

Which of these trade-offs occur in a memory hierarchy?

Selected Answer: b. Faster access means smaller memory size

Answers: a. Longer addresses mean smaller memory size
b. Faster access means smaller memory size
c. Longer addresses mean faster access
d. Closer to CPU means larger memory size

Question 5

1 out of 1 points

For a given size of a cache memory, a fully associative implementation is likely to result in a better hit rate than a direct mapped implementation

Selected Answer: True

Answers: True
False

Response Feedback: A direct mapped memory is extremely restrictive with only one mapping for a given cache line. Since caches are much smaller size than memory, the likelihood of a line being hit multiple times is high. In fully associative case, some of these conflicts could be resolved by a block getting mapped to a different line and therefore a better hit rate for future accesses based on temporal locality.

Monday, May 3, 2021 12:21:45 PM CDT

← OK

Review Test Submission: Q24

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q24
Started	4/15/21 11:09 PM
Submitted	4/15/21 11:11 PM
Due Date	4/15/21 11:59 PM
Status	Completed
Attempt Score	5 out of 5 points
Time Elapsed	1 minute
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

1 out of 1 points

A write-allocate policy during cache write miss requires the “missed” block to also be placed as a line in the cache

Selected Answer: True

Answers: True
False

Response Feedback: This is done with the intent to take advantage of temporal locality and the expectation that the written line will likely be read or written in the near future.

Question 2

1 out of 1 points

The bit width of the LRU counter for a 32 KB 16-way set associative cache with 32 Byte line size is

Selected Answer: a. 4 bits

Answers: a. 4 bits
b. 5 bits
c. 10 bits
d. 6 bits

Response The cache is set associative with 16 ways per set. We will therefore need 4 bits to

Feedback: uniquely keep the LRU count of each of the 16 ways of any given set.

Question 3

1 out of 1 points

The reason we do not need an eviction policy for Direct Mapped Cache is because there is only one candidate line for eviction.

Selected Answer: True
Answers: True
False

Response Feedback: By comparison, set associative or fully associative caches offer choice among the many ways in the indexed set as potential eviction candidates.

Question 4

1 out of 1 points

READ miss handling is easier in Write Through Caches because we do not need to worry about writing the 'dirty' evicted line in the main memory.

Selected Answer: True
Answers: True
False

Response Feedback: Write through ensures that main memory always remains consistent with cache memory. So lines that were written can simply be evicted from the cache without being copied to the main memory at eviction.

Question 5

1 out of 1 points

LRU Policy is more likely to return better Hit Rate compared to FIFO (First In First Out) for cache access patterns where the oldest line may also be the most frequently used line in the cache.

Selected Answer: True
Answers: True
False

Response Feedback: The problem statement captures the justification correctly. Example: Imagine a loop that executes x=x+a[i] for increasing i. Once the cache gets full with array elements, a FIFO would end up removing x from the cache to make room for a new a[i] even though x was being accessed repeatedly.

Monday, May 3, 2021 12:31:44 PM CDT

← OK

Review Test Submission: Q25

User	Mualla Argin
Course	21 SPRING CSCE 312 200,500-503,506-513: CSCE 312 SP 2021
Test	Q25
Started	5/3/21 12:35 PM LATE
Submitted	5/3/21 12:41 PM LATE
Due Date	4/22/21 11:59 PM
Status	Needs Grading
Attempt Score	0 out of 5 points
Time Elapsed	5 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

0 out of 1 points

In a 5-stage pipeline, where 2 stages are 150 ps each and 3 stages are 200 ps each, the frequency of the pipeline is 5Ghz.

Note that ps is 10^{-12} seconds

Selected Answer: ✗ False

Answers: ✓ True

False

Response Feedback: In a 5-stage pipeline, where 2 stages are 150 ps each and 3 stages are 200 ps each, the frequency of the pipeline is set by the stage delay of the slowest stage, which in this case is 200ps. The frequency corresponding to this stage delay is 1/200ps = 5Ghz.

Question 2

0 out of 1 points

In a 5-stage pipeline, where 2 stages are 150 ps each and 3 stages are 200 ps each, what is the latency of

instruction execution in pipelined execution with no data or control hazards? Note that the slowest stage determines the frequency of the pipeline.

Selected Answer: ✗ 900 ps

Answers: 750ps

900 ps

✓ 1000 ps

600 ps

Response Feedback: The slowest stage sets the stage delay of the pipeline. Therefore the total latency for an instruction in our 5-stage pipeline is 200 * 5 = 1000 ps.

Question 3

0 out of 1 points

Say an operation takes total 10 units of time and I decide to pipeline the operation by subdividing it into 10 stages. The ideal throughput of the pipelined operation would now be

Selected Answer: ✗ c. 1 completed operation every 5 units of time

Answers: a. 1 completed operation every 10 units of time

✓ b. 1 completed operation every 1 units of time

c. 1 completed operation every 5 units of time

d. None of the above answers are correct

Response Feedback: We now have 10 stages that allow us to have up to 10 sub-stages of the operation be engaged in parallel resulting in idealized throughput of 1 operation completed every unit of time

Question 4

1 out of 1 points

Deep pipelines are typically discouraged because they involve high branch (control) hazard penalties.

Selected Answer: True
Answers: True
False

Response Feedback: The deeper the pipeline, the more the number of instructions that have entered the pipeline when flush is called. This affects pipeline performance adversely. As a remedy, branch prediction has become an advanced science that allows bet to be made whether the branch will be taken or not resulting in fetching the instruction at the target address as soon as the branch instruction is decoded.

Question 5

0 out of 1 points

In CPU pipelined execution, data dependency hazards result in flushes and control hazards result in stalls.

Selected Answer: True
Answers: True
False

Response Feedback: The answer is just the opposite. Data dependency hazards result in pipeline stalls so that the dependent instruction may wait for its source data to become available. Control hazards pertain to branch (conditional or unconditional) instructions and they would require the pipeline to be flushed to get rid of instructions that were already in the pipeline once it was known which instruction to be fetched next in the pipeline.

Monday, May 3, 2021 12:41:31 PM CDT

← OK