CLP2_TESTING [CPU 1214C DC/DC/DC]

CLP2_TESTING			
General\Project information			
Name	CLP2_TESTING	**Author**	LAI-09
Comment		**Slot**	1
Rack	0		
General\Catalog information			
Short designation	CPU 1214C DC/DC/DC	**Description**	Work memory 100 KB; 24VDC power supply with DI14 x 24VDC SINK/ SOURCE, DQ10 x 24VDC and AI2 on board; 6 high-speed counters and 4 pulse outputs on board; signal board expands on-board I/O; up to 3 communication modules for serial communication; up to 8 signal modules for I/O expansion; 0.04 ms/1000 instructions; PROFINET interface for programming, HMI and PLC to PLC communication
Article number	6ES7 214-1AG40-0XB0	**Firmware version**	V4.2
General\Identification & Maintenance			
Plant designation		**Location identifier**	
Installation date	2023-05-04 14:13:24.297	**Additional information**	
General\Checksums			
Text lists	FA 70 E8 75 1D 5A 8E 29	**Software**	C3 C0 4A 97 11 DC B8 5E
PROFINET interface [X1]\General			
Name	PROFINET interface_1	**Author**	LAI-09
Comment			
PROFINET interface [X1]\General\Project information			
Name	DI 14/DQ 10_1	**Comment**	
Name	AI 2_1	**Comment**	
Name	AQ 1x12BIT_1	**Comment**	
PROFINET interface [X1]\General\Catalog information			
Short designation	AQ1 Signal board	**Description**	Signal board AQ1 x 12 bits; plug-in terminal blocks; output: +/-10V and 0 to 20 mA; configurable diagnostics; configurable substitute output value
Article number	6ES7 232-4HA30-0XB0	**Firmware version**	V1.0
PROFINET interface [X1]\Ethernet addresses\Interface networked with			
Subnet:	Not connected		
PROFINET interface [X1]\Ethernet addresses\IP protocol			
IP configuration	Set IP address in the project	**IP address:**	150.162.14.24
Subnet mask:	255.255.0.0	**Use router**	False
PROFINET interface [X1]\Ethernet addresses\PROFINET			
PROFINET device name is set directly at the device	False	**Generate PROFINET device name automatically**	True
PROFINET device name:	clp2_testing	**Converted name:**	clp2xbtestingab04
Device number:	0		
PROFINET interface [X1]\Time synchronization			
Enable time synchronization via NTP server	Enable time synchronization via NTP server		IP addresses
Server 1	0.0.0.0	**Server 2**	0.0.0.0
Server 3	0.0.0.0	**Server 4**	0.0.0.0
Update interval	10sec	**Empty**	

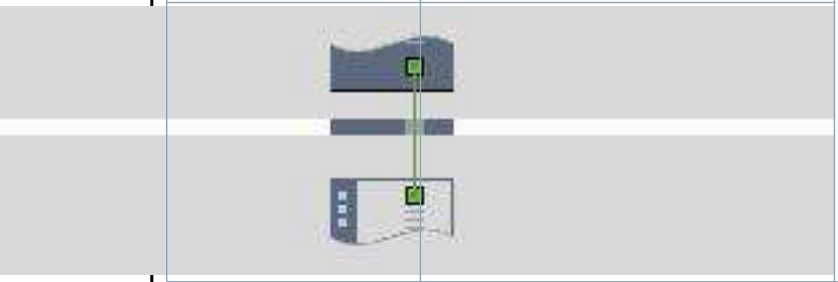
CPU synchronizes the modules of the device.	No synchronization		
PROFINET interface [X1]\Digital inputs\Channel0			
Channel address	I0.0	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel0			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49152
Event name:	0	**Hardware interrupt:**	0
Rising edge0	Rising edge0		
PROFINET interface [X1]\Digital inputs\Channel0			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49280
Event name:	0	**Hardware interrupt:**	0
Falling edge0	Falling edge0		
PROFINET interface [X1]\Digital inputs\Channel1			
Channel address	I0.1	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel1			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49153
Event name:	0	**Hardware interrupt:**	0
Rising edge1	Rising edge1		
PROFINET interface [X1]\Digital inputs\Channel1			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49281
Event name:	0	**Hardware interrupt:**	0
Falling edge1	Falling edge1		
PROFINET interface [X1]\Digital inputs\Channel2			
Channel address	I0.2	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel2			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49154
Event name:	0	**Hardware interrupt:**	0
Rising edge2	Rising edge2		
PROFINET interface [X1]\Digital inputs\Channel2			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49282
Event name:	0	**Hardware interrupt:**	0
Falling edge2	Falling edge2		
PROFINET interface [X1]\Digital inputs\Channel3			
Channel address	I0.3	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel3			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49155
Event name:	0	**Hardware interrupt:**	0
Rising edge3	Rising edge3		
PROFINET interface [X1]\Digital inputs\Channel3			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49283
Event name:	0	**Hardware interrupt:**	0
Falling edge3	Falling edge3		
PROFINET interface [X1]\Digital inputs\Channel4			
Channel address	I0.4	**Input filters**	6.4 millisec
Enable pulse catch	0		

PROFINET interface [X1]\Digital inputs\Channel4			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49156
Event name:	0	**Hardware interrupt:**	0
Rising edge4	Rising edge4		
PROFINET interface [X1]\Digital inputs\Channel4			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49284
Event name:	0	**Hardware interrupt:**	0
Falling edge4	Falling edge4		
PROFINET interface [X1]\Digital inputs\Channel5			
Channel address	I0.5	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel5			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49157
Event name:	0	**Hardware interrupt:**	0
Rising edge5	Rising edge5		
PROFINET interface [X1]\Digital inputs\Channel5			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49285
Event name:	0	**Hardware interrupt:**	0
Falling edge5	Falling edge5		
PROFINET interface [X1]\Digital inputs\Channel6			
Channel address	I0.6	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel6			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49158
Event name:	0	**Hardware interrupt:**	0
Rising edge6	Rising edge6		
PROFINET interface [X1]\Digital inputs\Channel6			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49286
Event name:	0	**Hardware interrupt:**	0
Falling edge6	Falling edge6		
PROFINET interface [X1]\Digital inputs\Channel7			
Channel address	I0.7	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel7			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49159
Event name:	0	**Hardware interrupt:**	0
Rising edge7	Rising edge7		
PROFINET interface [X1]\Digital inputs\Channel7			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49287
Event name:	0	**Hardware interrupt:**	0
Falling edge7	Falling edge7		
PROFINET interface [X1]\Digital inputs\Channel8			
Channel address	I1.0	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel8			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49160
Event name:	0	**Hardware interrupt:**	0
Rising edge8	Rising edge8		

PROFINET interface [X1]\Digital inputs\Channel8			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49288
Event name:	0	**Hardware interrupt:**	0
Falling edge8	Falling edge8		
PROFINET interface [X1]\Digital inputs\Channel9			
Channel address	I1.1	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel9			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49161
Event name:	0	**Hardware interrupt:**	0
Rising edge9	Rising edge9		
PROFINET interface [X1]\Digital inputs\Channel9			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49289
Event name:	0	**Hardware interrupt:**	0
Falling edge9	Falling edge9		
PROFINET interface [X1]\Digital inputs\Channel10			
Channel address	I1.2	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel10			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49162
Event name:	0	**Hardware interrupt:**	0
Rising edge10	Rising edge10		
PROFINET interface [X1]\Digital inputs\Channel10			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49290
Event name:	0	**Hardware interrupt:**	0
Falling edge10	Falling edge10		
PROFINET interface [X1]\Digital inputs\Channel11			
Channel address	I1.3	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel11			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49163
Event name:	0	**Hardware interrupt:**	0
Rising edge11	Rising edge11		
PROFINET interface [X1]\Digital inputs\Channel11			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49291
Event name:	0	**Hardware interrupt:**	0
Falling edge11	Falling edge11		
PROFINET interface [X1]\Digital inputs\Channel12			
Channel address	I1.4	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel13			
Channel address	I1.5	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Analog inputs\Noise reduction			
Integration time	50 Hz (20 ms)		
PROFINET interface [X1]\Analog inputs\Channel0			
Channel address	IW64	**Measurement type**	Voltage
Voltage range	0..10 V	**Smoothing**	Weak (4 cycles)
Empty		**Enable overflow diagnostics**	1
PROFINET interface [X1]\Analog inputs\Channel1			
Channel address	IW66	**Measurement type**	Voltage

Voltage range	0..10 V	**Smoothing**	Weak (4 cycles)
Empty		**Enable overflow diagnostics**	1
PROFINET interface [X1]\Digital outputs			
Reaction to CPU STOP	Use substitute value		
PROFINET interface [X1]\Digital outputs\Channel0			
Channel address	Q0.0	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel1			
Channel address	Q0.1	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel2			
Channel address	Q0.2	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel3			
Channel address	Q0.3	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel4			
Channel address	Q0.4	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel5			
Channel address	Q0.5	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel6			
Channel address	Q0.6	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel7			
Channel address	Q0.7	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel8			
Channel address	Q1.0	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel9			
Channel address	Q1.1	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Operating mode			
IO controller	True	**IO system**	
Device number	0	**IO device**	False
PROFINET interface [X1]\Analog outputs			
Reaction to CPU STOP	Use substitute value		
PROFINET interface [X1]\Analog outputs\Channel0			
Channel address	QW80	**Analog output type**	Voltage
Voltage range	+/- 10 V	**Substitute value for channel on a change from RUN to STOP**	0.000V
Empty		**Enable short circuit diagnostics**	1
Enable overflow diagnostics	1	**Enable underflow diagnostics**	1
PROFINET interface [X1]\I/O addresses\Input addresses			
Start address	0.0	**End address**	1.7

Organization block	0	**Process image**	0
PROFINET interface [X1]\I/O addresses\Input addresses			
Start address	64	**End address**	67
Organization block	0	**Process image**	0
PROFINET interface [X1]\I/O addresses\Output addresses			
Start address	0.0	**End address**	1.7
Organization block	0	**Process image**	0
PROFINET interface [X1]\I/O addresses\Output addresses			
Start address	80	**End address**	81
Organization block	0	**Process image**	0
PROFINET interface [X1]\Advanced options\Interface options			
Support device replacement without exchangeable medium	True	**Permit overwriting of device names of all assigned IO devices**	False
Use IEC V2.2 LLDP mode	False	**Keep-Alive connection monitoring:**	30s
PROFINET interface [X1]\Advanced options\Real time settings\IO communication			
Send clock:	1.000ms		
PROFINET interface [X1]\Advanced options\Real time settings\Real time options			
Calculated bandwidth for cyclic IO data:	0.000ms	**Calculated bandwidth for cyclic IO data:**	0.000%
PROFINET interface [X1]\Advanced options\Port [X1 P1]\General			
Name	Port_1	**Author**	LAI-09
Comment			
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port interconnection\Local port:			
Local port:	CLP2_TESTING\PROFINET interface_1 [X1]\Port_1 [X1 P1 R]	**Medium:**	Copper
Cable name:	---		



PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port interconnection\Partner port:			
	Monitoring of partner port is not possible	**Partner port:**	Any partner
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Activate			
Activate this port for use	True		
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Connection			
Transmission rate / duplex:	Automatic	**Monitor**	False
Enable autonegotiation	True		
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Boundaries			
End of detection of accessible devices	False	**End of topology discovery**	False
End of the sync domain	False		
PROFINET interface [X1]\Web server access			
Enable Web server using this interface	False	**The Web server must also be activated in the properties of the PLC.**	

High speed counters (HSC)\HSC1\General\Enable			
Enable this high speed counter	0	**Enable this high speed counter**	0
Enable this high speed counter	0	**Enable this high speed counter**	0
Enable this high speed counter	0	**Enable this high speed counter**	0
High speed counters (HSC)\HSC1\General\Project information			
Name	HSC_1	**Comment**	
Name	HSC_2	**Comment**	
Name	HSC_3	**Comment**	
Name	HSC_4	**Comment**	
Name	HSC_5	**Comment**	
Name	HSC_6	**Comment**	
High speed counters (HSC)\HSC1\I/O addresses\Input addresses			
Start address	1000.0	**End address**	1003.7
Start address	1004.0	**End address**	1007.7
Organization block	0	**Start address**	1008.0
End address	1011.7	**Organization block**	0
Process image	0	**Start address**	1012.0
End address	1015.7	**Organization block**	0
Process image	0	**Start address**	1016.0
End address	1019.7	**Organization block**	0
Process image	0	**Start address**	1020.0
End address	1023.7	**Organization block**	0
Process image	0	**Organization block**	0
Process image	0	**Process image**	0
Pulse generators (PTO/PWM)\PTO1/PWM1\General\Enable			
Enable this pulse generator	0	**Enable this pulse generator**	0
Pulse generators (PTO/PWM)\PTO1/PWM1\General\Project information			
Name	Pulse_1	**Comment**	
Name	Pulse_2	**Comment**	
Pulse generators (PTO/PWM)\PTO1/PWM1\I/O addresses\Output addresses			
Start address	1000.0	**End address**	1001.7
Start address	1002.0	**End address**	1003.7
Organization block	0	**Organization block**	0
Process image	0	**Process image**	0
Startup			
Startup after POWER ON	Warm restart - mode before POWER OFF	**Comparison preset to actual configuration**	Startup CPU even if mismatch
Configuration time	60000ms	**OBs should be interruptible**	1
Cycle			
Cycle monitoring time	150ms		
Enable minimum cycle time for cyclic OBs	0	**Minimum cycle time**	1ms
Communication load			
Cycle load due to communication	20%		
System and clock memory\System memory bits			
Enable the use of system memory byte	0	**Address of system memory byte (MBx)**	1
First cycle		**Diagnostic status changed**	
Always 1 (high)		**Always 0 (low)**	
System and clock memory\Clock memory bits			
Enable the use of clock memory byte	0	**Address of clock memory byte (MBx)**	0

10 Hz clock		**5 Hz clock**	
2.5 Hz clock		**2 Hz clock**	
1.25 Hz clock		**1 Hz clock**	
0.625 Hz clock		**0.5 Hz clock**	
Web server\General			
Activate Web server on all modules of this device	False	**Permit access only with HTTPS**	True
Web server\Automatic update			
Enable automatic update	True	**Update interval**	0s

Web server\User interface languages

Assign project language	User interface languages
English (United States)	German
English (United States)	English
English (United States)	French
English (United States)	Spanish
English (United States)	Italian
English (United States)	Chinese (simplified)

Web server\User management

User name	User rights
Everybody	

Web server\User-defined web pages

Application name	HTML source path	Default HTML page	Files with dynamic content	Web DB number	Fragment DB number
		index.htm	.htm;.html	333	334

Web server\Overview of interfaces

Device	Interface	Enabled web server access
CLP2_TESTING	PROFINET interface_1	False

User interface languages

Assign project language	User interface languages
English (United States)	German
English (United States)	English
English (United States)	French
English (United States)	Spanish
English (United States)	Italian
English (United States)	Chinese (simplified)

Time of day\Local time			
Time zone	(UTC +01:00) Berlin, Bern, Brussels, Rome, Stockholm, Vienna		
Time of day\Daylight saving time			
Activate daylight saving time	1	**Difference between standard and daylight saving time**	60mins
Time of day\Daylight saving time\Start of daylight saving time			
Starting week of the month:	Last		Sunday
of	March	**at**	01:00 a.m.
Time of day\Daylight saving time\Start of standard time			
	Last		Sunday
of	October	**at**	02:00 a.m.
Protection & Security			
Level of protection	No protection		
Protection & Security\Connection mechanisms			
Permit access with PUT/GET communication from remote partner	False		

Protection & Security\Security event			
Summarize security events in case of high message volume	True	**Length of an interval**	20
Unit	seconds		

Protection & Security\External load memory	
Disable copying from internal load memory to external load memory	False

Configuration control\Configuration control for central configuration	
Allow to reconfigure the device via the user program	0

Connection resources

	Station resources - Reserved - Maximum	Station resources - Reserved - Configured	Station resources - Dynamic - Configured	Module resources - CLP2_TESTING [CPU 1214C DC/DC/DC] - Configured
Maximum number of resources:		62	6	68
	Maximum	Configured	Configured	Configured
PG communication:	4	-	-	-
HMI communication:	12	0	0	0
S7 communication:	8	0	0	0
Open user communication:	8	0	0	0
Web communication:	30	-	-	-
Other communication:	-	-	0	0
Total resources used:		0	0	0
Available resources:		62	6	68

Overview of addresses\Overview of addresses\Overview of addresses			
Inputs	True	**Outputs**	True
Address gaps	False	**Slot**	True

Type	Addr. from	Addr. to	Module	PIP	Device name	Device number	Size	Master / IO system	Rack	Slot
I	0	1	DI 14/DQ 10_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 1
O	0	1	DI 14/DQ 10_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 1
I	64	67	AI 2_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 2
I	1000	1003	HSC_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 16
I	1004	1007	HSC_2	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 17
I	1008	1011	HSC_3	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 18
I	1012	1015	HSC_4	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 19
I	1016	1019	HSC_5	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 20
I	1020	1023	HSC_6	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 21
O	1000	1001	Pulse_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 32
O	1002	1003	Pulse_2	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 33
O	1004	1005	Pulse_3	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 34
O	1006	1007	Pulse_4	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 35
O	80	81	AQ 1x12BIT_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 3
I	8	8	DI 8/DQ 8x24VDC_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	1 Bytes	-	0	2

Type	Addr. from	Addr. to	Module	PIP	Device name	Device number	Size	Master / IO system	Rack	Slot
O	8	8	DI 8/DQ 8x24VDC_ 1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	1 Bytes	-	0	2

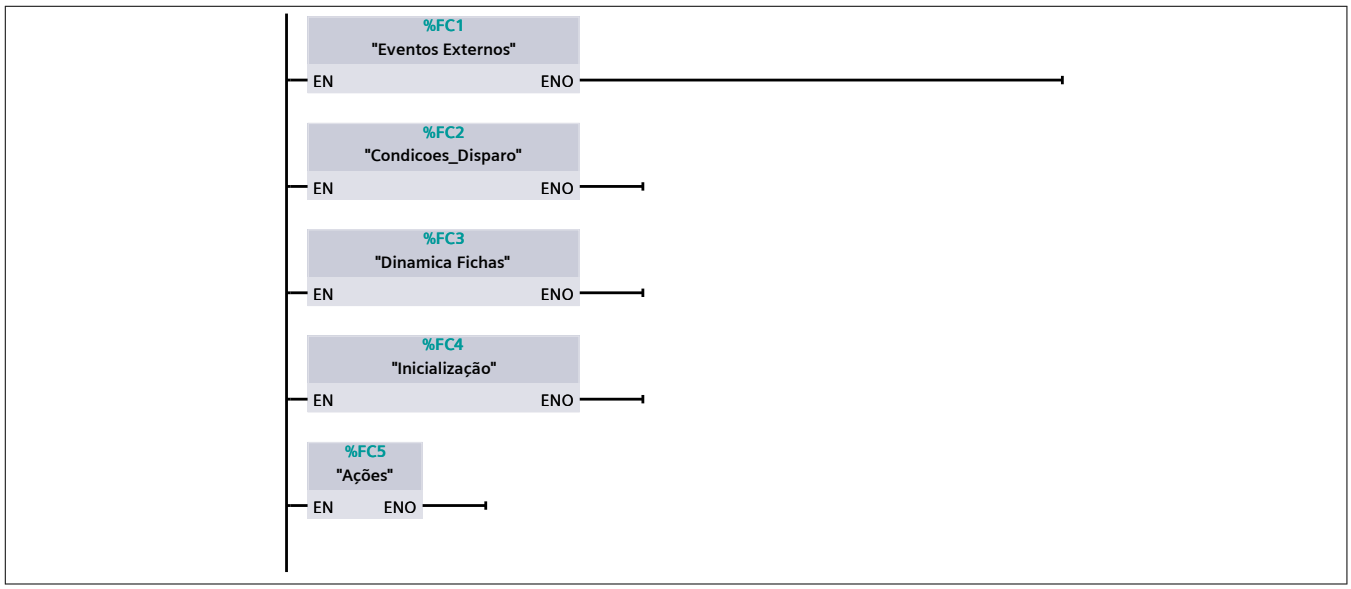
CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks

Main [OB1]

Main Properties					
General					
Name	Main	**Number**	1	**Type**	OB
Language	LAD	**Numbering**	Automatic		
Information					
Title	"Main Program Sweep (Cycle)"	**Author**		**Comment**	
Family		**Version**	0.1	**User-defined ID**	

Name	Data type	Default value	Comment
▼ Input			
Initial_Call	Bool		Initial call of this OB
Remanence	Bool		=True, if remanent data are available
Temp			
Constant			

Network 1:



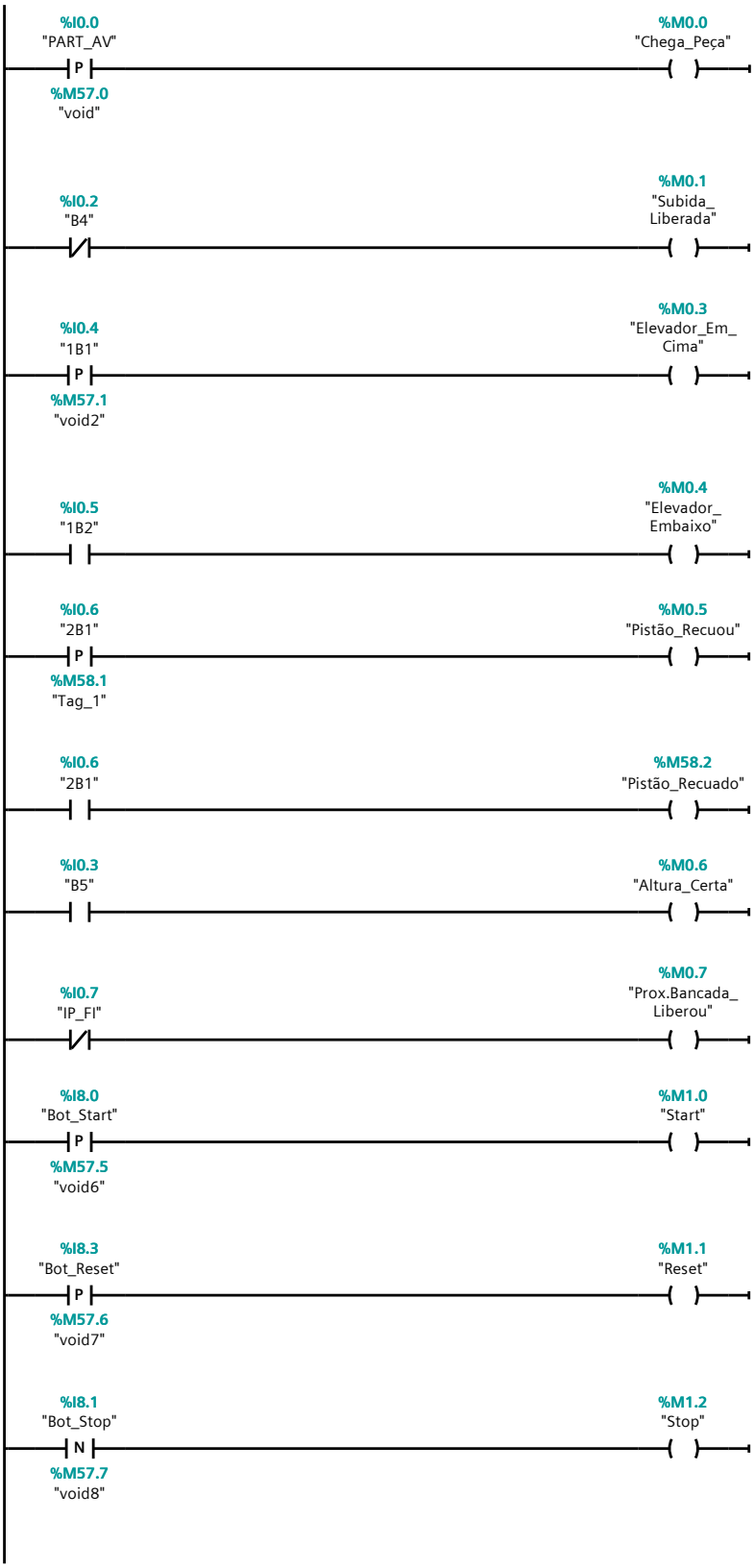
CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks

Eventos Externos [FC1]

Eventos Externos Properties					
General					
Name	Eventos Externos	**Number**	1	**Type**	FC
Language	LAD	**Numbering**	Automatic		
Information					
Title		**Author**		**Comment**	
Family		**Version**	0.1	**User-defined ID**	

Name	Data type	Default value	Comment
Input			
Output			
InOut			
Temp			
Constant			
▼ Return			
Eventos Externos	Void		

Network 1:


%I0.0
"PART_AV"
P
%M57.0
"void"
%M0.0
"Chega_Peça"
%I0.2
"B4"
%M0.1
"Subida_
Liberada"
%I0.4
"1B1"
P
%M57.1
"void2"
%M0.3
"Elevador_Em_
Cima"
%I0.5
"1B2"
%M0.4
"Elevador_
Embaixo"
%I0.6
"2B1"
P
%M58.1
"Tag_1"
%M0.5
"Pistão_Recuou"
%I0.6
"2B1"
%M58.2
"Pistão_Recuado"
%I0.3
"B5"
%M0.6
"Altura_Certa"
%I0.7
"IP_FI"
%M0.7
"Prox.Bancada_
Liberou"
%I8.0
"Bot_Start"
P
%M57.5
"void6"
%M1.0
"Start"
%I8.3
"Bot_Reset"
P
%M57.6
"void7"
%M1.1
"Reset"
%I8.1
"Bot_Stop"
N
%M57.7
"void8"
%M1.2
"Stop"

CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks

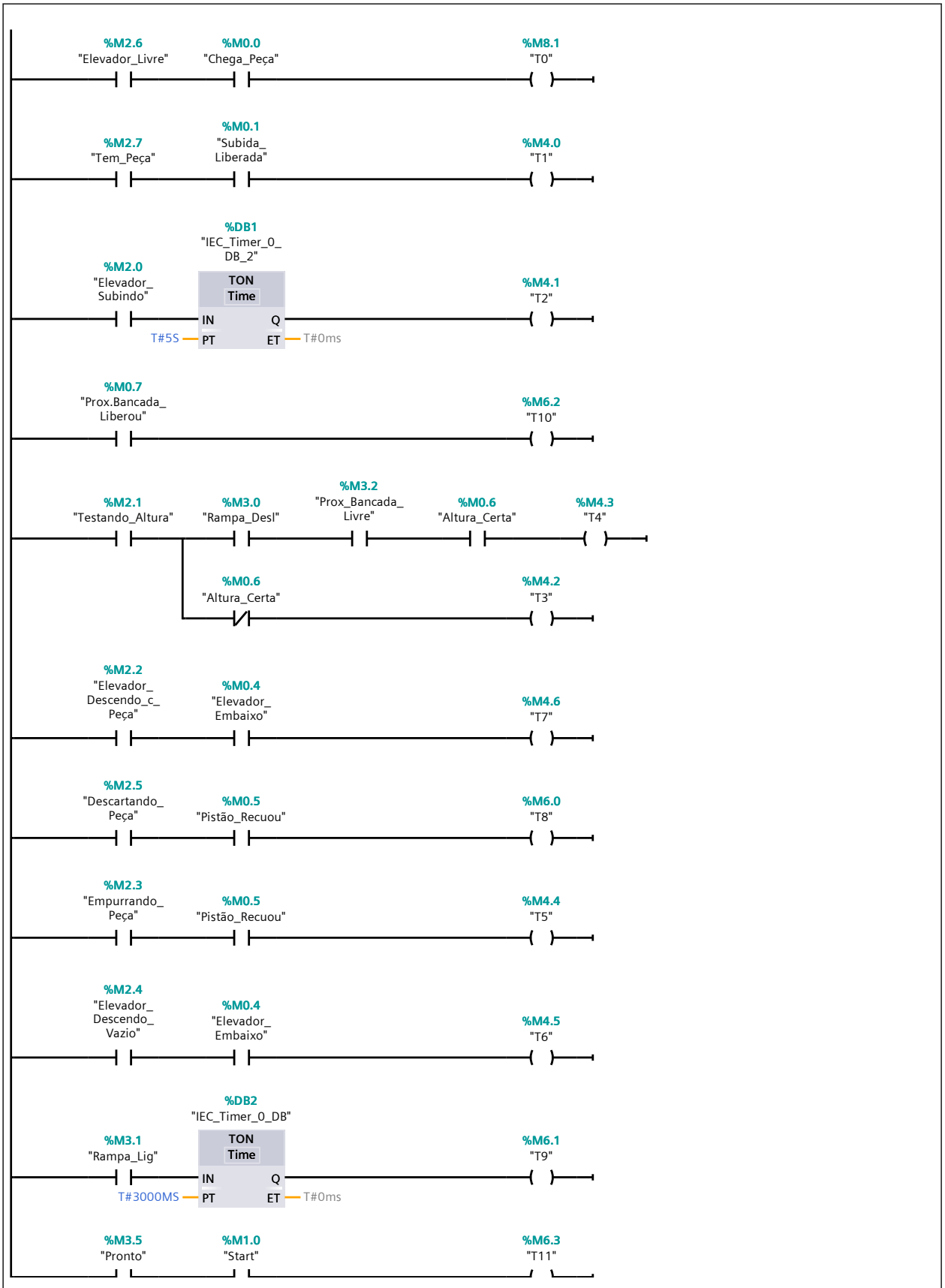
Condicoes_Disparo [FC2]

Condicoes_Disparo Properties					
General					
Name	Condicoes_Disparo	**Number**	2	**Type**	FC
Language	LAD	**Numbering**	Automatic		
Information					
Title		**Author**		**Comment**	
Family		**Version**	0.1	**User-defined ID**	

Name	Data type	Default value	Comment
Input			
Output			
InOut			
Temp			
Constant			
▼ Return			
Condicoes_Disparo	Void		

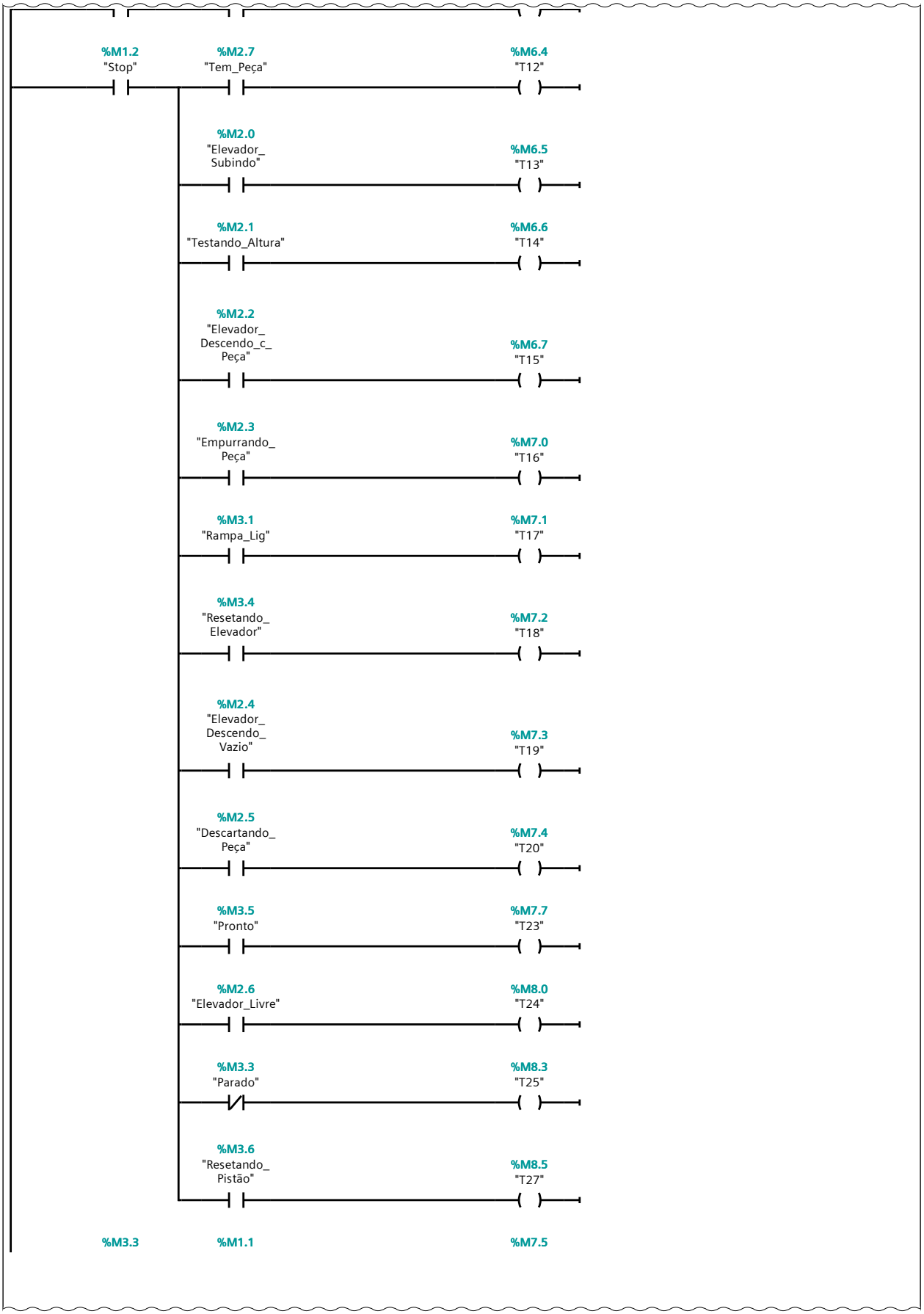
Network 1:

Network 1: (1.1 / 3.1)



Network 1: (2.1 / 3.1)

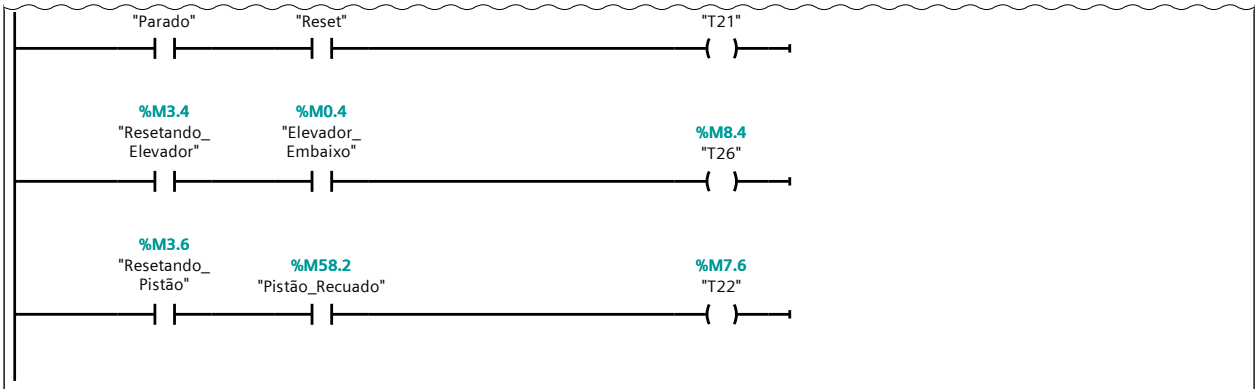
1.1 (Page4 - 2)



3.1 (Page4 - 4)

Network 1: (3.1 / 3.1)

2.1 (Page4 - 3)



CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks

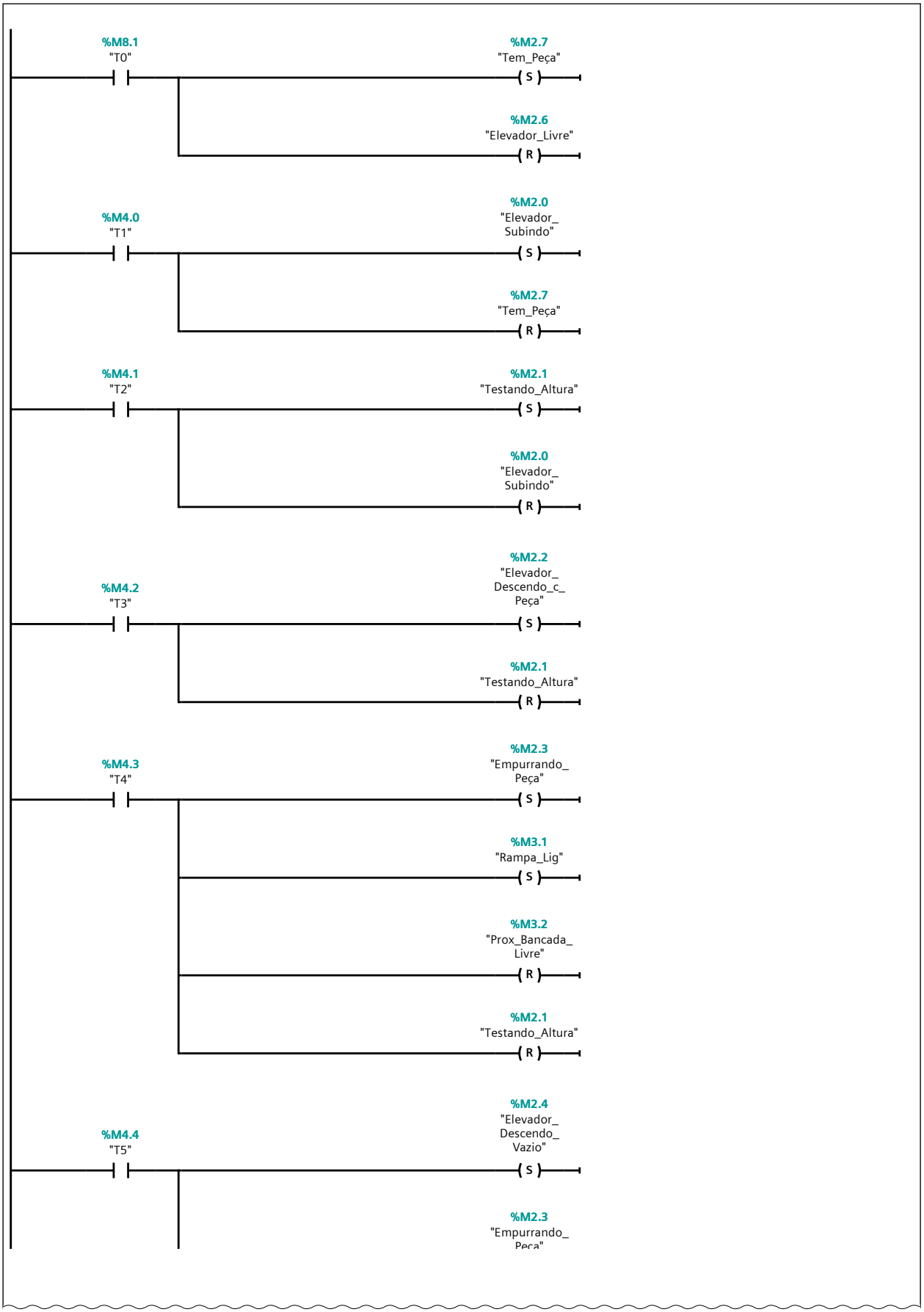
Dinamica Fichas [FC3]

Dinamica Fichas Properties					
General					
Name	Dinamica Fichas	**Number**	3	**Type**	FC
Language	LAD	**Numbering**	Automatic		
Information					
Title		**Author**		**Comment**	
Family		**Version**	0.1	**User-defined ID**	

Name	Data type	Default value	Comment
Input			
Output			
InOut			
Temp			
Constant			
▼ Return			
Dinamica Fichas	Void		

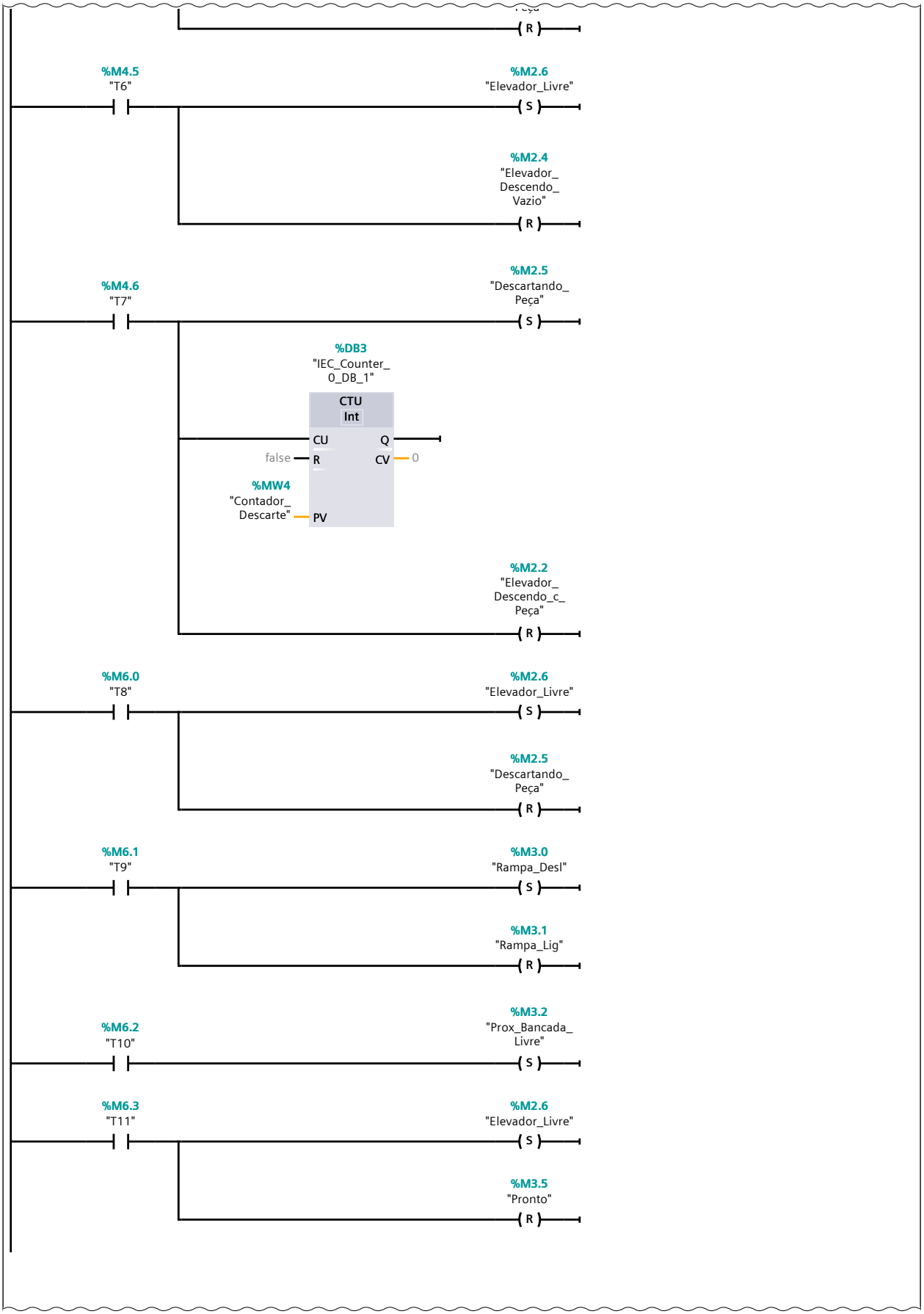
Network 1:

Network 1: (1.1 / 4.1)



Network 1: (2.1 / 4.1)

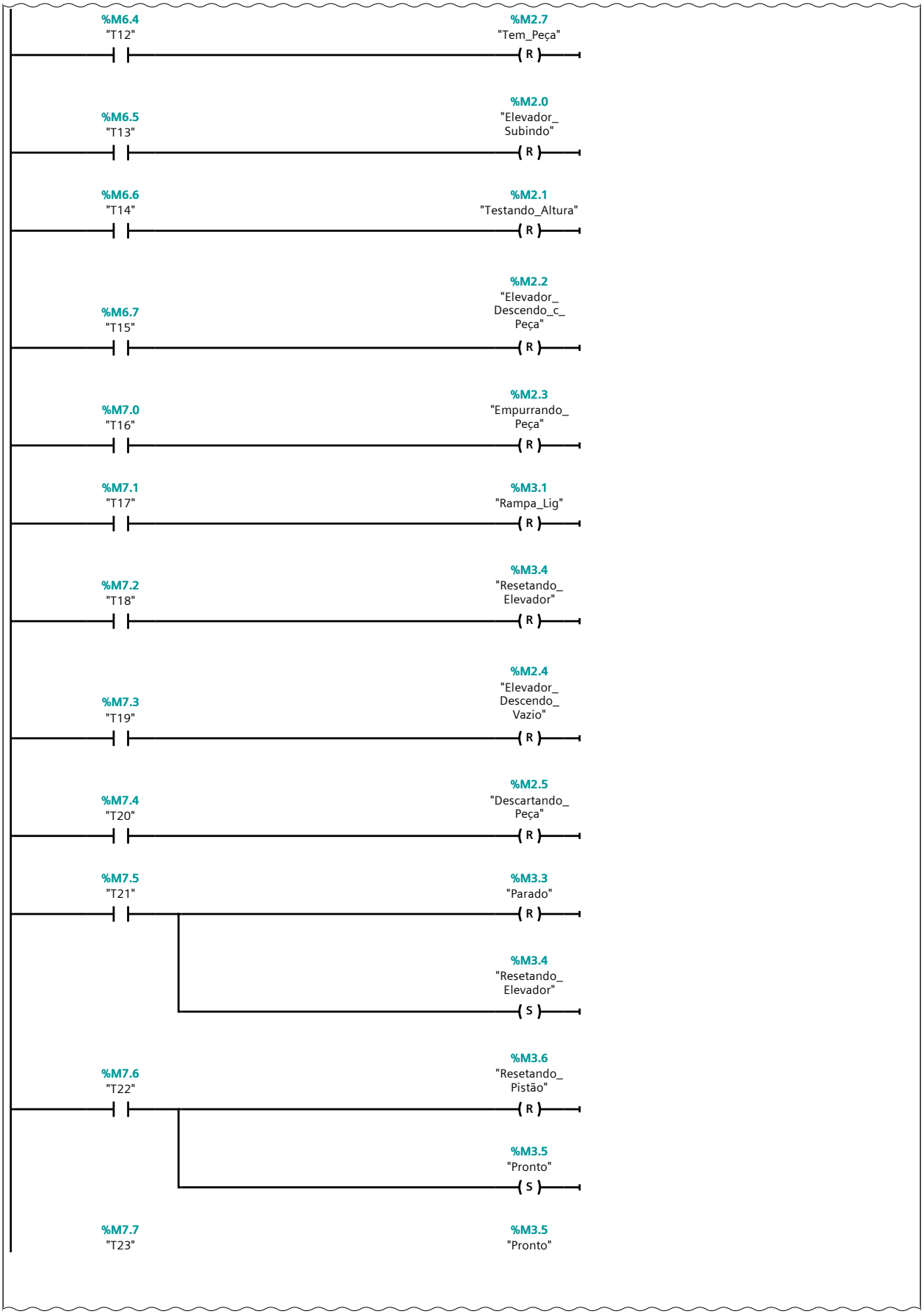
1.1 (Page5 - 2)



3.1 (Page5 - 4)

Network 1: (3.1 / 4.1)

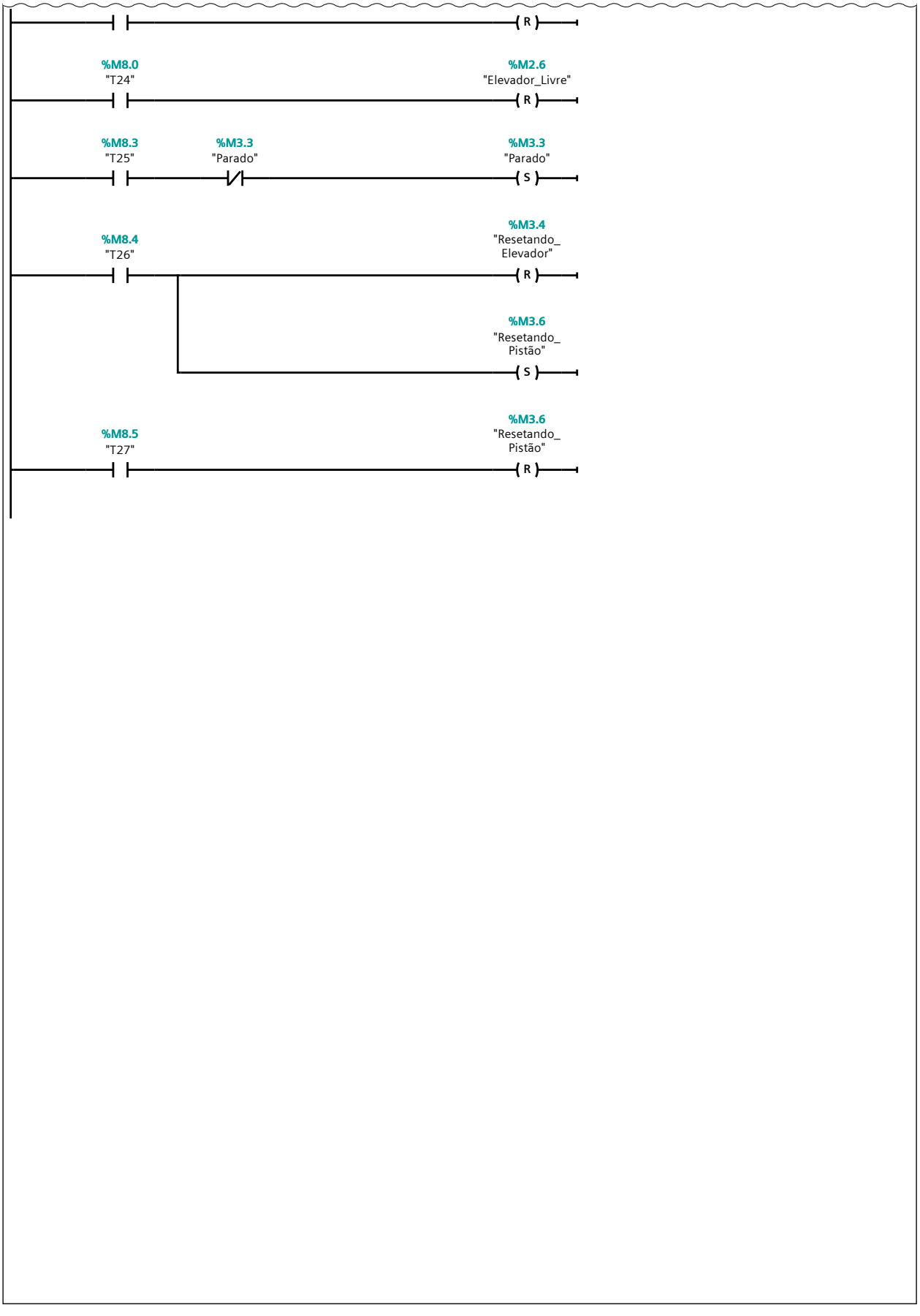
2.1 (Page5 - 3)



4.1 (Page5 - 5)

Network 1: (4.1 / 4.1)

3.1 (Page5 - 4)



CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks

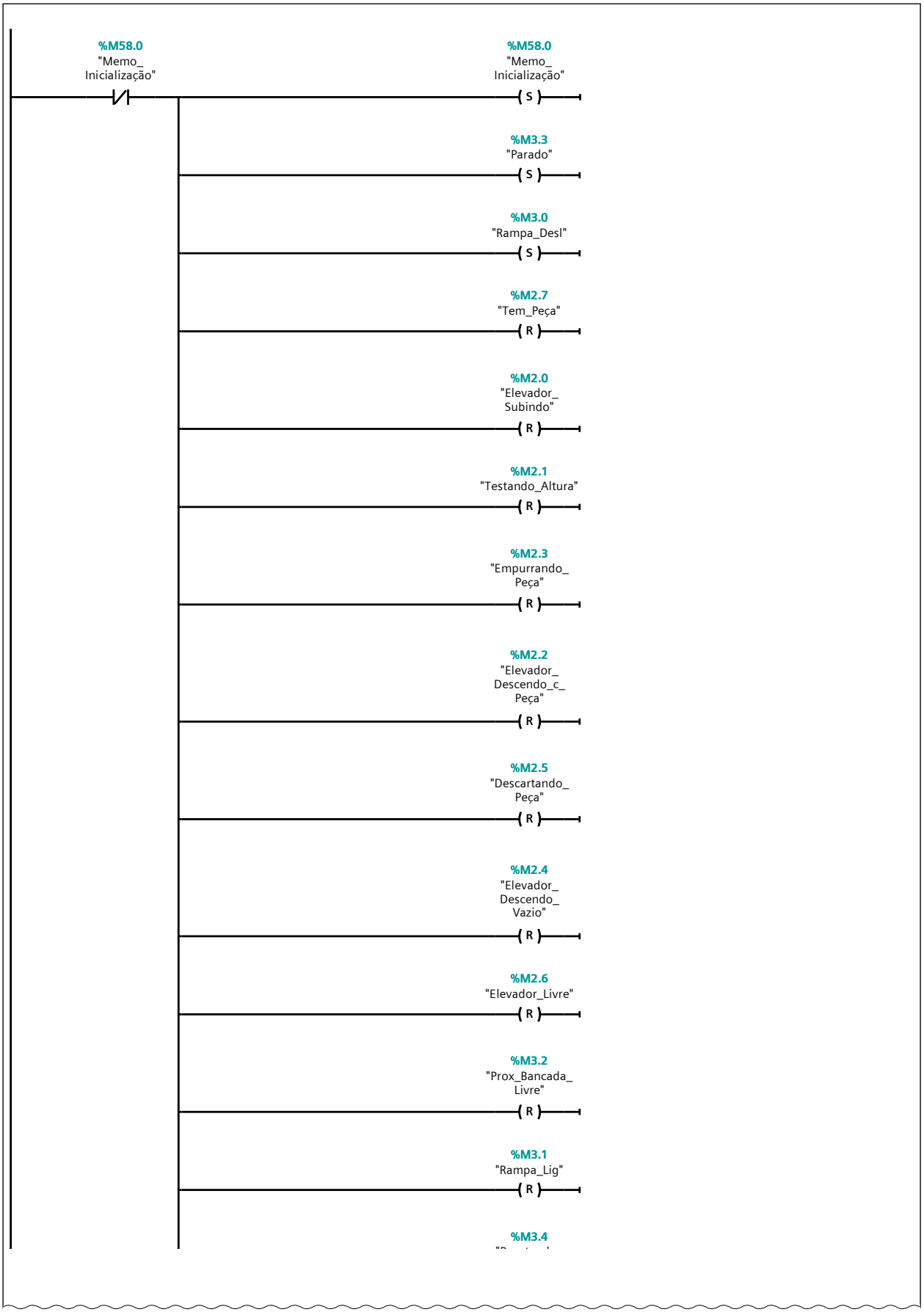
Inicialização [FC4]

Inicialização Properties					
General					
Name	Inicialização	**Number**	4	**Type**	FC
Language	LAD	**Numbering**	Automatic		
Information					
Title		**Author**		**Comment**	
Family		**Version**	0.1	**User-defined ID**	

Name	Data type	Default value	Comment
Input			
Output			
InOut			
Temp			
Constant			
▼ Return			
Inicialização	Void		

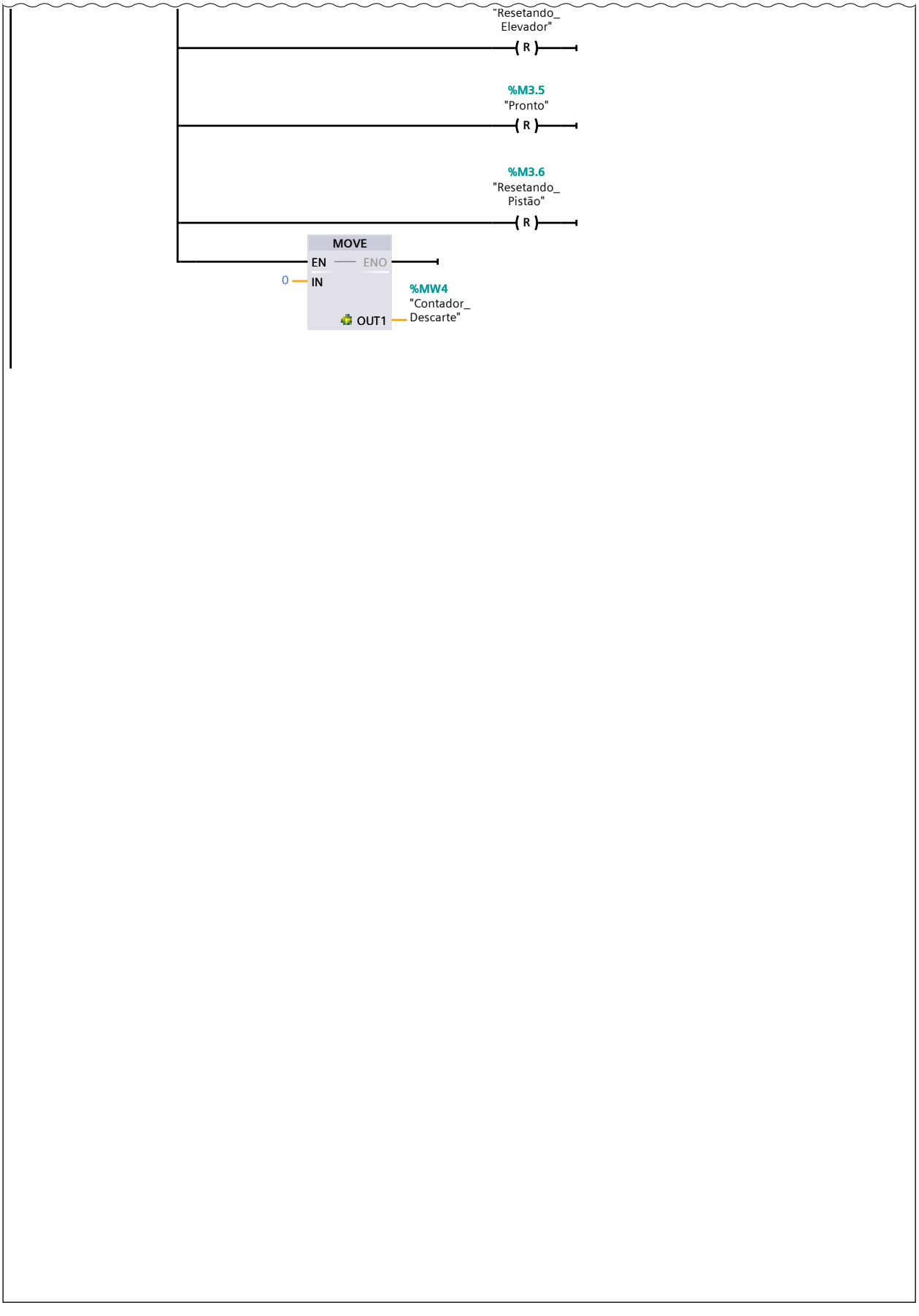
Network 1:

Network 1: (1.1 / 2.1)



Network 1: (2.1 / 2.1)

1.1 (Page6 - 2)



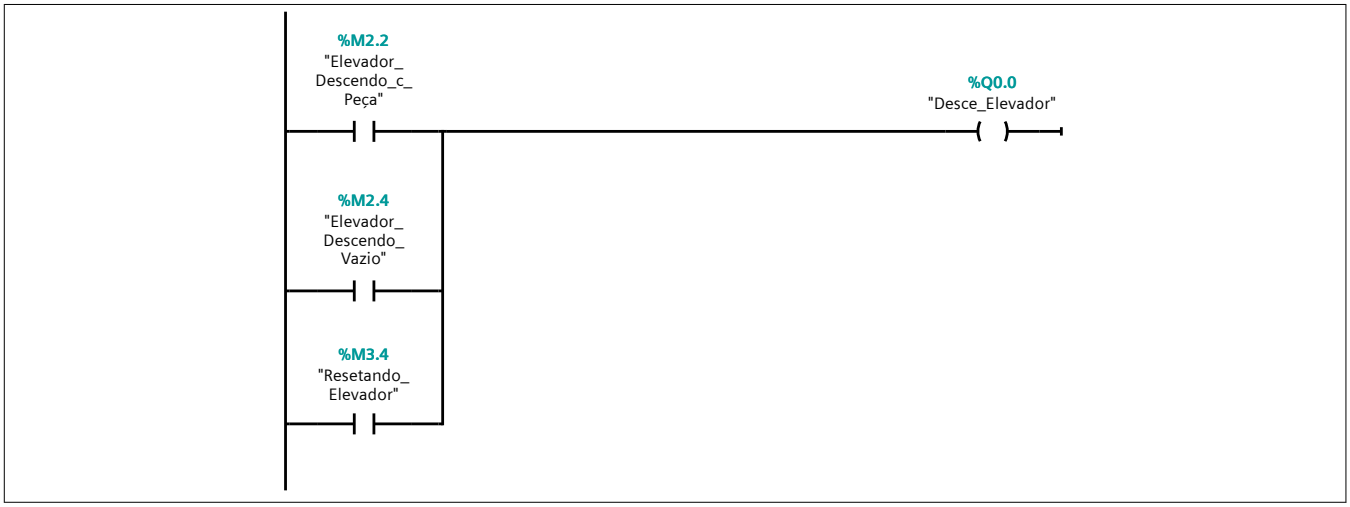
CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks

Ações [FC5]

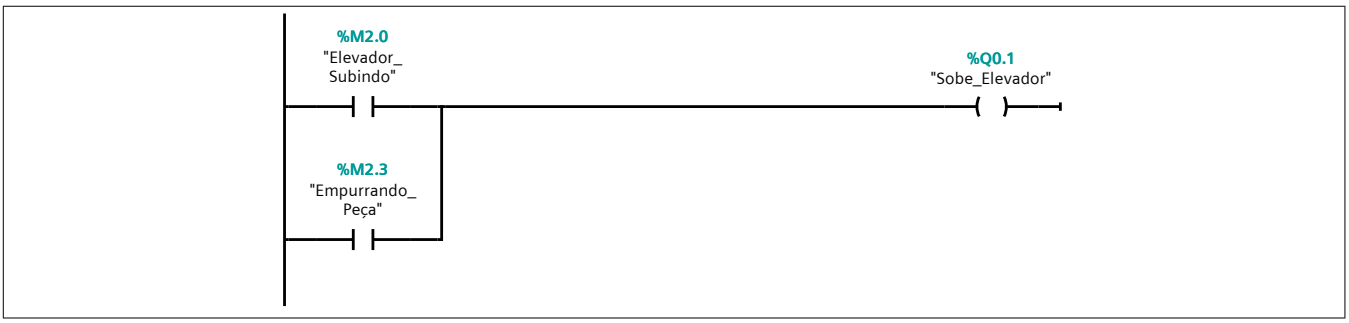
Ações Properties					
General					
Name	Ações	**Number**	5	**Type**	FC
Language	LAD	**Numbering**	Automatic		
Information					
Title		**Author**		**Comment**	
Family		**Version**	0.1	**User-defined ID**	

Name	Data type	Default value	Comment
Input			
Output			
InOut			
Temp			
Constant			
▼ Return			
Ações	Void		

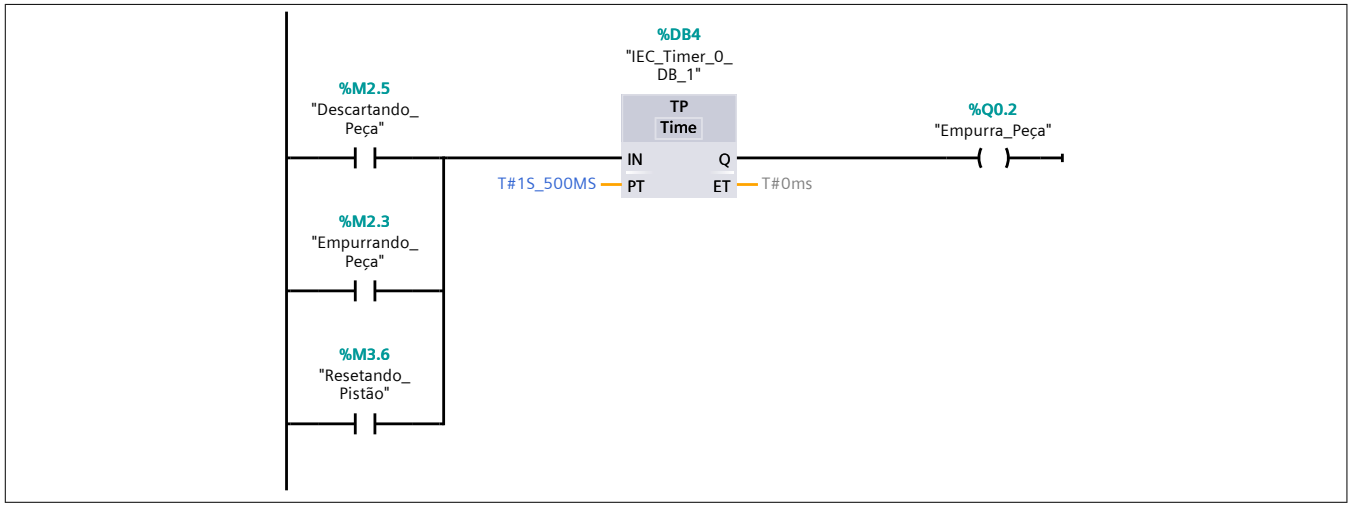
Network 1:



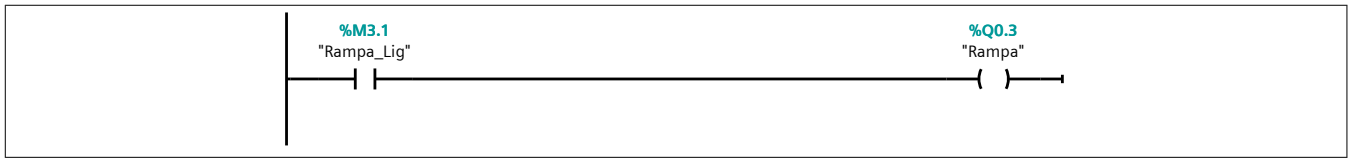
Network 2:



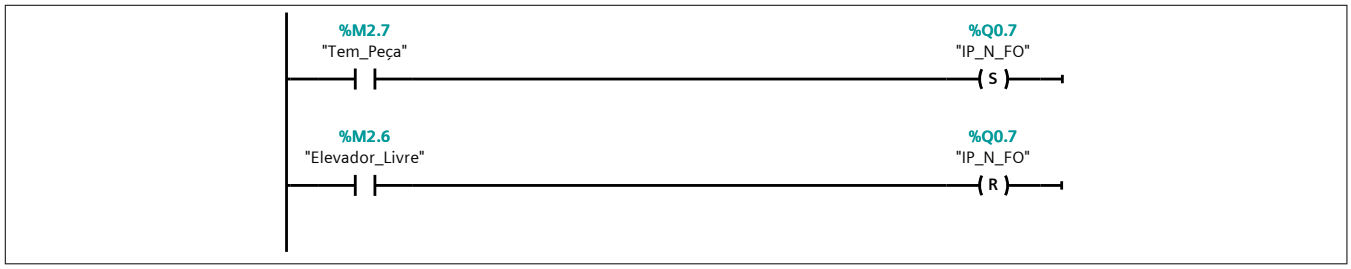
Network 3:



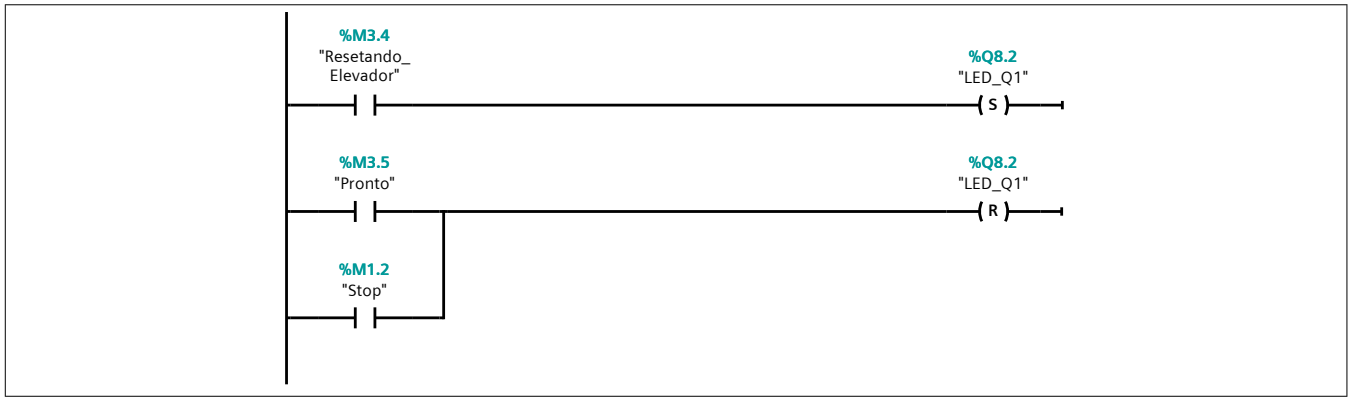
Network 4:



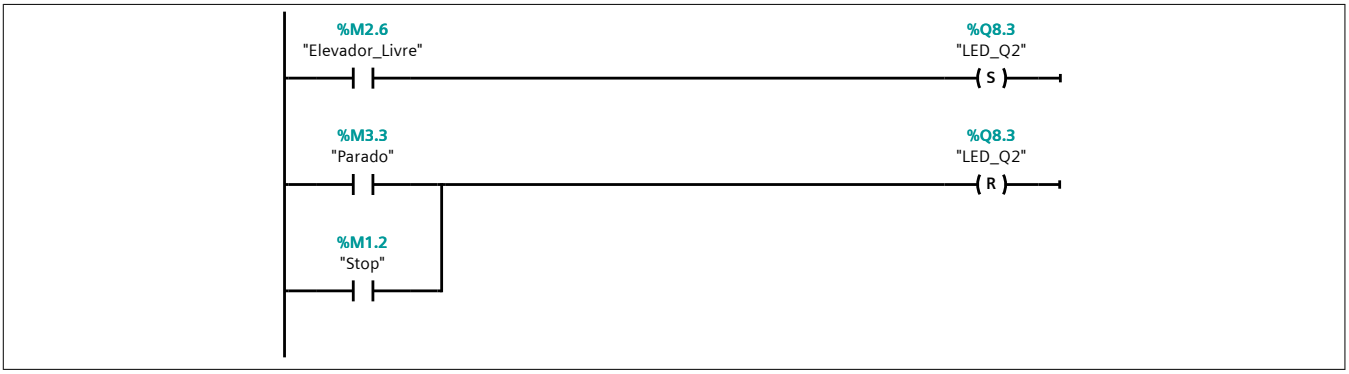
Network 5:



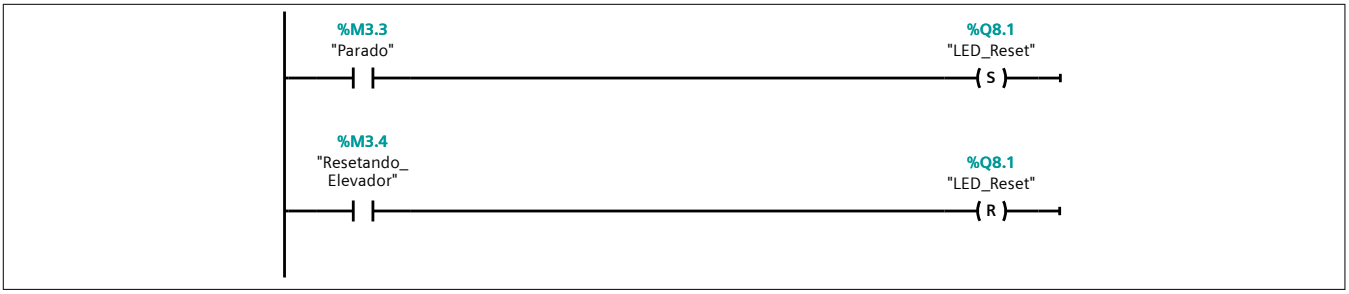
Network 6:



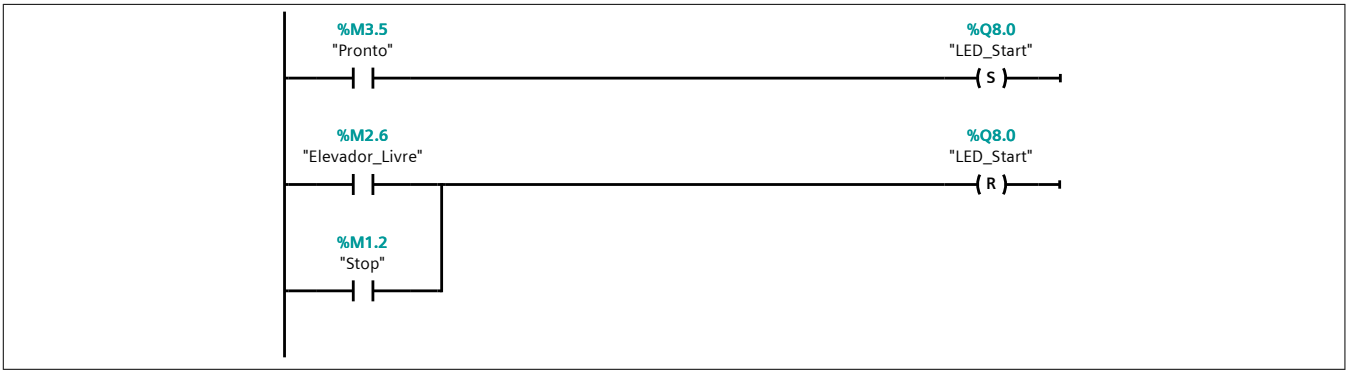
Network 7:



Network 8:



Network 9:



CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks / System blocks / Program resources

IEC_Timer_0_DB [DB2]

IEC_Timer_0_DB Properties					
General					
Name	IEC_Timer_0_DB	**Number**	2	**Type**	DB
Language	DB	**Numbering**	Automatic		
Information					
Title		**Author**	Simatic	**Comment**	
Family	IEC	**Version**	1.0	**User-defined ID**	IEC_TMR

Name	Data type	Start value	Retain	Accessible from HMI/OPC UA	Writable from HMI/OPC UA	Visible in HMI engineering	Setpoint	Supervision	Comment
▼ Static									
PT	Time	T#0ms	False	True	True	True	False		
ET	Time	T#0ms	False	True	False	True	False		
IN	Bool	false	False	True	True	True	False		
Q	Bool	false	False	True	False	True	False		

CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks / System blocks / Program resources

IEC_Counter_0_DB_1 [DB3]

IEC_Counter_0_DB_1 Properties					
General					
Name	IEC_Counter_0_DB_1	**Number**	3	**Type**	DB
Language	DB	**Numbering**	Automatic		
Information					
Title		**Author**	Simatic	**Comment**	
Family	IEC	**Version**	1.0	**User-defined ID**	CNTR

Name	Data type	Start value	Retain	Accessible from HMI/OPC UA	Writable from HMI/OPC UA	Visible in HMI engineering	Setpoint	Supervision	Comment
▼ Static									
CU	Bool	false	True	True	True	True	False		
CD	Bool	false	True	True	True	True	False		
R	Bool	false	True	True	True	True	False		
LD	Bool	false	True	True	True	True	False		
QU	Bool	false	True	True	True	True	False		
QD	Bool	false	True	True	True	True	False		
PV	Int	0	True	True	True	True	False		
CV	Int	0	True	True	True	True	False		

CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks / System blocks / Program resources

IEC_Timer_0_DB_1 [DB4]

IEC_Timer_0_DB_1 Properties					
General					
Name	IEC_Timer_0_DB_1	**Number**	4	**Type**	DB
Language	DB	**Numbering**	Automatic		
Information					
Title		**Author**	Simatic	**Comment**	
Family	IEC	**Version**	1.0	**User-defined ID**	IEC_TMR

Name	Data type	Start value	Retain	Accessible from HMI/OPC UA	Writable from HMI/OPC UA	Visible in HMI engineering	Setpoint	Supervision	Comment
▼ Static									
PT	Time	T#0ms	False	True	True	True	False		
ET	Time	T#0ms	False	True	False	True	False		
IN	Bool	false	False	True	True	True	False		
Q	Bool	false	False	True	False	True	False		

CLP2_TESTING [CPU 1214C DC/DC/DC] / Program blocks / System blocks / Program resources

IEC_Timer_0_DB_2 [DB1]

IEC_Timer_0_DB_2 Properties					
General					
Name	IEC_Timer_0_DB_2	**Number**	1	**Type**	DB
Language	DB	**Numbering**	Automatic		
Information					
Title		**Author**	Simatic	**Comment**	
Family	IEC	**Version**	1.0	**User-defined ID**	IEC_TMR

Name	Data type	Start value	Retain	Accessible from HMI/OPC UA	Writable from HMI/OPC UA	Visible in HMI engineering	Setpoint	Supervision	Comment
▼ Static									
PT	Time	T#0ms	False	True	True	True	False		
ET	Time	T#0ms	False	True	False	True	False		
IN	Bool	false	False	True	True	True	False		
Q	Bool	false	False	True	False	True	False		

CLP2_TESTING [CPU 1214C DC/DC/DC]

Technology objects

This folder is empty.

CLP2_TESTING [CPU 1214C DC/DC/DC] / PLC tags / Default tag table [116]

PLC tags

PLC tags									
	Name	Data type	Address	Retain	Acces-sible from HMI/OPC UA	Writa-ble from HMI/OPC UA	Visi-ble in HMI engi-neer-ing	Supervision	Comment
	PART_AV	Bool	%I0.0	False	True	True	True		
	B2	Bool	%I0.1	False	True	True	True		
	B4	Bool	%I0.2	False	True	True	True		
	B5	Bool	%I0.3	False	True	True	True		
	1B1	Bool	%I0.4	False	True	True	True		
	1B2	Bool	%I0.5	False	True	True	True		
	2B1	Bool	%I0.6	False	True	True	True		
	IP_FI	Bool	%I0.7	False	True	True	True		
	Bot_Start	Bool	%I8.0	False	True	True	True		
	Bot_Stop	Bool	%I8.1	False	True	True	True		
	Bot_Reset	Bool	%I8.3	False	True	True	True		
	Desce_Elevador	Bool	%Q0.0	False	True	True	True		
	Sobe_Elevador	Bool	%Q0.1	False	True	True	True		
	Empurra_Peça	Bool	%Q0.2	False	True	True	True		
	Rampa	Bool	%Q0.3	False	True	True	True		
	IP_N_FO	Bool	%Q0.7	False	True	True	True		
	LED_Start	Bool	%Q8.0	False	True	True	True		
	LED_Reset	Bool	%Q8.1	False	True	True	True		
	LED_Q1	Bool	%Q8.2	False	True	True	True		
	LED_Q2	Bool	%Q8.3	False	True	True	True		
	void	Bool	%M57.0	False	True	True	True		
	Chega_Peça	Bool	%M0.0	False	True	True	True		
	Subida_Liberada	Bool	%M0.1	False	True	True	True		
	void2	Bool	%M57.1	False	True	True	True		
	Elevador_Em_Cima	Bool	%M0.3	False	True	True	True		
	void3	Bool	%M57.2	False	True	True	True		
	Elevador_Embaixo	Bool	%M0.4	False	True	True	True		
	void4	Bool	%M57.3	False	True	True	True		
	Pistão_Recuou	Bool	%M0.5	False	True	True	True		
	void5	Bool	%M57.4	False	True	True	True		
	Altura_Certa	Bool	%M0.6	False	True	True	True		
	Prox.Bancada_Liber-ou	Bool	%M0.7	False	True	True	True		
	void6	Bool	%M57.5	False	True	True	True		
	void7	Bool	%M57.6	False	True	True	True		
	void8	Bool	%M57.7	False	True	True	True		
	Start	Bool	%M1.0	False	True	True	True		

	Name	Data type	Address	Retain	Accessible from HMI/OPC UA	Writable from HMI/OPC UA	Visible in HMI engineering	Supervision	Comment
	Reset	Bool	%M1.1	False	True	True	True		
	Stop	Bool	%M1.2	False	True	True	True		
	Elevador_Subindo	Bool	%M2.0	False	True	True	True		
	Testando_Altura	Bool	%M2.1	False	True	True	True		
	Elevador_Descendo_c_Peça	Bool	%M2.2	False	True	True	True		
	Empurrando_Peça	Bool	%M2.3	False	True	True	True		
	Elevador_Descendo_Vazio	Bool	%M2.4	False	True	True	True		
	Descartando_Peça	Bool	%M2.5	False	True	True	True		
	Elevador_Livre	Bool	%M2.6	False	True	True	True		
	Contador_Descarte	Int	%MW4	False	True	True	True		
	Rampa_Desl	Bool	%M3.0	False	True	True	True		
	Rampa_Lig	Bool	%M3.1	False	True	True	True		
	Prox_Bancada_Livre	Bool	%M3.2	False	True	True	True		
	Parado	Bool	%M3.3	False	True	True	True		
	Resetando_Elevador	Bool	%M3.4	False	True	True	True		
	Pronto	Bool	%M3.5	False	True	True	True		
	Tem_Peça	Bool	%M2.7	False	True	True	True		
	T1	Bool	%M4.0	False	True	True	True		
	T2	Bool	%M4.1	False	True	True	True		
	T3	Bool	%M4.2	False	True	True	True		
	T4	Bool	%M4.3	False	True	True	True		
	T5	Bool	%M4.4	False	True	True	True		
	T6	Bool	%M4.5	False	True	True	True		
	T7	Bool	%M4.6	False	True	True	True		
	T8	Bool	%M6.0	False	True	True	True		
	T9	Bool	%M6.1	False	True	True	True		
	T10	Bool	%M6.2	False	True	True	True		
	T11	Bool	%M6.3	False	True	True	True		
	T12	Bool	%M6.4	False	True	True	True		
	T13	Bool	%M6.5	False	True	True	True		
	T14	Bool	%M6.6	False	True	True	True		
	T15	Bool	%M6.7	False	True	True	True		
	T16	Bool	%M7.0	False	True	True	True		
	T17	Bool	%M7.1	False	True	True	True		
	T18	Bool	%M7.2	False	True	True	True		
	T19	Bool	%M7.3	False	True	True	True		
	T20	Bool	%M7.4	False	True	True	True		
	T21	Bool	%M7.5	False	True	True	True		
	T22	Bool	%M7.6	False	True	True	True		
	T23	Bool	%M7.7	False	True	True	True		

	Name	Data type	Address	Retain	Accessible from HMI/OPC UA	Writable from HMI/OPC UA	Visible in HMI engineering	Supervision	Comment
	T24	Bool	%M8.0	False	True	True	True		
	T0	Bool	%M8.1	False	True	True	True		
	Fim_Reset	Bool	%M8.2	False	True	True	True		
	T25	Bool	%M8.3	False	True	True	True		
	Memo_Inicialização	Bool	%M58.0	False	True	True	True		
	T26	Bool	%M8.4	False	True	True	True		
	Resetando_Pistão	Bool	%M3.6	False	True	True	True		
	T27	Bool	%M8.5	False	True	True	True		
	Tag_1	Bool	%M58.1	False	True	True	True		
	Pistão_Recuado	Bool	%M58.2	False	True	True	True		

CLP2_TESTING [CPU 1214C DC/DC/DC] / PLC tags / Default tag table [116]

User constants

User constants				
	Name	Data type	Value	Comment

CLP2_TESTING [CPU 1214C DC/DC/DC] / PLC data types

System data types

This folder is empty.

CLP2_TESTING [CPU 1214C DC/DC/DC] / Watch and force tables

Force table

Name	Address	Display format	Force value	Comment

CLP2_TESTING [CPU 1214C DC/DC/DC]

Traces

Name

CLP2_TESTING [CPU 1214C DC/DC/DC] / Traces

Measurements

This folder is empty.

CLP2_TESTING [CPU 1214C DC/DC/DC] / Traces

Combined measurements

Name

CLP2_TESTING [CPU 1214C DC/DC/DC]

PLC alarm text lists

This folder is empty.

CLP2_TESTING [CPU 1214C DC/DC/DC] / Local modules

CLP2_TESTING [CPU 1214C DC/DC/DC]

CLP2_TESTING			
General\Project information			
Name	CLP2_TESTING	**Author**	LAI-09
Comment		**Slot**	1
Rack	0		
General\Catalog information			
Short designation	CPU 1214C DC/DC/DC	**Description**	Work memory 100 KB; 24VDC power supply with DI14 x 24VDC SINK/ SOURCE, DQ10 x 24VDC and AI2 on board; 6 high-speed counters and 4 pulse outputs on board; signal board expands on-board I/O; up to 3 communication modules for serial communication; up to 8 signal modules for I/O expansion; 0.04 ms/1000 instructions; PROFINET interface for programming, HMI and PLC to PLC communication
Article number	6ES7 214-1AG40-0XB0	**Firmware version**	V4.2
General\Identification & Maintenance			
Plant designation		**Location identifier**	
Installation date	2023-05-04 14:13:24.297	**Additional information**	
General\Checksums			
Text lists	FA 70 E8 75 1D 5A 8E 29	**Software**	C3 C0 4A 97 11 DC B8 5E
PROFINET interface [X1]\General			
Name	PROFINET interface_1	**Author**	LAI-09
Comment			
PROFINET interface [X1]\General\Project information			
Name	DI 14/DQ 10_1	**Comment**	
Name	AI 2_1	**Comment**	
Name	AQ 1x12BIT_1	**Comment**	
PROFINET interface [X1]\General\Catalog information			
Short designation	AQ1 Signal board	**Description**	Signal board AQ1 x 12 bits; plug-in terminal blocks; output: +/-10V and 0 to 20 mA; configurable diagnostics; configurable substitute output value
Article number	6ES7 232-4HA30-0XB0	**Firmware version**	V1.0
PROFINET interface [X1]\Ethernet addresses\Interface networked with			
Subnet:	Not connected		
PROFINET interface [X1]\Ethernet addresses\IP protocol			
IP configuration	Set IP address in the project	**IP address:**	150.162.14.24
Subnet mask:	255.255.0.0	**Use router**	False
PROFINET interface [X1]\Ethernet addresses\PROFINET			
PROFINET device name is set directly at the device	False	**Generate PROFINET device name automatically**	True
PROFINET device name:	clp2_testing	**Converted name:**	clp2xbtestingab04
Device number:	0		
PROFINET interface [X1]\Time synchronization			
Enable time synchronization via NTP server	Enable time synchronization via NTP server		IP addresses
Server 1	0.0.0.0	**Server 2**	0.0.0.0
Server 3	0.0.0.0	**Server 4**	0.0.0.0

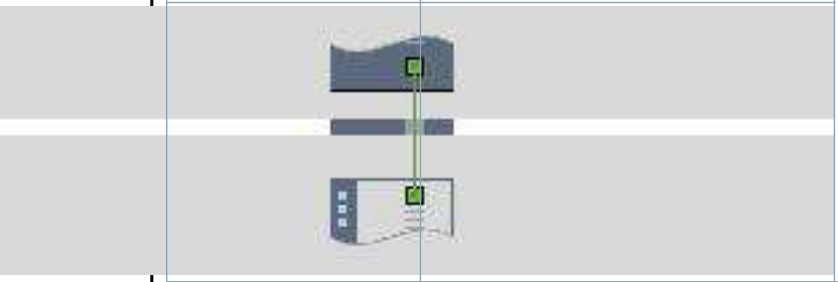
Update interval	10sec	**Empty**	
CPU synchronizes the modules of the device.	No synchronization		
PROFINET interface [X1]\Digital inputs\Channel0			
Channel address	I0.0	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel0			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49152
Event name:	0	**Hardware interrupt:**	0
Rising edge0	Rising edge0		
PROFINET interface [X1]\Digital inputs\Channel0			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49280
Event name:	0	**Hardware interrupt:**	0
Falling edge0	Falling edge0		
PROFINET interface [X1]\Digital inputs\Channel1			
Channel address	I0.1	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel1			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49153
Event name:	0	**Hardware interrupt:**	0
Rising edge1	Rising edge1		
PROFINET interface [X1]\Digital inputs\Channel1			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49281
Event name:	0	**Hardware interrupt:**	0
Falling edge1	Falling edge1		
PROFINET interface [X1]\Digital inputs\Channel2			
Channel address	I0.2	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel2			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49154
Event name:	0	**Hardware interrupt:**	0
Rising edge2	Rising edge2		
PROFINET interface [X1]\Digital inputs\Channel2			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49282
Event name:	0	**Hardware interrupt:**	0
Falling edge2	Falling edge2		
PROFINET interface [X1]\Digital inputs\Channel3			
Channel address	I0.3	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel3			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49155
Event name:	0	**Hardware interrupt:**	0
Rising edge3	Rising edge3		
PROFINET interface [X1]\Digital inputs\Channel3			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49283
Event name:	0	**Hardware interrupt:**	0
Falling edge3	Falling edge3		
PROFINET interface [X1]\Digital inputs\Channel4			
Channel address	I0.4	**Input filters**	6.4 millisec
Enable pulse catch	0		

PROFINET interface [X1]\Digital inputs\Channel4			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49156
Event name:	0	**Hardware interrupt:**	0
Rising edge4	Rising edge4		
PROFINET interface [X1]\Digital inputs\Channel4			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49284
Event name:	0	**Hardware interrupt:**	0
Falling edge4	Falling edge4		
PROFINET interface [X1]\Digital inputs\Channel5			
Channel address	I0.5	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel5			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49157
Event name:	0	**Hardware interrupt:**	0
Rising edge5	Rising edge5		
PROFINET interface [X1]\Digital inputs\Channel5			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49285
Event name:	0	**Hardware interrupt:**	0
Falling edge5	Falling edge5		
PROFINET interface [X1]\Digital inputs\Channel6			
Channel address	I0.6	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel6			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49158
Event name:	0	**Hardware interrupt:**	0
Rising edge6	Rising edge6		
PROFINET interface [X1]\Digital inputs\Channel6			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49286
Event name:	0	**Hardware interrupt:**	0
Falling edge6	Falling edge6		
PROFINET interface [X1]\Digital inputs\Channel7			
Channel address	I0.7	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel7			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49159
Event name:	0	**Hardware interrupt:**	0
Rising edge7	Rising edge7		
PROFINET interface [X1]\Digital inputs\Channel7			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49287
Event name:	0	**Hardware interrupt:**	0
Falling edge7	Falling edge7		
PROFINET interface [X1]\Digital inputs\Channel8			
Channel address	I1.0	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel8			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49160
Event name:	0	**Hardware interrupt:**	0
Rising edge8	Rising edge8		

PROFINET interface [X1]\Digital inputs\Channel8			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49288
Event name:	0	**Hardware interrupt:**	0
Falling edge8	Falling edge8		
PROFINET interface [X1]\Digital inputs\Channel9			
Channel address	I1.1	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel9			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49161
Event name:	0	**Hardware interrupt:**	0
Rising edge9	Rising edge9		
PROFINET interface [X1]\Digital inputs\Channel9			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49289
Event name:	0	**Hardware interrupt:**	0
Falling edge9	Falling edge9		
PROFINET interface [X1]\Digital inputs\Channel10			
Channel address	I1.2	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel10			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49162
Event name:	0	**Hardware interrupt:**	0
Rising edge10	Rising edge10		
PROFINET interface [X1]\Digital inputs\Channel10			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49290
Event name:	0	**Hardware interrupt:**	0
Falling edge10	Falling edge10		
PROFINET interface [X1]\Digital inputs\Channel11			
Channel address	I1.3	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel11			
Enable rising edge detection	0	**RidPrefixRisingEdgeEvent**	49163
Event name:	0	**Hardware interrupt:**	0
Rising edge11	Rising edge11		
PROFINET interface [X1]\Digital inputs\Channel11			
Enable falling edge detection	0	**RidPrefixFallingEdgeEvent**	49291
Event name:	0	**Hardware interrupt:**	0
Falling edge11	Falling edge11		
PROFINET interface [X1]\Digital inputs\Channel12			
Channel address	I1.4	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Digital inputs\Channel13			
Channel address	I1.5	**Input filters**	6.4 millisec
Enable pulse catch	0		
PROFINET interface [X1]\Analog inputs\Noise reduction			
Integration time	50 Hz (20 ms)		
PROFINET interface [X1]\Analog inputs\Channel0			
Channel address	IW64	**Measurement type**	Voltage
Voltage range	0..10 V	**Smoothing**	Weak (4 cycles)
Empty		**Enable overflow diagnostics**	1
PROFINET interface [X1]\Analog inputs\Channel1			
Channel address	IW66	**Measurement type**	Voltage

Voltage range	0..10 V	**Smoothing**	Weak (4 cycles)
Empty		**Enable overflow diagnostics**	1
PROFINET interface [X1]\Digital outputs			
Reaction to CPU STOP	Use substitute value		
PROFINET interface [X1]\Digital outputs\Channel0			
Channel address	Q0.0	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel1			
Channel address	Q0.1	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel2			
Channel address	Q0.2	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel3			
Channel address	Q0.3	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel4			
Channel address	Q0.4	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel5			
Channel address	Q0.5	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel6			
Channel address	Q0.6	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel7			
Channel address	Q0.7	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel8			
Channel address	Q1.0	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Digital outputs\Channel9			
Channel address	Q1.1	**Substitute a value of 1 on a change from RUN to STOP.**	0
PROFINET interface [X1]\Operating mode			
IO controller	True	**IO system**	
Device number	0	**IO device**	False
PROFINET interface [X1]\Analog outputs			
Reaction to CPU STOP	Use substitute value		
PROFINET interface [X1]\Analog outputs\Channel0			
Channel address	QW80	**Analog output type**	Voltage
Voltage range	+/- 10 V	**Substitute value for channel on a change from RUN to STOP**	0.000V
Empty		**Enable short circuit diagnostics**	1
Enable overflow diagnostics	1	**Enable underflow diagnostics**	1
PROFINET interface [X1]\I/O addresses\Input addresses			
Start address	0.0	**End address**	1.7

Organization block	0	**Process image**	0
PROFINET interface [X1]\I/O addresses\Input addresses			
Start address	64	**End address**	67
Organization block	0	**Process image**	0
PROFINET interface [X1]\I/O addresses\Output addresses			
Start address	0.0	**End address**	1.7
Organization block	0	**Process image**	0
PROFINET interface [X1]\I/O addresses\Output addresses			
Start address	80	**End address**	81
Organization block	0	**Process image**	0
PROFINET interface [X1]\Advanced options\Interface options			
Support device replacement without exchangeable medium	True	**Permit overwriting of device names of all assigned IO devices**	False
Use IEC V2.2 LLDP mode	False	**Keep-Alive connection monitoring:**	30s
PROFINET interface [X1]\Advanced options\Real time settings\IO communication			
Send clock:	1.000ms		
PROFINET interface [X1]\Advanced options\Real time settings\Real time options			
Calculated bandwidth for cyclic IO data:	0.000ms	**Calculated bandwidth for cyclic IO data:**	0.000%
PROFINET interface [X1]\Advanced options\Port [X1 P1]\General			
Name	Port_1	**Author**	LAI-09
Comment			
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port interconnection\Local port:			
Local port:	CLP2_TESTING\PROFINET interface_1 [X1]\Port_1 [X1 P1 R]	**Medium:**	Copper
Cable name:	---		



PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port interconnection\Partner port:			
	Monitoring of partner port is not possible	**Partner port:**	Any partner
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Activate			
Activate this port for use	True		
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Connection			
Transmission rate / duplex:	Automatic	**Monitor**	False
Enable autonegotiation	True		
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Boundaries			
End of detection of accessible devices	False	**End of topology discovery**	False
End of the sync domain	False		
PROFINET interface [X1]\Web server access			
Enable Web server using this interface	False	**The Web server must also be activated in the properties of the PLC.**	

High speed counters (HSC)\HSC1\General\Enable			
Enable this high speed counter	0	**Enable this high speed counter**	0
Enable this high speed counter	0	**Enable this high speed counter**	0
Enable this high speed counter	0	**Enable this high speed counter**	0
High speed counters (HSC)\HSC1\General\Project information			
Name	HSC_1	**Comment**	
Name	HSC_2	**Comment**	
Name	HSC_3	**Comment**	
Name	HSC_4	**Comment**	
Name	HSC_5	**Comment**	
Name	HSC_6	**Comment**	
High speed counters (HSC)\HSC1\I/O addresses\Input addresses			
Start address	1000.0	**End address**	1003.7
Start address	1004.0	**End address**	1007.7
Organization block	0	**Start address**	1008.0
End address	1011.7	**Organization block**	0
Process image	0	**Start address**	1012.0
End address	1015.7	**Organization block**	0
Process image	0	**Start address**	1016.0
End address	1019.7	**Organization block**	0
Process image	0	**Start address**	1020.0
End address	1023.7	**Organization block**	0
Process image	0	**Organization block**	0
Process image	0	**Process image**	0
Pulse generators (PTO/PWM)\PTO1/PWM1\General\Enable			
Enable this pulse generator	0	**Enable this pulse generator**	0
Pulse generators (PTO/PWM)\PTO1/PWM1\General\Project information			
Name	Pulse_1	**Comment**	
Name	Pulse_2	**Comment**	
Pulse generators (PTO/PWM)\PTO1/PWM1\I/O addresses\Output addresses			
Start address	1000.0	**End address**	1001.7
Start address	1002.0	**End address**	1003.7
Organization block	0	**Organization block**	0
Process image	0	**Process image**	0
Startup			
Startup after POWER ON	Warm restart - mode before POWER OFF	**Comparison preset to actual configuration**	Startup CPU even if mismatch
Configuration time	60000ms	**OBs should be interruptible**	1
Cycle			
Cycle monitoring time	150ms		
Enable minimum cycle time for cyclic OBs	0	**Minimum cycle time**	1ms
Communication load			
Cycle load due to communication	20%		
System and clock memory\System memory bits			
Enable the use of system memory byte	0	**Address of system memory byte (MBx)**	1
First cycle		**Diagnostic status changed**	
Always 1 (high)		**Always 0 (low)**	
System and clock memory\Clock memory bits			
Enable the use of clock memory byte	0	**Address of clock memory byte (MBx)**	0

10 Hz clock		**5 Hz clock**	
2.5 Hz clock		**2 Hz clock**	
1.25 Hz clock		**1 Hz clock**	
0.625 Hz clock		**0.5 Hz clock**	
Web server\General			
Activate Web server on all modules of this device	False	**Permit access only with HTTPS**	True
Web server\Automatic update			
Enable automatic update	True	**Update interval**	0s

Web server\User interface languages

Assign project language	User interface languages
English (United States)	German
English (United States)	English
English (United States)	French
English (United States)	Spanish
English (United States)	Italian
English (United States)	Chinese (simplified)

Web server\User management

User name	User rights
Everybody	

Web server\User-defined web pages

Application name	HTML source path	Default HTML page	Files with dynamic content	Web DB number	Fragment DB number
		index.htm	.htm;.html	333	334

Web server\Overview of interfaces

Device	Interface	Enabled web server access
CLP2_TESTING	PROFINET interface_1	False

User interface languages

Assign project language	User interface languages
English (United States)	German
English (United States)	English
English (United States)	French
English (United States)	Spanish
English (United States)	Italian
English (United States)	Chinese (simplified)

Time of day\Local time			
Time zone	(UTC +01:00) Berlin, Bern, Brussels, Rome, Stockholm, Vienna		
Time of day\Daylight saving time			
Activate daylight saving time	1	**Difference between standard and daylight saving time**	60mins
Time of day\Daylight saving time\Start of daylight saving time			
Starting week of the month:	Last		Sunday
of	March	**at**	01:00 a.m.
Time of day\Daylight saving time\Start of standard time			
	Last		Sunday
of	October	**at**	02:00 a.m.
Protection & Security			
Level of protection	No protection		
Protection & Security\Connection mechanisms			
Permit access with PUT/GET communication from remote partner	False		

Protection & Security\Security event			
Summarize security events in case of high message volume	True	**Length of an interval**	20
Unit	seconds		

Protection & Security\External load memory	
Disable copying from internal load memory to external load memory	False

Configuration control\Configuration control for central configuration	
Allow to reconfigure the device via the user program	0

Connection resources

	Station resources - Reserved - Maximum	Station resources - Reserved - Configured	Station resources - Dynamic - Configured	Module resources - CLP2_TESTING [CPU 1214C DC/DC/DC] - Configured
Maximum number of resources:		62	6	68
	Maximum	Configured	Configured	Configured
PG communication:	4	-	-	-
HMI communication:	12	0	0	0
S7 communication:	8	0	0	0
Open user communication:	8	0	0	0
Web communication:	30	-	-	-
Other communication:	-	-	0	0
Total resources used:		0	0	0
Available resources:		62	6	68

Overview of addresses\Overview of addresses\Overview of addresses			
Inputs	True	**Outputs**	True
Address gaps	False	**Slot**	True

Type	Addr. from	Addr. to	Module	PIP	Device name	Device number	Size	Master / IO system	Rack	Slot
I	0	1	DI 14/DQ 10_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 1
O	0	1	DI 14/DQ 10_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 1
I	64	67	AI 2_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 2
I	1000	1003	HSC_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 16
I	1004	1007	HSC_2	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 17
I	1008	1011	HSC_3	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 18
I	1012	1015	HSC_4	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 19
I	1016	1019	HSC_5	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 20
I	1020	1023	HSC_6	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 21
O	1000	1001	Pulse_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 32
O	1002	1003	Pulse_2	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 33
O	1004	1005	Pulse_3	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 34
O	1006	1007	Pulse_4	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 35
O	80	81	AQ 1x12BIT_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 3
I	8	8	DI 8/DQ 8x24VDC_1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	1 Bytes	-	0	2

Type	Addr. from	Addr. to	Module	PIP	Device name	Device number	Size	Master / IO system	Rack	Slot
O	8	8	DI 8/DQ 8x24VDC_ 1	Automatic update	CLP2_TESTING [CPU 1214C DC/DC/DC]	-	1 Bytes	-	0	2

CLP2_TESTING [CPU 1214C DC/DC/DC] / Local modules

DI 8/DQ 8x24VDC_1

DI 8/DQ 8x24VDC_1			
General\Project information			
Name	DI 8/DQ 8x24VDC_1	**Author**	LAI-09
Comment		**Slot**	2
General\Catalog information			
Short designation	SM 1223 DI8/DQ8 x 24VDC	**Description**	Digital input/output module DI8 x 24VDC SINK/SOURCE and DQ8 x 24VDC; configurable input delay; plug-in terminal blocks
Article number	6ES7 223-1BH30-0XB0	**Firmware version**	V1.0
DI 8/DQ 8\Project information			
Name	DI 8/DQ 8x24VDC_1	**Comment**	
DI 8/DQ 8\Digital inputs\Input filters			
I8.0 - I8.3	6.40ms	**I8.4 - I8.7**	6.40ms
DI 8/DQ 8\Digital inputs\Channel0			
Channel address	I8.0		
DI 8/DQ 8\Digital inputs\Channel1			
Channel address	I8.1		
DI 8/DQ 8\Digital inputs\Channel2			
Channel address	I8.2		
DI 8/DQ 8\Digital inputs\Channel3			
Channel address	I8.3		
DI 8/DQ 8\Digital inputs\Channel4			
Channel address	I8.4		
DI 8/DQ 8\Digital inputs\Channel5			
Channel address	I8.5		
DI 8/DQ 8\Digital inputs\Channel6			
Channel address	I8.6		
DI 8/DQ 8\Digital inputs\Channel7			
Channel address	I8.7		
DI 8/DQ 8\Digital outputs			
Reaction to CPU STOP	Use substitute value		
DI 8/DQ 8\Digital outputs\Channel0			
Channel address	Q8.0	**Substitute a value of 1 on a change from RUN to STOP.**	0
DI 8/DQ 8\Digital outputs\Channel1			
Channel address	Q8.1	**Substitute a value of 1 on a change from RUN to STOP.**	0
DI 8/DQ 8\Digital outputs\Channel2			
Channel address	Q8.2	**Substitute a value of 1 on a change from RUN to STOP.**	0
DI 8/DQ 8\Digital outputs\Channel3			
Channel address	Q8.3	**Substitute a value of 1 on a change from RUN to STOP.**	0
DI 8/DQ 8\Digital outputs\Channel4			
Channel address	Q8.4	**Substitute a value of 1 on a change from RUN to STOP.**	0

DI 8/DQ 8\Digital outputs\Channel5			
Channel address	Q8.5	**Substitute a value of 1 on a change from RUN to STOP.**	0
DI 8/DQ 8\Digital outputs\Channel6			
Channel address	Q8.6	**Substitute a value of 1 on a change from RUN to STOP.**	0
DI 8/DQ 8\Digital outputs\Channel7			
Channel address	Q8.7	**Substitute a value of 1 on a change from RUN to STOP.**	0
DI 8/DQ 8\I/O addresses\Input addresses			
Start address	8.0	**End address**	8.7
Organization block	0	**Process image**	0
DI 8/DQ 8\I/O addresses\Output addresses			
Start address	8.0	**End address**	8.7
Organization block	0	**Process image**	0