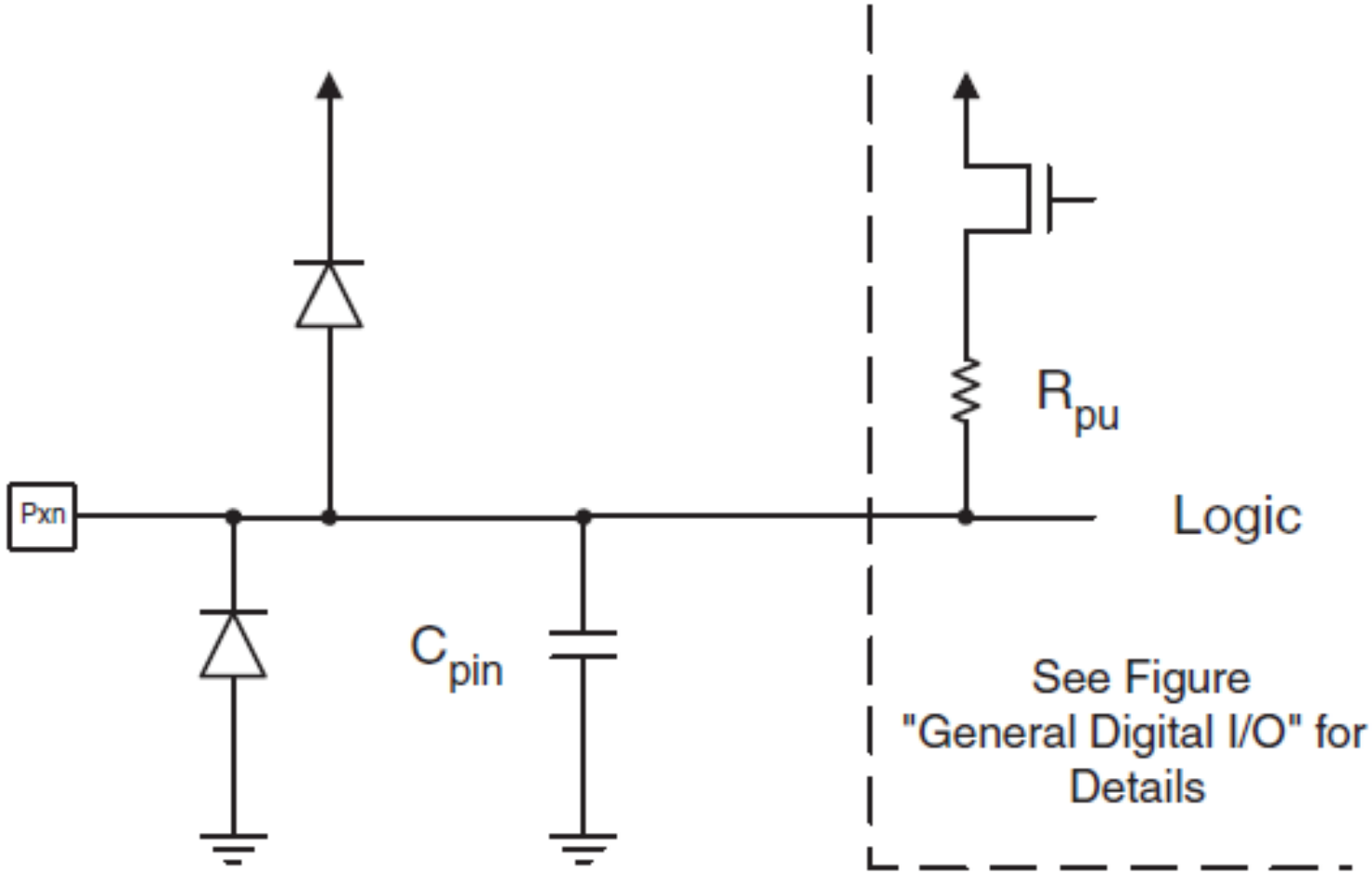
I/O Ports (Portas de entrada e saída)

Sistemas Microcontrolados


Pxn
C_{pin}
R_{pu}
Logic
See Figure
"General Digital I/O" for
Details

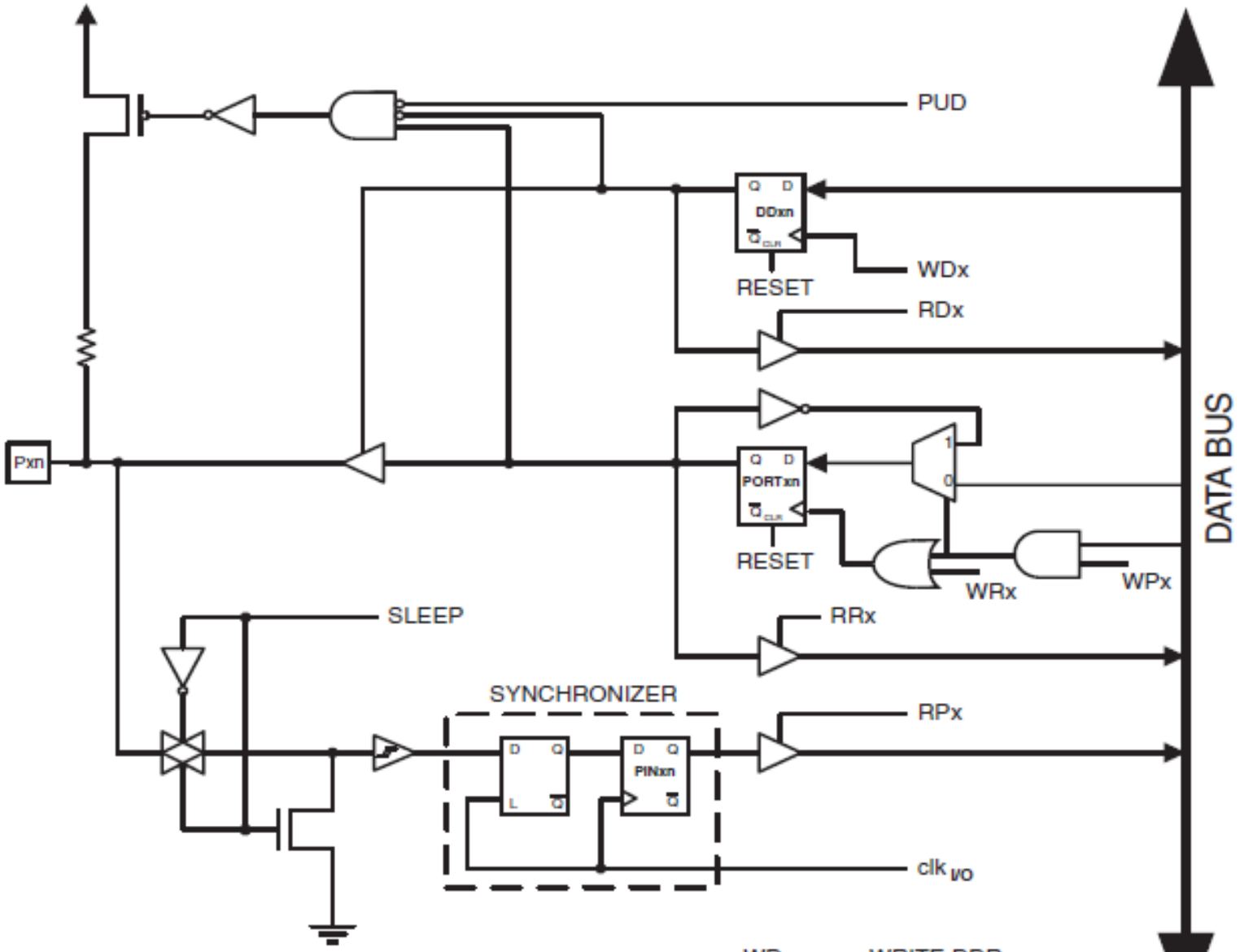
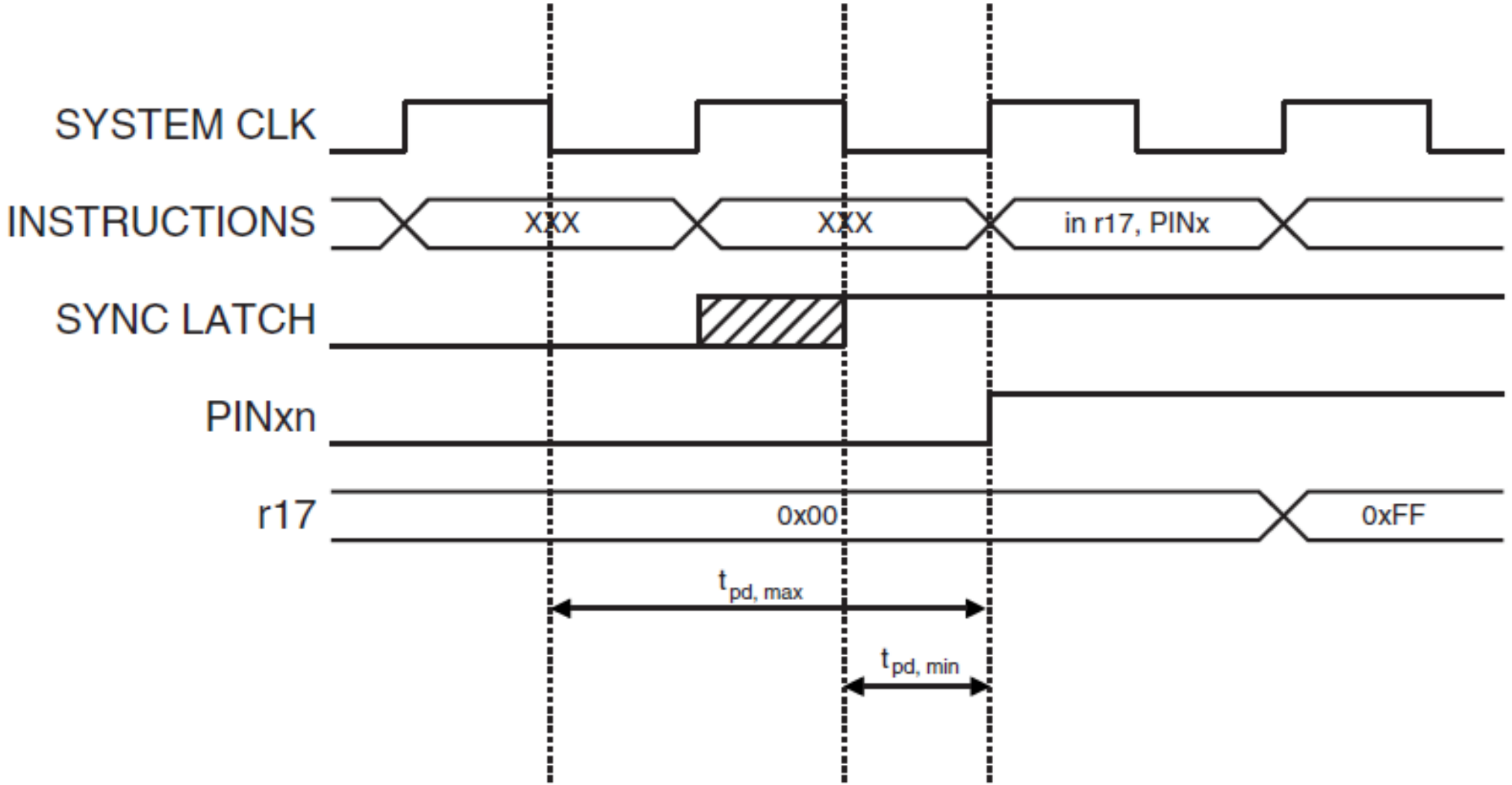

PUD
DDxn
RESET
WDx
RDx
Pxn
PORTxn
RESET
WRx
WPx
DATA BUS
SLEEP
RRx
SYNCHRONIZER
RPx
PINxn
clk I/O
PUD: PULLUP DISABLE
SLEEP: SLEEP CONTROL
clk I/O: I/O CLOCK
WDx: WRITE DDRx
RDx: READ DDRx
WRx: WRITE PORTx
RRx: READ PORTx REGISTER
RPx: READ PORTx PIN
WPx: WRITE PINx REGISTER

Figure 13-3. Synchronization when Reading an Externally Applied Pin value



Assembly Code Example[1]

```
...
; Define pull-ups and set outputs high
; Define directions for port pins
ldi   r16,(1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0)
ldi   r17,(1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0)
out   PORTB,r16
out   DDRB,r17
; Insert nop for synchronization
nop
; Read port pins
in    r16,PINB
...
```

C Code Example

```
unsigned char i;
  ...
  /* Define pull-ups and set outputs high */
  /* Define directions for port pins */
  PORTB = (1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0);
  DDRB = (1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0);
  /* Insert nop for synchronization*/
  __no_operation();
  /* Read port pins */
  i = PINB;
  ...
```

DDxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

13.4.1 MCUCR – MCU Control Register

Bit	7	6	5	4	3	2	1	0	
0x35 (0x55)	JTD	–	–	PUD	–	–	IVSEL	IVCE	MCUCR
Read/Write	R/W	R	R	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 4 – PUD: Pull-up Disable**

When this bit is written to one, the I/O ports pull-up resistors are disabled even if the DDxn and PORTxn Registers are configured to enable the pull-up resistor ({DDxn, PORTxn} = 0b01). See “Configuring the Pin” on page 68 for more details about this feature.

13.4.2 PORTA – Port A Data Register

Bit	7	6	5	4	3	2	1	0	
0x02 (0x22)	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	PORTA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

13.4.3 DDRA – Port A Data Direction Register

Bit	7	6	5	4	3	2	1	0	
0x01 (0x21)	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

13.4.4 PINA – Port A Input Pins Address

Bit	7	6	5	4	3	2	1	0	
0x00 (0x20)	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	PINA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

13.3.1 Alternate Functions of Port A

The Port A has an alternate function as the address low byte and data lines for the External Memory Interface.

Table 13-3. Port A Pins Alternate Functions

Port Pin	Alternate Function
PA7	AD7 (External memory interface address and data bit 7)
PA6	AD6 (External memory interface address and data bit 6)
PA5	AD5 (External memory interface address and data bit 5)
PA4	AD4 (External memory interface address and data bit 4)
PA3	AD3 (External memory interface address and data bit 3)
PA2	AD2 (External memory interface address and data bit 2)
PA1	AD1 (External memory interface address and data bit 1)
PA0	AD0 (External memory interface address and data bit 0)

13.3.2 Alternate Functions of Port B

The Port B pins with alternate functions are shown in Table 13-6.

Table 13-6. Port B Pins Alternate Functions

Port Pin	Alternate Functions
PB7	OC0A/OC1C/PCINT7 (Output Compare and PWM Output A for Timer/Counter0, Output Compare and PWM Output C for Timer/Counter1 or Pin Change Interrupt 7)
PB6	OC1B/PCINT6 (Output Compare and PWM Output B for Timer/Counter1 or Pin Change Interrupt 6)
PB5	OC1A/PCINT5 (Output Compare and PWM Output A for Timer/Counter1 or Pin Change Interrupt 5)
PB4	OC2A/PCINT4 (Output Compare and PWM Output A for Timer/Counter2 or Pin Change Interrupt 4)
PB3	MISO/PCINT3 (SPI Bus Master Input/Slave Output or Pin Change Interrupt 3)
PB2	MOSI/PCINT2 (SPI Bus Master Output/Slave Input or Pin Change Interrupt 2)
PB1	SCK/PCINT1 (SPI Bus Serial Clock or Pin Change Interrupt 1)
PB0	$\overline{SS}$/PCINT0 (SPI Slave Select input or Pin Change Interrupt 0)

13.3.3 Alternate Functions of Port C

The Port C alternate function is as follows:

Table 13-9. Port C Pins Alternate Functions

Port Pin	Alternate Function
PC7	A15 (External Memory interface address bit 15)
PC6	A14 (External Memory interface address bit 14)
PC5	A13 (External Memory interface address bit 13)
PC4	A12 (External Memory interface address bit 12)
PC3	A11 (External Memory interface address bit 11)
PC2	A10 (External Memory interface address bit 10)
PC1	A9 (External Memory interface address bit 9)
PC0	A8 (External Memory interface address bit 8)

13.3.5 Alternate Functions of Port E

The Port E pins with alternate functions are shown in Table 13-15.

Table 13-15. Port E Pins Alternate Functions

Port Pin	Alternate Function
PE7	INT7/ICP3/CLK0 (External Interrupt 7 Input, Timer/Counter3 Input Capture Trigger or Divided System Clock)
PE6	INT6/ T3 (External Interrupt 6 Input or Timer/Counter3 Clock Input)
PE5	INT5/OC3C (External Interrupt 5 Input or Output Compare and PWM Output C for Timer/Counter3)
PE4	INT4/OC3B (External Interrupt4 Input or Output Compare and PWM Output B for Timer/Counter3)
PE3	AIN1/OC3A (Analog Comparator Negative Input or Output Compare and PWM Output A for Timer/Counter3)
PE2	AIN0/XCK0 (Analog Comparator Positive Input or USART0 external clock input/output)
PE1	PDO(1)/TXD0 (Programming Data Output or USART0 Transmit Pin)
PE0	PDI(1)/RXD0/PCINT8 (Programming Data Input, USART0 Receive Pin or Pin Change Interrupt 8)

13.3.6 Alternate Functions of Port F

The Port F has an alternate function as analog input for the ADC as shown in Table 13-18. If some Port F pins are configured as outputs, it is essential that these do not switch when a conversion is in progress. This might corrupt the result of the conversion. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a Reset occurs.

Table 13-18. Port F Pins Alternate Functions

Port Pin	Alternate Function
PF7	ADC7/TDI (ADC input channel 7 or JTAG Test Data Input)
PF6	ADC6/TDO (ADC input channel 6 or JTAG Test Data Output)
PF5	ADC5/TMS (ADC input channel 5 or JTAG Test Mode Select)
PF4	ADC4/TCK (ADC input channel 4 or JTAG Test ClocK)
PF3	ADC3 (ADC input channel 3)
PF2	ADC2 (ADC input channel 2)
PF1	ADC1 (ADC input channel 1)
PF0	ADC0 (ADC input channel 0)

13.3.7 Alternate Functions of Port G

The Port G alternate pin configuration is as follows:

Table 13-21. Port G Pins Alternate Functions

Port Pin	Alternate Function
PG5	OC0B (Output Compare and PWM Output B for Timer/Counter0)
PG4	TOSC1 (RTC Oscillator Timer/Counter2)
PG3	TOSC2 (RTC Oscillator Timer/Counter2)
PG2	ALE (Address Latch Enable to external memory)
PG1	$\overline{RD}$ (Read strobe to external memory)
PG0	$\overline{WR}$ (Write strobe to external memory)

13.3.8 Alternate Functions of Port H

The Port H alternate pin configuration is as follows:

Table 13-24. Port H Pins Alternate Functions

Port Pin	Alternate Function
PH7	T4 (Timer/Counter4 Clock Input)
PH6	OC2B (Output Compare and PWM Output B for Timer/Counter2)
PH5	OC4C (Output Compare and PWM Output C for Timer/Counter4)
PH4	OC4B (Output Compare and PWM Output B for Timer/Counter4)
PH3	OC4A (Output Compare and PWM Output A for Timer/Counter4)
PH2	XCK2 (USART2 External Clock)
PH1	TXD2 (USART2 Transmit Pin)
PH0	RXD2 (USART2 Receive Pin)

13.3.9 Alternate Functions of Port J

The Port J alternate pin configuration is as follows:

Table 13-27. Port J Pins Alternate Functions

Port Pin	Alternate Function
PJ7	–
PJ6	PCINT15 (Pin Change Interrupt 15)
PJ5	PCINT14 (Pin Change Interrupt 14)
PJ4	PCINT13 (Pin Change Interrupt 13)
PJ3	PCINT12 (Pin Change Interrupt 12)
PJ2	XCK3/PCINT11 (USART3 External Clock or Pin Change Interrupt 11)
PJ1	TXD3/PCINT10 (USART3 Transmit Pin or Pin Change Interrupt 10)
PJ0	RXD3/PCINT9 (USART3 Receive Pin or Pin Change Interrupt 9)

13.3.10 Alternate Functions of Port K

The Port K alternate pin configuration is as follows:

Table 13-30. Port K Pins Alternate Functions

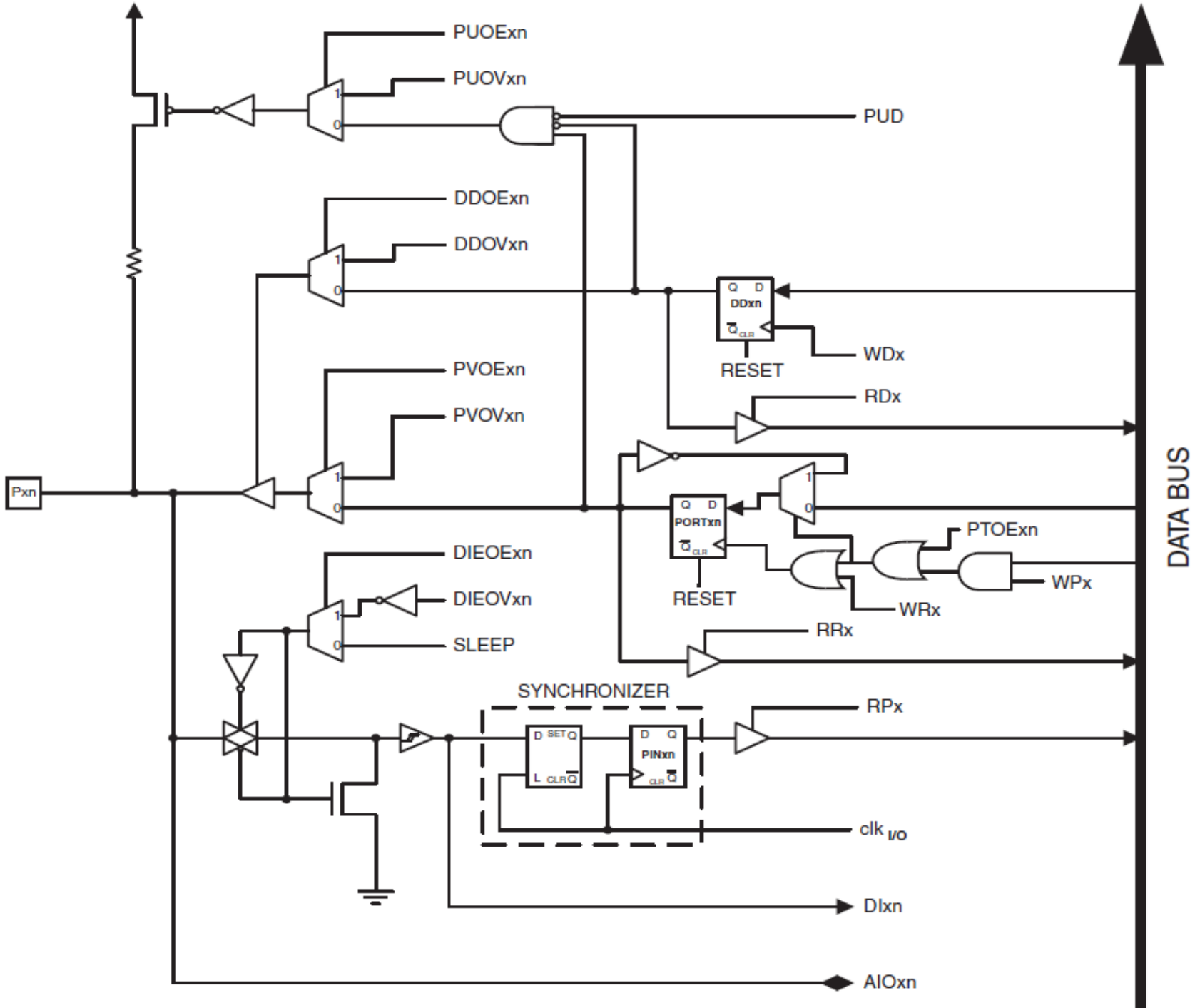
Port Pin	Alternate Function
PK7	ADC15/PCINT23 (ADC Input Channel 15 or Pin Change Interrupt 23)
PK6	ADC14/PCINT22 (ADC Input Channel 14 or Pin Change Interrupt 22)
PK5	ADC13/PCINT21 (ADC Input Channel 13 or Pin Change Interrupt 21)
PK4	ADC12/PCINT20 (ADC Input Channel 12 or Pin Change Interrupt 20)
PK3	ADC11/PCINT19 (ADC Input Channel 11 or Pin Change Interrupt 19)
PK2	ADC10/PCINT18 (ADC Input Channel 10 or Pin Change Interrupt 18)
PK1	ADC9/PCINT17 (ADC Input Channel 9 or Pin Change Interrupt 17)
PK0	ADC8 /PCINT16 (ADC Input Channel 8 or Pin Change Interrupt 16)

13.3.11 Alternate Functions of Port L

The Port L alternate pin configuration is as follows:

Table 13-33. Port L Pins Alternate Functions

Port Pin	Alternate Function
PL7	–
PL6	–
PL5	OC5C (Output Compare and PWM Output C for Timer/Counter5)
PL4	OC5B (Output Compare and PWM Output B for Timer/Counter5)
PL3	OC5A (Output Compare and PWM Output A for Timer/Counter5)
PL2	T5 (Timer/Counter5 Clock Input)
PL1	ICP5 (Timer/Counter5 Input Capture Trigger)
PL0	ICP4 (Timer/Counter4 Input Capture Trigger)


PUOExn
PUOVxn
PUD
DDOExn
DDOVxn
DDxn
RESET
WDx
PVOExn
PVOVxn
RDx
Pxn
PORTxn
RESET
PTOExn
WPx
WRx
DIEOExn
DIEOVxn
SLEEP
RRx
SYNCHRONIZER
RPx
PINxn
clk I/O
DIxn
AIOxn
DATA BUS

PUOExn:	Pxn PULL-UP OVERRIDE ENABLE
PUOVxn:	Pxn PULL-UP OVERRIDE VALUE
DDOExn:	Pxn DATA DIRECTION OVERRIDE ENABLE
DDOVxn:	Pxn DATA DIRECTION OVERRIDE VALUE
PVOExn:	Pxn PORT VALUE OVERRIDE ENABLE
PVOVxn:	Pxn PORT VALUE OVERRIDE VALUE
DIEOExn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE ENABLE
DIEOVxn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE VALUE
SLEEP:	SLEEP CONTROL
PTOExn:	Pxn, PORT TOGGLE OVERRIDE ENABLE

PUD:	PULLUP DISABLE
WDx:	WRITE DDRx
RDx:	READ DDRx
RRx:	READ PORTx REGISTER
WRx:	WRITE PORTx
RPx:	READ PORTx PIN
WPx:	WRITE PINx
$clk_{I/O}$:	I/O CLOCK
DIxn:	DIGITAL INPUT PIN n ON PORTx
AIOxn:	ANALOG INPUT/OUTPUT PIN n ON PORTx