Cairo University

Faculty of Engineering – Credit Hours System

Logic Design -1 (CMPN101)

Fall 2022

Phase 1

Team:

1- Amira Mohamed Essam Ahmed Abdelghany (1210200)
2- Mariam Mahrous Mohammed Abd El Aal (1210301)
3- Mohanad Tarek Ibrahim Elmahalawy (1210313)
4- Omar Ahmed Shawky Adbdelgawad (1210259)

Work Distribution:

- Two of team members are responsible for the Addition and Subtraction operations and binary to BCD circuit and BCD to seven segments circuit (Mariam and Mohanad)
- one member implements the multiplication operation. (Omar)
- one member implements the remainder operation. (Amira)

Test Cases:

1. (00) Addition

Note: left-most bit in output is the sign bit

1st Operand (A)	2nd Operand (B)	SW actual output	expected output	Status
1111	0100	10011	10011	Success
1111	1100	11011	11011	Success
0111	0100	01011	01011	Success
0111	1000	00111	00111	Success
0000	1111	10111	10111	Success

2. (01) Subtraction

Note: left-most bit in output is the sign bit

1st Operand (A)	2nd Operand (B)	SW actual output	expected output	Status
1111	1100	10011	10011	Success
0111	1100	01011	01011	Success
0000	1111	00111	00111	Success
0000	0111	10111	10111	Success
0110	0101	00001	00001	Success
0101	0110	10001	10001	Success

3. (10) Multiplication

Note: left-most bit in output is the sign bit

1st Operand (A)	2nd Operand (B)	SW actual output	expected output	Status
1111	1010	0001110	0001110	Success
0010	1011	1001100	1001100	Success
0000	0011	0000000	0000000	Success
1000	0100	0000000	0000000	Success
0010	0001	0000010	0000010	Success

4. (11) Remainder

Note: left-most bit in output is the sign bit

1st Operand (A)	2nd Operand (B)	SW actual output	expected output	Status
1111	0000	0000	0000	Success
1111	0010	0001	0001	Success
0111	0001	0000	0000	Success
0110	0010	0000	0000	Success
1101	1011	1010	1010	Success

➔ All Testcases Passed ✔ 😎

Note: Division by Zero Flag only lights up when the Remainder operation is chosen (11) and the 2nd Operand (B) = 0000 or 1000

Note: When the Zero Flag lights up no negative sign is output (if exists). Otherwise, the sign is output on the 7-Segment

Software Modifications (to accommodate for only 2 bits + sign bit)

1. **2. (00) Addition & (01) Subtraction**

- Used Comparator IC instead of the Comparator that was made.
- Use of Full adders instead of Full adders that was made.
- Removed parts related to the 3rd bit.
- The last mux in sign was done in an easier way.
- Removed any unnecessary parts.
- Integrated the whole adder into 2 circuits instead of 4 (sign/control and adder in same circuit)

3. **(10) Multiplication**

- 2 bits instead of 3 bits
- Used 4-bit full adder

4. **(11) Remainder**

- Used 2 bits instead of 3
- Made eliminations for unnecessary usage of gates