

Files

- Circ3_tbit_fulladder.vhd
- Circ3_tbit_adder.vhd
- Circ3_tbit_extender.vhd
- Circ3_tbit.vhd
- Circ3_cinest.vhd
- Circ3_UAA_toplevel.vhd
- Circ3_calculator_toplevel.vhd
- Circ3_calculator_toplevel_tb.vhd
- SevenSegmentDisplay.vhd

Tasks

- Netlist Views
- RTL Viewer
- State Machine Viewer
- Technology Map View
- Design Assistant (Post-Maj)

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Analysis & Synthesis Summary

Analysis & Synthesis Status: Successful - Fri Jun 07 21:12:31 2024

RTL Viewer - C:/Users/7930966/OneDrive/calculator/calculator - calculator

Netlist Navigator

- Circ3_calculator_toplevel

Diagram showing logic components and connections.

Messages

Type	ID	Message
12133	Instantiated megafunction "binto7seg01"	
12021	Found 1 design units, including 1 entit	
12021	Found 1 design units, including 1 entit	
12021	Found 1 design units, including 1 entit	
12130	Elaborated megafunction instantiation	
12133	Instantiated megafunction "binto7seg01"	
12133	Instantiated megafunction "binto7seg01"	
12133	Instantiated megafunction "binto7seg01"	
286030	Timing-driven Synthesis is running	
16010	Generating hard_block partition "hard_b	
21057	Implemented 319 device resources after	
Quartus Prime Analysis & Synthesis was		
Running Quartus Prime Netlist Viewers		
command: quartus_rpn calculator -c cal		
18236	Number of processors has not been specified which may cause overloading on shared machines. set the global assignment NUP_PARALLEL_PROCESSORS in your QSF to an appropriate value for best perform	
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning		

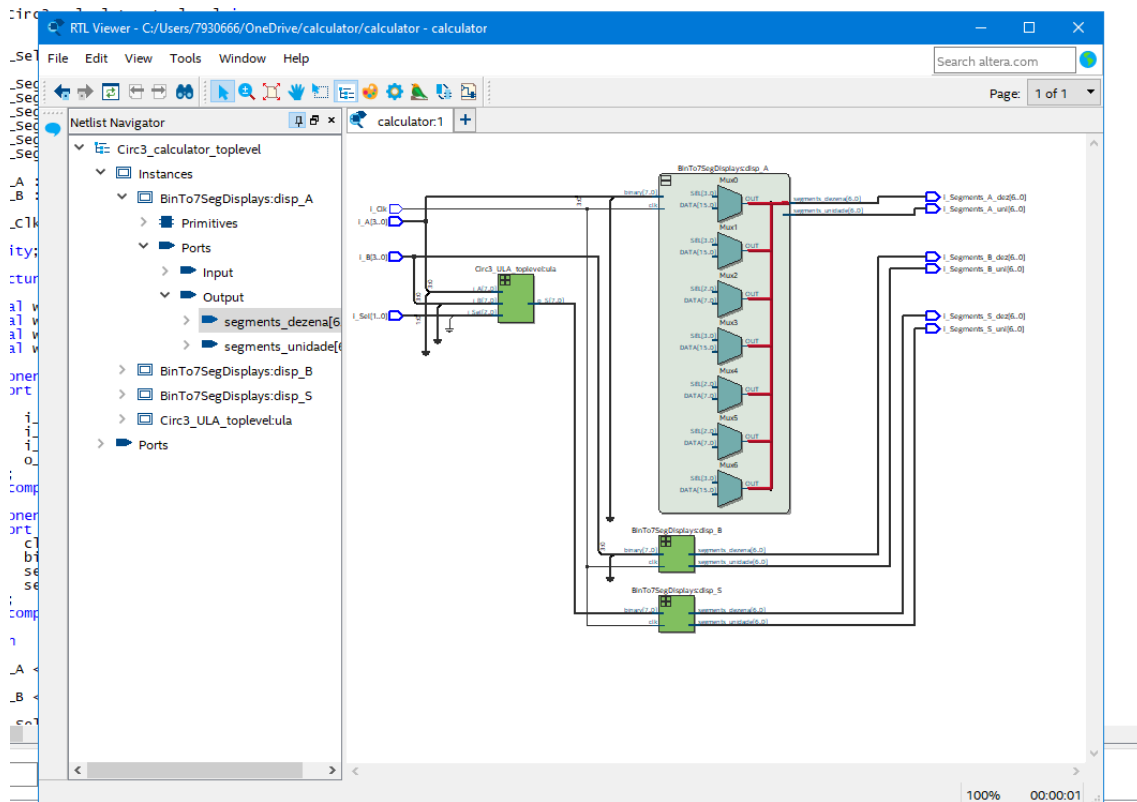
System Processing (52)

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Edit Settings
- View Report
- Analysis & Elaboration
- Partition Merge
- Netlist Views
 - RTL Viewer
 - State Machine Viewer
 - Technology Map View



Analysis & Synthesis Summary	
Analysis & Synthesis Status	Successful - Fri Jun 07 21:12:31 2024
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	calculator
Top-level Entity Name	Circ3_calculator_toplevel
Family	Cyclone V
Logic utilization (in ALMs)	N/A
Total registers	37
Total pins	53
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	0
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0

Total de registradores e total de pins