TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Integrated Master in Aerospace Engineering, Técnico, University of Lisbon

Lab4: Audio Amplifier circuit

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João Maria Mendes, 95804
Maria Magalhães, 95825
Mariana Afonso, 95827

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1 Introduction

The objective of this laboratory assignment is to build an audio amplifier, developing a circuit containing 2 stages, the voltage stage and the output stage. The maximum Audio In is 10 mV, the supply voltage V_{cc} is 12 V and the Audio Out is an 8 Ω speaker. The circuit created and analysed in this assignment can be seen in Figure 1.
In order to evaluate how successfully our goal has been achieved, we calculate the merit M of our work, using the following expression:

$$M = \frac{gain * bandwidth}{cost * lowerCutoffFrequency} \tag{1}$$

where the cost is given by cost = cost of resistors + cost of capacitors + cost of transistors, knowing that each kOhm costs 1 monetary unit (MU), each μF costs 1 MU and each transistor costs 0,1 MU. In Section 2, a theoretical analysis of the circuit is presented, using Octave. In Section 3, the circuit is analysed by simulation using ngspice. The conclusions of this study are outlined in Section 4. In addiction, the results are compared to the theoretical results obtained in Section 2.

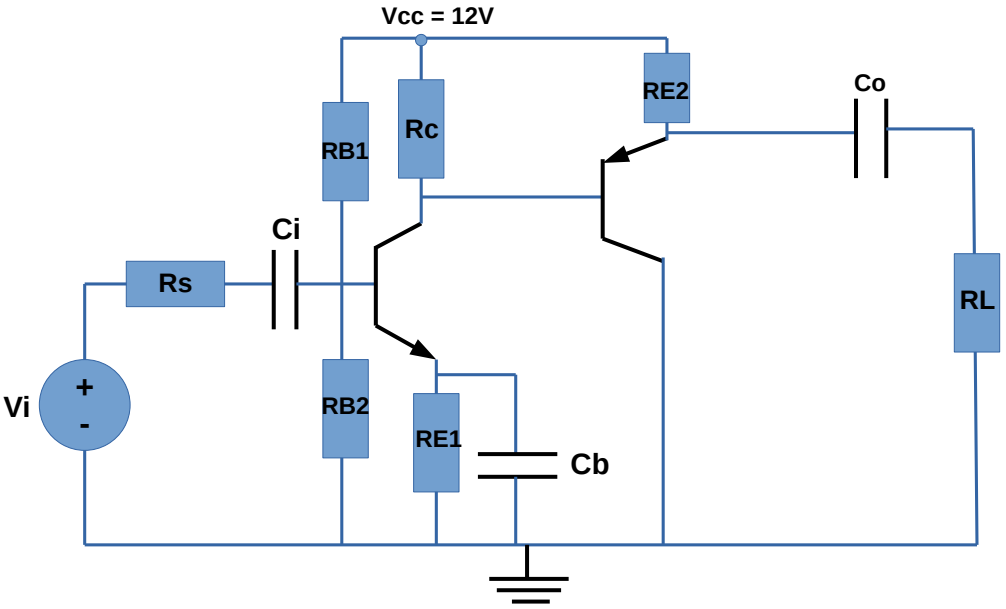

Figure 1: Circuit analysed.

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically.
As already mentioned, the audio amplifier is a circuit with two different stages: the gain stage, in which the voltage input signal is amplified, and the output stage, in which the output impedance is low, so the circuit can be connected to a speaker, while the signal degradation is minimized. In the first stage, the purpose is to have the higher possible gain and the degradation of the signal is avoided with a high input impedance. In the transition between the two stages, the degradation is also prevented, since the input impedance in the second stage is lower than the output impedance of the gain stage, because of the way the two sub-circuits are connected. Finally, in the output stage, the goal is not to amplify the signal, but it should not be attenuated either- this is well achieved since the gain is very close to 1.
The incremental circuit used to compute gain, input and outuput impedances is shown in Figure 2.

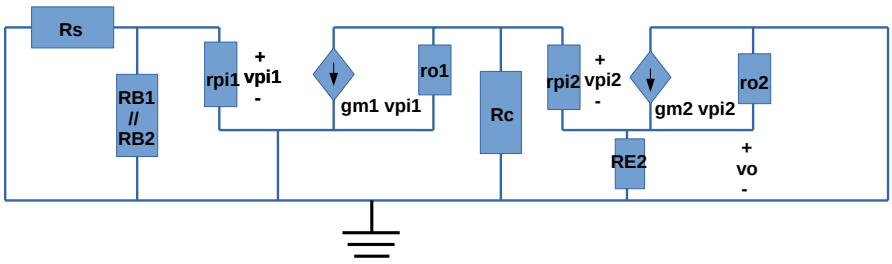

Figure 2: Incremental circuit.

The values used for the parametres are showed in the following table:

Table 1: Values of the circuit parameters

$n_{transistors}$	2.00000000e+00
C_i	1.00000000e-03
C_b	3.00000000e-03
C_o	1.75000000e-03
$RE1$	1.00000000e+02
$RE2$	1.00000000e+02
RC	1.10000000e+03
$RB1$	1.45000000e+05
$RB2$	2.00000000e+04
RS	1.00000000e+02

2.1 Gain Stage

The circuit used in the gain stage uses a capacitor C_E to bypass the resistor R_E. To simplify, we consider that C_E behaves like a short-circuit for high frequencies (AC current) and as an open-circuit for low frequencies (DC current). In AC, the current only flows through the short-circuit (since it has 0 impedance), improving the gain. In DC, the current only flows through the resistor (since it cannot flow through an open-circuit), which stabilizes the temperature effect. The first step of the theoretical analysis is to compute the operating point using the DC model. To do that

we used the expressions below:

$$R_B = \frac{1}{R_{B1}||R_{B2}} \tag{2}$$

$$V_{EQ} = \frac{R_{B2}V_{CC}}{R_{B1} + R_{B2}} \tag{3}$$

$$I_{B1} = \frac{V_{EQ} - V_{BEON}}{R_B + 1 + B_{FN}R_{E1}} \tag{4}$$

$$I_{C1} = B_{FN}I_{B1} \tag{5}$$

$$I_{E1} = 1 + B_{FN}I_{B1} \tag{6}$$

$$V_{E1} = R_{E1}I_{E1} \tag{7}$$

$$V_{O1} = V_{CC} - R_{C1}I_{C1} \tag{8}$$

$$V_{CE} = V_{O1} - V_{E1} \tag{9}$$

We have verified that both BJTs are in the Forward Active Region. The condition considered for that purpose was, for the NPN transistor: $V_{CE} > V_{BE} <=> V_C > V_B$ and for the PNP transistor: $V_{EC} > V_{EB} <=> V_C < V_B$ Next, we can compute the gain, input and output impedances separately for the 2 stages, using the incremental analysis. For the first stage, we use the following expressions to calculate such parameters.

$$Gain_1 = -g_{m1}r_{o1}||R_c\frac{R_B||r_{pi}}{R_B||r_{pi1} + R_s} \tag{10}$$

$$Z_{in1} = R_B||r_{pi1} \tag{11}$$

$$Z_{out1} = r_{o1}||R_C \tag{12}$$

2.2 Output Stage

For the second stage, we analysed the operating point using the following equations:

$$V_{I2} = V_{O1} \tag{13}$$

$$I_{E2} = \frac{V_{CC} - V_{EBON} - V_{I2}}{R_{E2}} \tag{14}$$

$$I_{C2} = \frac{B_{FP}I_{E2}}{B_{FP} + 1} \tag{15}$$

$$V_{O2} = V_{CC}\breve{}R_{E2}I_{E2} \tag{16}$$

By inspection of the circuit, we can see that the voltage of the base is equal to Veq (since there is no current passing through the resistor at the DC model- C is an open-circuit); the voltage in the collector of the gain stage is equal to Vout1 (since it connects the collector to the ground); for the same reason, the voltage in the emitor of the output stage is equal to Vout2; the input voltage of the gain stage is AC, hence in the operating point model it is seen as 0; the voltage in2 is 0 too, since there is no current flowing through the resistor, as explained before; finally, the output voltage in DC analysis is 0, since the capacitor is replaced with a short-circuit, which means that there is no current flowing through the resistor. All this values are summarized in the table bellow.
Using the incremental circuit in Figure 2, we have computed gain, input and output impedances, for this stage, using the expressions below:

$$Gain_2 = \frac{g_{pi2} + g_{m2}}{g_{pi2} + g_{o2} + gE2 + g_{m2}} \tag{17}$$

Table 2: Operating Point: Node Voltages(V)

$base$	1.45454545e+00
$coll$	7.82732202e+00
$emitter1$	3.81457106e-01
$emitter2$	8.52732202e+00
in	0.00000000e+00
$in2$	0.00000000e+00
out	0.00000000e+00
Vcc	1.20000000e+01

$$Z_{in2} = \frac{r_{pi2}}{1 - \frac{g_{pi2}+g_{m2}}{g_{pi2}+g_{o2}+g_{E2}+g_{m2}}} \tag{18}$$

$$Z_{out2} = \frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{R_E} + \frac{1}{r_{pi2}}} \tag{19}$$

Calculating the values of the previous expressions, for both gain and output stage, the following table is obtained:

Table 3: Results obtained for stages separately

$Gain(GainStage)$	-1.44397121e+02
$ImputImpedance(GainStage)$	1.10375986e+03
$OutputImpedance(GainStage)$	1.03786680e+03
$Gain(OutputStage)$	9.87847264e-01
$ImputImpedance(OutputStage)$	1.35240676e+04
$OutputImpedance(OutputStage)$	7.14285398e-01

2.3 Total circuit

To complete the last task, we analysed the incremental circuit above. The goal is to compute the total gain as a function of the frequency. To do that we need to compute the cut off frequencies. Since the upper cut off frequency is too high to be evaluated in the considered problem, we can assume it as infinity, since it is not in the range of audible frequencies, from 20Hz to 20kHz. The lower cut off frequency was calculated as a function of the capacitances of the capacitors, considering that for each equivalente impendance that the others capacitors are short-circuits:

$$lco = \frac{1}{2pi}(\frac{1}{ZOCo} + \frac{1}{ZICi} + \frac{1}{ZbCb}) \tag{20}$$

For frequencies bellow the lower cut off frequency, we considered a linear relation between the gain and the frequency with a slope of 20 dB per decade. Once this frequency is achieved, the graph is constant since we considered the higher cut off frequency as infinite. The only unknown variable by now is that constant value, which can be calculated with the following expression, in which $Gain_1$ is the value obtained in equation 10.

$$A_V = \frac{g_B + \frac{g_{m2}g_B}{g_{pi2}}}{g_B + g_{e2} + g_{o2} + \frac{g_{m2}g_B}{g_{pi2}}} Gain_1 \tag{21}$$

The following plot shows the frequency response of the total circuit.
It is evident that the input impedance of the total circuit is the same as for the gain stage, since the input voltage is not connected to the output stage. So, the last unknown we need to compute is the total output impedances, for which we used the following expression:

$$Z_{Ottotal} = \frac{1}{g_{o2} + \frac{g_{m2}g_B}{g_{pi2}} + g_{e2} + g_B} \tag{22}$$

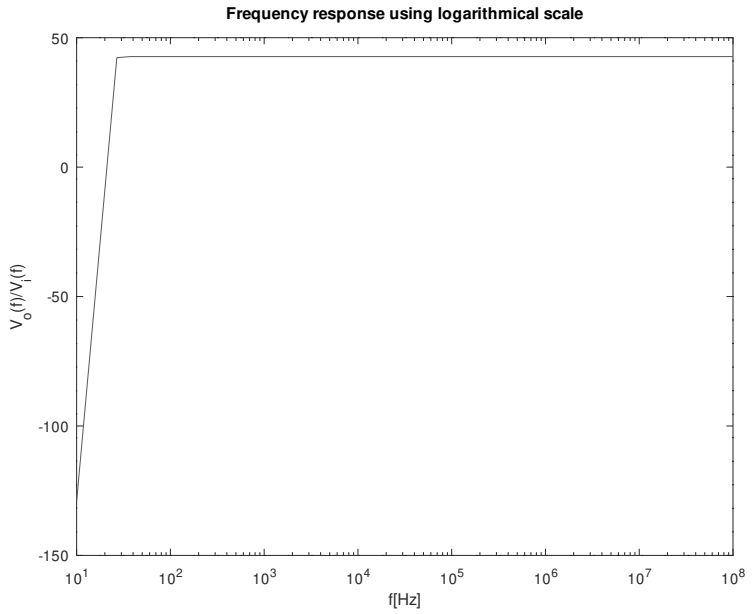

Figure 3: Frequency response.

Since we considered the upper cut off frequency as infinity, the bandwidth is also infinity, therefore, for the theoretical analysis it makes no sense to calculate the merit value. Finally, the following table presents the theoretical obtained results for: total circuit gain, lower cut off frequency, bandwidth, cost, input and output impedances.

Table 4: Results obtained

$TotalGain$	-1.36538763e+02
$LowerCutoffFrequency$	2.68926639e+01
$Bandwidth$	∞
$cost$	5.91660000e+03
$ImputImpedance$	1.10375986e+03
$OutputImpedance$	4.97938733e+00

3 Simulation Analysis

This section covers circuit simulation in ngspice, where the output voltage gain, the lower and upper cutoff frequencies and the input and output impedances were measured. However, in order to calculate the output impedance of the whole circuit, a different circuit had to be used. In this circuit the voltage source V_in and the resistance R_in were replaced by a short circuit and the load R_L was replaced by a voltage source V_o.

In the following table gain, the cutoff frequencies, the bandwidth, the input and output impedances and the cost and merit of the circuit are presented. Furthermore, the graphs also show the frequency response of the output voltage gain and input and output impedances.

Name	Value
gain	6.059407e+01
lower	8.155929e+00
upper	2.178859e+06
bandwidth	2.178851e+06
zin	1.215084e+03
cost	5.916600e+03
merit	2.735974e+03
zout	7.866317e+00

Table 5: Measured values (gain, cutoff frequencies, bandwidth, input and output impedances and the cost and merit of the circuit).

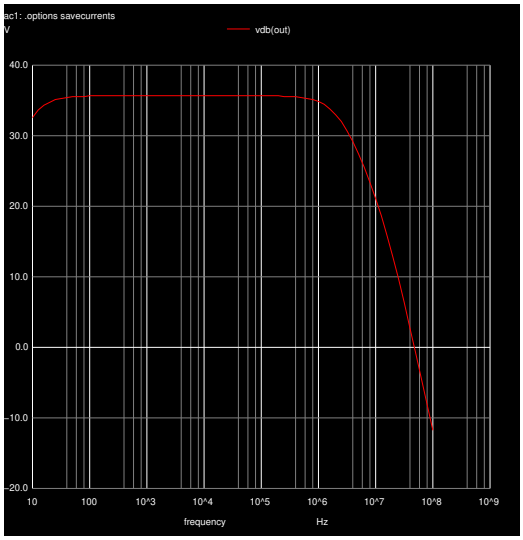

Figure 4: Frequency response of the output voltage gain in the passband.

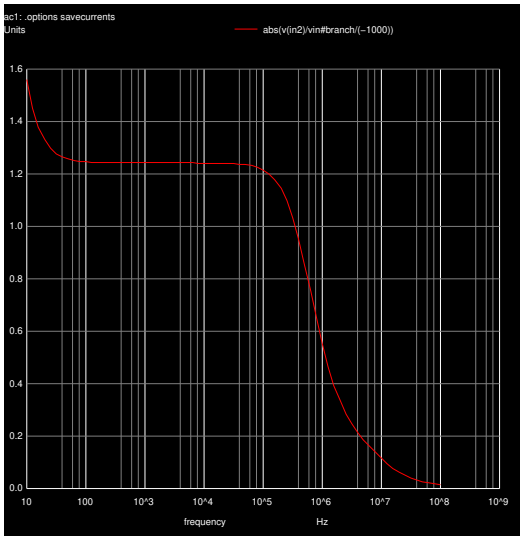

Figure 5: Frequency response of the input impedance of the circuit.

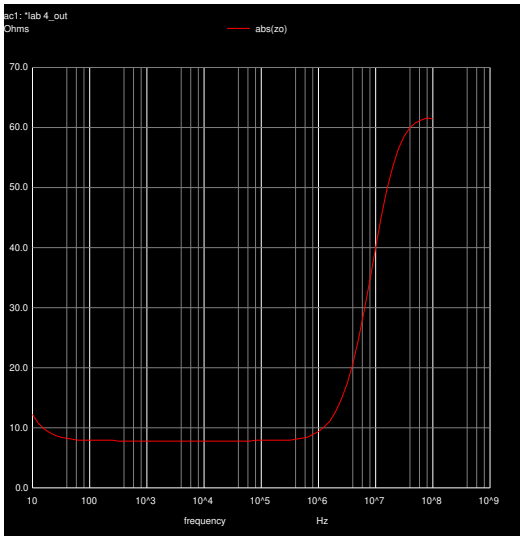

Figure 6: Frequency response of the output impedance of the circuit.

4 Conclusion

In order to analysis the similarities or discrepancies in the theoretical analysis and the simulation, the following tables made with ngspice and octave are presented.

Name	Value
base	1.081464e+00
coll	7.833017e+00
emit	3.990681e-01
emit2	8.590473e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vcc	1.200000e+01

Name	Value
$base$	1.45454545e+00
$coll$	7.82732202e+00
$emitter1$	3.81457106e-01
$emitter2$	8.52732202e+00
in	0.00000000e+00
$in2$	0.00000000e+00
out	0.00000000e+00
Vcc	1.20000000e+01

Table 6: Simulation (left) and Theoretical (right) operating point results.

Name	Value
gain	6.059407e+01
lower	8.155929e+00
upper	2.178859e+06
bandwidth	2.178851e+06
zin	1.215084e+03
cost	5.916600e+03
merit	2.735974e+03
zout	7.866317e+00

Name	Value
$TotalGain$	-1.36538763e+02
$LowerCutoffFrequency$	2.68926639e+01
$Bandwidth$	∞
$cost$	5.91660000e+03
$ImputImpedance$	1.10375986e+03
$OutputImpedance$	4.97938733e+00

Table 7: Simulation (left) and Theoretical (right) results obtained.

Comparing the values obtained in Octave and Ngspice, the values obtained in the operating point analysis are similar. However, the values obtained in the second table are notably different. This can be explained due to the fact that the transistor models used in ngspice are significantly more complex than the models used in the theoretical analysis. Taking this into account, both analysis were still able to create an audio amplifier circuit, even if the octave's model is not the best representation of the reality.