Impedance Controlled Routing

Summary

With increasing device switching speeds impedance controlled routing has become *the* hot topic for the digital designer. This article will discuss how you can use Altium Designer's Signal Integrity analysis engine to match component impedances, and the impedance controlled routing capabilities in the PCB editor.

Application Note
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There is a saying bandied about in engineering circles – there are only two kinds of electronics engineers working in digital design: those who have had signal integrity problems, and those who will. Not so many years ago the term signal integrity was one for the specialist, you only had to deal with it on high-speed designs. But the device switching speeds in those high-speed designs are no longer anything special, in fact they are rapidly becoming the norm. As improving integrated circuit technology drives the size of the transistor down, the speeds at which they can switch goes up. And it is this switching speed that effects the integrity of digital signals.

Thankfully many potential signal integrity issues can be avoided by following good design principals, and implementing the design as an impedance controlled board. Achieving this does require specific design tool capabilities – you need analysis tools that can detect nets with potential ringing and reflection issues, and board design tools that allow the designer to achieve the correct routing impedances. Altium Designer has these capabilities.

This article will help you understand what causes signal integrity issues, and if your board is likely to suffer from them. It will also discuss the two design approaches you must employ to minimizing potential SI issues – matching component impedances, and impedance controlled routing.

Do I need impedance controlled routing?

Do I need to bother with impedance controlled routing, you ask?

In an ideal situation all of the energy that comes out of a component output pin would be coupled into the connected track on the PCB, flow through the PCB routing to the load input pin at the other end, and be absorbed by that load. If all the energy is not absorbed by the load then the left over energy can be reflected back into the PCB routing, flowing to the source output pin. This reflected energy can interact with the original signal, adding to and subtracting from it (depending on the polarity of the energy), resulting in ringing. If the ringing is large enough it will effect the integrity of the signal, resulting in unpredictable, erroneous circuit behavior.

And how do you know if this might occur? If the source pin is able to complete its edge transition before the signal reaches the load pin, then the conditions exist for your design to be impacted by reflected energy. A common rule of thumb that is used to determine if SI issues are likely is the "1/3 rise time"

rule. This rule states that if the trace is more than 1/3 of a rise time long, reflections (ringing) can occur. If the source pin has a 1 nSec rise time, then a route longer than .33 nSec – which is approximately 2 inches in FR4 – must be considered to be a transmission line, a candidate for signal integrity issues. If your devices have this sort of rise time and you know you will have routing of this sort of length, then you might well end up with signal integrity issues on the PCB.

The speed at which the electrical energy can travel along the route it known as the propagation velocity, where

V_P = speed of light / √dielectric constant

Using

Time = 1/3 * rise time

ε_R = 4 (approximation for FR4)

C = 11.811 in/nSec (speed of light, in inches per nanosecond)

To find the length of route above which the integrity of the signal could become a problem:

L_R = Time * V_P

= Time * C / √ ε_R

L_R = .33 * 11.811 / 2

= 1.95 in

How do I control the impedances?

So how do you avoid this situation where there is energy being reflected back and forth between the source and the load – you avoid it by matching the impedances. Impedance matching ensures that all the energy is coupled from the source into the routing, and then from the routing into the load. Routing the board with regard to the impedance is referred to as impedance controlled routing, or another way of saying it is that a board where impedances have been managed is called a controlled impedance PCB.

There are two distinct elements to achieving impedance matching: the first is matching the components; and the second is routing the board to give the required impedance.

Impedance matching the components

You cannot achieve a controlled impedance PCB with routing alone. Firstly you must check, and if necessary, match the impedances of the components.

Ideally you want to detect nets that could have potential signal integrity issues during the design capture phase, so that any additional termination components can be included before the board design process starts. And since output pins are low impedance and input pins high impedance, it is likely that you will need to add termination components to the design to achieve impedance matching.

In Altium Designer you can perform a signal integrity analysis on your design at the schematic capture stage. If you do (**Tools** menu), you will be prompted to provide an average track impedance and route length, and define the supply nets. Once this is done the design can be analyzed, and any potential problem nets identified in the **Signal Integrity** panel, as shown in Figure 1.

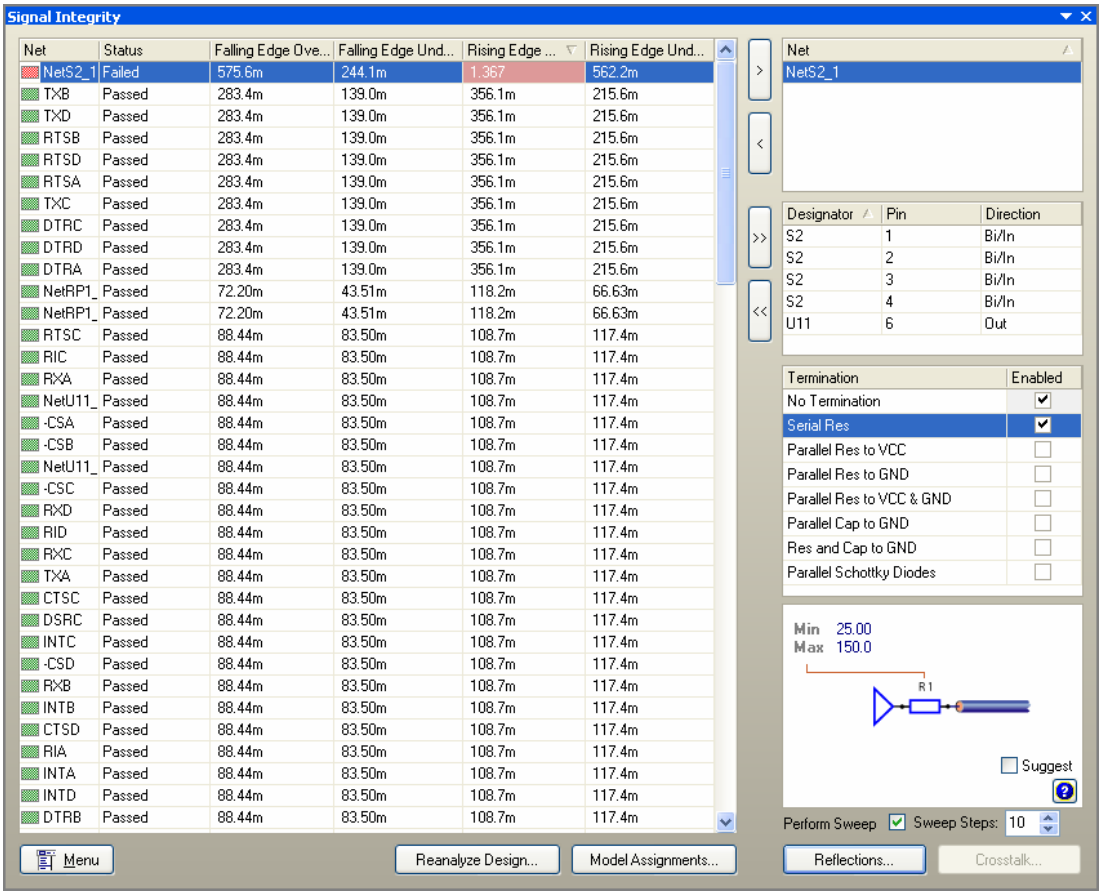


Figure 1. Testing the design for potential signal integrity issues during design capture.

From the panel you can perform a reflection analysis on selected nets. You can also experiment with possible termination configurations and values, note that the **Termination** region of the **Signal Integrity** panel shown in Figure 1 has the **Serial Res** option enabled. The section of the panel just below that shows a series termination resistor, this is where you define the minimum and maximum series termination resistance values that will be used for the reflection analysis.

Figure 2 shows two graphs of a net displaying ringing, the first is the net without termination, the second with the theoretical series termination resistance included at the source pin.

10 passes of the reflection analysis were performed, with the theoretical terminator stepping from 25 ohms to 150 ohms. The 10 passes are listed down the right-hand side of the graph, clicking on each highlights that result, and displays the theoretical termination resistance value at the bottom right. For this net a series termination resistance of 38.89 ohms would produce the graph selected in Figure 2. Press F1 over the **Signal Integrity** panel for more information on using the features in the panel.

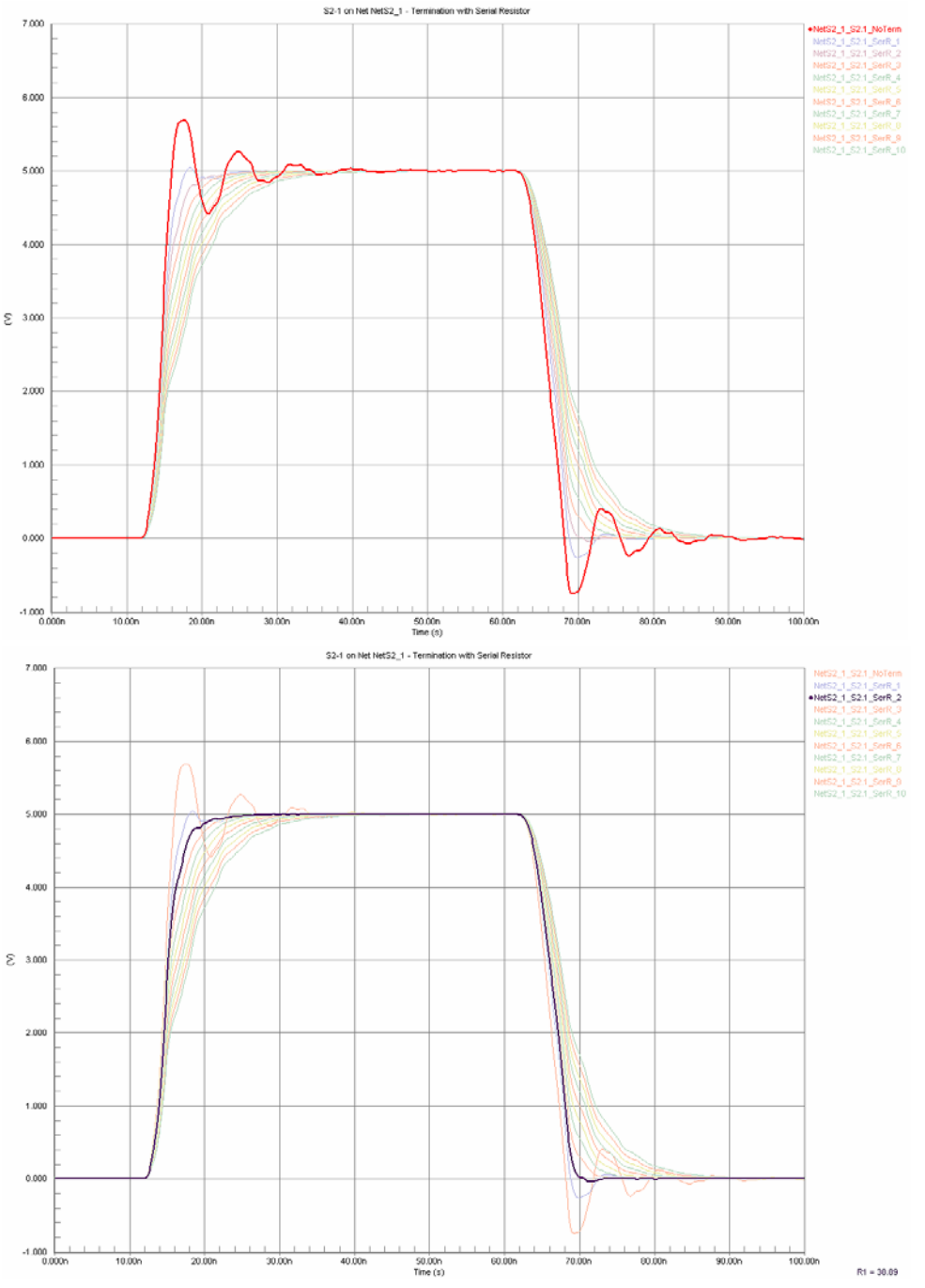


Figure 2. The first graph shows a net with potential signal integrity issues, the second graph is the same net with a theoretical series termination resistor of approximately 40 ohms added.

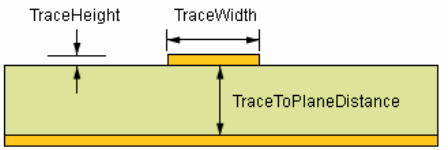
What determines the routing impedance?

The second part of achieving a controlled impedance PCB is to route the board so that the tracks are a defined impedance. There are a number of factors that influence the impedance of your signal routing, including the physical dimensions and properties of the materials used to fabricate the PCB.

Below are the two formulas that Altium Designer uses to calculate the routing impedance, the appropriate one being selected depending on whether the route has a plane layer present on only one side of it (referred to as a microstrip), or has planes present on both sides (referred to as a stripline). Note that if the plane layer(s) are not adjacent to the signal layer then the nearest plane layer(s) will be used in the calculations. Note also that an offset stripline configuration is not supported.

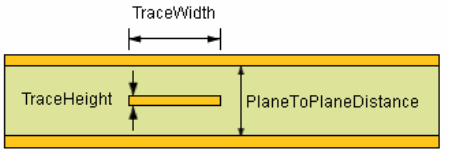
Microstrip characteristic impedance formula

Zo=(87/SQRT(Er+1.41))*LN(5.98*TraceToPlaneDistance /(0.8*TraceWidth + TraceHeight))



Stripline characteristic impedance formula

Zo=(60/SQRT(Er))*LN((1.9*PlaneToPlaneDistance) /(0.8*TraceWidth + TraceHeight))



From the formulae you can see that the copper and insulation (dielectric) thicknesses, the routing width, and the Er all contribute to the impedance. Er is the dielectric constant of the dielectric material, for the standard fiberglass dielectric most commonly used in PCB fabrication (FR-4) this can vary by up to 20%, over the range of 4 to 5. There are other more stable dielectric materials available, such as polyimide and Teflon.

These formula are user-definable, edit them in the **Impedance Formula Editor**, accessed through the **Layer Stack Manager**.

Calculating the routing width for each layer

As you can see from the formula there are many inter-related values that contribute to the routing impedance. To complicate matters, as the board designer you have to consider these requirements alongside the normal tradeoffs you have to make – such as selecting the most appropriate routing widths / clearances and minimizing the layer count to meet the project budget.

Ideally you will have an impedance that you have been asked to achieve, typically something in the range of 40 to 90 ohms. Rather than you needing to calculate the routing width for each layer so that you can achieve the specified impedance, Altium Designer lets you specify the impedance, and it will calculate the routing width required on each layer to achieve this.

To do this simply enable the **Characteristic Impedance Driven Width** option when you are setting up the Routing Width design rule in the **PCB Rules and Constraint Editor**, then enter the required minimum/preferred/maximum impedances – these will automatically be translated into widths for each signal layer. A six layer (4 signal + 2 plane) example is shown in Figure 3.

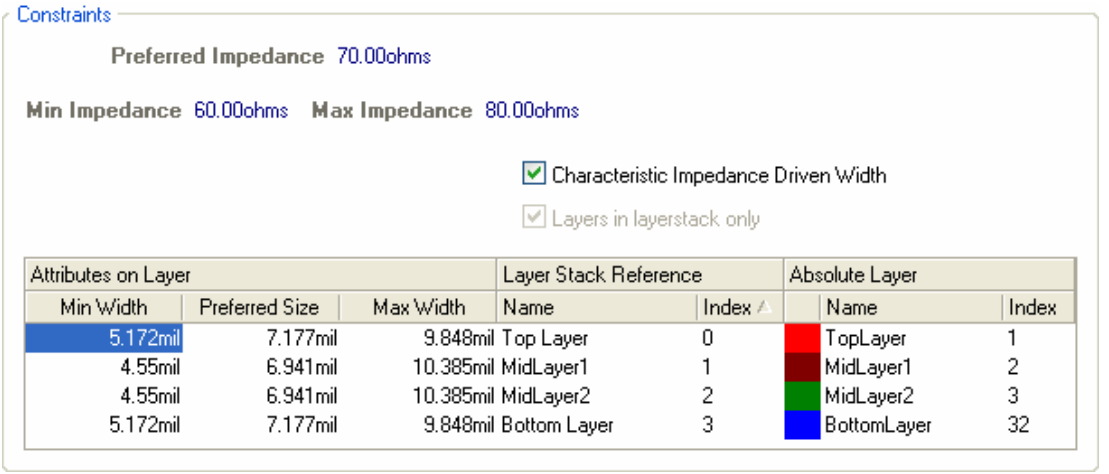


Figure 3. Enable the Characteristic Impedance Driven Width option to specify the Width as an impedance.

As you route the board and change layers Altium Designer will automatically change the width to the size needed to achieve the specified impedance. This interactive impedance controlled routing greatly simplifies the task of designing a controlled impedance PCB.

Note that the built-in impedance calculator does not account for the effect of vias, it assumes lossless transference from one signal layer to the next. Additionally, it only takes into account single-ended structures (not differential), and determines the routing width of target nets on a whole-layer basis.

Defining the layer stackup

A fundamental requirement for controlling the impedance is to include power planes. These planes should be distributed through the board stackup, ideally they are arranged so that there is at least one plane adjacent to each signal layer. The adjacent plane provides each signal return path, and for reasons that will not be covered here, does so regardless of the DC voltage distributed by that plane.

The return path current flowing through the plane will attempt to follow the same physical path as the route on the signal layer, so you should always try to avoid introducing discontinuities such as a split or blowout in the power plane, underneath any critical routing.

As well as the selecting a suitable order for signal and plane layers, you also need to define the material properties of each layer, including:

- Copper thickness
- Dielectric thickness
- Dielectric constant

These values, and the routing width, all contribute to the final impedance.

Achieving the required impedance then becomes a process of tuning all these values. Keep in mind that possible copper and dielectric thickness values may be limited too, determined by the materials available from your PCB fabricator.

For example, typical values of copper thickness used are 0.7mil ($^1/_2$ oz) for signal layers, and 1.4mil (1 oz) for plane layers. But if your stackup is such that one signal and one plane layer are a pair on either

side of one of the original thin panels used in the multilayer process, then they may need to have the same copper thickness.

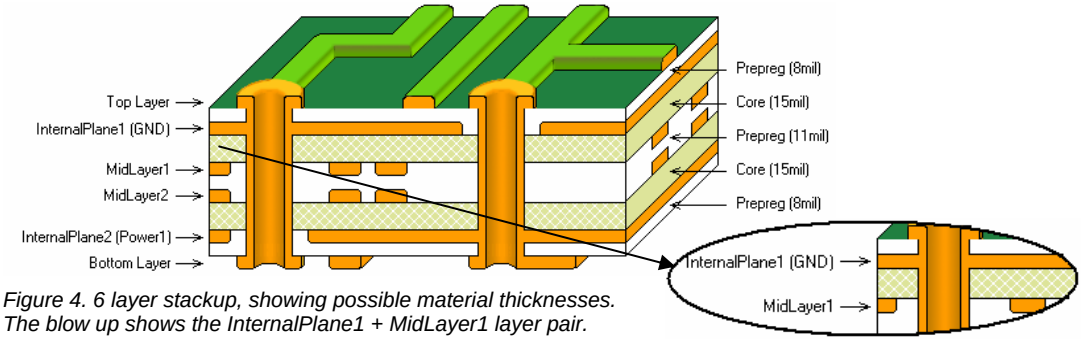


Figure 4. 6 layer stackup, showing possible material thicknesses. The blow up shows the InternalPlane1 + MidLayer1 layer pair.

Figure 4 shows a six-layer stackup, note that each of the internal signal layers is paired with a plane layer, as shown in the blow up section of the image.

Ideally you would have used 0.7mil thickness for all signal layers, which would have resulted in the routing thicknesses shown in Figure 5. Note that the **Preferred Size** tracks are all very close to 7mils, making the routing process straightforward.

Constraints

Preferred Impedance 70.00ohms

Min Impedance 60.00ohms **Max Impedance** 80.00ohms

☑ Characteristic Impedance Driven Width

☑ Layers in layerstack only

Attributes on Layer			Layer Stack Reference		Absolute Layer	
Min Width	Preferred Size	Max Width	Name	Index	Name	Index
5.172mil	7.177mil	9.848mil	Top Layer	0	TopLayer	1
4.55mil	6.941mil	10.385mil	MidLayer1	1	MidLayer1	2
4.55mil	6.941mil	10.385mil	MidLayer2	2	MidLayer2	3
5.172mil	7.177mil	9.848mil	Bottom Layer	3	BottomLayer	32

Figure 5. Routing widths required to achieve 70 ohm impedance, using 0.7mil thick signal layers.

But if the fabrication process requires that MidLayer1 and 2 use 1.4mil thick copper since each of them is paired with one of the plane layers, then the routing widths show in Figure 6 must be used to achieve the 70 ohm impedance. In this case the range of preferred routing width values is still acceptable, but you need to keep this in mind.

Like copper thickness, core thickness will only be available in specific increments since the core thickness is defined by the thickness of the layer-pair panel used in the multilayer process. You will probably have greater freedom with prepreg thicknesses. And then there is the overall final board thickness, this must also be a realistic value (around 62mils is typical).

From this simple example you can see that there is a process of working from available materials and desired impedances to arrive at the final board stackup and routing widths.

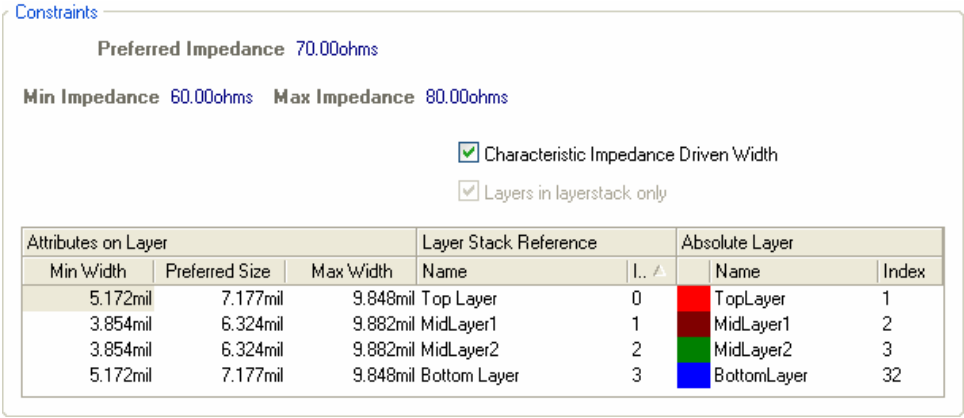


Figure 6. Routing widths required to achieve 70 ohm impedance, using 1.4mil thick copper internal signal layers.

Testing the signal integrity of the routed board

In the same way that you tested the nets during design capture using an assumed routing length and routing impedance, once the routing is complete you should repeat this process on the board to check for potential impedance mismatches and reflection issues. Launch the Signal Integrity test from the PCB editor **Tools** menu. Since the PCB is part of the project Altium Designer will now use the material properties and dimensions defined in the **Layer Stack Manager** and the actual widths of the routes on the board to calculate the impedances it uses for the signal integrity tests.

Achieving the specified impedances

Beyond the iterative dimension tuning process that you go through to achieve the correct impedances, there are other factors that influence the final impedance that will be achieved on your fabricated PCB. These include the consistency and stability of the dielectric material used in the PCB, and also the consistency and quality of the etching process. If you require a controlled impedance PCB you should discuss this with your PCB fabricator. Some fabricators can advise on track geometries if you supply them with your preferred stackup. Many will also be able to include an impedance test coupon on each panel that they fabricate – this can be used to measure the real impedances achieved on the board.

Additional reading and resources

This article only gives an introduction to the topic of signal integrity and controlled impedance PCB design. Use the following links to learn more, where you can access resources developed by recognized industry experts.

http://www.speedingedge.com/

http://www.sigcon.com/

http://www.bethesignal.com

http://www.epanorama.net/links/basics.html#highspeed

Revision History

Date	Version No.	Revision
9-Dec-2003	1.0	New product release
26-Aug-2005	1.1	Rewritten for Altium Designer 2004
30-Nov-2005	1.2	Updated for Altium Designer 6.0
13-Jun-2006	1.3	References to stripline and microstrip corrected